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Radiation Robustness of XOR and Majority Voter Circuits at FinFET Technology under Variability

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“You’ll find that life is still worthwhile,
if you just smile.”
— CHARLES CHAPLIN

ABSTRACT

Advances in microelectronics have contributed to the size reduction of the technological node, lowering the threshold voltage and increasing the operating frequency of the systems. Although it has positive outcomes related to the performance and power consumption of VLSI circuits, it does also have a strong negative impact in terms of the reliability of designs. As technology scales down, the circuits are becoming more susceptible to numerous effects due to the reduction of robustness to external noise as well as the increase of uncertainty degree related to the many sources of variability. Fault-tolerant techniques are usually used to improve the robustness of safety critical applications. However, the implications of the scaling of technology have interfered against the effectiveness of fault-tolerant approaches to provide the fault coverage. For this reason, this work has evaluated the radiation robustness of different circuits designed in FinFET technology under variability effects. In order to determine the best design options to implement fault-tolerant techniques such as the Triple-Module Redundancy (TMR) and/or Duplication with Comparison (DWC) schemes, the set of analyzed circuits is composed of ten different exclusive-OR (XOR) logic gate topologies and two majority voter (MJV) circuits. To investigate the effect of gate configuration of FinFET devices, the XOR circuits is analyzed using double-gate configuration (DG FinFET) and tri-gate configuration (TG FinFET). Environmental Variability such as Temperature and Voltage Variability are evaluated in the set of analyzed circuits. Additionally, the process-related variability effect Work-Function Fluctuation (WFF) is also evaluated. In order to provide a more precise study, the layout design of the MJV circuits using a $7nm$ FinFET PDK is evaluated by the predictive MUSCA SEP3 tool to estimate the Soft-Error Rate (SER) of the circuits considering the layout contrainsts and Back-End-Of-Line (BEOL) and Front-End-Of-Line (FEOL) layers of an advanced technology node.

Keywords: Microelectronics. Fault Tolerance. Radiation Effects. Variability. FinFET.

RESUMO

Os avanços na microeletrônica contribuíram para a redução de tamanho do nó tecnológico, diminuindo a tensão de limiar e aumentando a freqüência de operação dos sistemas. Embora tenha resultado em ganhos positivos relacionados ao desempenho e ao consumo de energia dos circuitos VLSI, a miniaturização também tem um impacto negativo em termos de confiabilidade dos projetos. À medida que a tecnologia diminui, os circuitos estão se tornando mais suscetíveis a inúmeros efeitos devido à redução da robustez ao ruído externo, bem como ao aumento do grau de incerteza relacionado às muitas fontes de variabilidade. As técnicas de tolerancia a falhas geralmente são usadas para melhorar a robustez das aplicações de segurança crítica. No entanto, as implicações da redução da tecnologia interferem na eficácia de tais abordagem em fornecer a cobertura de falhas desejada. Por esse motivo, este trabalho avaliou a robustez aos efeitos de radiação de diferentes circuitos projetados na tecnologia FinFET sob efeitos de variabilidade. Para determinar as melhores opções de projeto para implementar técnicas de tolerancia a falhas, como os esquemas de Redundância de módulo triplo (TMR) e/ou duplicação com comparação (DWC), o conjunto de circuitos analisados é composto por dez diferentes topologias de porta lógica OR-exclusivo (XOR) e dois circuitos votadores maioritários (MJV). Para investigar o efeito da configuração do gate dos dispositivos FinFET, os circuitos XOR são analisados usando a configuração de *double-gate* (DG FinFET) e *tri-gate* (TG FinFET). A variabilidade ambiental, como variabilidade de temperatura e tensão, são avaliadas no conjunto de circuitos analisados. Além disso, o efeito da variabilidade de processo *Work-Function Fluctuation* (WFF) também é avaliado. A fim de fornecer um estudo mais preciso, o projeto do leiaute dos circuitos MJV usando $7nm$ FinFET PDK é avaliado pela ferramenta preditiva MUSCA SEP3 para estimar o *Soft-Error Rate* (SER) dos circuitos considerando as características do leiaute e as camadas de *Back-End-Of-Line* (BEOL) e *Front-End-Of-Line* (FEOL) de um nó tecnológico avançado.

Palavras-chave: Microeletrônica, Tolerância a Falhas, Efeitos de Radiação, Variabilidade, FinFET.

LIST OF ABBREVIATIONS AND ACRONYMS

ALD	*Atomic Layer Deposition*
BEOL	*Back-End-Of-Line*
CAD	*Computer Aided Design*
CMOS	*Complementary Metal-Oxide-Semiconductor*
CPP	*Contacted Poly Pitch*
DD	*Displacement Damage*
DIBL	*Drain-Induced Barrier Lowering*
DRAM	*Dynamic Random Access Memory*
DTCO	*Design/Technology Co-Optimization*
DWC	*Duplication With Comparison*
EDA	*Electronic Design Automation*
EUV	*Extreme Ultra-Violet*
FEOL	*Front-End-Of-Line*
FET	*Field Effect Transistor*
FinFET	*Fin-Shaped Field Effect Transistor*
FIT	*Failure In Time*
GDS	*Graphic Database System*
GIDL	*Gate Induced Drain Leakage*
HP	*High Performance*
HKMG	*High-K Metal Gate*
IRPS	*International Reliability Physics Symposium*
LET	*Linear Energy Transfer*
LIG	*Local-Interconnect Gate*
LISD	*Local-Interconnect Source-Drain*

LSTP *Low Stand-By Power*

MBU *Multiple-Bit Upset*

MCU *Multiple-Cell Upset*

MJV *Majority Voter*

MOL *Middle-Of-Line*

MOS *Metal Oxide Semiconductor*

NAND *Not AND*

NIEL *Non-ionizing Energy Loss*

NOR *Not OR*

PDK *Process Design Kit*

PTL *Pass-Transistor Logic*

PTM *Predictive Technology Model*

RDF *Random Dopant Fluctuation*

SADP *Self-Aligned Double Patterning*

SAQP *Self-Aligned Quadruple Patterning*

SCE *Short-Channel Effects*

SEE *Single Event Effects*

SEGR *Single Event Gate Rupture*

SEL *Single Event Latch-up*

SER *Soft Error Rate*

SET *Single Event Transient*

SEU *Single Event Upset*

SOI *Silicon-on-Insulator*

SPICE *Simulation Program with Integrated Circuit Emphasis*

SS *Subthreshold Slope*

TCAD *Technology Computer Aided Design*

TID	*Total Ionizing Dose*
TMR	*Triple Modular Redundancy*
VLSI	*Very large-system Integration*
WFF	*Work-Function Fluctuation*
XOR	*Exclusive-OR*

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1 INTRODUCTION

Within the advancement of technology scaling, new challenges are raised in VLSI designs. Besides the area, power and performance concern, one should consider reliability issues due to increased soft error rates, pronounced variability effects and Short-channel Effects (SCE) encountered at advanced nodes. For instance, particles with low energy found on the surface of the earth, previously neglected, are now able to interfere with the operation of a circuit (DODD et al., 2010)(BAUMANN, 2005b). Also, electrical characteristics of devices from the same circuit can vary widely, resulting in high deviation on performance metrics and abnormal power consumption due to process, voltage and temperature variations (ZIMPECK; MEINHARDT; REIS, 2015)(BROWN et al., 2013). Additionally, the increased chip integration provided by the technology scaling has enabled denser designs leading to thermal and power issues (CHOI; MURTHY; ROY, 2007). Thus, if no effort is spent to overcome these issues, it potentially can lead to catastrophic failure, malfunction of the circuits or thermal runaway. For instance, intra-die fluctuation in power dissipation leads to local temperature variation causing hot spots. This effect is worsened by the supply voltage and process variability causing performance shifts throughout the chip.

To overcome the challenges imposed by the technology scaling, many works have been carried out to propose new materials or device structures (PRADHAN et al., 2016) (GAUTAM et al., 2013). Accordingly, the microelectronics industry has been through a changing of concept in order to keep with the transistor scaling. Devices using different structures and material are being investigated to meet the requirements of advanced technology nodes such as the Fully Depleted Silicon on Insulator (FDSOI) and Fin-shaped Field Effect Transistor (FinFET) devices. For instance, the FinFET technology is replacing the planar bulk CMOS at sub-22nm nodes due to its improved short-channel controllability, lower leakage and better yield. The reduced coupling between the source and drain region provided by the multiple gate electrodes in FinFET devices provides a strong gate electrostatic control over the channel potential (FERAIN et al., 2011).

These devices can be designed either on Silicon-on-Insulator (SOI) substrate or on bulk-silicon substrate due to the fabrication process similarity with the bulk CMOS one. Besides the lower fabrication cost and better process compatibility, bulk-silicon based FinFET are widely used to improve heat transfer to the substrate (COLINGE et al., 2008). Fin-like structure devices have reduced thermal conductivity due to small and

confined dimensions of the fin and bulk-based substrate devices exhibit better thermal performance compared to SOI substrates devices (KUMAR; RAO, 2016). Among of the multigate transistors (MuGFET) proposed in the past few years in the literature, the FinFET (double- or tri-gate configuration) is the most indicated as promising candidates to further transistor scaling down to 7nm (HISAMOTO et al., 2000)(SUN et al., 2008).

Regarding the radiation robustness, the three-dimensional multigate technology provides a better response to the ionizing radiation effects due to its small sensitivity volumes compared to its counterpart planar devices (HUBERT; ARTOLA; REGIS, 2015). Although multigate devices show better robustness, when the bulk substrate is used over the SOI, additional charges are accumulated due to the diffusive component in the charge collection process. At SOI-based devices, the buried oxide structure suppresses this diffusion mechanism leading to eight times less of collected charge (EL-MAMOUNI et al., 2012). The differences in the collected charges are significant in advanced technologies where the critical charge is on the order of tens of femto coulombs (ALLES et al., 2011). Further, the FinFET structure along with the aggressive transistor scaling raises questions regarding the full understanding of the radiation effects of advanced technology, as well as its prediction and mitigation (NSENGIYUMVA et al., 2017).

1.1 Motivation

The design of VLSI circuits, not restricted only to space and defense applications, requires the analysis of the susceptibility to radiation effects due to its impact on the reliability of advanced technologies (AZAMBUJA; KASTENSMIDT; BECKER, 2014). As the FinFET technology has already been introduced in the industry and adopted to a variety of applications, it is imperative the need for the study and analysis of its robustness to radiation effects.

Additionally, redundancy is one of the most commonly fault-tolerant technique used to increase the robustness of a given design or application. Hardware redundancy can be classified into three different groups of techniques (DUBROVA, 2013):

1. ***Passive Redundancy:*** concerns the techniques which the system achieves fault tolerance by masking the faults itself, without a previous detection and further recovery mechanism. For example, the most common passive hardware redundancy approach is the Triple-Modular Redundancy (TMR) technique, which basically masks

the faults when it occurs, rather than detects it (KASTENSMIDT; REIS, 2007). This approach is used in applications which require high reliable systems when no single fault is tolerated or the repair process is not feasible such as aircraft flight control systems, satellites or even embedded medical devices;

2. ***Active Redundancy:*** to provide fault tolerance this approach requires the fault detection and location to further recover the system to a safe and operational state. In this case, momentaneous errors can be allowed since it is recovered within a specified period of time. Often, the active redundancy is used in applications which it is required a high availability, such as transactions processing systems (DUBROVA, 2013). One active redundancy approach is the Duplication with Comparison (DWC) in which a module is duplicated and its output compared. Whether a disagreement is observed at its output, an error signal is generated;

3. ***Hybrid Redundancy:*** combines both passive and active approaches to prevent momentary errors and to provide the recovery of the system. This approach is preferable in safety-critical applications.

Most of the mitigation techniques based on hardware redundancy rely on the voting and comparing operations. The Triple-Modular Redundancy (TMR) technique is widely explored in a variety of strategies implementation. The concept of TMR is to have three identical copies processing data and a majority voter circuit voting its output to mask faults in one of the copies as shown in Figure 1.1. TMR can be implemented in hardware at gate level, for instance, where each module is triplicated and voters are added.

According to the granularity of the TMR, the majority voters do not need to be placed only at the outputs, but also in the designs after some combinational logic or flip-flops (DO, 2011). A majority voter can mask the occurrence of a single fault in any of the triplicated circuit modules. Therefore, the voter circuit constitutes the critical point of failure for the TMR scheme, i.e., a soft error in the voter circuit leads to a faulty output as can be seen in Figure 1.1.

While the TMR approach relies on the robustness of the voter circuit, the DWC requires an ideal fault-free comparator circuit as seen in Figure 1.2. If a soft error occurs in the comparator circuit, the mitigation technique fails by excessively recovering the systems even if there were no fault, leading to degradation of performance, or by disqualifying the error detection mechanism, i.e., allowing a fault to be propagated. The

exclusive-OR logic gate is the most used circuit to perform the comparison function in this technique and many other fault-tolerant techniques (DUBROVA, 2013)(AZAMBUJA; KASTENSMIDT; BECKER, 2014).

Figure 1.1: TMR Scheme - the voter circuit constitutes the critical point of failure in the technique

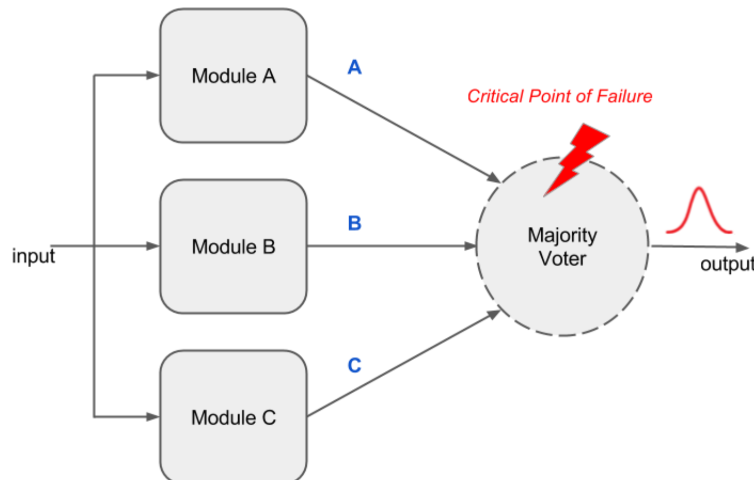
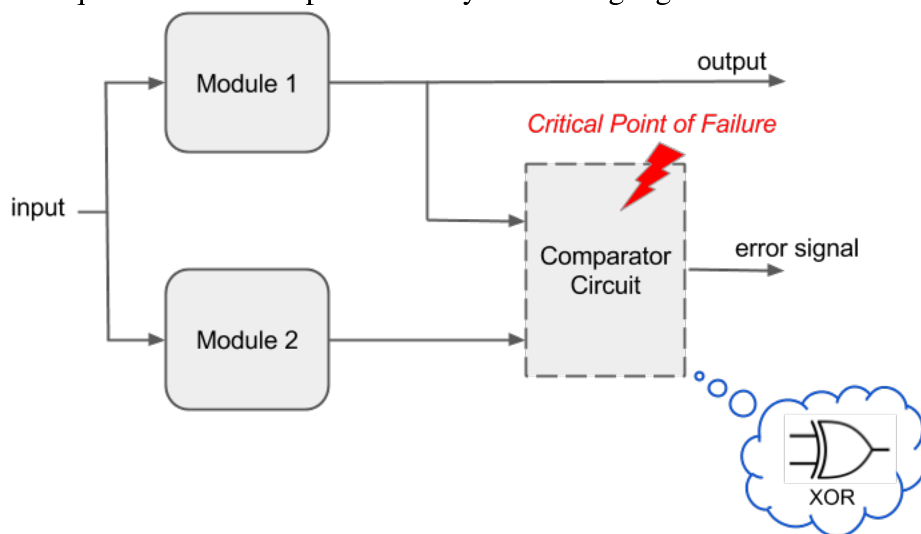


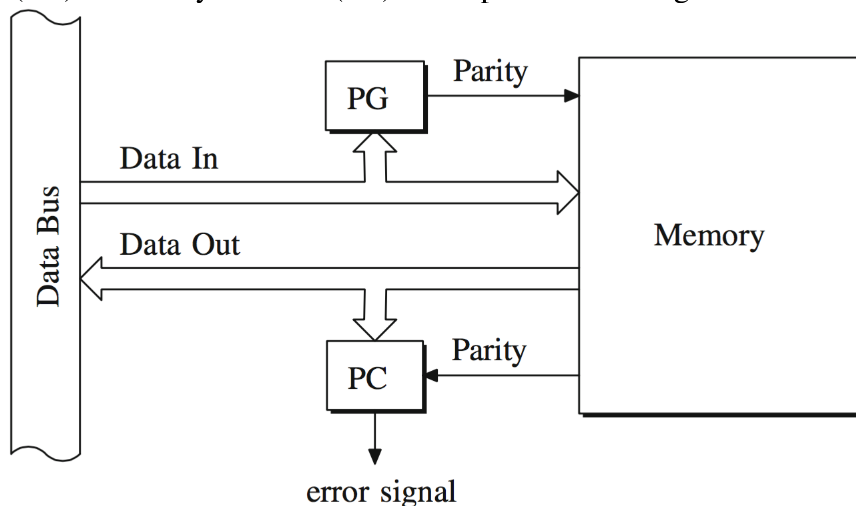
Figure 1.2: DWC Scheme – the comparator circuit constitutes the critical point of failure in the technique and it is often performed by a XOR logic gate



Besides the importance of the usage of XOR logic gates in hardware redundancy, it is also vastly applied in fault-tolerant techniques based on information redundancy. For example, error detection techniques based on parity generator and checker circuits can be implemented using a tree of XOR gates to protect memories under parity codes (DUBROVA, 2013). In Figure 1.3 a memory block is protected by applying a parity code, which requires a Parity Generator (PG) to generate the parity bit, and a Parity Checker

(PC) to verify if the data was corrupted by a soft error occurrence (whether the data correspond to its parity bit, i.e., if it is an even or odd number). Further, the XOR logic gate is also fundamental for Error Correction Codes (ECC) such as Hamming Codes or even for Built-in Self-Test (BIST) logic circuits as in Linear Feedback Shift Register (LFSR) or Multiple Input Signature Register (MISR) approaches (BUSHNELL; AGRAWAL, 2004). Thus, the designer of the XOR logic gates must have in mind its importance, besides the timing and power requirements, it needs to match the requirements for reliability issues.

Figure 1.3: Parity Code – A memory can be protected using parity codes. The Parity Generator (PG) and Parity Checker (PC) are implemented using trees of XOR logic gates



Source: (DUBROVA, 2013)

1.2 Objectives and Contributions

The change from the conventional planar to FinFET devices introduced new challenges in understanding and predicting the radiation effects as the actual sensitive area and the charge collection processes suffered from this change. As discussed in the previous section, the increase of radiation susceptibility in advanced technologies requires predictive studies to investigate its reliability and also to guarantee the effectiveness of fault-tolerant approaches. Accordingly, the goal of this work relies on the study and analysis of the radiation robustness of different topologies of the exclusive-OR logic gate and Majority Voter circuits using bulk FinFET devices at advanced technology nodes, mainly the $7nm$ technology.

To provide a broader understanding of the behavior of such devices under radiation effects, it is performed process, voltage and temperature variability along with the particle interaction into the silicon. The circuits are analyzed at SPICE level and/or layout level.

This work examines ten different topologies of XOR gates exploiting the advantages of complementary CMOS logic family and the Pass-Transistor Logic (PTL) family. With the results obtained in this work, a designer can choose the most radiation robust XOR topology to be used in fault-tolerant techniques, as in the DWC, and then provide reliable applications.

Further, in addition to the SPICE level analysis, two majority voter circuits based on cell implementation are designed and evaluated at layout level using a Monte-Carlo Predictive tool named MUSCA SEP3. The majority voters are implemented using basic logic cells as the NOR and NAND gates. The most common fault masking technique, i.e. the TMR approach, relies on the reliability of the voter circuitry. Thus, choosing the best majority voter impacts the effectiveness of the fault masking schemes significantly.

The results were explored, discussed and presented in national and international conferences. A list of the publications during the master degree can be found in the Appendix A.

1.3 Dissertation Organization

This work is divided as follows. The theoretical foundation and the review of the state-of-the-art regarding the radiation effects in electronic circuits and FinFET technology are discussed in the Chapter 2 and Chapter 3, respectively. Chapter 4 explains the methodologies adopted to analyze the radiation robustness of the circuits. Then, the results are discussed in Chapter 5. It is divided into two parts: the results obtained from the analysis of the XOR circuits and the results obtained for the majority voter circuits. Finally, the conclusions and future work follow in the Chapter 6.

2 RADIATION EFFECTS ON ELECTRONIC CIRCUITS

Reliability is one of the major concerns in the development of VLSI circuits at advanced technologies (BORKAR, 2005). It occurs due to the increase in functionality and complexity of the systems, along with the use of deeply scaled transistors under low voltage and high frequency. As technology advances, it is observed an increase in the susceptibility of the circuit relative to the noise from the environment and particularly the bombardment of particles of radiation (BAUMANN, 2005b)(DODD et al., 2010). This Chapter explores the mechanisms of radiation interaction in electronics and its modeling, discusses the emerging effects at advanced technologies highlighting the state-of-the-art.

2.1 Single Event Effects

The research focused on the study of the radiation effects in electronic systems was initially considered a primary concern of extreme relevance only in projects developed for military or space applications. However, the first work that predicted the influence of particle bombardment on electronic circuits was developed by Wallmark and Marcus of RCA Laboratories in Princeton (WALLMARK; MARCUS, 1962), where they investigated the miniaturization trends of electronic circuits. It has been observed that, with the reduction of the transistor dimensions, cosmic rays could be a source of disturbance in the integrated circuits. But Binder et al., in 1975, first observed anomalies in a satellite and attributed to the effect of space radiation (BINDER; SMITH; HOLMAN, 1975). Binder et al. (1975) identified state changes in the flip-flop circuits caused by the critical accumulation of charges stored in capacitors of the transistors junctions of the integrated circuits. Later, in 1978, May and Woods from Intel Corporation published a paper which showed a significant error rate in DRAMs due to radiation at sea level and the increased integration density of components (MAY; WOODS, 1978). They determined that the failures were caused by alpha particles emitted by the decay of radioactive elements as uranium and thorium, which contaminated the encapsulation material in the manufacturing of memory chips process. This was the first study published in the International Reliability Physics Symposium (IRPS) and was the first work to define the anomalies as "soft errors". This term was used to differentiate and characterize the random effects caused by radiation memory elements. Guenzer et al. (1979) reported that the occurrence of soft errors may also be derived from nuclear reactions in which particles of protons and high-energy neu-

trons are produced (GUENZER; WOLICKI; ALLAS, 1979). These radiation effects can be classified as:

1. ***Total Ionizing Dose* (TID):** it is a cumulative, reversible, long-term effect that degrades some electrical properties of the irradiated circuits due to the accumulation of charges in the SiO_2 layer and Si/SiO_2 interface. The trapped charges induces threshold voltage shift, mobility degradation and leakage;

2. ***Displacement Damage* (DD):** it is a physical damage to the crystalline structure of the material caused by Non-Ionizing Energy Loss (NIEL) of the incident particles, degrading the device and its properties (VELAZCO; FOUILLAT; REIS, 2007);

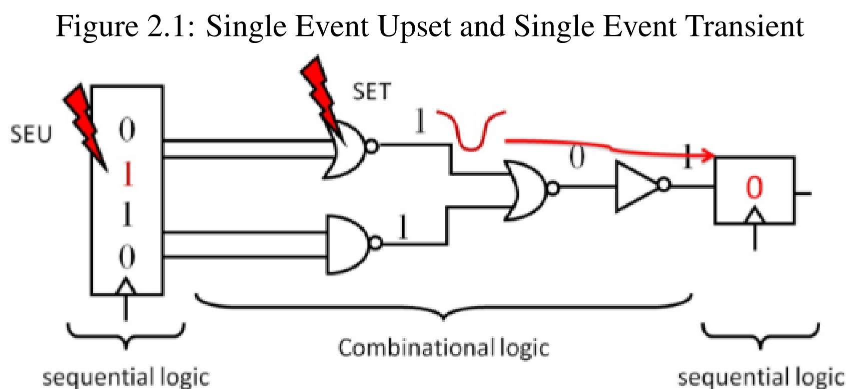
3. ***Single Event Effects* (SEEs):** are effects that occur due to the bombardment of particles (neutrons, electrons, protons, alpha particles and heavy ions) that hit the silicon, ionizing it densely and releasing energy that can damage the device permanently or induce transient behavior, compromising the good functioning of the circuit. SEEs can be classified as destructive and nondestructive (AZAMBUJA; KASTENSMIDT; BECKER, 2014). The most well-known are the non-destructive effect, commonly named as Soft Errors (SE): the **Single Event Upset (SEU)**, the affected circuit is a sequential element, causing the change of the stored bit; and the **Single Event Transient (SET)**, the particle hits a combinational element, for example a multiplexer, inducing a transient pulse that may or may not be captured by a memory element.

Total Ionizing Dose (TID) and Single Event Effects (SEEs) are the most common radiation effects in electronic systems, being the object of many studies in the scientific community (CLEMENS, 2012). Initially, the faults caused by TID were considered of greater importance since their more significant occurrence when compared with the soft errors. However, with the advancement of technology, research has focused on the problems caused by SEEs due to their increasing rate of occurrence, and the reduction of TID effects (HOLMAN, 2008). The main reasons for the decrease of the TID effect in current technologies were the improvement between the oxide and silicon layers of the transistors, such as the reduction of oxide thickness (CLEMENS, 2012). Further, the considerable increase of soft errors is due to the miniaturization of the dimensions of the integrated circuits along with the increasing reduction of the supply voltage. This voltage reduction is directly related to the decrease in the power consumption and the intrinsic

capacitances of the circuit, increasing the chances of a transient pulse generated by a particle to have sufficient intensity to overcome the reduced capacitances of the circuit and induce a fault. Therefore, the Single Event Effects induced by heavy ions, protons, and neutrons has become an increasing limitation when it comes to the reliability of electronic components, circuits and systems in general. This concern stimulated the development of many research work in the area to improve the understanding of this phenomenon and the development of techniques to mitigate these faults.

The generation mechanism of SET and SEU are similar in nature, differing only in the hit circuit by the radiation. The Single Event Upset occurs in memory cells or registers and is characterized as a bit flip - when the charge deposited by the particle has sufficient energy to modify the logical states of the storage device (BALEN, 2010). The Single Event Transient is a transient that can propagate as a voltage or current pulse and occurs when the particle strikes at sensitive nodes of combinational elements of a circuit (SIMIONOVSKI, 2012). Figure 2.1 gives an example of the occurrence of these faults. An SEU was identified in the first sequential element of the circuit, where the logical value of a bit was changed, in red. In the first NOR2 logic gate of the circuit, it is observed the generation of a transient pulse in its output induced by a SET occurrence. In this example, the transient pulse had enough amplitude to reach the second sequential element of the circuit and induce a bit flip.

Figure 2.1: Single Event Upset and Single Event Transient

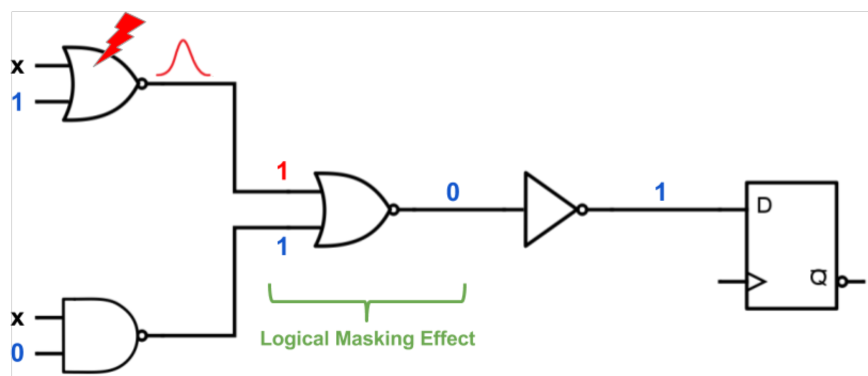


Source: (AZAMBUJA; KASTENSMIDT; BECKER, 2014).

Regarding the SET fault, combinational circuits present inherent ability of fault masking its propagation throughout a logic path (SAYIL, 2016). The fault masking effects are classified as: **Electrical Masking**, **Logical Masking** and **Latching-Window Masking** (or temporal masking). Logical masking occurs when the fault affects a region of the circuit that is not determinant for the output result at the instant that the fault has occurred. An example would be an NAND2 logic gate, where if one of its inputs is 0, no

matter the value assigned in the other inputs, the output will always be 1. Analogously, an NOR2 logic gate can exhibit a masking effect when one of its input is assigned to 1 logic level. In Figure 2.2 we can see an example of a transient fault propagated towards an NOR2 logic gate that has one of the inputs equal to 1. Since the output of the circuit has already been determined by one of its inputs, the transient fault present in the other input will not affect the output result, so we can say that there was the logical masking of the fault in question. As the logic depth of combinational logic in advanced VLSI designs is reduced, the effectiveness of logical masking is diminished (SAYIL, 2016).

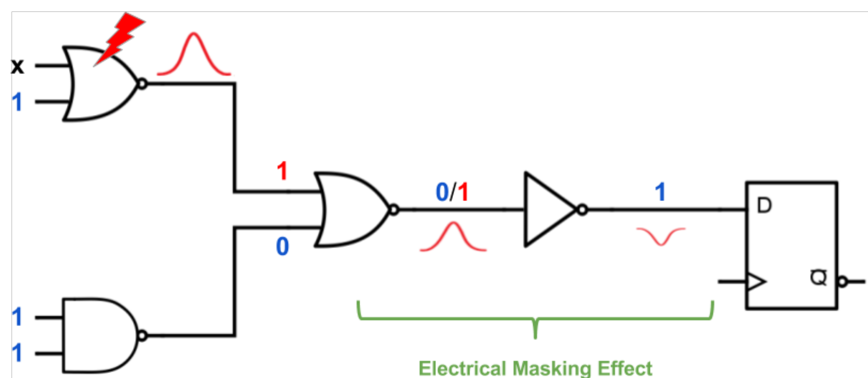
Figure 2.2: Logical Masking of SET occurrence in a NOR2 logic gate.



Source: From the author.

In the electrical masking, the transient fault is not propagated to a memory element due to electrical losses during the circuit path that attenuates its magnitude and amplitude. In Figure 2.3 we can observe that after at each logic gate the transient pulse signal has an attenuation in its magnitude, practically extinguishing itself near the memory element. In this case, the pulse has not arrived at the memory element with pulse width and peak sufficient to change the state of the stored bit.

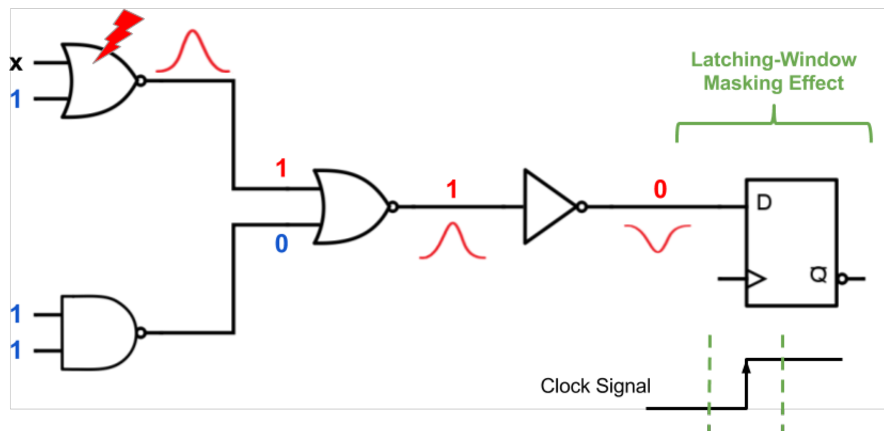
Figure 2.3: Electrical Masking of SET occurrence in a logic path.



Source: From the author.

If the SET fault has not been masked logically or electrically, it may be masked through the latching window of a memory element. A wrong value will only be stored if the SET pulse is able to traverse all combinational logic path and reach the memory element during its window of vulnerability to failure (latching-window), as shown in Figure 2.4. Otherwise, the fault will not manifest itself as an error.

Figure 2.4: Latching-Window Masking of SET occurrence in a logic path.



Source: From the author.

In summary, the ion strike must induce a SET pulse with sufficient amplitude and duration to propagate through an open logic path and reach a memory element during a clock pulse enabling the latching of the input value. Thus, as the clock frequency increases and the supply voltage reduces, the probability of a SET pulse to be latched by a memory element increases (MUNTEANU; AUTRAN, 2008).

2.2 Physical Mechanisms of Deposition and Charge Collection

Soft errors occur when energetic particles interact with silicon colliding with a sensitive area of the circuit and depositing an additional charge on the P-N junction region of the transistor. There are basically two mechanisms of charge deposition attributed to the interaction of radiation with the silicon of a chip (DODD; MASSENGILL, 2003):

1. **Direct Ionization**: when a charged particle travels through a semiconductor material, it loses energy along its path by releasing electron-hole pairs. This resulting ionizing track, when collected by the electric field of the device, generates a transient current/voltage. Direct ionization is considered as a primary mechanism of charge deposition caused by the incidence of alpha particles or heavy ions (ions

with an atomic number greater than or equal to 2). Lighter particles such as protons do not produce enough direct ionization charge to generate an observable transient pulse.

2. **Indirect Ionization**: it is a secondary mechanism of charge deposition, where due to nuclear reactions in the semiconductor material, light particles such as protons and neutrons can release energy in the silicon through secondary particles product of the nuclear reaction. That is, once a nuclear reaction has occurred, the charge deposition can occur by particles product of this reaction.

The energy deposited by the particle due to its ionization in silicon is an important metric in the study of radiation effects in nanotechnologies, because it is directly related to the magnitude and amplitude of the transient pulse generated. **Linear Energy Transfer (LET)** is the amount of energy that a particle releases per unit of length from the path traveled, as defined in Equation 2.1 (VELAZCO; FOUILLAT; REIS, 2007).

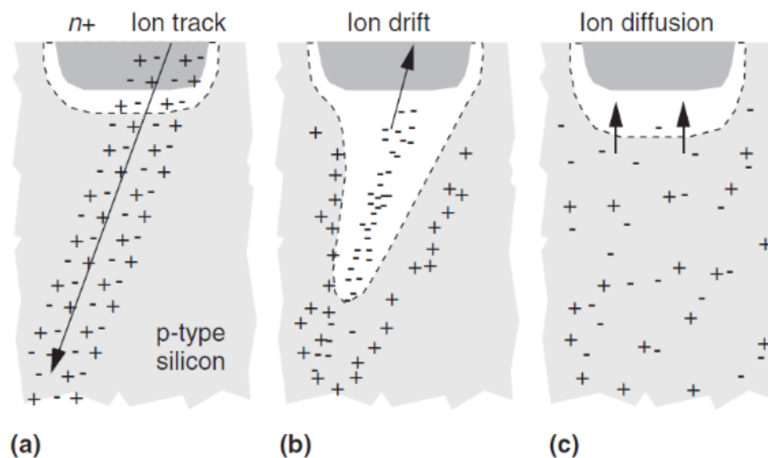
$$LET = \frac{\partial E}{\partial x} \tag{2.1}$$

LET is dependent on the mass and energy of the particle and the ionized material, so particles with higher mass and energy ionized in denser materials have higher LETs (BAUMANN, 2005b). LET can be normalized by the density of the semiconductor material and be expressed by capacitance per unit length ($pC/\mu m$ ou $fC/\mu m$). This conversion allows the comparison of the physical dimension of the device and the deposited charge. After the ionization of the particle in the silicon, i.e., after deposition of an additional charge on the affected device, the process of charge collection proceeds through two main mechanisms: Drift and Diffusion.

When the resulting ionization path crosses or approaches the depletion region formed at the p-n junctions, as in Figure 2.5 (a), the additional carriers deposited by the ion are rapidly collected by the high intensity electric field in this region (MUNTEANU; AUTRAN, 2008). This charge collection process is called as **Drift** (Figure 2.5, b). The passage of the particle through the depletion region is responsible for its temporary deformation, in a matter of picoseconds, in the form of a funnel, and for this purpose it was called the **Funneling Effect**. This effect leads to an increase in the efficiency of the collection of charge due to the increase of the area of the depletion region (BAUMANN, 2005a).

And, finally, the **Diffusion** process is responsible for collecting all the remain-

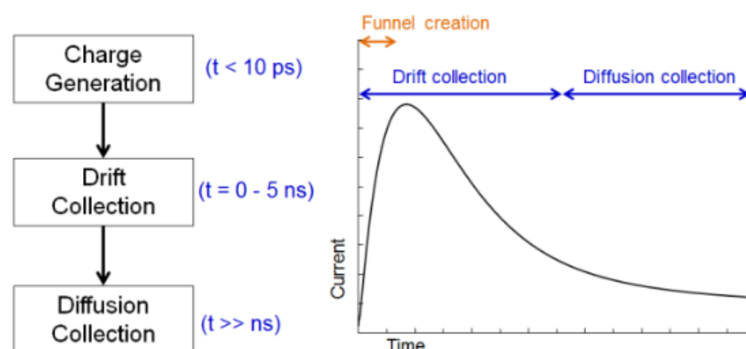
Figure 2.5: Charge Collection Mechanisms due to an Ion strike in a P-N junction.



Source: (BAUMANN, 2005b).

ing carriers that were generated besides the depletion layer (Figure 2.5, c). The typical waveform of the resulting current from the charge collection induced by the incidence of a particle can be seen in Figure 2.6. The Drift and Funneling are very rapid processes, almost instantaneous due to deformation of the electric field of the junction and the consequent increase in charge collection efficiency. Therefore, it is responsible for controlling the rapid rise of the transient current as seen in Figure 2.6. In the Diffusion process, a longer time is needed to collect the charge and, therefore, the transient pulse has a slower fall time.

Figure 2.6: Transient Current Waveform induced by a radiation strike.



Source: (CUMMINGS, 2010).

The analytic model proposed in (MESSENGER, 1982) is widely used and proposes a current source whose behavior obeys a double exponential. The modeling of this transient current according to MESSENGER (1982) is described by the following Equation 2.2 and Equation 2.3. Due to emerging effects in deeply scaled technologies (briefly discussed in the next section), the double exponential model for a radiation hit into the silicon might not accurately model the generated transient pulse, especially for higher

LET (SAYIL, 2016). It is observed a “plateau” behavior on the transient pulse waveform, especially for particle hit with LET > 10 MeV (DASGUPTA et al., 2007). However, double exponential current sources still provide a reasonable first-order estimate and it is widely used as a base model for SEE analysis (ARTOLA et al., 2015)(WROBEL et al., 2014)(KAUPPILA et al., 2009)(UZNANSKI et al., 2010).

$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \tag{2.2}$$

$$Q_{coll} = 10.8 \times L \times LET \tag{2.3}$$

where:
Q_{coll} is the total charge collected in the junction;
τ_α is the collection time constant for the device;
τ_β is the ion track establishment time constant;
L is the depth of the ion track into the silicon.

The critical charge is the minimum charge required for the generated pulse to change the output state of the affected logic gate and/or the stored data of a memory cell, for example. Besides depending on the total charge collected by the junction, it also relies on the duration of the transient pulse and the supply voltage of the analyzed device. For this, a parameter called "switching time" t_{th} is defined, which corresponds to the time interval from the incidence of the particle in the substrate until when the voltage generated reaches the threshold voltage of the device (WANG; AGRAWAL, 2008). At that time, the output capacitor will be charged with the critical charge Q_{crit} and can be calculated by integrating the value of the transient current into the affected node as in:

$$Q_{crit} = \int_0^{t_{th}} I(t)dt \tag{2.4}$$

A condition for the transient pulse to propagate is that the induced voltage must be greater than or equal to the voltage generated by the critical load in the device, i.e., it must follow the Equation 2.5 (WANG; AGRAWAL, 2008):

$$V \geq Q_{crit} = \frac{1}{C}\int_0^{t_{th}} I_{drain}(t)dt \tag{2.5}$$

For example, if the output capacitance of a circuit is equal to $C = 100fF$ and the total charge collected is $Q_{coll} = 0.65pC$, the voltage amplitude induced by the transient pulse is:

$$V = \frac{0.65pC}{100fF} = \frac{0.65 \times 10^{-12}C}{100 \times 10^{-15}F} \tag{2.6}$$

$$V = 6.5V \tag{2.7}$$

Note that for a smaller output capacitance, and for the same total load collected, the amplitude of the induced voltage is higher. For this reason, the susceptibility of current technologies for SET and SEU occurrence is pronounced, even with the incidence of energetically low particles. Due to the reduction of the intrinsic capacitances of the integrated circuits, particles that previously did not pose a threat to the proper functioning of the circuits now already have enough energy to induce a considerable voltage pulse in the output nodes. For a transient pulse generated by a particle with $LET = 1.46MeV\text{-}cm^2/mg$, following the Equation 2.3, the total collected charge for this particle with $L = 2\mu m$ would be:

$$Q_{coll} = 10.8f \times 2\mu \times 1.46M \tag{2.8}$$

$$Q_{coll} = 31.5fC \tag{2.9}$$

If the transient current pulse is sufficiently high, the radiation impact can induce permanent damage (destructive SEEs) such as Single-Event Gate Rupture (SEGR) or Single-Event Latch-up (SEL) (MUNTEANU; AUTRAN, 2008). The SEE sensitivity can be measured in terms of soft error rate (SER) or the Error Cross-Section (σ_{SEU}). The SER expresses the probability of a soft error occurs at usual conditions. It is typically measured as Failure In Time (FIT), which relates to the number of failures in 10^9 hours of operation. On the other hand, the σ_{SEU} represents the sensitive area of a design as it expresses the ratio of the number of events and the total particle fluence as defined in Equation 2.10 (VELAZCO; FOUILLAT; REIS, 2007).

$$\sigma_{SEU} = \frac{\#Events}{fluence} = \frac{\#Events}{[\frac{\#particles}{cm^2}]} \tag{2.10}$$

The SER and σ_{SEU} are obtained in the SEE characterization of a design throw irradiation testing campaigns or even by simulation methods in order to predict information of error probabilities and reduce testing cost.

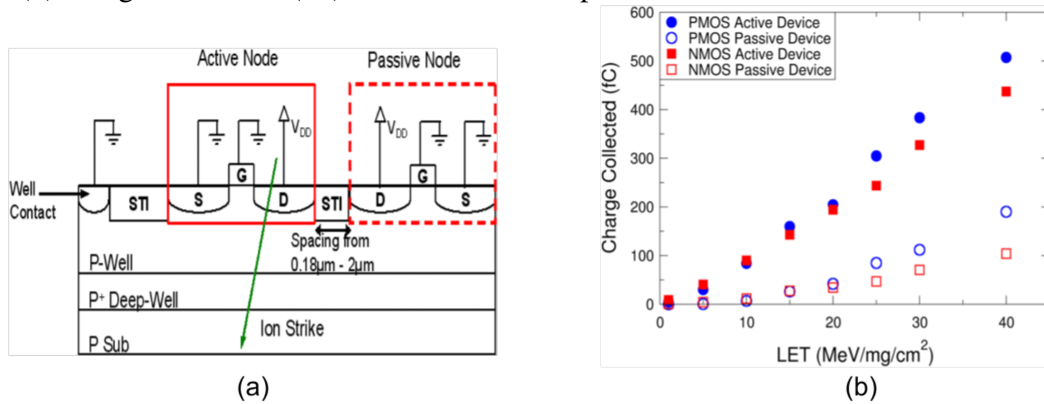
2.2.1 Emerging Effects at Advanced Technologies

Driven by the eager to achieve improved performance and functionality, VLSI circuits are denser and operating at low supply voltage, increasing the probability of SEE due to radiation ionization into the matter. Additionally, the high-density integration and reduction on the nodal capacitances have enhanced the charge sharing effect at advanced technologies, thereby increasing its susceptibility to radiation effects (OLSON et al., 2005). The charge sharing effect is characterized by the close proximity of adjacent devices, leading to the multiple node charge collection from a single ion strike. For instance, two adjacent NMOS devices are depicted in Figure 2.7 (a). As the distance between devices is reduced, an active node, i.e., the stroke node by the ion incidence and actively collecting the deposited charge, is in close proximity to an adjacent node; therefore, carriers may be able to diffuse at the passive adjacent node and induce a secondary transient current pulse (AMUSAN et al., 2006).

The charge collection of the PMOS and NMOS devices are investigated by Amusan et al. (2006). The active and passive device collected charges are shown in Figure 2.7 (b). The passive PMOS device was able to collect 40% of the total charge collected by the active device, while the passive NMOS collected less than 25%. Besides the carrier diffusion process, the bipolar amplification effect is also responsible for the enhancement of charge sharing, explaining the higher collected charge for the passive PMOS device than for the passive NMOS device (AMUSAN et al., 2006)(LIU et al., 2009).

Further, due to this mechanism, a single ion strike can lead to two or more bits from the same word to be upset in a memory (GIOT et al., 2008). It is known as Multiple-Bit Upset (MBU), and within the downscaling of technology, it has significantly contributed to the total SER (BORUZDINA et al., 2015)(EBRAHIMI et al., 2016). Also, a single particle strike can lead to multiple cell upsets (MCU) in combinational designs. Different benchmark circuits were synthesized to $45nm$ (planar device) and $15nm$ (FinFET device) Nangate Standard Cell library and the probability of multiple affected cells was evaluated in function of the particle energies in (EBRAHIMI et al., 2016). The occurrence probability of MCU is depicted in Figure 2.8 for each benchmark circuit with different particle

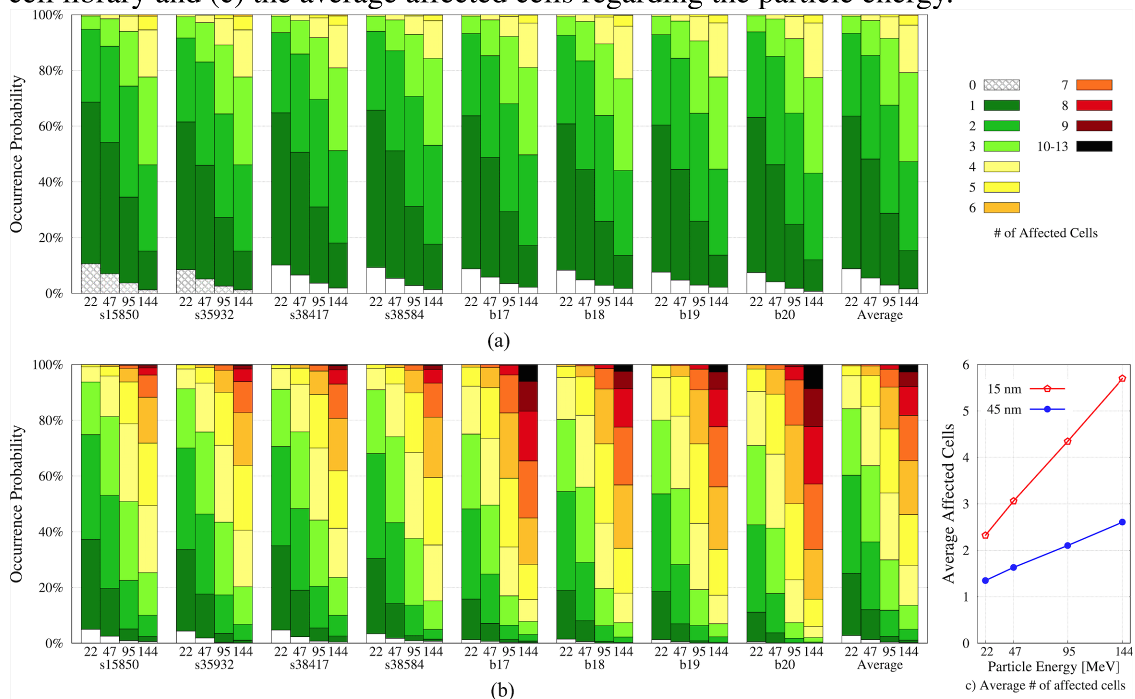
Figure 2.7: (a) configuration of adjacent devices which enhances the charge sharing effect and (b) charge collection (fC) for the active and passive devices



Source: (AMUSAN et al., 2006).

energies at both technology nodes. The results reveal that the average number of upset cells by a single particle strike is almost doubled from 45 to 15 nm. Also, the $15nm$ technology node exhibited a stronger relation to the particle energy as it provides a steep increase of the average affected cells as the energy is increased, see Figure 2.8 (c).

Figure 2.8: Occurrence probability of MCU by particle strikes with 22, 47, 95, and 144 MeV for benchmark circuits synthesized to (a) $45nm$ and (b) $15nm$ Nangate standard cell library and (c) the average affected cells regarding the particle energy.



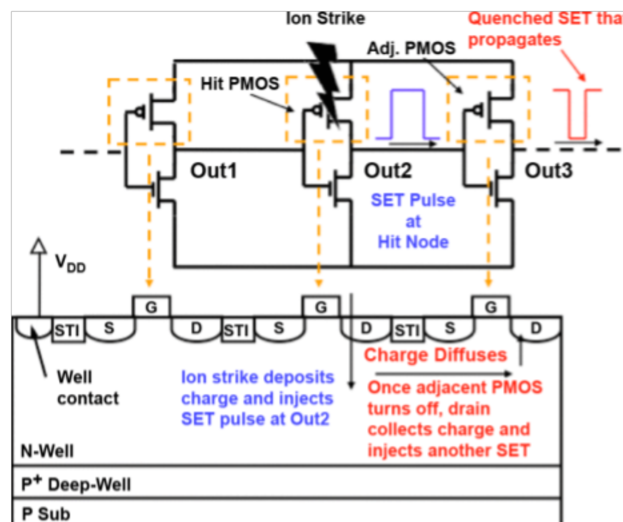
Source: (EBRAHIMI et al., 2016).

The sensitivity to MCU/MBU is dependent upon a variety of factors, as the Linear Energy Transfer (LET), the bipolar amplification effect, temperature variation, different angle and direction of the ion strike and so on (GIOT et al., 2008)(BORUZDINA et al.,

2015). As the conventional fault-tolerant techniques rely on the assumption of single node charge collection, such as the Dual-Interlocked Storage Cell (DICE) latch and TMR design, the SEE mitigation approach becomes more complicated as emerging effects are observed at advanced technology nodes.

Although the charge sharing mechanism mostly induces a negative effect by affecting a greater number of adjacent cells, some researchers have noted that it can also reduce the SET pulse width in combinational cells (AHLBIN et al., 2009)(ATKINSON et al., 2011). As the signal propagation time in deeply scaled technology is reduced, the multi-collection process provided by charge sharing occurs with a similar time constant. This phenomenon can lead to shortening the SET pulse width, and it is known as the Pulse Quenching Effect (AHLBIN et al., 2009)(AHLBIN et al., 2010). Figure 2.9 shows the schematic of a three-stage inverter chain and its respective PMOS devices in a cross-section perspective. Consider the input signal of the first inverter is at a low level, it will lead to the second PMOS device to turn OFF while the first and third are ON. If an ion strikes the sensitive off-state PMOS transistor of the second inverter as in Figure 2.9, the resulting SET pulse at OUT2 will propagate to the next inverter, turning the adjacent PMOS device OFF. By doing so, the third PMOS device will be susceptible to the charge collection by diffusion of the carriers from the charge sharing mechanism. It just occurs due to the delayed charge collection at the stroke device and the propagation of the generated SET to the adjacent device, allowing it to collect the carriers from charge sharing effect and inducing a transient pulse to revert the output of the chain as shown in Figure 2.9.

Figure 2.9: SET Pulse Quenching Effect in a inverter chain.

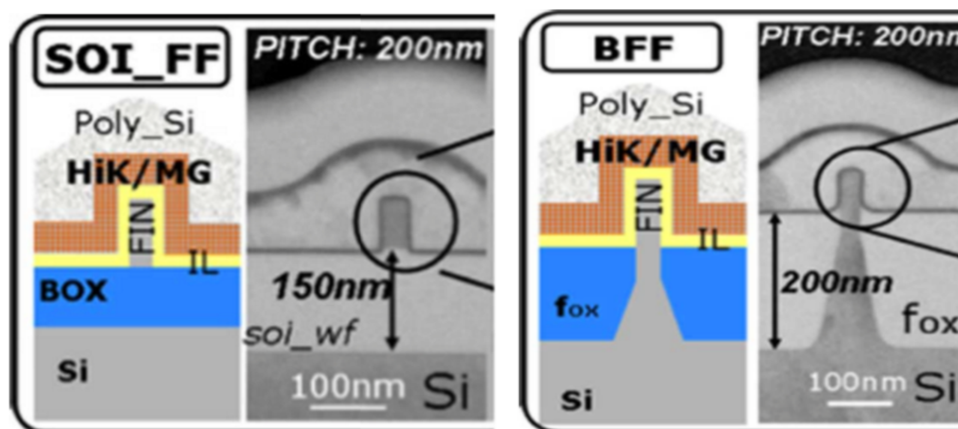


Source: (AHLBIN et al., 2009).

If two adjacent devices collect charge simultaneously, the overall SET pulse can be reduced in virtue of charge sharing effects and consequently decreasing the Single-Event vulnerability of the circuit (ATKINSON et al., 2011) (ENTRENA et al., 2012). A layout technique based on the charge sharing and pulse quenching effect is proposed in (ATKINSON et al., 2011) to reduce the single-event cross section of conventional logic cell layouts. Another work has proposed a cell-placement approach to mitigate multiple transient faults by considering pairs of nodes that induce the pulse quenching effect (ENTRENA et al., 2012).

Recently, with the breakthrough of the multigate transistors, as the FinFET technology, extensive research has been developed to understand the behavior of such devices under radiation effects (CHATTERJEE et al., 2014) (ARTOLA; HUBERT; ALIOTO, 2014) (KING et al., 2017) (NSENGIYUMVA et al., 2017) (AGUIAR; MEINHARDT; REIS, 2017). The device structure is very important to be considered for the radiation resilience analysis, especially for the VLSI designs at advanced technology nodes. The usage of tridimensional devices such FinFET leads to changes in the sensitive volume and the charge collection related to a particle strike (NSENGIYUMVA et al., 2017). Experimental results can be found in (EL-MAMOUNI et al., 2012), a work developed at Vanderbilt University in cooperation with Imec and Sandia National Laboratories. This paper compared the transient currents induced by heavy ions in bulk and SOI FinFETs. The cross sections of both analyzed devices are illustrated in Figure 2.10.

Figure 2.10: Cross Section of a SOI and bulk FinFET

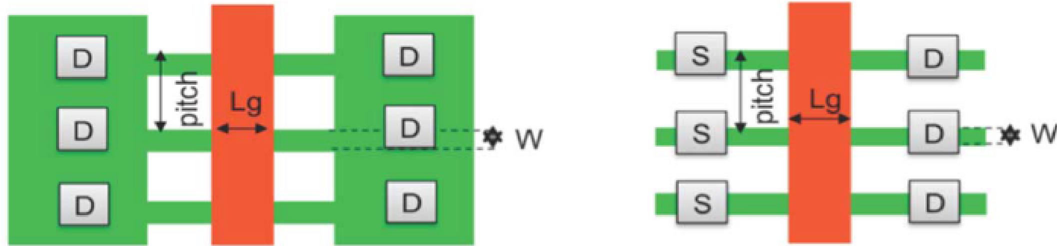


Source: (EL-MAMOUNI et al., 2012).

In a first moment, two different junction contact schemes were evaluated: the dumbbell contacts and the saddle contacts (Figure 2.11 illustrates the top layout view for both contacts). The dumbbell contact scheme is the conventional one (identical to a planar MOSFET contact), with a large area of the drain region. Besides touching only

the top surface, the saddle contacts touch the sidewalls of the fins as well, reducing the contact resistance. The main drawbacks of the sophisticated contact configuration are the contact to fin alignment and the contact pitch which needs to be as small as the fin pitch (COLINGE et al., 2008).

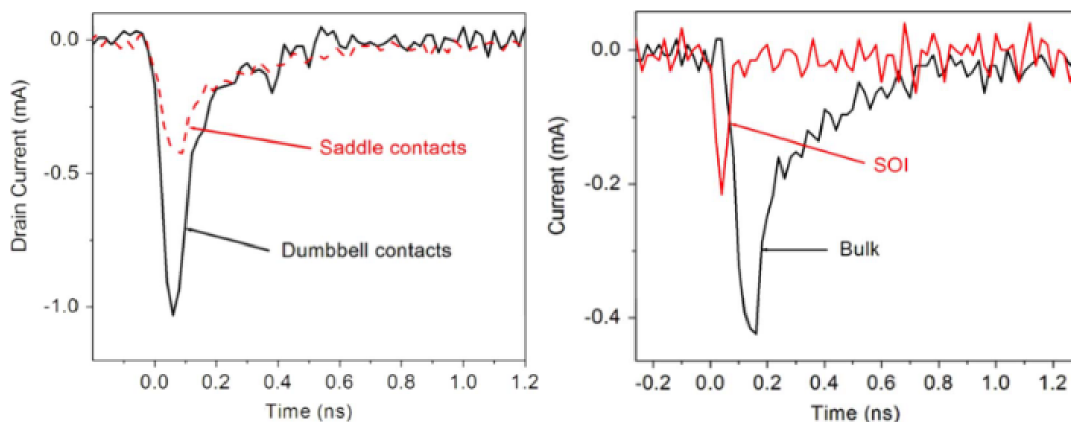
Figure 2.11: Layout for Junction Contact Schemes



Source: (EL-MAMOUNI et al., 2012).

Devices with the traditional dumbbell contacts have shown a maximum transient of 40% greater than the saddle contacts. Further, on average, the FinFETs with saddle contacts collected about 17% less charge than the amount collected by the FinFETs with dumbbell contacts (EL-MAMOUNI et al., 2012). However, both contacts show similar slow component (diffusive component) of the current transients. It means that reducing the area of the drain region does not affect the diffusion contribution to the charge collected in these devices as seen in Figure 2.12. These results highlight the importance of the drain contact and the layout design to achieve robustness to the radiation effects (SIMOEN et al., 2013).

Figure 2.12: Induced Transient Current pulse in the drain for (a) different contact schemes and (b) diferent substrates (SOI and Bulk)



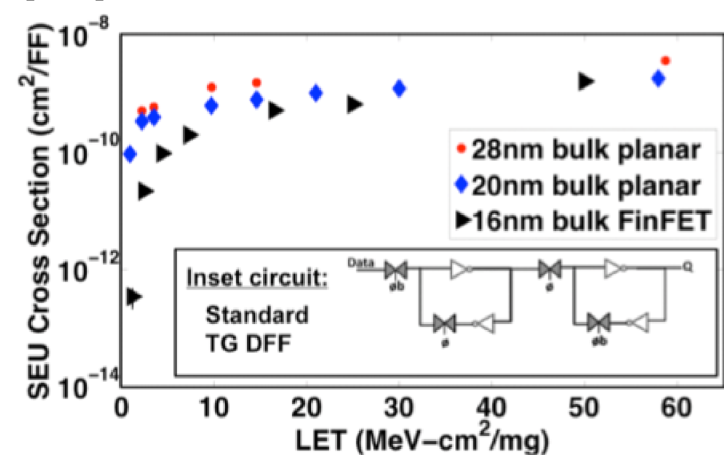
Source: (EL-MAMOUNI et al., 2012).

Comparing to the bulk device, it was verified that SOI FinFET shows current transients with lower amplitude, smaller FWHM ($\sim 50ps$) and negligible tails (EL-MAMOUNI

et al., 2012). As expected, the Buried Oxide (BOX) in the SOI FinFETs isolates the fin from the substrate, eliminating the diffusion component in the drain current transient. This explains the absence of the tail and the lower amplitude of the current.

Different cross-section trend for heavy ions was observed for flip-flop (FF) designs at $16nm$ bulk FinFET compared to planar bulk $20nm$ and $28nm$ FFs in (NSENGIYUMVA et al., 2016). For low-LET particles, the FF designs at FinFET exhibited SEU cross sections orders of magnitude as shown in Figure 2.13. However, for high LET particles, the SEU cross sections for FinFET-based FF were very comparable to the ones obtained for its bulk planar counterparts. One possible explanation for this behavior is that the SET pulse widths induced for LET >= $10\ MeV\text{-}cm^2/mg$ are wider than the feedback loop delay of $11ps$ provided by the FF designs at $16nm$ bulk FinFET (NSENGIYUMVA et al., 2016).

Figure 2.13: Experimental SEU Cross Section for $16nm$ bulk FinFET, $20nm$ and $28nm$ bulk planar D Flip-Flop (DFF)



Source: (NSENGIYUMVA et al., 2016).

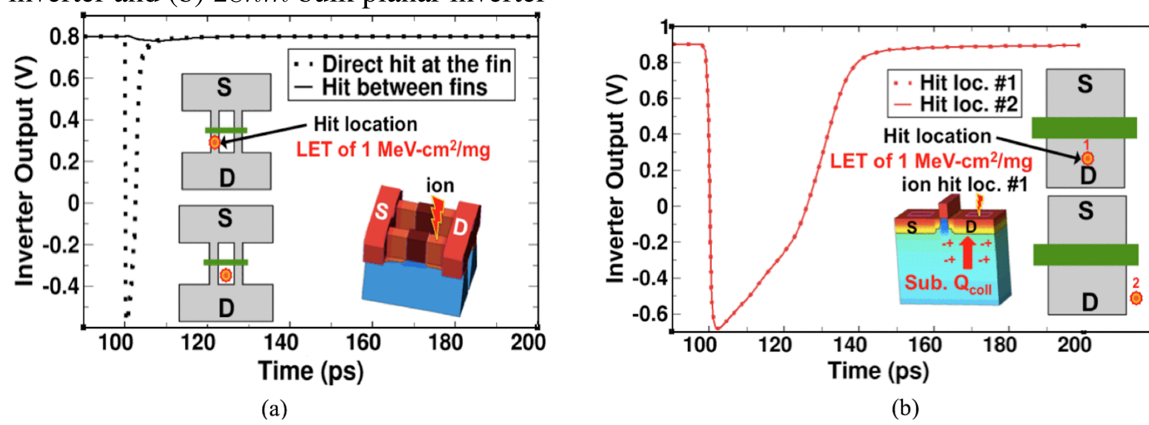
Later, in (NSENGIYUMVA et al., 2017), the authors investigated the FinFET structural effects on the SE cross-section to better understand this FinFET behavior for low LET particles. Through 3D TCAD simulations, the SET response of $16nm$ bulk FinFET and $28nm$ planar bulk inverters were evaluated under different hit locations. The impact of transistor structure and hit location for low LET particles is shown in Figure 2.14.

The FinFET inverter has exhibited a strong SET dependence on the strike location for the LET of $1\ MeV\text{-}cm^2/mg$). When the strike was evaluated between the fins, no transient pulse was observed. However, for particle hit exactly at the fin structure, a narrow, but observable, SET pulse was observed at the inverter output. On the other hand, the radiation response for the planar inverter showed no dependence on the strike location

(NSENGIYUMVA et al., 2017).

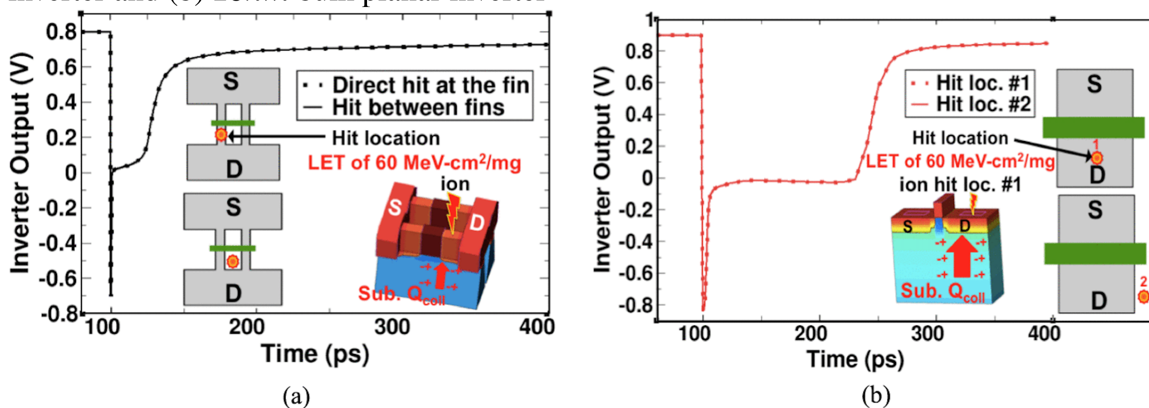
Additionally, the heavy-ion impact for LET of 60 MeV-cm^2/mg was also evaluated to verify the dependence of the SET response of FinFET for high LET particles. As shown in Figure 2.15, no dependence was observed to either device technologies. The results revealed that the SET response for bulk FinFET based circuit loses its dependence on the strike location due to the enhanced substrate diffusion charge collection at high LET particles (EL-MAMOUNI et al., 2011) (NSENGIYUMVA et al., 2017).

Figure 2.14: 3D TCAD Simulations for low LET particles for (a) $16nm$ bulk FinFET inverter and (b) $28nm$ bulk planar inverter



Source: (NSENGIYUMVA et al., 2017).

Figure 2.15: 3D TCAD Simulations for high LET particles for (a) $16nm$ bulk FinFET inverter and (b) $28nm$ bulk planar inverter



Source: (NSENGIYUMVA et al., 2017).

With the introduction of different device structures and novel materials, the understanding and the mitigation techniques of radiation effects need to be reassessed cautiously in order to accurately predict the radiation susceptibility for future advanced technology nodes.

2.2.2 Monte-Carlo Predictive Simulation for SEE

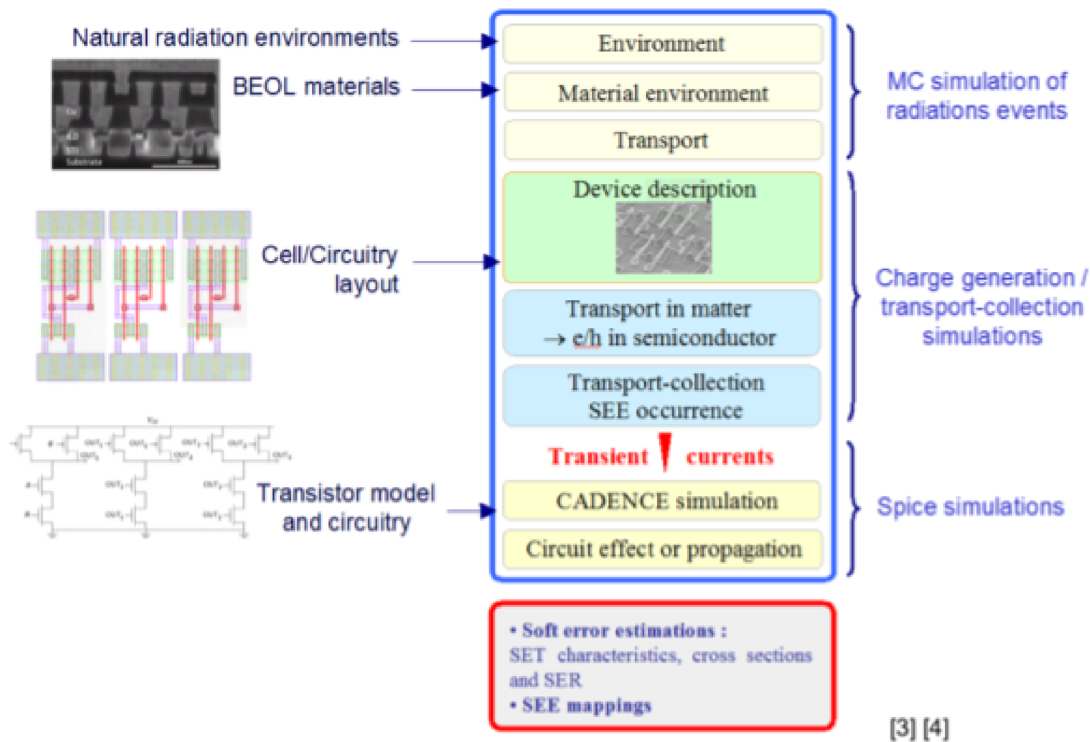
The analysis of SEE in scaled technologies requires dedicated test campaigns to estimate the design failure rates and to further improve its robustness through specific mitigation approaches (ARTOLA et al., 2015). The characterization of circuits under radiation effects is a complex and expensive process. However, the advancement in microelectronics has provided the possibility of high-performance computers with very cost-effective simulation approaches in science and engineering applications. For example, the modeling and simulation of device physical phenomena compose a very effective approach to provide predictive information regarding SEE susceptibility and reduce the radiation experiments (MUNTEANU; AUTRAN, 2008). Further, new emerging phenomena as described in the last subsection and different device structures or conditions can be explored in order to achieve a broader understanding of the implications of radiation effects in electronic systems.

The modeling of radiation effects on electronic systems depends on the structure of the devices (its geometry and materials), the circuit design itself and technology parameters such as the supply voltage and Front-End Of Line (FEOL) and Back-End Of Line (BEOL) layers. Therefore, many multiple scales and multi-physics approaches based on Monte-Carlo simulations have been developed in the literature (RAINE et al., 2011b)(WEULERSSE et al., 2011)(WARREN et al., 2007)(HUBERT et al., 2009)(REED et al., 2015). A complete description of several tools developed using a Monte-Carlo approach to analyze SEE in microelectronics is chronologically reviewed in (REED et al., 2013).

One example from this extensive list is the MUSCA SEP3 tool, which is a single event effects prediction tool based on a Monte-Carlo approach developed at ONERA The French Aerospace Lab since 2007 (HUBERT et al., 2009). The prediction tool allows for performing a full flow of simulations from the interaction of the radiation particles with the device down to the occurrence of the soft error in the circuit, as shown in Figure 2.16. The complete principle of the modeling is reported in previous works (ARTOLA et al., 2011)(HUBERT; ARTOLA, 2013)(HUBERT; ARTOLA; REGIS, 2015).

These simulations use GEANT-4 database for a complete description of the generation of free carrier (nuclear interaction, ionization, etc.). The 3D radial distribution of generated charges in the silicon is calculated for each incident particle considering the BEOL (RAINE et al., 2011a). The modeling of the charge diffusion accounts for the am-

Figure 2.16: SEE Simulation flow for soft error prediction using MUSCA SEP3



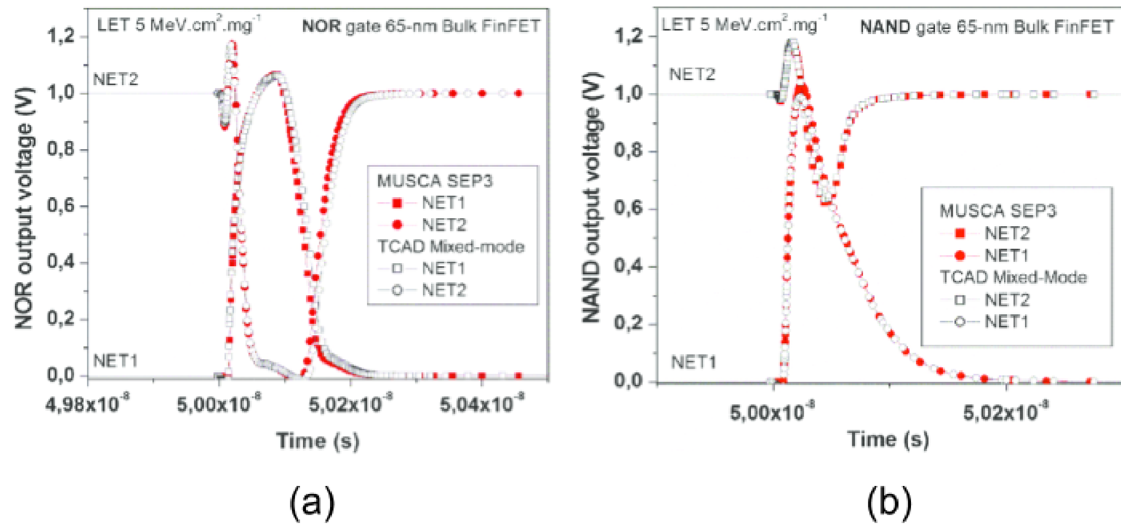
Source: (ARTOLA; HUBERT; ALIOTO, 2014).

bipolar diffusion mechanisms and recombination processes (ARTOLA et al., 2011). The modeling of the charge collection accounts for the dynamic transport and the multi-charge collection mechanisms as the charge sharing and the pulse quenching effects (HUBERT et al., 2009)(ARTOLA; HUBERT, 2016), the bias voltage, the layout, the bipolar amplification, the shallow trench isolation (STI) and the fabrication process.

The bipolar amplification model depends on two mechanisms. First, the model uses the equivalent access resistances of the tri-gate device to determine the triggering of the bipolar transistor. Second, the model takes into account the variability of the amplification of charge collection as a function of LET (ARTOLA; HUBERT; SCHRIMPF, 2013). The tool was extensively validated for different devices and technology nodes, including FinFET technology (ARTOLA et al., 2011)(ARTOLA; HUBERT; SCHRIMPF, 2013)(HUBERT; ARTOLA, 2013)(ARTOLA; HUBERT; ALIOTO, 2014)(HUBERT; ARTOLA; REGIS, 2015). The SET response from the MUSCA SEP3 is in agreement with the results obtained from the TCAD mixed-mode simulation as shown in Figure 2.17.

For this comparison, the authors claim to choose a LET of $5\ MeV\text{-}cm^2/mg$ to be able to represent the secondary ions induced by neutrons through indirect ionization (ARTOLA; HUBERT; ALIOTO, 2014). In Figure 2.17 (a), the induced SET pulse was able to propagate to the next logic gate, while in Figure 2.17 (b) the SET pulse only

Figure 2.17: MUSCA SEP3 Validation for FinFET devices through 3D CAD mixed-mode simulations. An NOR2 and NAND2 logic gate is evaluated under a particle hit with LET of 5 $MeV\text{-}cm^2/mg$



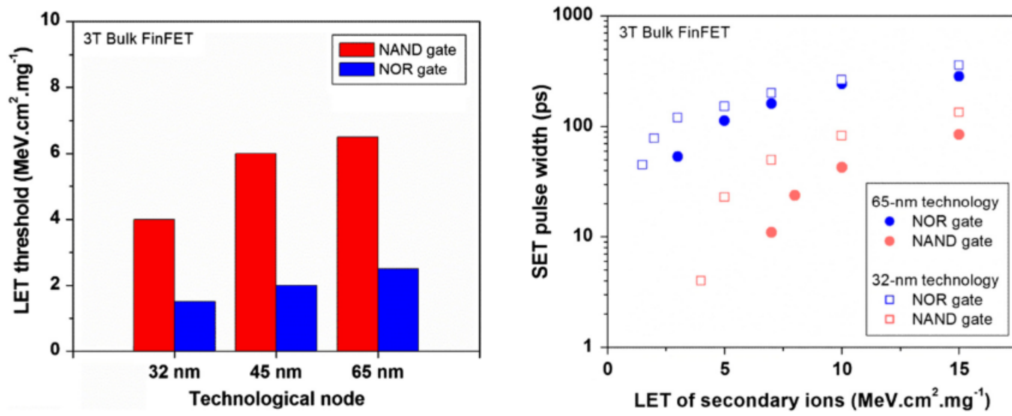
Source: (ARTOLA; HUBERT; ALIOTO, 2014).

induced a small disturbance in the output signal, i.e. electrical masking occurred.

After validating the predictive tool, a comparative soft error evaluation for the layout of the NAND2 and NOR2 logic gates designed at bulk FinFET is evaluated regarding the SET pulse width, the threshold LET and the SET cross section (ARTOLA; HUBERT; ALIOTO, 2014). The impact of supply voltage and the drive strength are also considered on the soft error sensitivity evaluation. Due to the width quantization of FinFET devices, its drive strength can only be improved by increasing the number of fins, i.e., transistor sizing becomes a discrete technique based on the number of fins. The LET threshold ($MeV\text{-}cm^2/mg$) and SET pulse width (ps) for both analyzed logic gate can be seen in Figure 2.18. It is interestingly to note that the NAND gate has shown to be less sensitive with a higher LET threshold and narrower SET pulse width than the NOR gate.

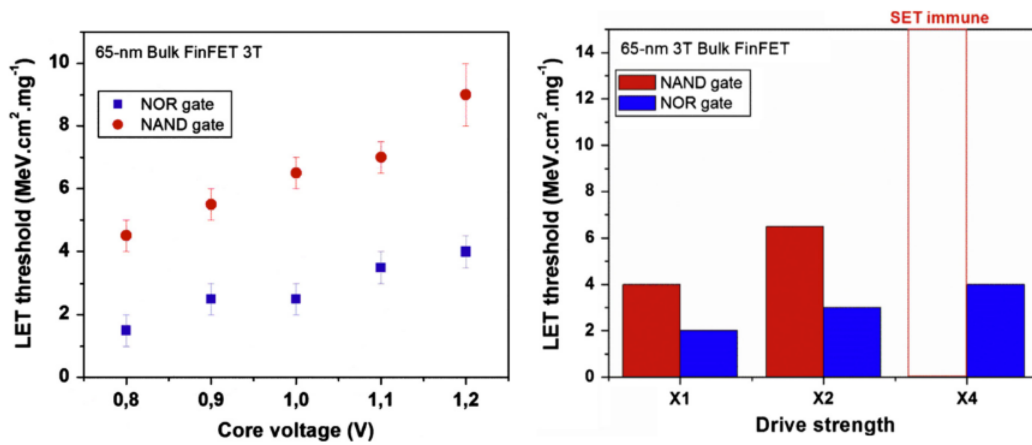
Another fact is that $32nm$ technology node is more sensitive to radiation effect, i.e., lower LET threshold and wider SET pulse width. The impact of supply voltage and the drive strength on the LET threshold can be observed in Figure 2.19. As expected, the radiation susceptibility is dependent on the supply voltage and the strength of the cell. The LET threshold can be increased up to 60% (38%) with an increase of 20% of the supply voltage for the NOR (NAND) gate (ARTOLA; HUBERT; ALIOTO, 2014). Further, the drive strength improvement can also improve the robustness of the cells. For example, an NAND2 X4 has shown to be completely immune to SETs induced by atmospheric neutrons.

Figure 2.18: MUSCA SEP3 Validation for FinFET devices through 3D CAD mixed-mode simulations



Source: (ARTOLA; HUBERT; ALIOTO, 2014).

Figure 2.19: MUSCA SEP3 Validation for FinFET devices through 3D CAD mixed-mode simulations



Source: (ARTOLA; HUBERT; ALIOTO, 2014).

3 FINFET TECHNOLOGY

Firstly, this chapter explains the unavoidable effects encountered for deeply scaled devices in advanced technology nodes. Then, it is presented the novel devices used to overcome the limiting barriers of technology scaling.

3.1 CMOS Scaling

At the microelectronics industry, the silicon planar MOSFET devices was the dominant technology since the 1980s (LEE, 2016). The scaling of technology has given to MOSFET transistors the possibility of improving performance and cost metrics over the years. However, the atomic-scale features of advanced technology nodes are detaining it from scaling further (FERAIN et al., 2011). Short-channel effects (SCEs), such as increased leakage current, are some of the main challenges to be surpassed in order to keep the pace of transistor scaling and its improvement in power and performance. As the device channel length is reduced, the drain potential influence on the channel increases, leading to a degradation on the gate effectiveness of controlling the channel current.

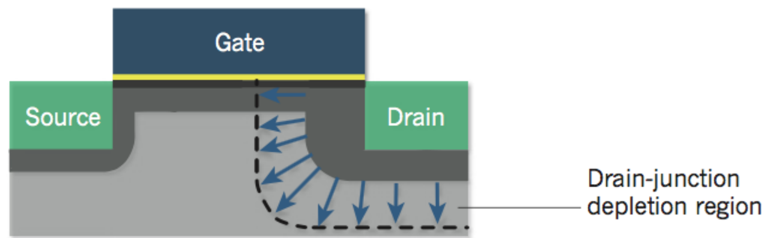
The reduction of gate oxide thickness was pointed as a solution to reduce these effects, though as the thinner the oxide layer, the greater is the gate leakage current (HU, 1996)(YEO; KING; HU, 2003). This issue can be observed in terms of power-supply voltage since the introduction of the 90nm technology node to the market. Instead of using the nominal supply voltage of 0.9V, as expected from the historical scaling trend, the industry has opted to use 1.2V to alleviate the leakage problem. Because of the observed increase in SCEs, new approaches are needed beyond 22nm to continue the improvement provided from device scaling. One approach is to use different device structures such as ultrathin body silicon on insulator (SOI) or multigate transistors (FERAIN et al., 2011)(LEE, 2016). The scope of this dissertation focus on the usage of multigate technology.

The scaling process of reducing the gate length L_G degrades the electrical characteristics of planar MOS devices over the past years. These degradation effects are commonly known as Short-Channel Effects (SCE) and downgrade transistor electrical characteristics significantly.

The SCE are induced by two primary constraints: the proximity between the source and drain region; and the distance between the gate electrode and the channel

region (FERAIN et al., 2011). The depletion region created by p-n junctions in the transistors penetrates the inversion layer, underneath the gate, reducing the effective channel length and consequently the gate controllability over the channel potential. This effect is known as Drain-Induced Barrier Lowering (DIBL) and it is illustrated in Figure 3.1. As the device drain voltage increases, the depletion region formed by the p-n junction increases and enhances the DIBL effect in the drain current. Therefore, this effect grows in importance as the feature size of transistors is reduced.

Figure 3.1: Drain-Induced Barrier Lowering (DIBL)



Source: (FERAIN et al., 2011)

Due to DIBL, the threshold voltage decreases as the drain voltage is increased, leading to increase in leakage current (FERAIN et al., 2011). As DIBL estimates the gate controllability over the channel electrostatics, it is used as a comparative parameter to measure the short-channel effect in nanoscale devices.

The MOSFET devices do not behave as a perfect switch, resulting in a subthreshold current between the drain and source when the transistor is in off-state, i.e., $V_{GS} < V_{TH}$. This undesired current contributes to the off-state current of the device (I_{OFF}), being a significant concern at advanced technologies due to the increase in the static power consumption (DADGOUR; LIN; BANERJEE, 2007). An alternative would be to increase the threshold voltage V_{TH} of the devices. However, besides the leakage reduction, it does also reduce the drive current (I_{ON} current), which is a figure of merit for the circuit performance. Additionally, for low power applications, it is required the adoption of devices which exhibit low I_{OFF} current with reasonable drive current I_{ON}. The Subthreshold Slope (SS) of a device relates the balance between its drive and off current. It expresses the rate for the exponential increase of drain current below the threshold voltage (subthreshold region) and it is defined by the relationship in Equation 3.1:

$$SS = \frac{\delta V_G}{\delta(\log I_D)} \tag{3.1}$$

The SS is expressed in millivolts per decade of current and it is a parameter used to measure the short-channel effect impact. A typical value for SS is between 60mV to 70mV per decade. The decrease of threshold voltage with decreased gate length is a well-known SCE called Threshold Voltage Roll-off (V_{TH} roll-off). The threshold voltage variation can be found by Eq. 3.2 (NEAMEN, 2003)

$$\Delta V_{th} = -\frac{qN_aW_mr_j}{C_{ox}L_{ch}}\left[\sqrt{1+\frac{2W_m}{r_j}}-1\right] \tag{3.2}$$

where: r_j is the depth of the source and drain junction, W_m the maximum width of the depletion layer, L_{ch} is the device channel length.

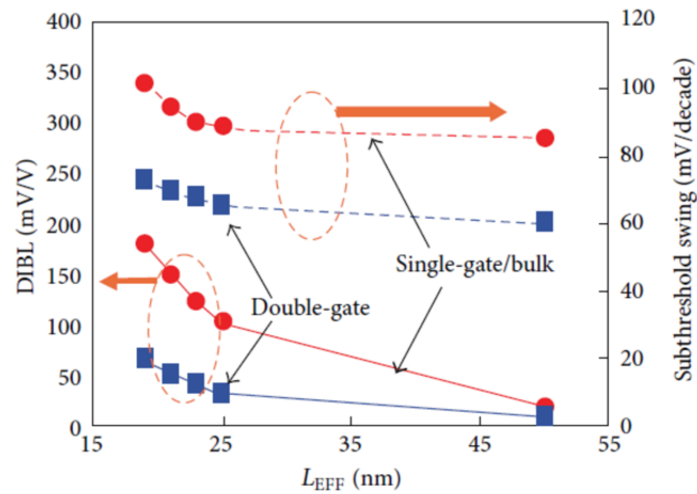
3.2 Multigate devices

The main challenge when dealing with short-channel devices is to reduce the SCE by providing better gate controllability over the channel. A variety of approaches have been conducted in the literature to overcome the short-channel effects previously discussed in this chapter. The usage of a thinner gate oxide increases the gate-to-channel capacitance, however, direct tunneling through the gate dielectric limits this approach in modern VLSI circuits (SHIN, 2016). Another approach would be higher channel doping concentration, which reduces the charge sharing between the gate and drain in the channel (YEO; KING; HU, 2003). However, this approach reduces carrier mobility and increases Gate Induced Drain Leakage (GIDL). Thus, one of the most effective approach was the restructure of the traditional planar MOSFET to multigate transistors, also known as MuGFETs devices (SKOTNICKI et al., 2005).

The first to propose a planar multigate device to reduce the SCE was Sekiwaga and Hayashi in 1984 (SEKIGAWA; HAYASHI, 1984). Later, in 1989, the fully depleted lean-channel transistor (DELTA), was the first double-gate MOSFET device to be fabricated (HISAMOTO et al., 1990). But only in 2011 a multigate transistor reached mass production. The third generation IntelR© CoreTM processor (code-named Ivy Bridge) was the first chip to ever use a multigate device such as the 22nm trigate transistor in a mass production scale (AUTH, 2012). The use of multiple gate electrodes makes MuGFETs superior to conventional planar MOSFET in terms of short-channel metrics, such as the SS, DIBL, and threshold voltage V_{TH} roll-off (BHATTACHARYA; JHA, 2014)(FERAIN et al., 2011). A comparison between planar single-gate and double-gate bulk devices

regarding DIBL and SS in function of the device channel (L_{EFF}) can be verified in Figure 3.2. The double-gate device has a great improvement in SCE metrics compared to the single-gate device. A higher doping concentration could improve the DIBL effect in the single-gate device, however it implies reduction on carrier mobility and increase in subthreshold leakage worsen the SS (NOWAK et al., 2004). Similarly, by reducing the doping concentration, an improvement on the SS metric could be observed at the cost of increased DIBL effect.

Figure 3.2: Comparison between Single- and Double-gate devices in terms of SCE metrics



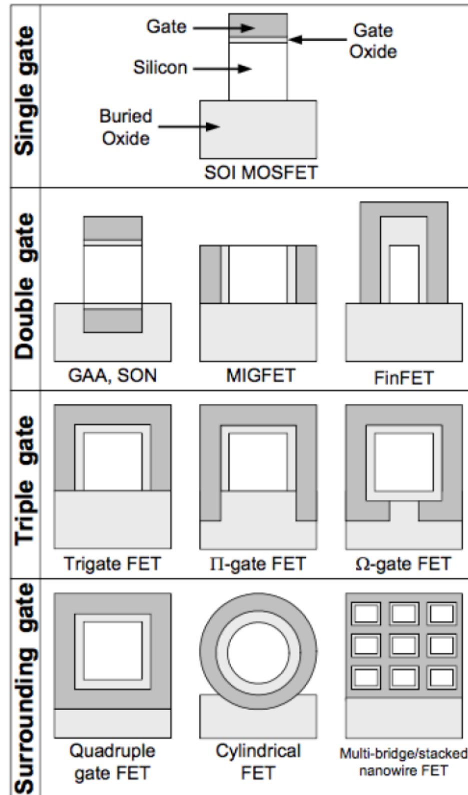
Source: (BHATTACHARYA; JHA, 2014)

Vertical multigate devices (or also named 3D transistors) have the gate electrode wrapped around a vertical silicon structure (called as "finger" or more commonly as "fin"), increasing the gate-channel capacitance (NOWAK et al., 2004)(SKOTNICKI et al., 2005). A higher gate-channel capacitance improves the gate controllability over the channel potential by reducing the coupling between source and drain regions (BHATTACHARYA; JHA, 2014)(FERAIN et al., 2011).

These devices originally were known as fabricated exclusively on SOI wafers. Although SOI-based devices avoid extra leakage path near the junction depth of the source/drain regions, it has higher wafer cost and higher defect density than bulk-Si wafers (COLINGE et al., 2008). Besides that, the thermal confinement encountered at fin-like structures are exacerbated due to the poor heat transfer rate at the thick buried oxide (BOX). In the Figure 3.3 it can be seen the classification of a variety of multigate devices built at SOI wafers.

Due to the aforementioned aspects and in order to be more attractive to the foundries, these devices are also available to be built on bulk-Si wafers (COLINGE et al., 2008)(BHAT-

Figure 3.3: Different architecture of Multigate devices (MuGFET) on SOI substrate

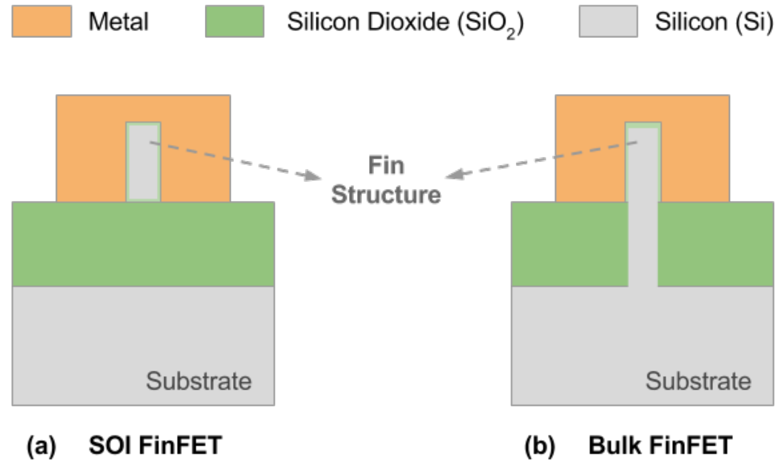


Source: (COLINGE et al., 2008)

TACHARYA; JHA, 2014). Figure 3.4 presents the cross-section of a SOI-based and bulk FinFET device for comparison. When the bulk FinFET was first reported in the literature, it was referred to as Omega (Ω) MOSFET. It happened due to its cross-section similarity to the Greek letter, as can be seen in the Figure 3.4 (LEE, 2016)(YANG et al., 2002). Among the devices of Figure 3.3, the double-gate FinFET (Fin-Shaped Field Effect Transistor) and Trigate MOSFET (Trigate fully-depleted MOSFET) are the most indicated as promising candidates to further transistor scaling due to good improvement in SCE metrics and similarity to planar CMOS manufacturing process (BHATTACHARYA; JHA, 2014)(HISAMOTO et al., 2000)(SUN et al., 2008). The trigate MOSFET device is commonly referred to as a FinFET device as well. Thus, in this work the term FinFET will be addressed to either a double-gate or a tri-gate device.

The FinFET devices are non-planar structures due to the adoption of three dimensional device channel formed in a finger of silicon, or more commonly called the fin (See Figure 3.4). At these devices, the fin dimension relates to the effective device channel width, W_{EFF}. A 3D cross-section of a FinFET device is drawn in Figure 3.5 and its important dimensions are highlighted: the fin height H_{FIN}, the fin thickness T_{FIN} and the gate length L_G. The effective channel width W_{EFF} of a single-fin device is defined by Equa-

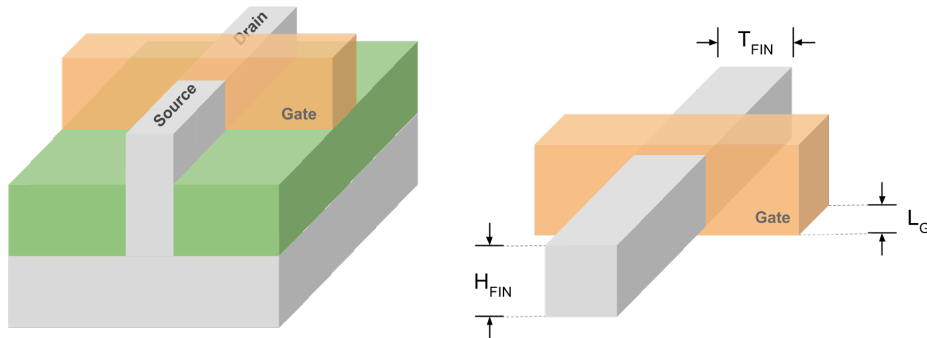
Figure 3.4: SOI FinFET (a) and Bulk FinFET (b)



Source: From the author

tion 3.3. However, the height and the thickness of the fin are two fixed parameter defined by process engineers at each technology node. Thus, the sizing of the FinFET transistors is addressed by the total number of parallel fins that connect the source and drain region of the device. This characteristic is known as width quantization, because the channel width is composed by a quantized value of the minimum (single-fin) width W_{MIN}, defined in Equation 3.3. Thus, the transistor sizing in FinFETs relies on the number of fins, where the effective channel width W_{EFF} can be rewritten from Equation 3.3 to Equation 3.4, where the total number of fins N_{FIN} are taken into consideration.

Figure 3.5: 3D cross-section of a Bulk FinFET and its important dimension: fin height H_{FIN}, the fin thickness T_{FIN} and the gate length L_G.



$$W_{MIN} = 2 \times H_{FIN} + T_{FIN} \tag{3.3}$$

$$W_{EFF} = W_{MIN} \times N_{FIN} \tag{3.4}$$

Due to the width quantization, the design flexibility of FinFET-based circuits which strongly rely on its transistor sizing might have its robustness compromised. For instance, the design of SRAM cells needs the adoption of co-optimization of the fin dimensions to enhance its performance, stability and robustness (GUPTA; ROY, 2013). More flexibility in the transistor sizing can be achieved with small fin heights, however, it leads to a greater number of fins increasing the device area. On the other hand, taller fin heights reduce the device area, but also reduce the flexibility of transistor sizing. Additionally, taller fin heights lead to structural instability which should be avoided due to the complexity of the manufacturing process (COLLAERT, 2005). To avoid such issues, the fin height is kept below four times the fin thickness (ALIOTO, 2011).

Discrete transistor sizing techniques applied to FinFET technology are lacking in the literature. In (POSSER et al., 2012), a gate sizing and continuous transistor sizing was proposed using Geometric Programming (GP) optimization to conventional planar devices. The sizing approach was to minimize the delay of sized Standard Cells by preserving the same power and area usage. The GP-based gate sizing was able to reduce the delay in 21%, on average. However, the transistor sizing reduced over 40% in delay and 2.9% in power compared to the gate sizing. Although transistor sizing presents better results, it has a longer run time (POSSER et al., 2012). The same authors have adapted this approach to consider the width quantization of FinFET devices in (POSSER et al., 2014). The transistor sizing solution provided by the GP optimization leads to a non-integer value which can not be directly applied to FinFET devices. Then, two techniques was used to define a discrete number of fins from the GP optimization: Truncation and Simple Rounding. The GP optimization solution W_{GP} is divided by the minimum (single-fin) sizing of a FinFET device, as in Equation 3.5, and the Truncation or Simple Rounding is applied to achieve a discrete number of fins N_{FIN}.

$$N_{FIN} = \frac{W_{GP}}{W_{MIN}} \tag{3.5}$$

3.3 Variability Effects

The evolution to innovative technologies brings new opportunities coupled with new challenges. Besides the well-known Short-Channel Effects (SCE), designers of VLSI circuits need to deal with variability effects due to increased complexity and lack of precision of the manufacturing process (SAPATNEKAR, 2011). Together with SCE, variabil-

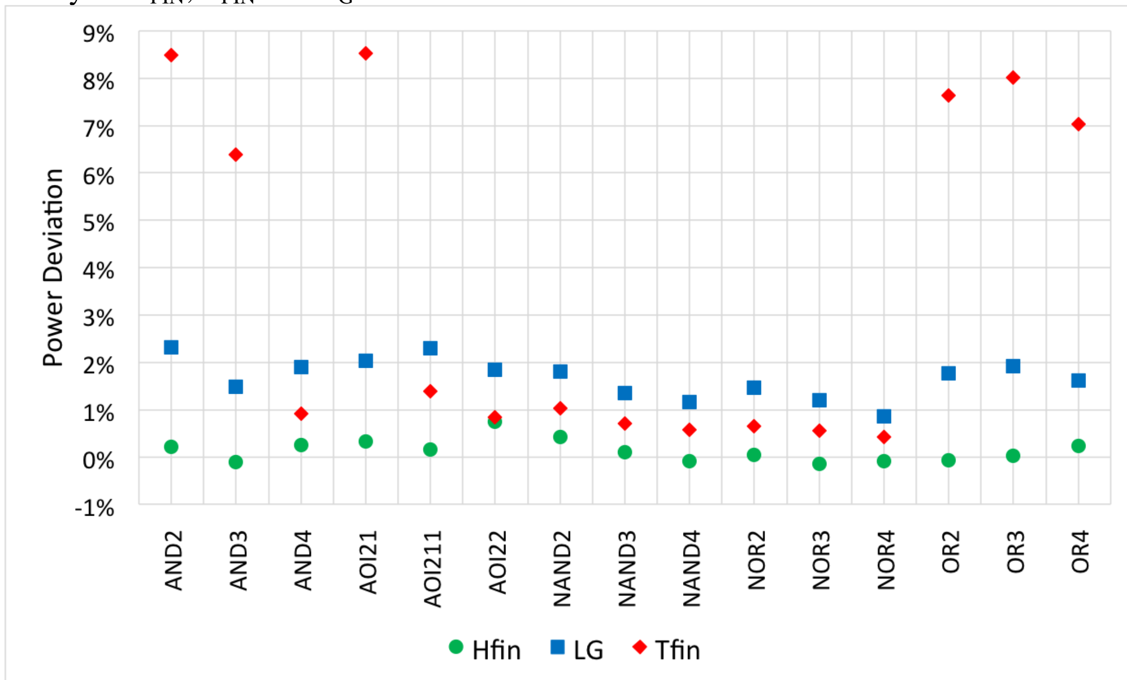
ity is a limitation to the further scaling of technology. The behavior of VLSI circuits is quite affected by variability effects, resulting in high deviation on performance and power consumption. As the microelectronics develops, challenges that were considered limiting, as the size of the die, chip manufacturing yield and productivity of the project, lost room for concern about the consumption and power dissipation, emerging new challenges such as variability in the manufacturing process, increased vulnerability to soft errors and degradation of components (aging) (BORKAR et al., 2003)(BORKAR, 2005). Additionally, the aging of circuits due to prolonged application of stress can lead to degradation in electrical characteristics or even catastrophic failures. Thus, the reliability of nanocircuit has been strongly affected by different sources of variability which leads to a degree of uncertainty in the design of modern VLSI circuits.

The impact of variability regarding system reliability is translated in a statistical distribution in the electrical characteristics of the devices and interconnections. One widely used technique to overcome this uncertainty degree is the adoption of design margins with respect to the worst-case scenario (SAPATNEKAR, 2011). For doing so, it is possible to provide designs with predictable parametric features.

3.3.1 Source of Variability

As stated before, the shrinking of technology dimensions has introduced the challenge of designing circuits accounting for a degree of uncertainty due to variations on the parameters initially specified in the design process. These deviations can be induced by many sources and can be classified as process variations, environmental variations and aging variations (SAPATNEKAR, 2011). A process variation is defined when a process parameter of the designed circuit has deviated from its nominal previously defined value. A major source of process variations is the precision of sub-wavelength lithography technology (KUHN et al., 2011). Due to the limitation of such technology, the length and width of the transistor channel deviate from the designed value. It is the primary cause of the occurrence of Line Edge-Roughness (LER), for example. Due to its small dimensions and aforementioned lithographic limitations, these process deviations can lead to aggressive Geometric Variability in physical parameters of fin-based structure devices (ZIMPECK et al., 2016). Figure 3.6 presents the impact of H_{FIN}, T_{FIN} and L_G on the total power consumption of basic logic cells. Some cells can reach up to 9% of power deviation from its nominal value.

Figure 3.6: Deviation on Power Consumption of basic logic cells due to Geometric Variability of H_{FIN}, T_{FIN} and L_G.

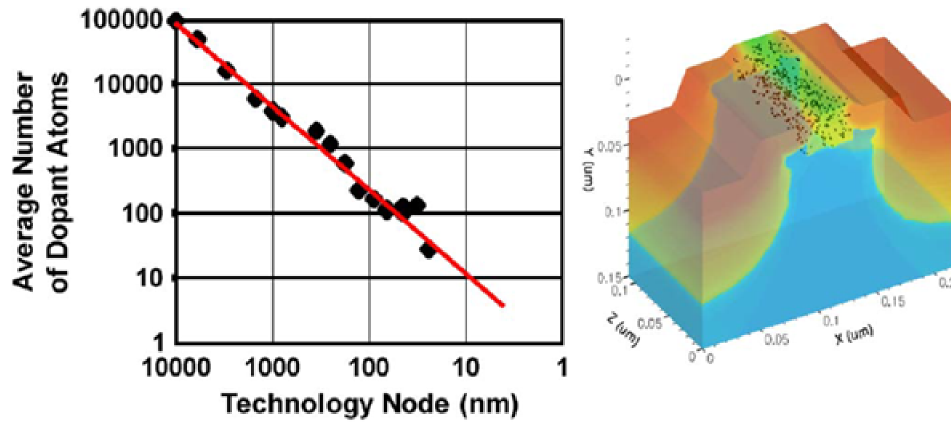


Source: From the author and published in (ZIMPECK et al., 2016).

Another primary source of process variation is the random dopant fluctuation (RDF) in the channel of the transistors. As the dimensions of transistors downscale, the number of dopant atoms in the channel decreases exponentially making it difficult to ensure the exact number and positions of dopant atoms in the implantation process (SAPATNEKAR, 2011). The Figure 3.7 shows the reduction of the average number of dopant atoms for each generation. It can be noticed the sharp reduction in the average of atoms as technology node is reduced, emphasizing the importance of the need to develop techniques to overcome process variability, mainly the effects of RDF in the channel of transistors (KUHN et al., 2011). However, as FinFET technology provides reduced SCE, the channel doping concentration is not required to be as high as the planar advanced technology. Therefore, the V_{TH} are not adjusted in accordance with the body doping concentration, but with the work-function of the metal gate. This approach reduces the effect of RDF in FinFET devices, however, new variability issues need to be addressed as the Metal-Gate Work-Function Fluctuation (WFF) and Geometric Variability (MEINHARDT; ZIMPECK; REIS, 2014)(ZIMPECK et al., 2016).

As previously discussed, the impact of Short-Channel Effects (SCE) has increased in deeply scaled devices. Thus, new approaches have been used to keep with the transistor scaling. Among them, concerning to the gate control over the channel potential, design-

Figure 3.7: Average Number of Dopant Atoms for technology node



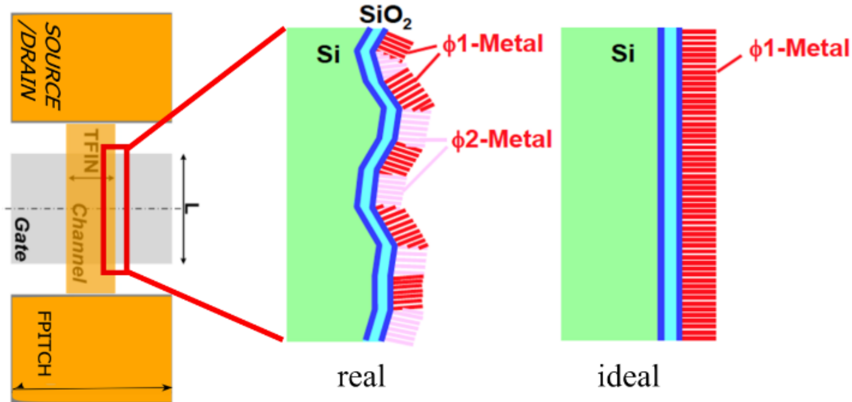
Source: (KUHN et al., 2011).

ers have first opted to increase the gate-to-channel capacitance by using a thinner gate oxide layer interface. However, the requirements for leakage current avoidance was no longer feasible by reducing the SiO_2 layer below to 1 nm (SHIN, 2016). Thus, the usage of high-k (HK) dielectric material has been adopted to work as an electrically thin and physically thick insulation layer interface. However, two major problems prevented the usage of the polysilicon gate together with high-k dielectric increasing the threshold voltage and reducing the mobility of electrons: Fermi Level Pinning and Phonon Scattering, respectively (DADGOUR et al., 2010a). Thus, besides lowering the gate resistance and increasing the on-current I_{ON}, the use of a metal gate was pointed as the solution for these two problems found in the polysilicon/high-k interface. After that, the high-k/metal gate (HKMG) technology was adopted ever since the 45nm technology node launch (MISTRY et al., 2007).

Despite the advantage of adopting metal gate in the MOS transistors, the orientation and granularity of the metal grains in the deposition phase (Atomic Layer Deposition - ALD) are not a controllable process, leading to multiple randomly oriented grains configuration. The Work-Function Fluctuation (WFF) is a process variability encountered in advanced technology nodes due to its dependency on the grain orientation of each metal grain, as shown in Figure 3.8.

Considering this multiple grain orientation, the total work function of a metal gate Θ_M can be calculated as Equation 3.6, where N is the total number of grains over the metal gate area, $X_1...X_N$ represent the random numbers of grains with work function of Θ_1 ... Θ_n, respectively (DADGOUR et al., 2010a). As the threshold voltage (V_{TH}) of a MOS device is a linear function of its gate work function, thus the WFF induces random V_{TH} variation.

Figure 3.8: Metal Grain Orientations in a HKMG transistor gate



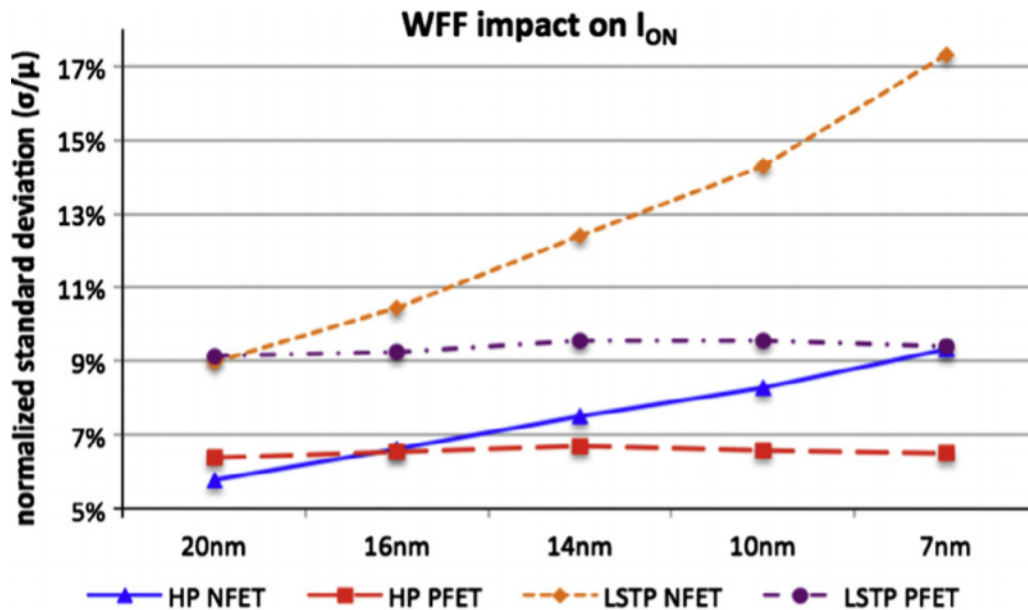
Source: (MEINHARDT; ZIMPECK; REIS, 2014).

$$\Theta_M = (\frac{X_1}{N})\Theta_1 + (\frac{X_2}{N})\Theta_2 + ... + (\frac{X_n}{N})\Theta_n \tag{3.6}$$

More information about the grain orientation and the metal-gate work-function fluctuation phenomenon can be found in (DADGOUR et al., 2010a)(DADGOUR et al., 2010b), where a statistical framework modeling this phenomenon is proposed and validated experimentally. Also, in (MEINHARDT; ZIMPECK; REIS, 2014), Standard Cells designed at 20nm HP FinFET were evaluated under WFF. It was observed that standard cells could suffer deviations about 8% in timing metrics, 24% in total power and above 60% in static power.

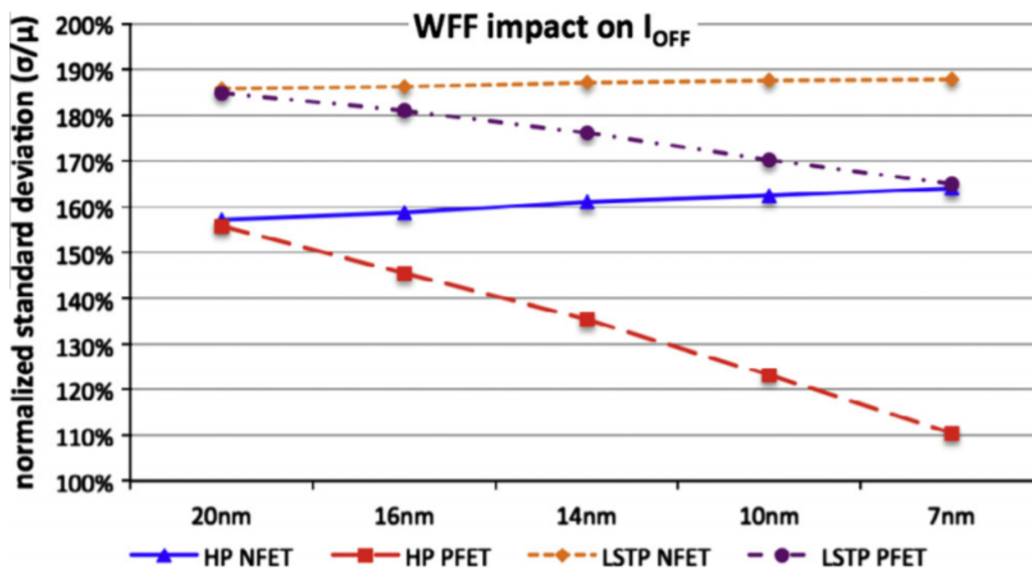
At (MEINHARDT; ZIMPECK; REIS, 2014), the impact of geometry variations due to process variability on the electrical characteristics, such as the drive current I_{ON} and the off current I_{OFF} of FinFET devices was investigated. The work has adopted the High Performance (HP) and Low Standby Power (LSTP) models for sub-20nm devices from PTM-MG models. The results appointed a low influence of gate length L_G, fin thickness T_{FIN} and fin height H_{FIN} variation on the I_{ON} of the devices analyzed. However, the work-function fluctuation (WFF) leads to a large deviation on I_{ON} for NFET and PFET devices at HP and LSTP model (MEINHARDT; ZIMPECK; REIS, 2014). As shown in Figure 3.9, the NFET devices are more susceptible to WFF as technology scales down. Within the scaling and aggressive process variability, I_{ON} can reach 17% of deviation in 7nm NFET LSTP devices. Additionally, the results have shown that I_{OFF} can be more than 100% deviated from its nominal value due to the WFF effect and, again, NFET devices proved to be the most susceptible (MEINHARDT; ZIMPECK; REIS, 2014). The results can be seen in Figure 3.10. This effect seems to be reduced with the technology scaling, however, it can still reach more than 65% of deviation at 7nm, for example.

Figure 3.9: Sub-20nm 3% of WFF tendency of deviation impact on I_{ON} for HP and LSTP devices.



Source: (MEINHARDT; ZIMPECK; REIS, 2014).

Figure 3.10: Sub-20 nm 10% of WFF tendency of deviation impact on I_{OFF} for HP and LSTP devices.

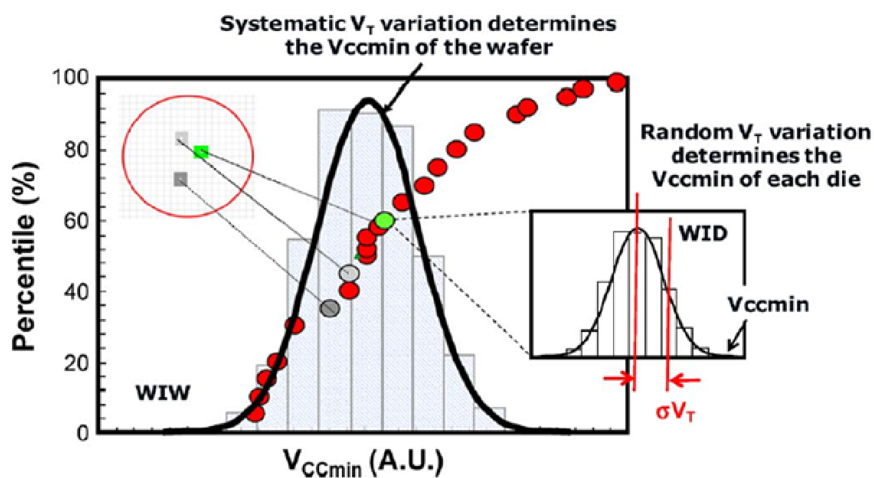


Source: (MEINHARDT; ZIMPECK; REIS, 2014).

The environmental variations, unlike process variation, is caused by dynamic factors, i.e. changes during the circuit operation, such as the supply voltage fluctuation, thermal effects and single event effects (SAPATNEKAR, 2011). In each new generation of technology, the number of transistors in a single chip greatly increases leading to an increase in the power density and imbalance in the thermal profile. These both variations affect directly the performance and power consumption of the nanometer designs (CHOI;

MURTHY; ROY, 2007)(KUHN et al., 2011). For process variability, statistical methods are used to optimize the manufacturing yield of a given design. However, the optimization regarding environmental variation needs to be carried under the worst-case analysis (SAPATNEKAR, 2011). As mobile applications are increasing, it is of utmost importance to ensure lower minimum operating supply voltage. Figure 3.11 highlights the impact of random variation of V_{TH} or the die minimum operating supply voltage VCCMIN and the systematic V_{TH} variation for the wafer.

Figure 3.11: Random and Systematic variations impact in minimum operating voltage



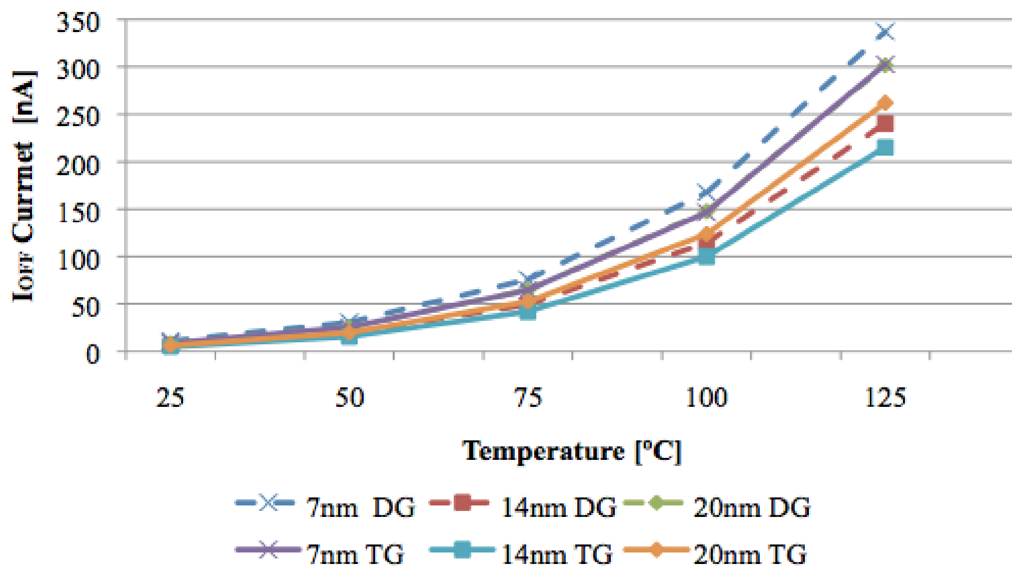
Source: (KUHN et al., 2011).

Intra-die power dissipation fluctuation leads to local temperature variation causing hot spots. This effect causes performance shifts throughout the chip. Transistor current is dependent on the channel mobility and threshold voltage that are temperature-dependent parameters (SAPATNEKAR, 2011). As temperature increases, the threshold voltage is reduced and the carrier mobility is degraded. The drain current I_D can increase depending on which effect is dominant: as the temperature increases, a threshold voltage reduction increases the I_D while mobility degradation reduces it. Thus, the performance of circuits may have negative temperature dependence when the delay is increased with temperature, or positive temperature dependence when the opposite is observed (GOEL; TRIPATHI, 2012).

Multigate devices have reduced thermal conductivity due to the confinement encountered at the fin structure. Thus, a greater increase in operating temperature with the increase in power density should be expected in these devices. However, changes in temperature affect system speed, power and reliability of these devices (ZHANG et al., 2016). In the temperature dependence region, circuits continue to speed up as temper-

ature increases. Higher temperatures can produce thermal runaway resulting from the exponential temperature dependence of leakage current, which may already be dominating the total power consumption in the nanoscale regime (MOHAPATRA; PRADHAN; SAHU, 2015). This behavior can be verified in Figure 3.12, which the I_{OFF} current exhibit an abrupt difference between the room temperature and a higher temperature.

Figure 3.12: I_{OFF} current for DG and TG FinFETs over a range of temperature



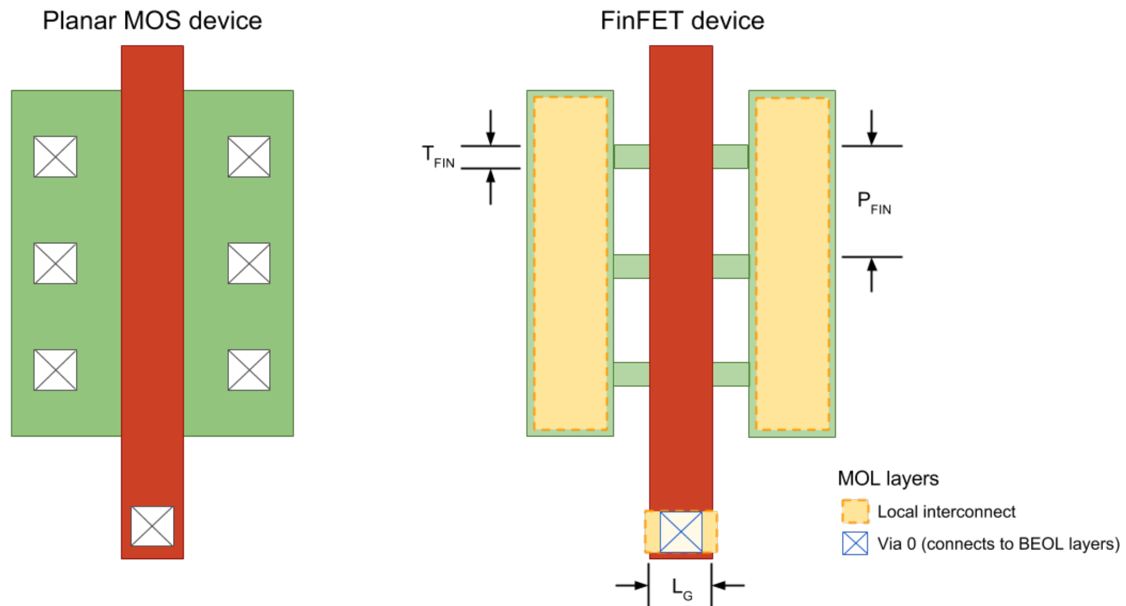
Source: From the author.

3.4 Layout Design in FinFET Technology

As FinFET technology has a process fabrication similarity with the traditional planar MOSFET, the layout design rules are composed of the standard set of rules for planar devices plus additional design rules concerned to the fin fabrication (ALIOTO, 2011). Figure 3.13 depicts a simple comparison between the layout of a planar MOS transistor and a FinFET transistor. The area occupied by a single FinFET device is proportional to the number of fins N_{FIN} and the fin pitch P_{FIN} defined by the process technology (COLINGE et al., 2008). In FinFET technologies, the epitaxial growth and local interconnect layers are required in the source/drain regions to connect multiple fins devices (LU; WACHNIK, 2015). The usage of Middle-Of-Line (MOL) layers was introduced before the FinFET technology concerning the performance degradation due to high resistance provided by multiple devices interconnected, and it requires metal silicides (such as TiSi2 or WSi2) to directly connect to the active layer of the device (TOPALOGLU, 2013). To connect

the local interconnection to the Back-End-Of-Line (BEOL) layers, as the M1, it is used a silicon via.

Figure 3.13: Comparison between the layout of a planar MOS device and a FinFET device.



Source: From the author.

A higher layout density can be achieved by reducing the number of fins or by decreasing the fin pitch. The number of fins can be reduced by increasing the minimum channel width W_{FIN}, i.e. by increasing the fin height H_{FIN} of the transistor (refer to Equation 3.3). However, as discussed previously, higher fin structures suffer from structural instability and limitations from etching technology (ALIOTO, 2010)(COLLAERT, 2005). Additionally, larger W_{FIN} can affect very low power designs in which great number of cells are minimum sized (ALIOTO, 2011). Concerning to the P_{FIN}, it is a litho-dependent parameter which suffers from limitation of manufacturing process. An improvement in the pitch can be realized with sophisticated spacer-defined technology (ALIOTO, 2011). However, FinFET-based standard cells provide better layout density compared to a planar technology even when using a conservative approach, i.e. ratio H_{FIN}/T_{FIN} equals to 1 and a lithography-defined technology as seen in Table 3.1. By using spacer-defined technology and an aggressive scaling of the fin dimensions, the average layout density of FinFET cells can be reduced to over 52% of a planar-based standard cell layout.

The use of multiple patterning lithography provides enhancement in the pitch density and consequently a higher layout density (ZHANG et al., 2011). The change from $193nm$ wavelength to EUV (Extrene Ultra-Violet) lithography is not yet a cost effective

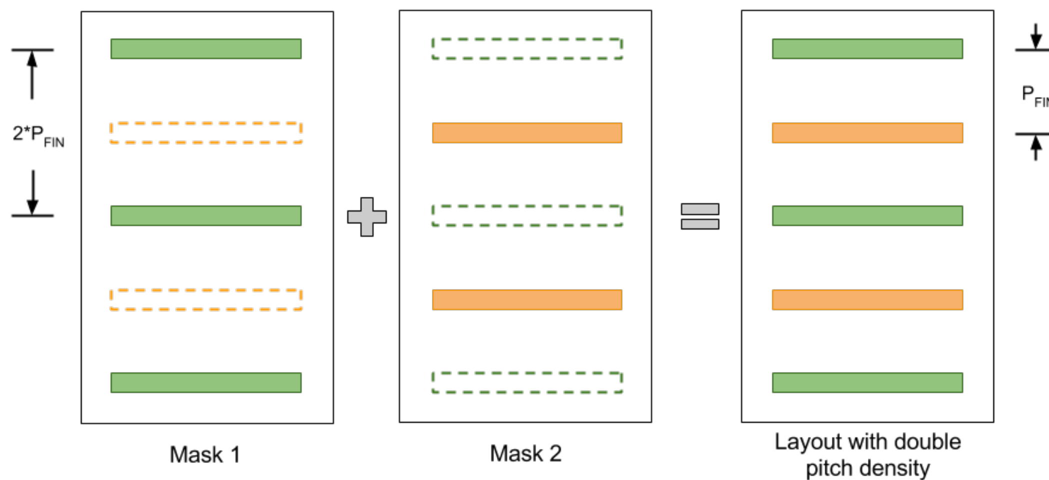
Table 3.1: Average FinFET Cell Area Normalized to its planar counterpart

H_{FIN}/T_{FIN}	1	2	3	4
Lithography-defined	0.95	0.7	0.59	0.58
Spacer-defined	0.68	0.57	0.55	0.52

Source: (ALIOTO, 2010).

alternative. Thus, Double-Patterning Lithography (DPL) is used to pattern critical layers in advanced technologies as the gate and local interconnect layers (TOPALOGLU, 2011). By applying Double Patterning, it can be achieved double pitch density by decomposing the layout into two different masks with two different colors as illustrated in Figure 3.14. In this Figure, the fin pitch P_{FIN} is improved by decomposing the fin features in the layout by two different masks (colors). One of the challenges of applying MPL is the layout decomposition targeting the avoidance of yield loss due to overlay errors.

Figure 3.14: Double Patterning Lithography: the layout is decomposed into two different masks with two different colors to improve pitch density.

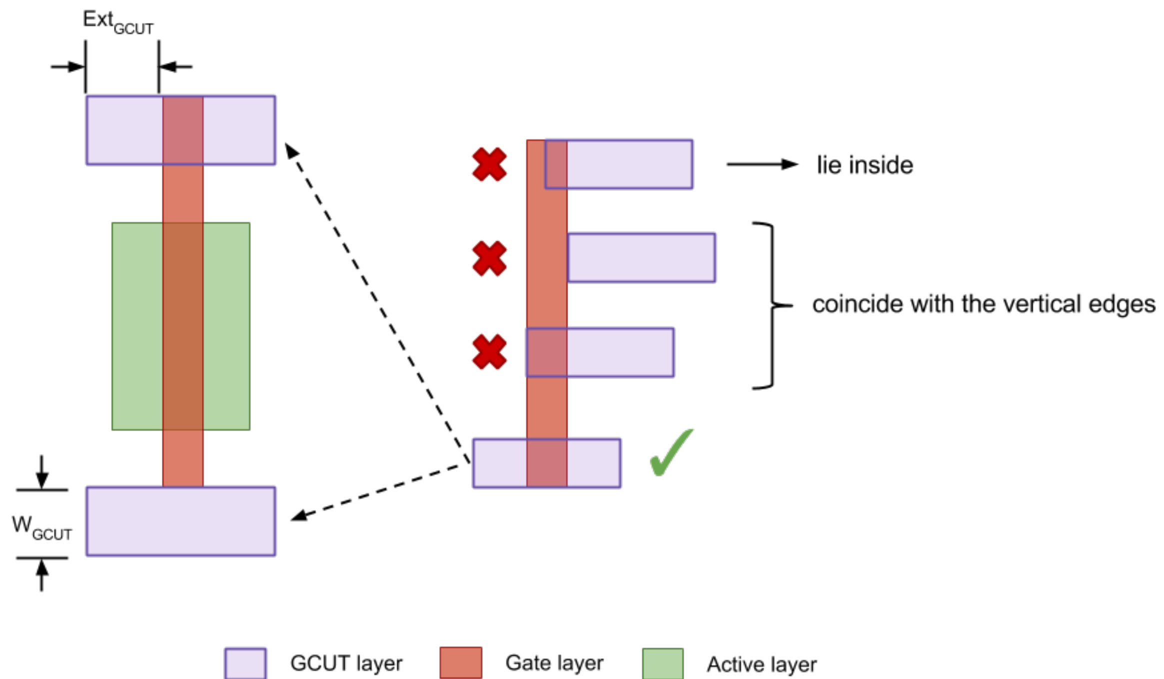


Source: From the author.

For example, a problem that is encountered in multiple patterning lithography is the misalignment of masks due to the increase in complexity on performing uniform printing as long as the feature sizes is reduced (BHANUSHALI, 2014). Misalignment can lead the drawn polygons to be printed closer/farther than previously defined in the layout design. The use of cut masks can remove the undesired features printed by the previous mask and then overcome the masks misalignment (ZHANG et al., 2011)(TOPALOGLU, 2013). The Boolean operations with the masks to perform the cut are hidden from the designer and the requirements are embedded into the design rules to provide a simple interface to the final printed features (TOPALOGLU, 2013). Some design rules to a gate

cut mask (GCUT layer) are depicted in Figure 3.15. For instance, to avoid overlay errors and ensure a proper cut to the Gate layer polygon. Additionally, its vertical edge can not lie inside or coincide with the gate layer to ensure that it will not be cut by an amount smaller than the minimum horizontal gate width of the technology. For these reasons, a minimum extension Ext_{GCUT} and width W_{GCUT} must be respected.

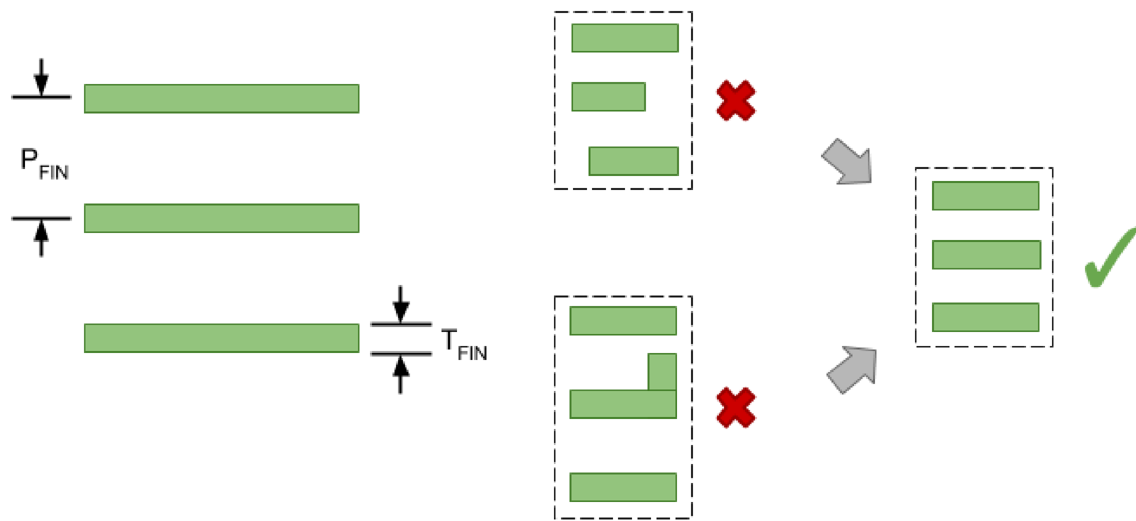
Figure 3.15: Some GCUT Layer Design Restrictions.



Source: From the author.

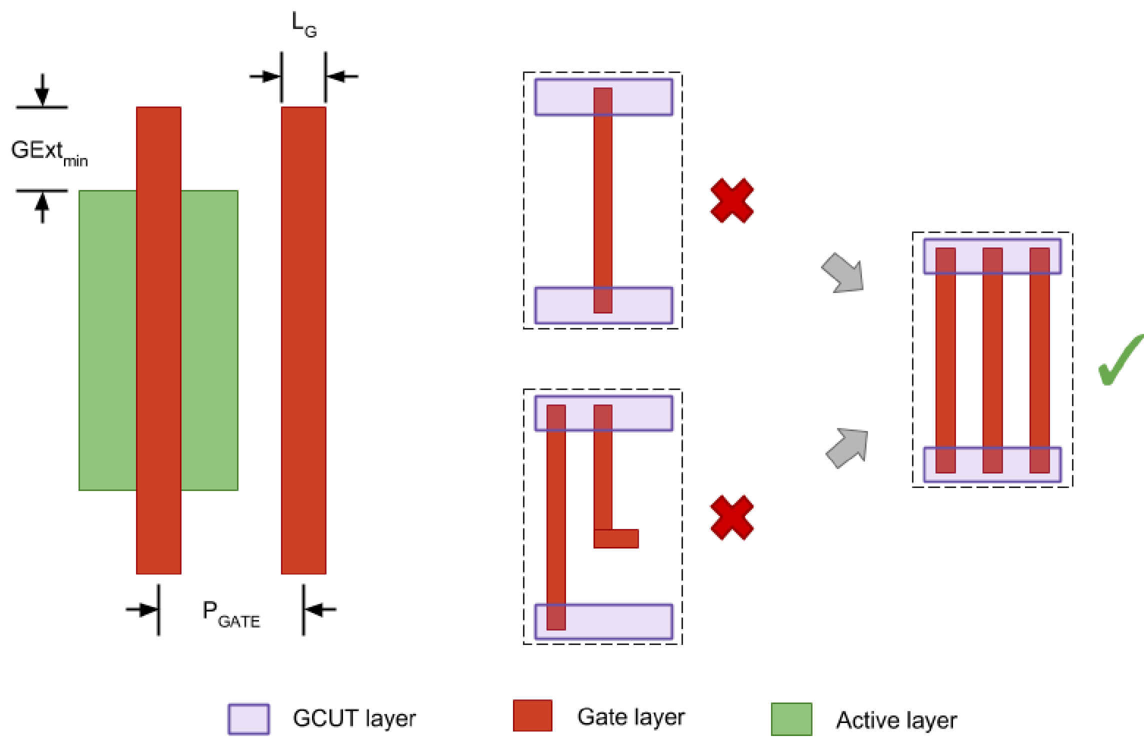
Similarly, Figure 3.16 illustrates some strict design rules regarding to the Fin Layer constraints.The fins can not bend and need to be uniformly placed respecting the fin pitch provided by the technology node. And, it must have the same length along the horizontal direction. As discussed previously, the fin pitch P_{FIN}, the fin hight H_{FIN} and the fin thickness T_{FIN} are fixed parameters and strongly dependent of the lithography technology. Accordingly, the gate layer presents some similar design rules to the fin layer. Gates need to be uniformly placed within a contacted poly pitch (CPP). The gate layer polygons can not bend or be discontinuous along the vertical direction as in Figure 3.17. The gate pitch P_{GATE} and the gate length L_G are fixed values. Additionally, to ensure process uniformity, dummy gates are needed at the end of the fins.

Figure 3.16: Some Fin Layer Design Rules.



Source: From the author.

Figure 3.17: Some Gate Layer Design Rules.

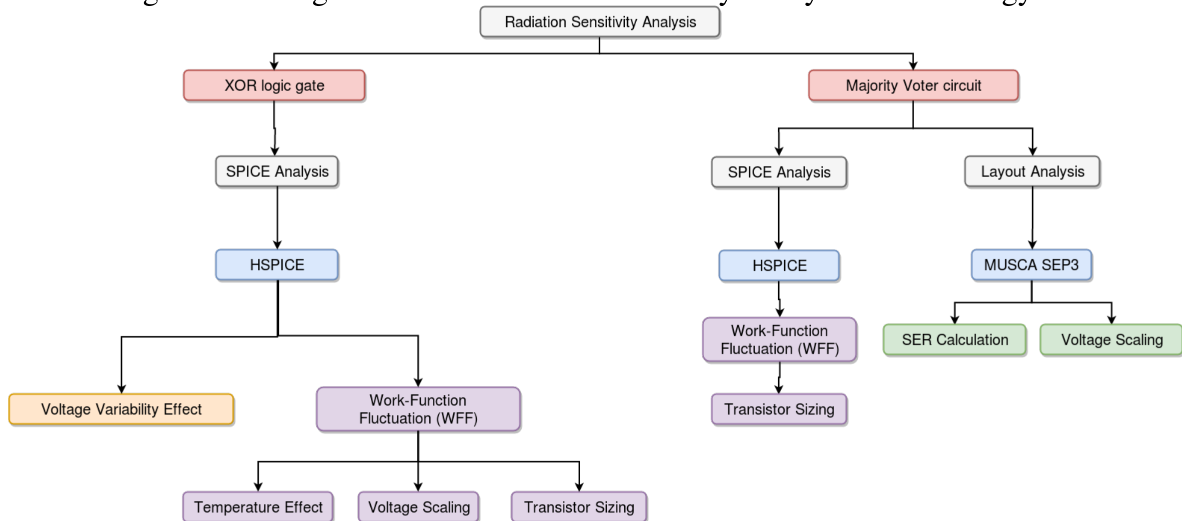


Source: From the author.

4 METHODOLOGY OF THE RADIATION ROBUSTNESS EVALUATION

Based on the high importance of redundancy-based techniques such as the DWC and TMR schemes, the radiation sensitivity analysis were performed for two different circuits: exclusive-OR (XOR) logic gate and Majority Voter (MJV) circuit. The diagram in Figure 4.1 summarizes the methodology used in this dissertation. Regarding to the radiation robustness of XOR logic gate, the experiments were mainly SPICE-based analysis using the HSPICE tool from Synopsys and the predictive models from PTM. For the MJV circuits, it was designed in SPICE level and evaluated under WFF with two different sizing. Additionally to the results of the MJV circuits, the predictive tool MUSCA SEP3 was used to obtain a more precise radiation experiment, considering aspects of the layout design and the BEOL and FEOL layers of a FinFET technology process. The cell layouts were designed in 7nm ASAP7 PDK using Virtuoso by Cadence, and Calibre from Mentor Graphics.

Figure 4.1: Diagram of the Radiation Sensitivity Analysis Methodology

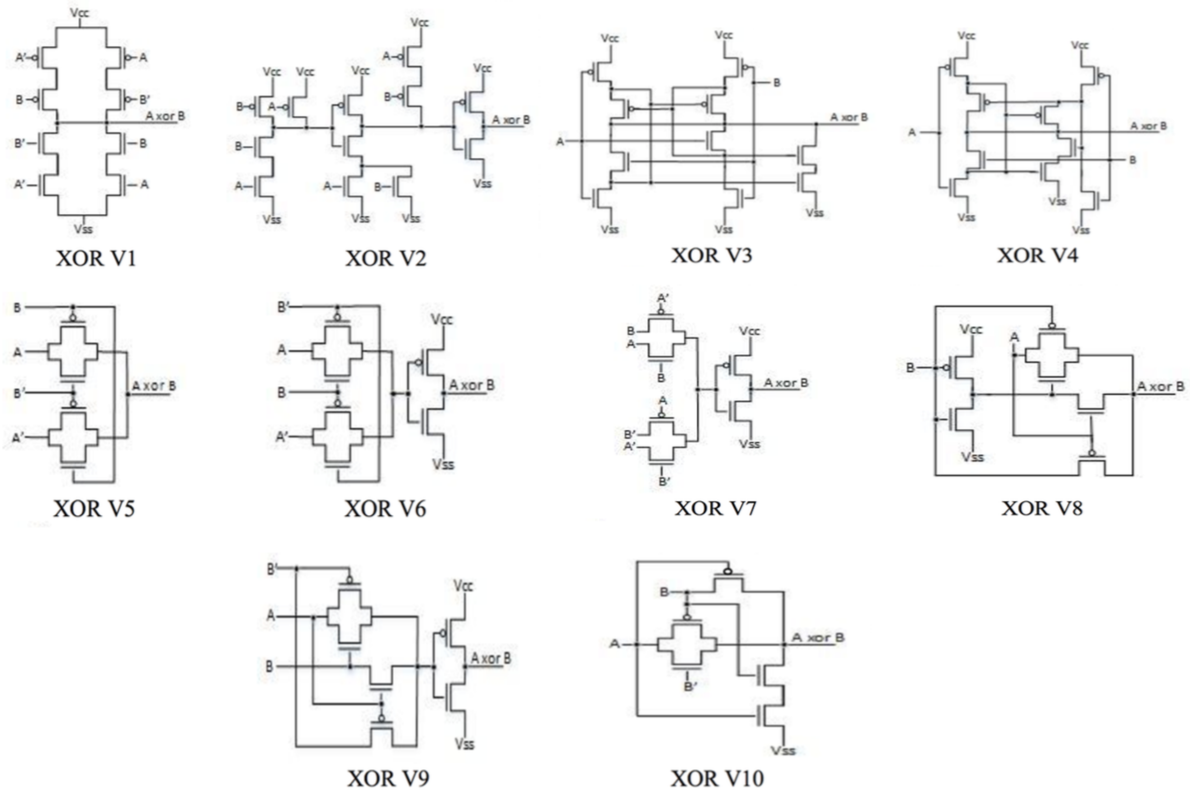


Source: From the author.

Due to its plurality of design implementations provided in the literature, ten different topologies of XOR logic gates were extensively evaluated under fault injection campaign to achieve the node sensitivity mapping and the Threshold Linear Energy Transfer (LET_{TH}) of each design implementation. Further, the effect of voltage variability is also analyzed in terms of the impact on the LET_{TH} of each circuit topology. The impact of the process-related WFF variability in the SET pulse width is evaluated through a 2000 Monte-Carlo Simulation Analysis. Different sizing approach, temperature effect and voltage scaling are also performed to provide a broader understanding of the WFF impact.

To the extent of our knowledge, no work has been done in order to specifically analyze different XOR topologies to the radiation effects using highly advanced technologies as FinFET devices. For this reason, the set of XOR topologies exploits the complementary CMOS and PTL (Pass-Transistor Logic) logic families in FinFET technology. In contrast to complementary CMOS logic family, which only allows inputs to drive gate terminals, the PTL concept allows the inputs to drive the source-drain terminal as well (RABAEY; CHANDRAKASAN; NIKOLIC, 2002). Because of this, a logic operation can be performed with only one transistor network (pull-down or pull-up) reducing the number of transistors compared to the CMOS implementation, which requires two complementary networks. Figure 4.2 shows the ten topologies analyzed in this work.

Figure 4.2: Exclusive-OR topologies



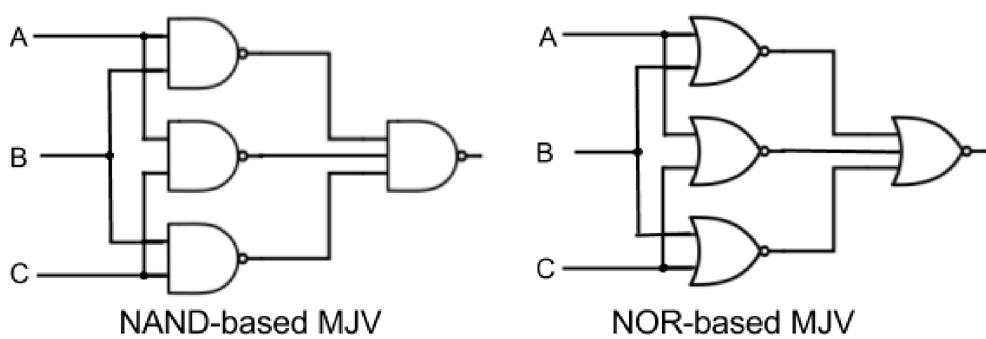
Source: (SILVA; BUTZEN; MEINHARDT, 2016).

Regarding to the voter circuits, the logical function that translates the MJV circuitry in a TMR scheme is represented by Equation 4.1, where A, B and C constitute the signal data provided by the triplicated modules in the TMR. Based on Boolean function described in Equation 4.1, the majority voting function can be implemented in a plurality of circuit topologies (LIEBL; MEINHARDT; BUTZEN, 2016)(AGUIAR et al., 2017a). For instance, one common approach is the use of a Standard Cells library.

$$MJV_{OUTPUT} = A \times B + B \times C + C \times A \tag{4.1}$$

Accordingly, this work analyzes two different majority voter circuits based on logic gates against radiation effects: the NOR-based and NAND-based majority voters as described in Figure 4.3. The NAND-based MJV is composed by three 2-input NAND logic gates connected to a 3-input NAND logic gate. Similarly, the NOR-based MJV comprises three 2-input NOR logic gates and a 3-input NOR logic gate.

Figure 4.3: Cell-based Majority Voter (MJV) circuits



Source: From the author.

4.1 SPICE-based Analysis

In a first glance, it was opted to evaluate two multigate devices (double-gate and tri-gate FinFET) in three bulk technology nodes against the effects of radiation. Both devices are simulated using the model provided by Berkeley University through PTM (Predictive Transistor Model) at $7nm$, $14nm$ and $20nm$ bulk technology node to provide a scaling perspective. The electrical and process parameters from the model are presented in Table 4.1. The same parameter values are used for both multigate devices, however, the double-gate FinFET devices have a hard mask (thick SiO_2 layer) on top of the fin to prevent the electrostatic influence from a third gate electrode.

4.1.1 Fault Injection Simulation

The fault injection simulation of a particle hit at the P-N junction of a device was carried at the circuit level using SPICE description. As discussed in the Chapter 2, the

Table 4.1: Electrical and Process parameters from PTM for bulk Multigate Technology

Parameter		Technology (nm)		
		7	14	20
Supply Voltage (V)		0.7	0.8	0.9
L_G (nm)		11	18	24
H_{FIN} (nm)		18	23	28
T_{FIN}		6.5	10	15
T_{OX}		1.15	1.3	1.4
Channel Doping (m^{-3})		1e22	5e22	5e23
Source/Drain (m^{-3})		3e26	3e26	3e26
Workfunction (eV)	N	4.42	4.42	4.38
	P	4.74	4.75	4.80

radiation-induced current pulse has a very characteristic waveform: a very fast linear rise due to the funneling process and an exponential slow decay due to the diffusive component in the charge collection process. Accordingly, it was modeled as a double exponential transient pulse by inserting a current source at the stroke sensitive node as described in Equation 4.2 and Equation 4.3 (repeated here from Chapter 2 for the sake of convenience), where Q_{COLL} is the amount of charge collected due to a radiation particle strike in the sensitive region (MESSENGER, 1982). The τ_α is the collection time constant of the junction and τ_β is the ion track establishment time constant. For the devices used in this work, theses constants can be approximated to $20ps$ for τ_α and $2ps$ for τ_β (ROYER; GARCÍA-REDONDO; LÓPEZ-VALLEJO, 2015)(LIU et al., 2014).

$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \tag{4.2}$$

$$Q_{coll} = 10.8 \times L \times LET \tag{4.3}$$

The Linear Energy Transfer (LET) is the amount of energy released by a particle per unit length crossed in sensitive region of the device. The charge collection depth (L) decreases with the technology scaling and depends on the device structure as well. Hence, the key dimensional parameter for the charge collection depth in fin-like technology is the thickness or the height of the fin structure (HUBERT; ARTOLA; REGIS, 2015)(ARTOLA et al., 2015).

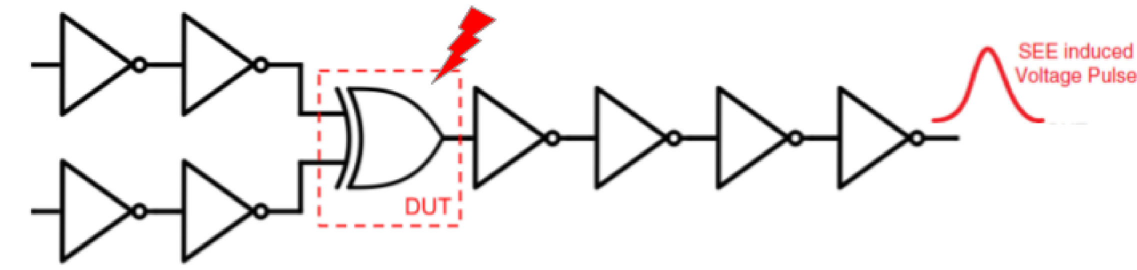
In this analysis, it was possible to obtain the node sensitivity mapping of the ten XOR topologies studied, i.e., all the internal node sensitive to particle strikes, leading to a transient pulse at the output (AGUIAR; MEINHARDT; REIS, 2017). Besides identifying

the internal sensitive nodes, the worst radiation sensitive scenario of each topology was characterized by the most sensitive node plus the input vector which leads to the highest and widest transient current pulse. The most sensitive node is the internal node which showed more transient pulses in the circuit output regardless of the input vector. Another metric used to evaluate the radiation sensitivity of a given circuit is the threshold Linear Energy Transfer (LET_{TH}). In this work, it is the minimum charge needed for a transient current pulse to propagate until the output of the inverter chain with amplitude greater than half the value of the nominal voltage as defined by Equation 4.4.

$$LET_{th}(pC/\mu m) = \min_{I_{peak} > \frac{VDD}{2}} \int I(t)dt \quad (4.4)$$

To evaluate the LET_{TH}, a fault injection in the worst radiation sensitive scenario was performed iteratively. The simulation setup was conducted with a 2-inverter chain coupled to the input signal of the XOR under test, and its output signal was connected to a 4-stage inverter chain as depicted in Fig. 4.4.

Figure 4.4: Simulation Setup to the Calculation of the Threshold LET



Source: From the author.

4.1.2 Variability Simulation

The effect of voltage variability was evaluated considering $\pm 10\%$ of the nominal supply voltage for each technology node studied and the correspond LET_{TH} calculated. Additionally, a voltage scaling experiment was performed to analyze the robustness of such circuits when applying low-power design techniques.

For the process variability effect, the WFF was introduced through statistical Monte Carlo simulation of 2000 runs over the work function parameter of each transistor type (PFET and NFET simultaneously). Both parameters were varied at 3σ deviation of 5%

from nominal value considering a Gaussian distribution. Temperature was varied from -10ºC to 125ºC. For all simulations, two inverters were used for each input of the circuit and the output was connected to a 4-inverter chain of fan-out 4 (FO4) at each stage. All circuits were initially designed considering the minimum sizing approach, i.e. number of fins (NFIN) equals to 1. For each XOR topology, it was measured the transient pulsewidth obtained at the output of the circuit in all 2000 runs. In this work, the SET pulsewidth is calculated when the transient pulse amplitude reaches half the value of nominal voltage.

4.2 Layout-based Analysis

In order to explore the contribution of the layout design and the BEOL and FEOL layers of advanced technology, the radiation sensitivity of the MJV circuits is evaluated using a Monte-Carlo Predictive tool at ONERA, The French Aerospace Lab (HUBERT et al., 2009). The MUSCA SEP3 is a single event effects prediction tool based on a Monte-Carlo approach developed at ONERA since 2007 to investigate the SER trends of modern and advanced technologies proposed by the technological roadmap (REED et al., 2013). The prediction tool allows for performing a full flow of simulations in different levels of abstractions, from physical simulations of the particle interaction within the device structure to the occurrence of the soft error in the circuit level. The tool was validated for different devices and technology nodes, including FinFET technology as can be verified at (HUBERT; ARTOLA, 2013) (ARTOLA; HUBERT; SCHRIMPF, 2013) (ARTOLA; HUBERT; ALIOTO, 2014).

The complete principle of the modeling is reported in previous works (WROBEL et al., 2009) (HUBERT; ARTOLA, 2013) (ARTOLA; HUBERT; SCHRIMPF, 2013). These simulations use a database generated by using the toolkit GEANT-4 for a complete description of the free carrier generation as the nuclear interactions, ionization, and etc. The 3D radial distribution of generated charges in the silicon is calculated for each incident particle considering the BEOL (ARTOLA et al., 2011). The modeling of the charge diffusion accounts for the ambipolar diffusion mechanisms and recombination processes (HUBERT et al., 2009). The modeling of the charge collection accounts for the dynamic transport and the multi-charge collection mechanisms as the charge sharing and pulse quenching effects (ARTOLA; HUBERT, 2016) (HUBERT et al., 2009), the bias voltage, the layout, the bipolar amplification, the shallow trench isolation (STI) and the fabrication process.

The bipolar amplification model depends on two mechanisms. First, the model uses the equivalent access resistances of the tri-gate device to determine the triggering of the bipolar transistor. Second, the model takes into account the variability of the amplification of charge collection as a function of LET (ARTOLA; HUBERT; SCHRIMPF, 2013). These simulations allow to build a SET currents database. Next this SET current database is used as a current generator in each relevant node of the studied cell at transistor level for an electrical transient simulation using SPICE simulator with the aim to estimate the soft error response of the majority voter cell.

The MJV circuits were designed using the $7nm$ FinFET Predictive Process Design Kit (ASAP7) developed at Arizona State University in partnership with ARM Ltd (CLARK et al., 2016). Based on current assumptions regarding the lithography and manufacturing processes, ASAP7 is a realistic and predictive PDK that allows exploring circuit designs at a not yet available technology node (the $7nm$ FinFET technology). The Extreme Ultra-violet (EUV) lithography was assumed for the major layers due to its cost-effectiveness, by not requiring multiple patterning (MP), and also to provide simpler layout design rules (CLARK et al., 2016)(MALLIK et al., 2015). Table 4.2 summarizes some of the layers and design rules adopted in the PDK development.

Table 4.2: Key layers and its widths and pitches for $7nm$ FinFET ASAP7 PDK

Layer	Lithography Technology	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

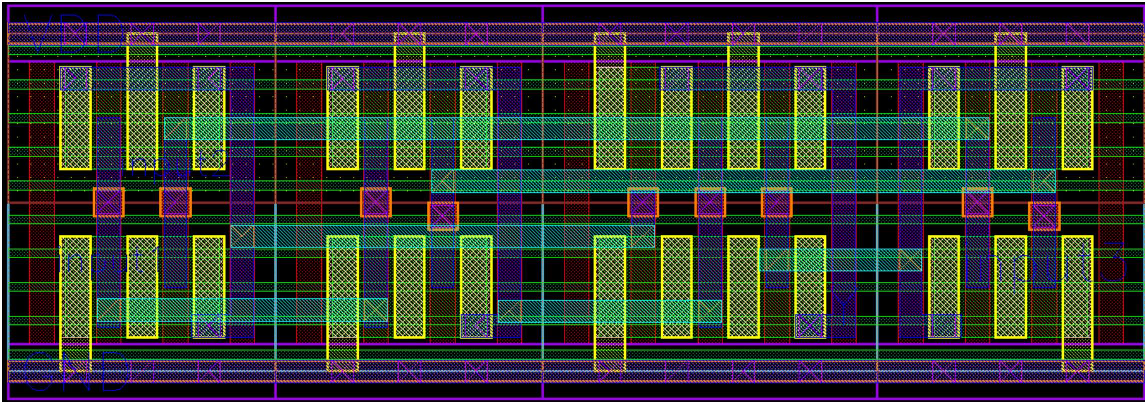
Source: (CLARK et al., 2016)

The Middle-Of-Line (MOL) metal layers are introduced in this technology to provide better cell connectivity while applying multiple patterning (MP) approaches. The Local-Interconnect Gate (LIG), Local-Interconnect Source-Drain (LISD) and VIA0 compose the MOL layers for this PDK (CLARK et al., 2016). These layers are used as metal local interconnect layers connected by shape overlap without need of a cut layer. The MP techniques are named to some of the design layers as self-aligned quadruple patterning (SAQP) and self-aligned double patterning (SADP).

The layout design of the voters was conducted based on the Standard Cell method-

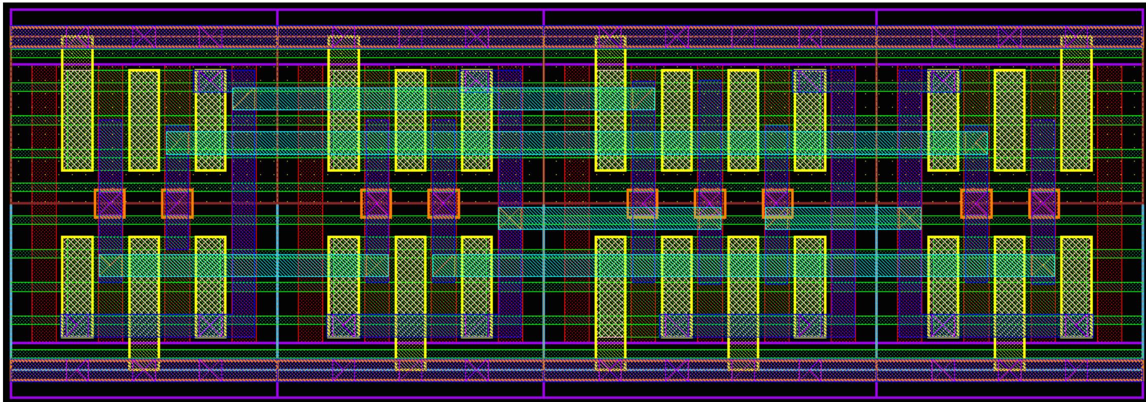
ology assumed for a Design/Technology Co-Optimization (DTCO) approach (CLARK et al., 2016)(CHAVA et al., 2015). The cell height is set to 7.5 tracks of M2 ($0.27\mu m$) and double diffusion breaks with dummy gates are used to provide better quality diffusion growth. With a $27nm$ fin pitch, a high-density layout design is achieved with three fins for each PFET and NFET devices (CHAVA et al., 2015). As silicon-based channel and strain engineering are assumed for this PDK, the obtained NFET/PFET drive ratio is approximately 10:9 (CLARK et al., 2016). For this reason, the cells are designed with symmetric sizing of NFET and PFET transistors. The designs of the two majority voters, i.e., NAND-based voter and NOR-based voter, are presented in Figure 4.5 and Figure 4.6 respectively. The layout of the circuits were designed using the Cadence Virtuoso and verified (DRC/LVS checks) with the Mentor Graphics tool, Calibre. Due to the high regularity of the designs, the total area of both cells is $0.248\mu m^2$.

Figure 4.5: Layout Design of the NAND-based Majority Voter at 7nm FinFET tecnology (ASAP7 PDK)



Source: From the author.

Figure 4.6: Layout Design of the NOR-based Majority Voter at 7nm FinFET tecnology (ASAP7 PDK)



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5 RESULTS

This chapter presents the radiation analysis for the XOR and Majority voter circuits. First, the results obtained for the XOR topologies are presented and discussed. Following, the results for the analysis of the MJV circuits are presented and discussed.

5.1 Radiation Analysis of XOR logic gate topologies

Besides the comparison function in redundancy approaches, the XOR logic gate is also a fundamental component in arithmetic circuits such as full adders, multipliers, comparators, parity-generators and majority voters. Therefore, providing significant effort to analyze its sensitivity to radiation effects will enhance the robustness of systems to these effects (AGUIAR; MEINHARDT; REIS, 2017).

5.1.1 Node Sensitive Mapping

The first step in the radiation sensitivity evaluation was to identify the node sensitivity mapping of each XOR topology. A fault injection for a particle with LET= $60fC/\mu m$ was performed at each node of the circuits considering all possible input vectors (8 possible input vectors). In these experiments, it was considered the error analysis, i.e., when the transient pulse propagates to the output of the circuit, and its amplitude and width. This information is important to further hardening by design techniques (LAZZARI et al., 2012)(MAHATME et al., 2013). This data allows determining which node is the most sensitive, as well as the input vector and nature of the radiation-induced pulse (strike at the P-type device or N-type device, i.e. 101 or 010 pulse waveform) characterizing the worst radiation sensitive case (AGUIAR; MEINHARDT; REIS, 2017). The most sensitive node was characterized as the node which has the highest and widest transient current pulse and has showed more transient pulses in the output of the circuit, regardless of the input vector. It was found that the output node is not necessarily the most sensitive node of a circuit, where 4 out of 10 topologies analyzed showed an internal node as the most sensitive one. Table 5.1 summarizes the obtained results.

Table 5.1: Number of Sensitive nodes, Critical node, Input Vector and Transient nature for the worst radiation sensitive case

Topology	# of sensitive nodes	Critical Node	Input Vector	Transient Pulse
XOR_V1	5/5	Output node	01	101
XOR_V2	3/6	Node CN	00	101
XOR_V3	3/4	Output node	00	010
XOR_V4	3/4	Output node	10	101
XOR_V5	3/3	Output node	10	101
XOR_V6	3/4	Node CN	00	101
XOR_V7	3/4	Node CN	00	101
XOR_V8	2/2	Output node	01	101
XOR_V9	2/3	Node CN	00	101
XOR_V10	3/3	Output node	01	101

Source: (AGUIAR; MEINHARDT; REIS, 2017).

The XOR_V1 is a classical implementation of the exclusive-or logic function. It has a number of five sensitive nodes while the alternative topologies own only three or two. Besides the area overhead, the XOR_V1 implementation provides a greater number of sensitive nodes, increasing the probability of SET occurrence. This comparison highlights that the XOR implementation usually found in cell libraries could not be the best option regarding the robustness to radiation effects. For reliable systems, one should reconsider the XOR implementation to increase the design radiation robustness. The smallest circuits with less sensitive nodes are the XOR_V8 and XOR_V9.

5.1.2 Threshold LET

After identifying the worst radiation sensitive case for each XOR circuit, the threshold LET is obtained iteratively by changing the amount of charge collected described in the transient current source netlist description. The threshold LET was defined according to Equation 4.4, as the minimum collected charge needed by a P-N junction to induce a transient current pulse able to propagate and reach the output node with an amplitude greater than half the value of the nominal voltage. Table 5.2 summarizes the threshold LET obtained for the double-gate (DG) and tri-gate (TG) FinFET at $7nm$, $14nm$ and $20nm$ technologies.

The TG-based XOR circuits have exhibited an improved robustness compared to the DG-based circuits at the three technologies analyzed in this work. This can be ex-

plained by the improved gate electrostatic control over the channel in the tri-gate configuration due to its additional gate electrode influence (AGUIAR; MEINHARDT; REIS, 2017). As observed in Table 5.2, the XOR_V6 circuit has shown to be the most robust topology, i.e. highest threshold LET, in both devices with $LET_{th} = 16.52fC/\mu m$ for TG FinFET and $LET_{th} = 15.33fC/\mu m$ for DG FinFET at $7nm$ technology node. This topology exhibited the highest LET_{th} for both devices in the three technology nodes.

Table 5.2: Threshold LET for double-gate (DG) and tri-gate (TG) FinFET ($fC/\mu m$)

Topology	7nm		14nm		20nm	
	DG	TG	DG	TG	DG	TG
XOR_V1	13.07	14.00	17.02	18.83	15.55	16.86
XOR_V2	13.76	14.76	18.07	20.02	17.33	18.99
XOR_V3	15.26	16.40	18.79	20.80	17.61	19.20
XOR_V4	12.76	13.67	16.71	18.45	14.83	16.02
XOR_V5	14.02	15.10	18.71	21.07	17.98	19.62
XOR_V6	15.33	16.52	20.44	22.83	20.29	22.42
XOR_V7	13.82	14.74	18.79	20.64	17.80	19.38
XOR_V8	12.81	13.71	16.63	18.43	15.12	16.40
XOR_V9	13.29	14.21	17.39	19.25	16.38	17.98
XOR_V10	12.86	11.19	16.86	18.63	15.24	16.55

Source: (AGUIAR; MEINHARDT; REIS, 2017).

The most sensitive circuit was the XOR_V4 topology with approximately 17% reduction on the threshold LET compared to the XOR_V6 for DG FinFET at $7nm$. It is even worse at $20nm$ technology node, which it has a reduction of about 28% for both devices. Considering the $14nm$, the XOR_V8 circuit has shown to be the most sensitive design. This topology achieved 19% lower LET_{th} than XOR_V6. To summarize the results, the Table 5.3 presents the most robust and the most sensitive XOR topology for each technology node and device structure.

5.1.3 Voltage Variability Impact

In order to analyze the impact of voltage variability encountered at VLSI circuits, experiments were conducted considering both a 10% increase of nominal supply voltage and a decrease of 10%. As expected, the radiation susceptibility of a circuit has a direct relationship with its supply voltage, and so does its threshold LET. In consequence, the voltage variability has a great impact on the LET_{th} by increasing it for higher supply

Table 5.3: Summary of the most robust (highest LET_{th}) and most sensitive (lowest LET_{th}) XOR designs with DG and TG FinFET

Device	Technology Node	Most robust	Most sensitive
DG FinFET	7nm	XOR_V6	XOR_V4
	14nm	XOR_V6	XOR_V8
	20nm	XOR_V6	XOR_V4
TG FinFET	7nm	XOR_V6	XOR_V10
	14nm	XOR_V6	XOR_V8
	20nm	XOR_V6	XOR_V4

Source: From the author.

voltages and by decreasing it for lower supply voltages (consequently, increasing the radiation sensitivity of the circuits). Table 5.4 and Table 5.5 summarize the voltage variability impact at the threshold LET for the DG and TG FinFET XOR circuits, respectively.

Table 5.4: Voltage Variability Impact to the threshold LET of double-gate FinFET XOR Circuits ($fC/\mu m$)

Topology	7nm		14nm		20nm	
	-10%	+10%	-10%	+10%	-10%	+10%
XOR_V1	10.67	15.52	14.02	20.07	13.38	18.97
XOR_V2	11.26	16.29	14.95	21.21	14.90	21.46
XOR_V3	12.48	18.07	15.60	21.98	15.15	21.61
XOR_V4	10.33	15.21	13.71	19.79	12.69	18.17
XOR_V5	11.10	17.40	14.98	22.76	15.12	22.62
XOR_V6	12.24	18.67	16.55	24.50	17.10	25.71
XOR_V7	11.21	16.50	15.35	22.35	15.08	22.29
XOR_V8	10.40	15.21	13.68	19.64	12.95	18.52
XOR_V9	10.86	15.76	14.36	20.45	14.05	16.38
XOR_V10	10.40	15.31	13.80	19.90	13.02	18.74

Source: (AGUIAR; MEINHARDT; REIS, 2017).

The circuit XOR_V5 has shown to be the most sensitive to the voltage variation at both devices in all three technology nodes. It is encountered a threshold LET reduction of around 20% for $7nm$ and $14nm$, and a reduction of around 15% for $20nm$ when the supply voltage equals to 90% of the nominal supply voltage. Considering only the circuits with DG FinFET devices, the results highlight that the most robust topology depends to the technology used. For $7nm$, the XOR_V2 shows the smallest reduction, approximately 18%. On the other hand, the XOR_V3 and XOR_V1 are the most robust for $14nm$ and $20nm$, respectively. Under voltage variability, the XOR_V3 and XOR_V1 suffer

Table 5.5: Voltage Variability Impact to the threshold LET of tri-gate FinFET XOR Circuits ($fC/\mu m$)

Topology	7nm		14nm		20nm	
	-10%	+10%	-10%	+10%	-10%	+10%
XOR_V1	11.48	16.50	15.57	22.07	14.60	18.97
XOR_V2	12.11	17.40	16.61	23.42	16.44	21.46
XOR_V3	13.45	19.40	17.33	24.27	16.67	21.61
XOR_V4	11.17	16.21	15.19	21.77	13.83	18.17
XOR_V5	11.95	18.71	16.81	25.35	16.64	22.62
XOR_V6	13.19	20.05	18.51	27.32	19.01	25.71
XOR_V7	12.00	17.52	16.87	24.40	16.50	22.29
XOR_V8	11.18	16.24	15.22	21.71	14.20	18.52
XOR_V9	11.67	16.83	15.94	22.57	15.51	16.38
XOR_V10	11.19	16.38	15.31	21.96	14.23	18.74

Source: (AGUIAR; MEINHARDT; REIS, 2017).

a reduction of 17% and 14% over the threshold LET, respectively. Considering the results obtained for the TG-based XOR circuits in Table 5.5, the XOR_V2 is the less sensitive to the decrease in the supply voltage (it shows 18% reduction on the threshold LET). At $14nm$ and $20nm$, the XOR_V3 shows the smallest reduction, approximately 17% and 13%, respectively.

In summary, for both devices, the less sensitive to these variations were the XOR_V2 at $7nm$ and the XOR_V3 at $14nm$. At $20nm$, the most robust were the XOR_V1 for the double-gate configuration and the XOR_V3 for the tri-gate device. And, the most sensitive is the XOR_V5 for both devices. Table 5.6 summarizes the results.

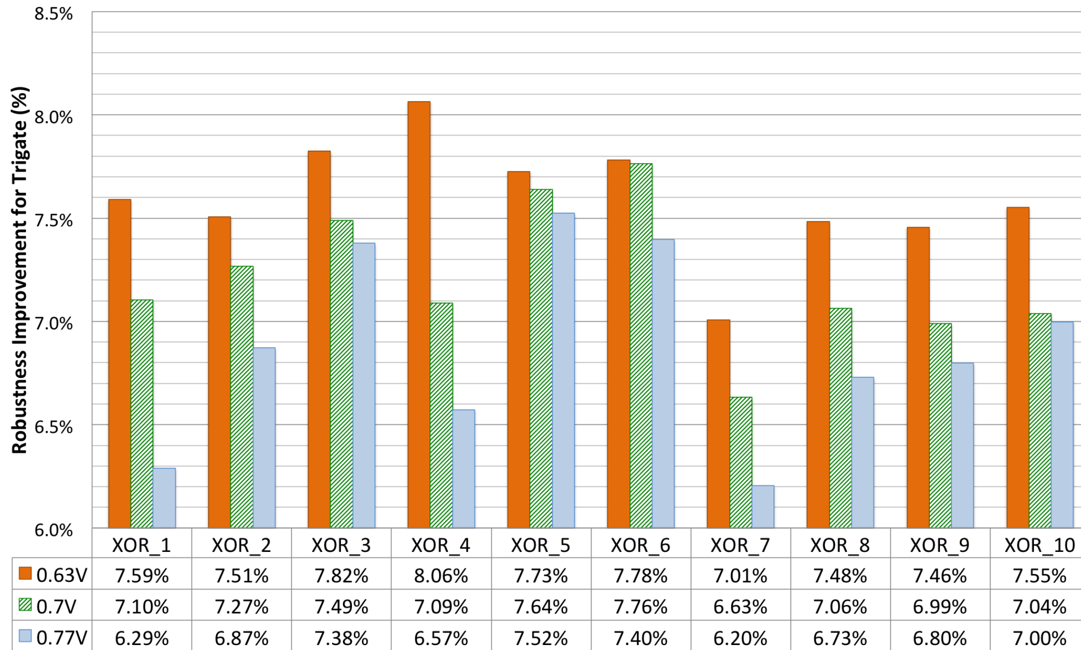
Table 5.6: Summary of the XOR designs most robust and most sensitive to Voltage Variability with DG and TG FinFET

Device	Technology Node	Most robust	Most sensitive
DG FinFET	7nm	XOR_V2	XOR_V5
	14nm	XOR_V3	XOR_V5
	20nm	XOR_V1	XOR_V5
TG FinFET	7nm	XOR_V2	XOR_V5
	14nm	XOR_V3	XOR_V5
	20nm	XOR_V3	XOR_V5

Source: From the author.

Overall, all circuits when designed with TG FinFETs have shown a better robustness to the effects of radiation. This improvement can be noted in terms of the threshold LET. Figure 5.1 and Figure 5.2 shows the TG FinFET improvement in percentage for each circuit for $7nm$ and $20nm$, respectively. At $7nm$ technology node, the improvement can range from 6.2% up to 8.1% considering the voltage variability.

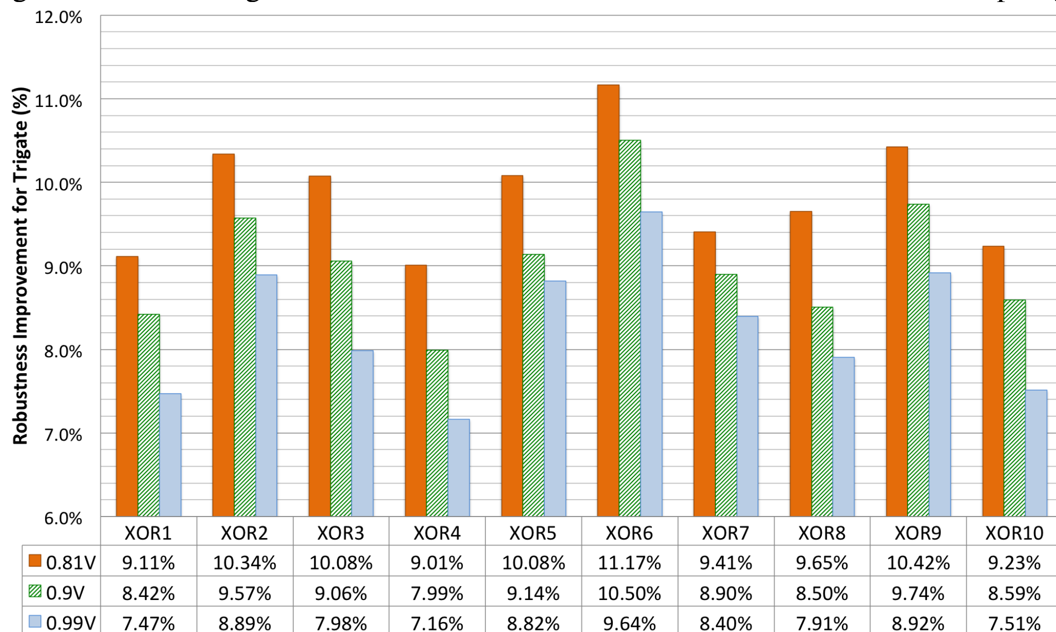
Figure 5.1: Percentage increase in Threshold LET for $7nm$ TG-based XOR topologies



	XOR_1	XOR_2	XOR_3	XOR_4	XOR_5	XOR_6	XOR_7	XOR_8	XOR_9	XOR_10
0.63V	7.59%	7.51%	7.82%	8.06%	7.73%	7.78%	7.01%	7.48%	7.46%	7.55%
0.7V	7.10%	7.27%	7.49%	7.09%	7.64%	7.76%	6.63%	7.06%	6.99%	7.04%
0.77V	6.29%	6.87%	7.38%	6.57%	7.52%	7.40%	6.20%	6.73%	6.80%	7.00%

Source: (AGUIAR; MEINHARDT; REIS, 2017).

Figure 5.2: Percentage increase in Threshold LET for $20nm$ TG-based XOR topologies



	XOR1	XOR2	XOR3	XOR4	XOR5	XOR6	XOR7	XOR8	XOR9	XOR10
0.81V	9.11%	10.34%	10.08%	9.01%	10.08%	11.17%	9.41%	9.65%	10.42%	9.23%
0.9V	8.42%	9.57%	9.06%	7.99%	9.14%	10.50%	8.90%	8.50%	9.74%	8.59%
0.99V	7.47%	8.89%	7.98%	7.16%	8.82%	9.64%	8.40%	7.91%	8.92%	7.51%

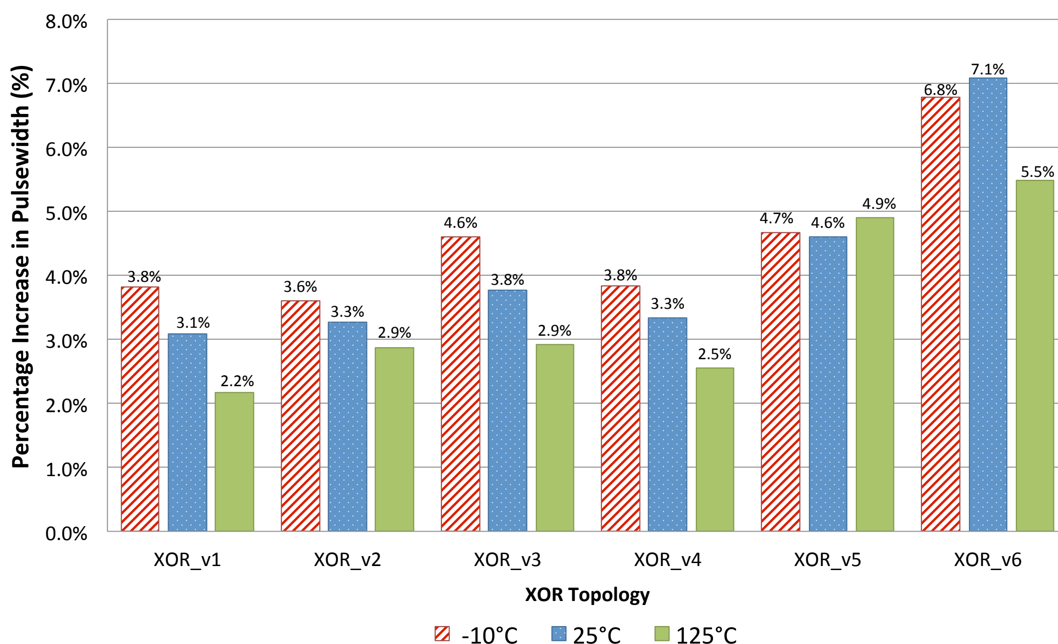
Source: (AGUIAR; MEINHARDT; REIS, 2017).

At nominal supply voltage, the maximum robustness improvement was 7.8% over the threshold LET for the XOR_V6 circuit. The improvement range predicted to these circuits at $14nm$ TG FinFET can range from 9.2% to 12.6%, with the maximum improvement, at nominal voltage, for the XOR_V5. In Figure 5.2, it can be observed a wider improvement range at $20nm$ technology node. It ranges from 7.2% to 11.2% with the minimum and maximum improvement for the XOR_V4 and XOR_V6, respectively.

5.1.4 Work-Function Fluctuation Impact

In order to carefully analyze the impact of WFF, only the first six versions of the XOR topologies from Figure 4.2 were evaluated as they exhibited the best results. Additionally, as the TG FinFET exhibited better results in terms of LET_{TH}, only the tri-gate configuration is used. For this reason, from this point on, only the denomination FinFET will be used to refer the tri-gate configuration. From the experiments performed in this work, it can be observed a negative impact on the radiation robustness of the analyzed cells under work-function fluctuation. In Figure 5.3 the percentage increase relative to the nominal SET pulsewidth at -10°C, 25°C e 125°C is shown for all analyzed circuit.

Figure 5.3: Relative increase in the transient pulsewidth under WFF at -10°C, 25°C (nominal temperature) and 125°C

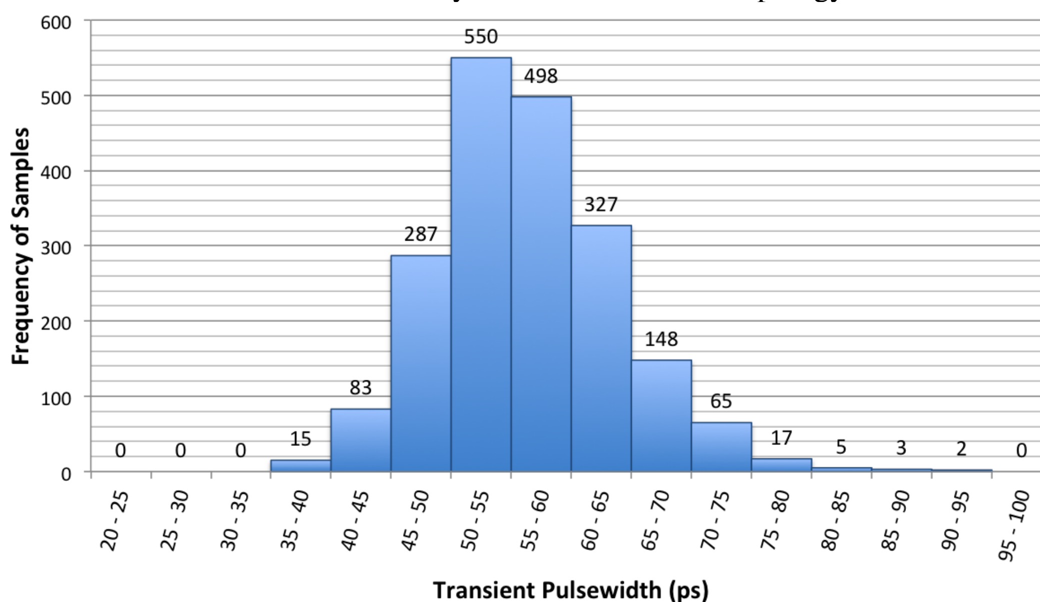


Source: (AGUIAR et al., 2017b).

These topologies have exhibited an increase in average from 2% up to 7% over the expected nominal transient pulsewidth when no work-function fluctuation is evaluated. The topologies based on pass-transistors such as the XOR_V5 and XOR_V6 exhibited the greatest increase, especially the latter one, which has a greater number of transistor compared to XOR_V5. The topologies based on Complementary CMOS logic family (XOR_V1 to XOR_V4) behaved similarly, ranging from 2% to the maximum of 5% of increase in the SET pulsewidth. The topology which exhibited the less increase, regardless the temperature, was the XOR_V1.

Although the WFF induced a slight increase in the mean value of the transient pulsewidth (less than 10%), it has led to a wide distribution deviation as depicted in Figure 5.4. It contains the frequency distribution histogram for the observed transient pulsewidth measured in the statistical Monte Carlo simulation analysis for the XOR_V4 circuit. In this case, for example, the XOR_V4 exhibits a nominal pulsewidth of $50ps$ when no WFF impact is evaluated. However, due to the WFF influence, there were a significant number of samples that produced transients 15% larger than the nominal pulsewidth. For instance, more than 1100 from the 2000 samples have produced a transient pulsewidth greater than $50ps$ due to the large standard deviation. It represents 55% from the Monte Carlo analysis population in the case of XOR_V4.

Figure 5.4: Frequency Distribution Histogram of the Transient Pulsewidth obtained from the 2000 statistical Monte Carlo Analysis for the XOR_V4 topology

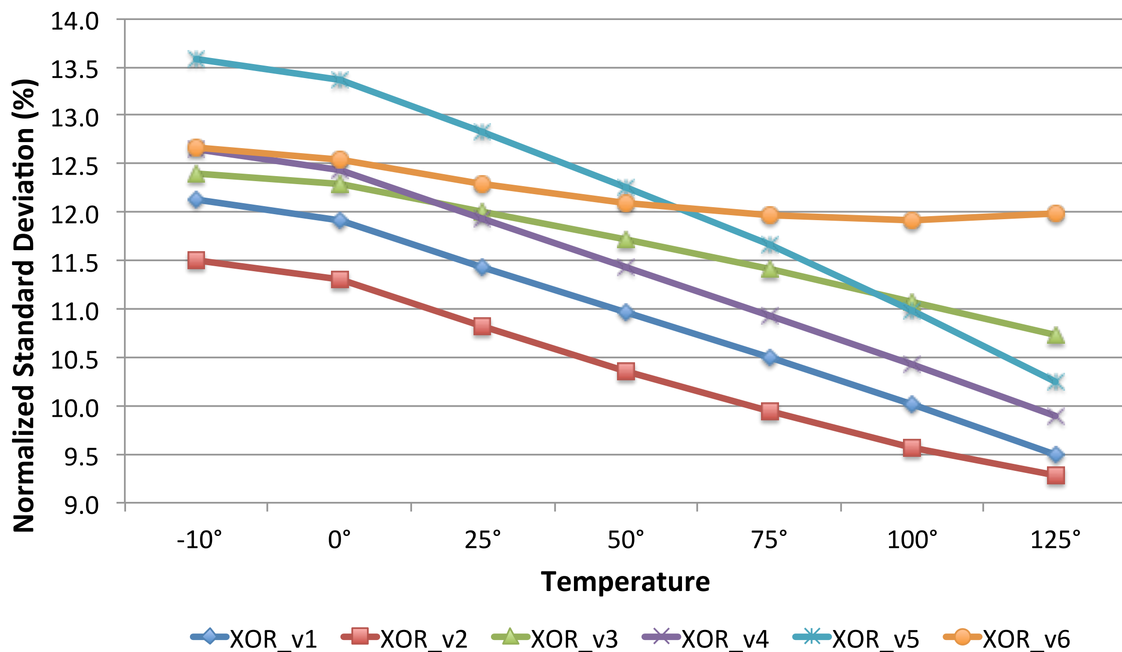


Source: (AGUIAR et al., 2017b).

Each circuit topology has shown a different behavior with different distribution profile. It highlights the need to perform statistical analysis of radiation sensitivity due to the presence of random variations in the highly complex manufacturing processes (AGUIAR et al., 2017b). The increase in the standard deviation of the SET pulsewidth due to process variability can invalidate the effectiveness of fault masking schemes which relies on temporal constraints.

Accordingly, the relative standard deviations σ/μ of the transient pulsewidth measured at each output of the XOR topologies was measured over a range of temperature and depicted in Figure 5.5. In overall, the circuits have shown an increase in the deviation as the temperature is cooled down. Except for the XOR_V6 that has proved to be more robust to the temperature variation, exhibiting a practically steady deviation of 12% from -10ºC to 125ºC. Considering the nominal temperature of 25ºC, XOR_V5 showed the highest normalized deviation, while the topology XOR_V2 revealed the lowest for the complete range of temperature analyzed in this study. Also, XOR_V5 was the most sensitive to temperature variation, increasing its standard deviation to over 33% from 125ºC to -10ºC.

Figure 5.5: Normalized standard deviation for the 6 XOR topologies under WFF in a range of temperature from -10ºC to 125ºC

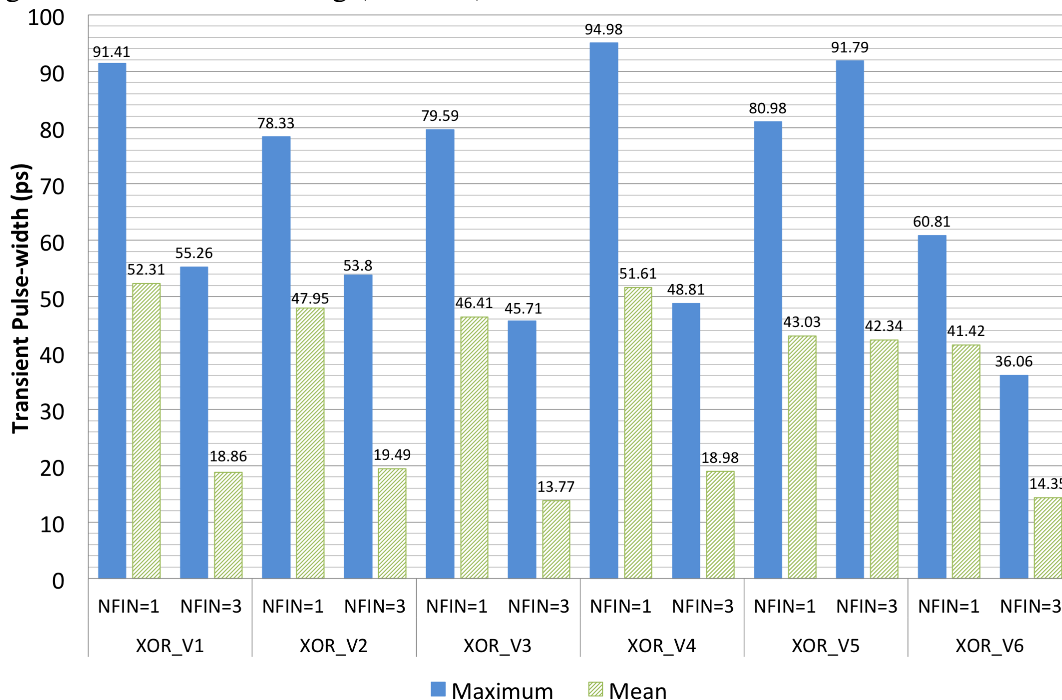


Source: (AGUIAR et al., 2017b).

FinFET technology requires a different approach for transistor sizing due to its width quantization characteristic. In order to evaluate the influence of the number of fins to the SET pulsewidth induced by radiation, the same experiments were performed for the transistors designed with the number of fins equals to 3 (NFIN = 3). In Figure 5.6, it is provided the maximum and mean values for the SET pulsewidth found for each topology studied in this work at nominal temperature with NFIN = 1 and NFIN = 3.

In most of the circuits, it can be observed that the maximum pulsewidth can be approximately 2x wider than the mean value, regardless of the number of the fins. In addition, the SET pulsewidth for the transistors designed with NFIN = 3 is reduced compared to the minimum sized designs. It can be explained by the increase in the restoring current as the strength of the cell is increased. This behavior is in agreement with previous results in the literature (ARTOLA; HUBERT; ALIOTO, 2014). The XOR_V3 was the circuit which presented the greater reduction on the SET pulsewidth, approximately 70.3%. Interestingly, the XOR_V5 was the only circuit to behave differently. It provided a minor reduction on the SET pulsewidth, about 1.6%. Further, the maximum pulsewidth increased in 13.3%.

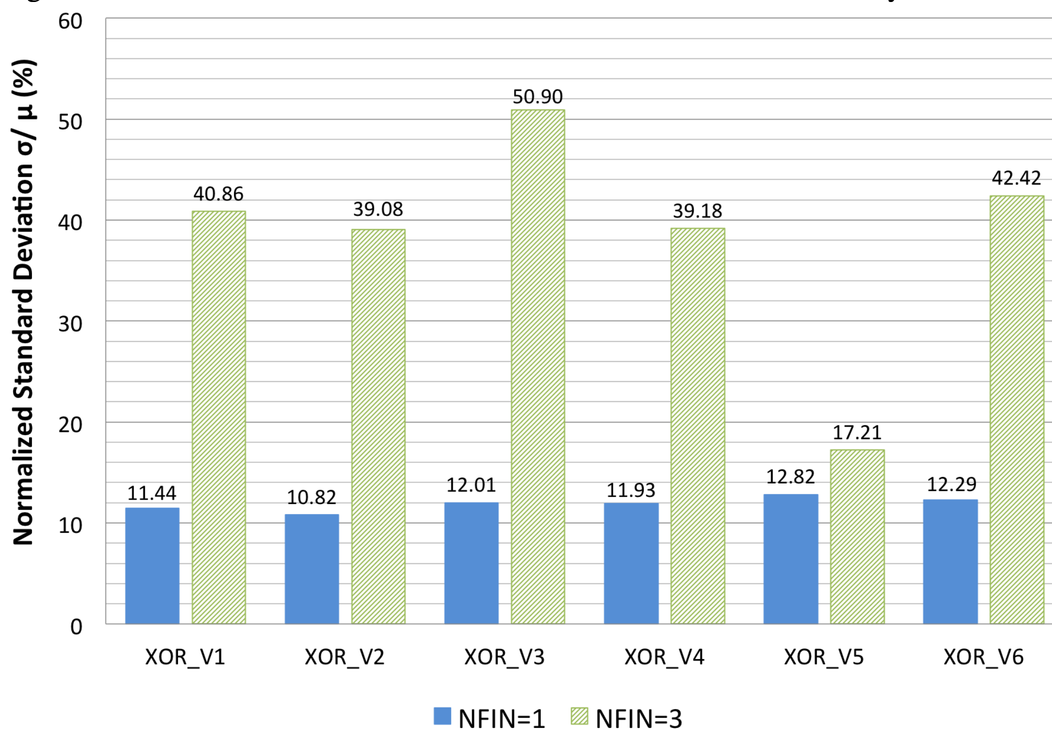
Figure 5.6: Comparison of Maximum and Mean transient pulsewidth of topologies designed with minimum sizing (NFIN=1) and with NFIN=3



Source: (AGUIAR et al., 2017b).

Despite the overall reduction, as the number of fins is increased, the impact of WFF displays a wider distribution deviation from the mean value of the SET pulsewidth observed in the Monte Carlo simulation analysis. These results are compared in Figure 5.7. For all circuits, the normalized deviation has increased abruptly, except for XOR_V5 that exhibited a slight increase. This trend is observed due to the increase of the effective width as the number of fins is increased, leading to a larger gate area and improved WFF impact.

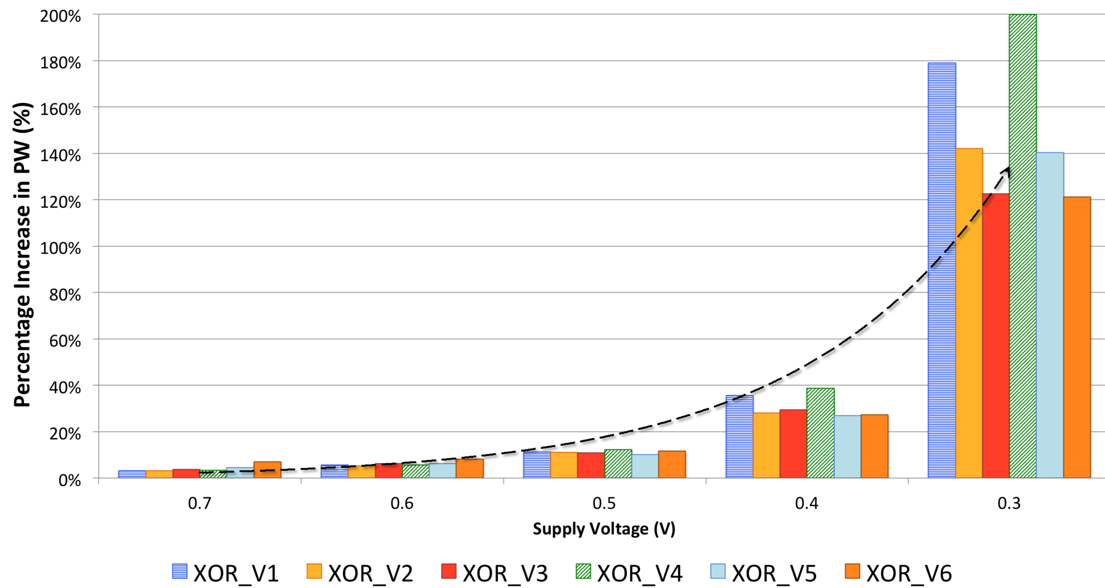
Figure 5.7: Comparison of Normalized Standard Deviation of Transient Pulsewidth for designs with NFIN=1 and NFIN=3 under 2000 WFF Monte Carlo Analysis



Source: (AGUIAR et al., 2017b).

Additionally, energy consumption efficiency of transistors is not scaling along with the high integration capacity of VLSI systems. Therefore, future designs in advanced technology nodes will suffer from power limitation. To overcome this problem novel low-power techniques are being addressed such as voltage scaling in multiple supply voltage designs. As supply voltage is a critical constraint for soft error sensitivity, it was also evaluated the impact of the process-variation WFF impact when applying Voltage Scaling. This analysis can be observed in Figure 5.8. For nominal supply voltage, the impact of WFF on the mean transient pulsewidth is less than 10%. However, when applying supply voltage scaling, the lower voltage can increase the impact of WFF to approximately 200%.

Figure 5.8: Voltage Scaling Effect in the SET pulsewidth for designs with NFIN=1 under 2000 WFF Monte Carlo Simulation Analysis



Source: (AGUIAR et al., 2017b).

5.2 Radiation Analysis of Majority Voter circuits

Initially, the majority voters were described in SPICE and evaluated under WFF effects. Then, the layout design using the ASAP7 PDK are evaluated using the predictive tool MUSCA SEP3.

5.2.1 Work-Function Fluctuation Analysis

At first, the threshold LET for each MJV circuit is calculated in its worst radiation sensitive case. Both circuits have shown a higher sensitivity in the output node. The critical node, input vector and the transient pulse which composes the worst radiation case for each MJV circuit and its correspondent threshold LET are presented in Table 5.7. The NAND-based MJV circuit exhibited the highest LET_{TH}, i.e., it is more robust than the NOR-based MJV circuit.

The WFF analysis was taken in the same manner as for the XOR topologies, i.e., 2000 statistical Monte Carlo simulations. As observed for the XOR circuits, the SET pulsewidth has also suffered deviation due to the WFF impact in the threshold voltage of the transistors changing the sensitivity of the circuits. In Figure 5.9 the obtained tran-

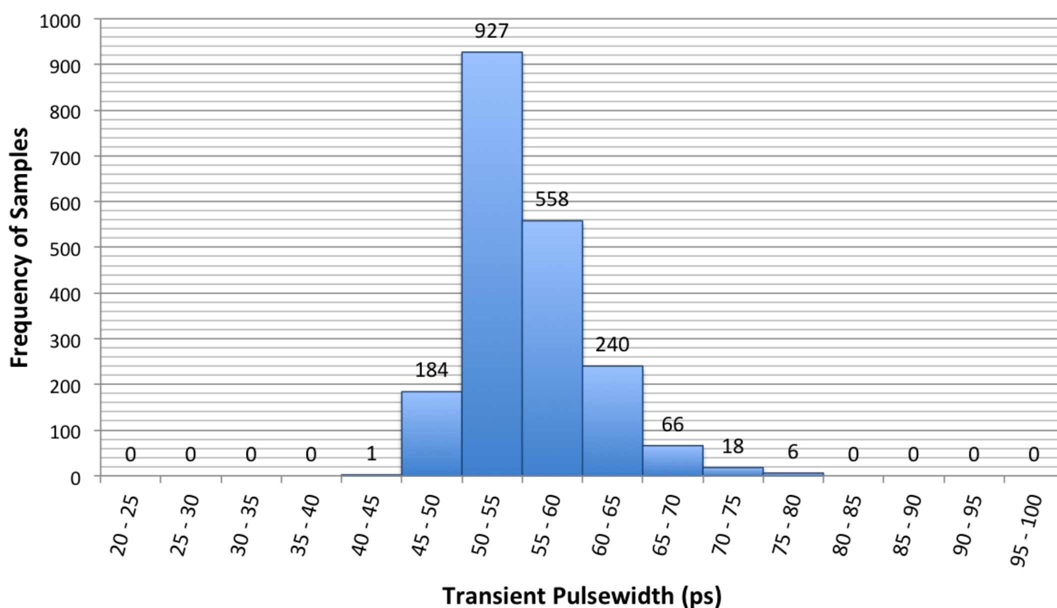
Table 5.7: Worst Radiation Sensitive Case and threshold LET for the Majority Voter Circuits

MJV Circuit	Critical Node	Input Vector	Transient Pulse	Threshold LET
NAND-based	Output node	000	010	13.45 $fC/\mu m$
NOR-based	Output node	111	101	11.33 $fC/\mu m$

Source: From the author.

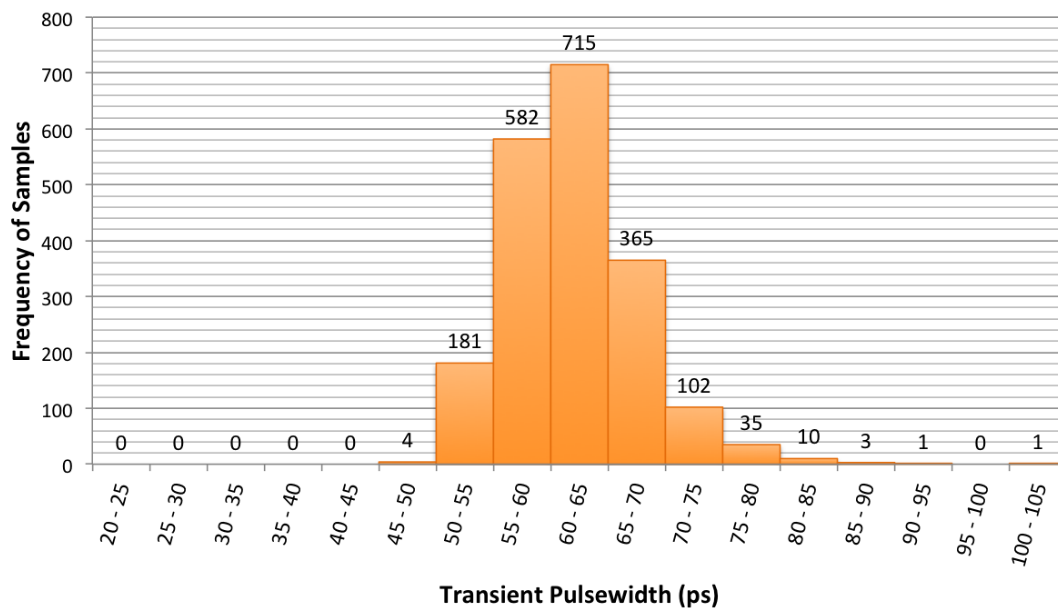
sient pulsewidth measured at the output node of NOR-based MJV circuit is displayed as a frequency distribution histogram for the 2000 Monte Carlo Simulation. The mean SET pulsewidth is of $55.3ps$. However, due to the large dispersion induced by the WFF, 837 samples exceeded this mean values, representing 42% of the Monte Carlo analysis population. The SET pulsewidth measured for the NAND-based MJV circuit is presented in Figure 5.10. The NAND-based MJV circuit exhibited a larger mean transient pulsewidth than the NOR version, approximately 12% of increase. Analyzing the dispersion induced by the WFF, 958 samples exceeded the mean of $62ps$, representing about 48% of the Monte Carlo analysis population.

Figure 5.9: Frequency Distribution Histogram of the transient pulsewidth obtained from 2000 statistical Monte Carlo Analysis for the NOR-based MJV circuit



Source: From the author.

Figure 5.10: Frequency Distribution Histogram of the transient pulsewidth obtained from 2000 statistical Monte Carlo Analysis for the NAND-based MJV circuit

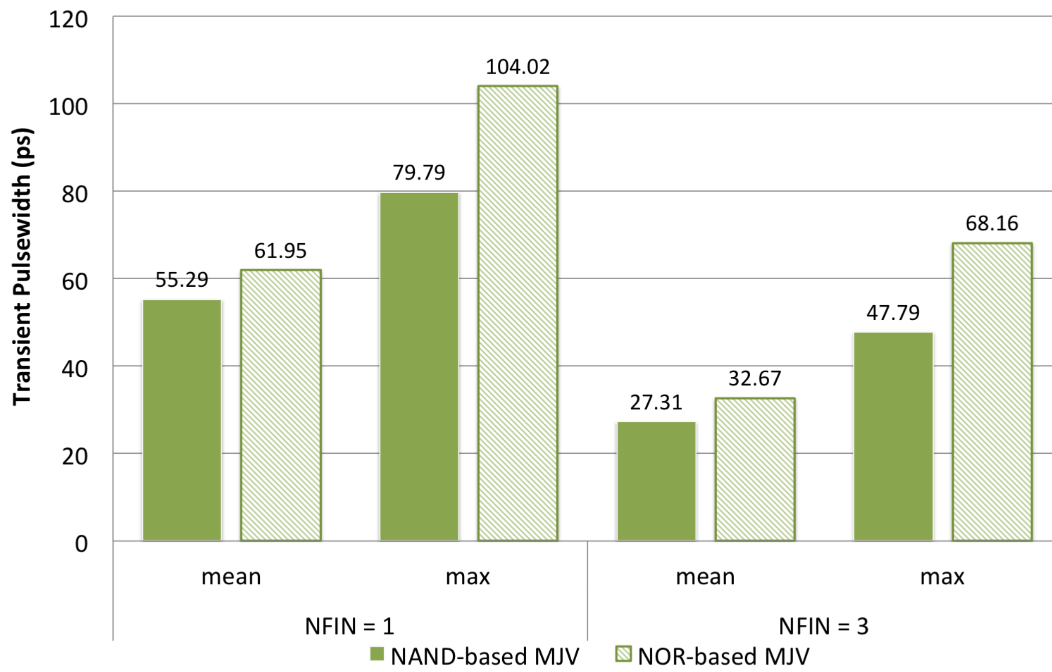


Source: From the author.

These results were obtained for the circuits under minimum sizing approach, which all transistors are designed with the number of fins NFIN equals to 1. As observed for the XOR circuits, up-sizing the circuits reduces the mean value of the SET pulsewidth and increases the impact of the WFF effect (AGUIAR et al., 2017b). Figure 5.11 presents the mean and the maximum SET pulsewidth for both designs when NFIN=1 and NFIN=3. The greater reductions on the transient pulsewidth were observed for the NAND-based circuit. The mean of the SET pulsewidth for the NAND-based MJV circuit exhibited a reduction of 50.6% and the maximum pulsewidth a reduction of 40.1%. For the NOR-based MJV circuit, a reduction of 47.3% in the mean value and 34.5% in the maximum SET pulsewidth.

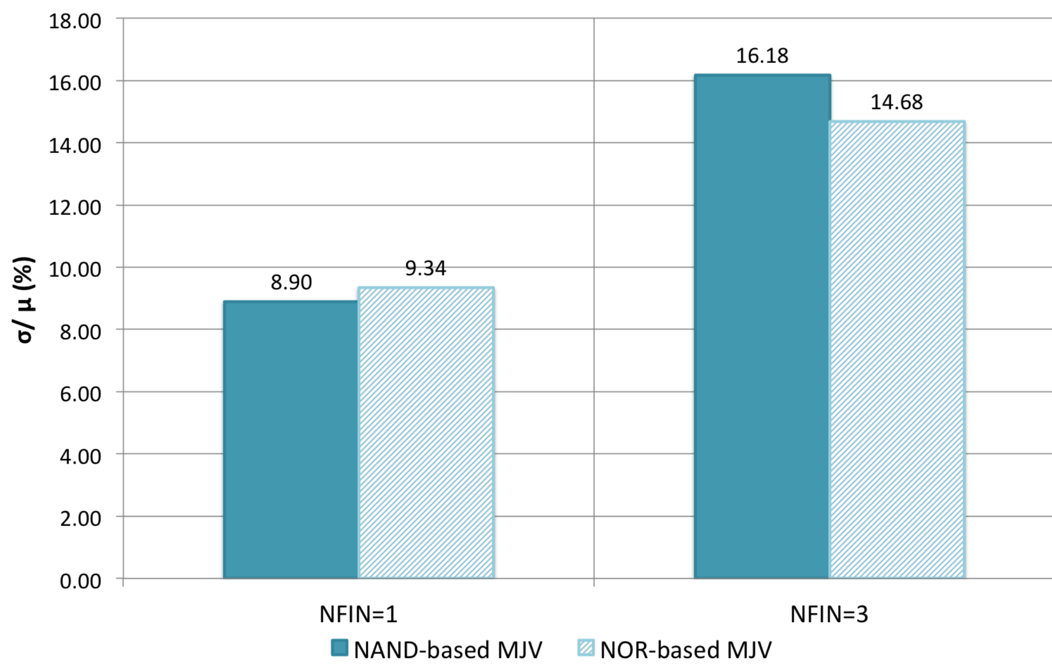
Although the mean pulsewidth is reduced with the increase of the number of fins, the standard deviation is increased. This behavior can interfere the validity of fault-tolerant schemes which rely on temporal constraints. Figure 5.12 presents the standard deviation normalized by the mean for both designs with NFIN=1 and NFIN=3. As observed, the NAND-based circuit increased 81.8% and the NOR-based circuit increased 57.2% in the normalized standard deviation of the SET pulsewidth. Despite the fact that the NAND-based MJV circuit has shown the greater reduction on the SET pulsewidth, it has shown the greater increase in the relative standard deviation, surpassing the NOR-based MJV circuit when NFIN=3.

Figure 5.11: The mean and maximum value of SET pulsewidth for the NAND-based and NOR-based MJV designed with NFIN=1 and NFIN=3



Source: From the author.

Figure 5.12: Relative Standard Deviation for the NAND-based and NOR-based MJV designed with NFIN=1 and NFIN=3

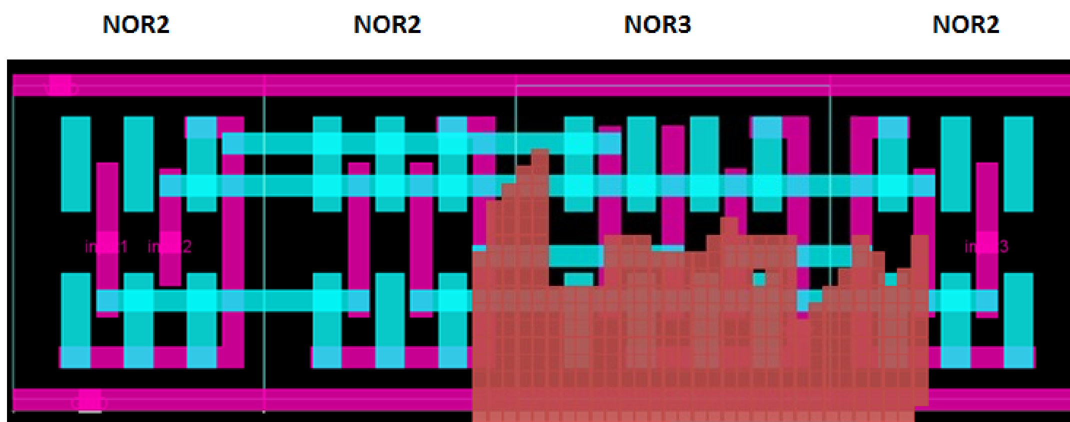


Source: From the author.

5.2.2 Layout Analysis

One of the interests of SEE prediction tool is the ability to determine the critical areas of device/gate. In this work, the critical area of NOR-based and NAND-based voters has been obtained from a simulation of heavy ion irradiation with an average LET of $10MeV\text{-}cm^2/mg$. Figure 5.13 presents the SET sensitivity mapping of the NOR-based majority voter in its most sensitive state, as reported in previous works (AHLBIN et al., 2013) (GADLAGE et al., 2011): the three inputs have been set at state “on”. The red area indicates the sensitive areas of the majority voter. A first interesting point is that most of the critical transistors are NFET transistors. Second, it is also interesting to note that the sensitive NFET transistors are issued from the NOR3 gate or from the adjacent NOR2 gates. Similarly, Figure 5.14 presents the SET sensitivity mapping of the NAND-based majority voter in its most sensitive state: the three inputs have been set at state “off”.

Figure 5.13: SET mapping of NOR majority voter obtained by simulation for a heavy ion at normal incidence with an average LET of about $10MeV\text{-}cm^2/mg$

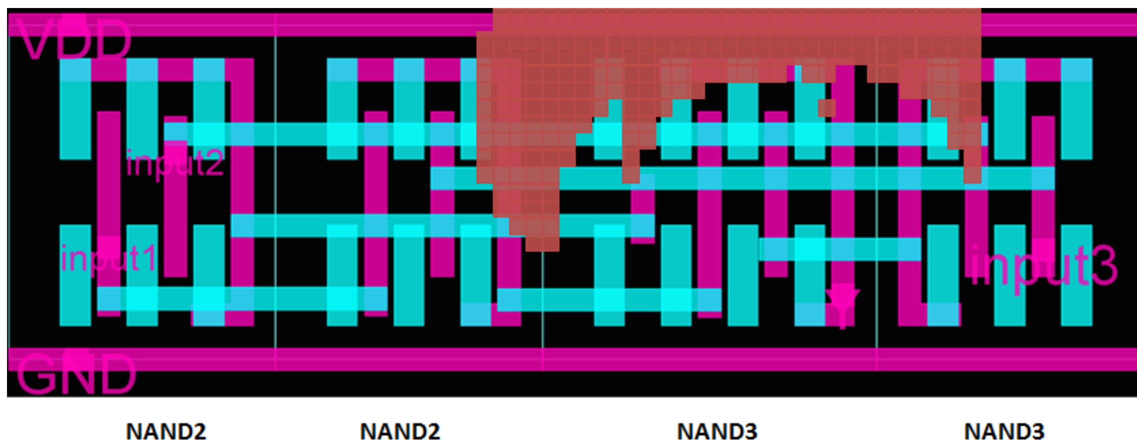


Source: (AGUIAR et al., 2017a).

Different from the observations for the NOR-based MJV, for this design most of the critical transistors are the PFET transistors. Additionally, it is also interesting to note that the sensitive PFET transistors are issued from the NAND3 gate or from the adjacent NAND2 gates.

These results are consistent with electrical simulations and are mainly induced by the strong multi-collection allowed by the bulk technology. The bulk substrate leads the diffusion of free carrier in the gate, which induces multiple SET pulses in the nodes of the majority voter. This effect is illustrated in the Figure 5.15, where the signals of internal and output nodes of the NOR-based majority voter can be observed. The majority

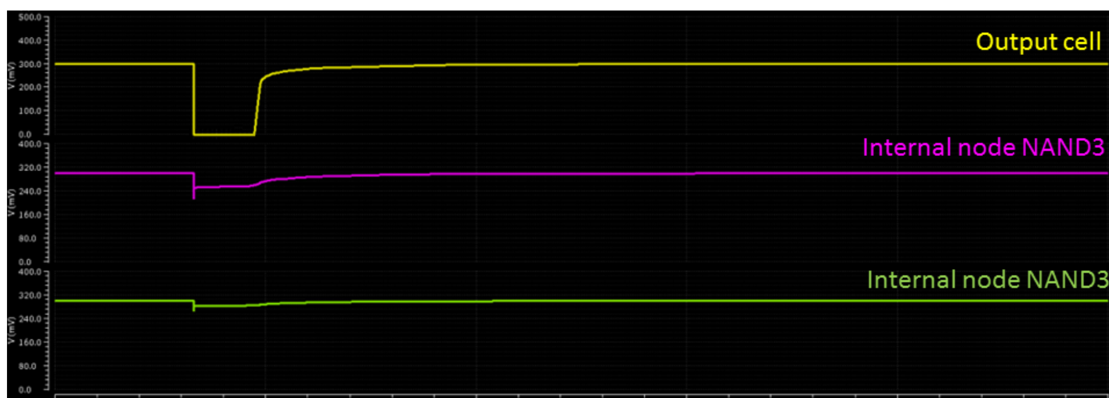
Figure 5.14: SET mapping of NAND majority voter obtained by simulation for a heavy ion at normal incidence with an average LET of about $10 MeV\text{-}cm^2/mg$



Source: (AGUIAR et al., 2017a).

voter is under a heavy ion at normal incidence with an average LET of about $15 MeV\text{-}cm^2/mg$. The SET event is observed in the output node (yellow curve). The multi-collection allowed by the bulk technology has induced the voltage drop of the two floating nodes of the NAND3 gate in the majority voter. The criticality of the SET pulse width will be discussed in the final section of this work.

Figure 5.15: SET waveform of internal and output nodes of majority voter based on NOR gate for a heavy ion at normal incidence with an average LET of about $15 MeV\text{-}cm^2/mg$



Source: (AGUIAR et al., 2017a).

5.2.3 Soft error sensitivity of majority voters at ground level

The goal of this section is to determine the SET sensitivity trends at ground level for the NAND and NOR-based majority voters. The atmospheric radiation environment

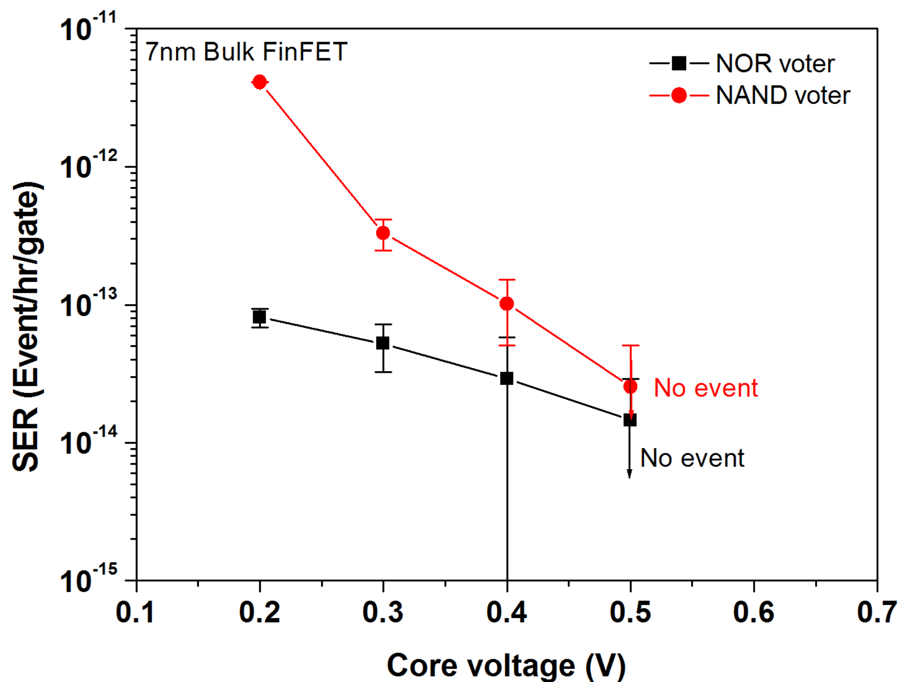
(neutron, protons and muons) and the alpha constrain are investigated. As mentioned, one of the constraints is the alpha particle. Alpha-emitting impurities can be found in some packaging materials, chemicals and materials used in the fabrication process of the chip. This alpha constraint can have a significant impact on the Soft Error Rate (SER) (HUBERT; ARTOLA; REGIS, 2015) (WROBEL et al., 2009). The emission rate can strongly vary depending on the quantity and purification grade of these materials. The α-emitter contamination effect is considered here as the sum of the package and wafer contributions. Four alpha emission categories can be considered for the package as summarized in Table 5.8. Figure 5.16 shows the evolution of SER induced by the atmospheric radiation environment at ground level, for the two voter designs as a function of core voltage.

Table 5.8: Alpha emissivity of the package in VLSI devices

Category of alpha emissivity	Alpha emissivity (α/cm/hr)
Standard	$\sim 10^{-2}$
Low Alpha	$\sim 5.10^{-3}$
Ultra Low Alpha	$\sim 5.10^{-4}$
Hyper Low Alpha	$\sim 5.10^{-5}$

Source: (AGUIAR et al., 2017a).

Figure 5.16: SER simulated for the NOR (black squares) and NAND (red dots) MJV circuits for the atmospheric constraint as a function of core voltage

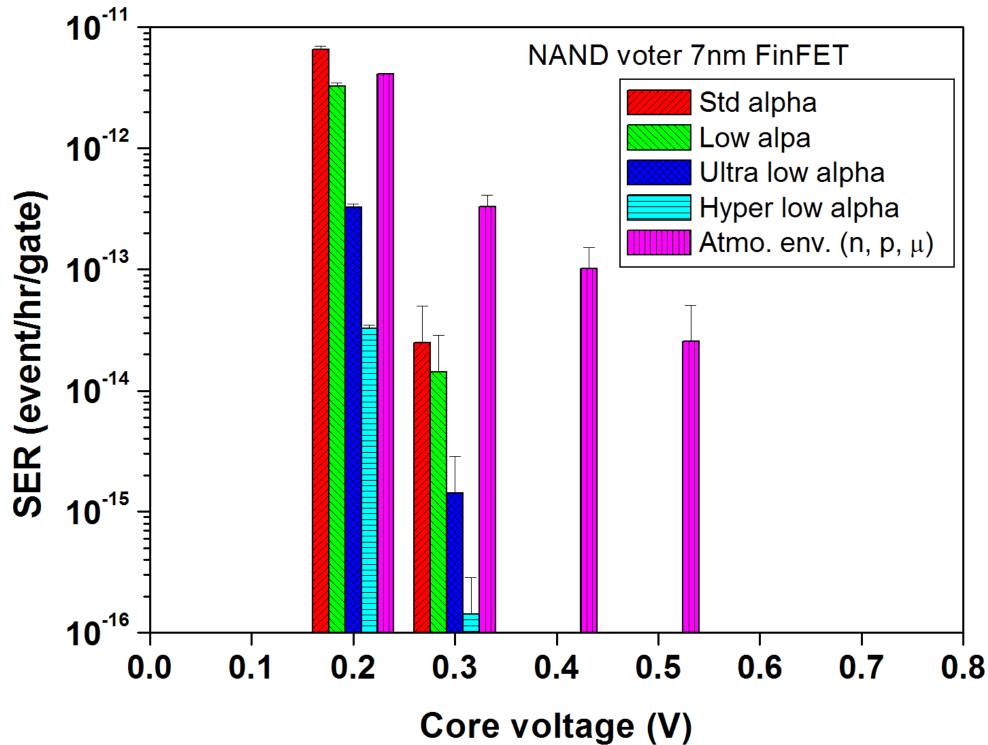


Source: (AGUIAR et al., 2017a).

The simulations highlight the higher soft error rate sensitivity of the NAND logic gate. The SER ratio between the NOR- and NAND-based MJV reaches 40X for the lowest core voltage, at 0.2V. At the threshold occurrence (0.5V), one SET has been considered and depicted by an arrow on the Figure 5.16. Note that the two majority voters are not sensitive to soft error at nominal voltage, 0.7V, considering operation at ground level. As future work, a stronger statistic analysis coupled with experimental irradiations with very high fluence, could be done in order to find rare events for this core voltage range.

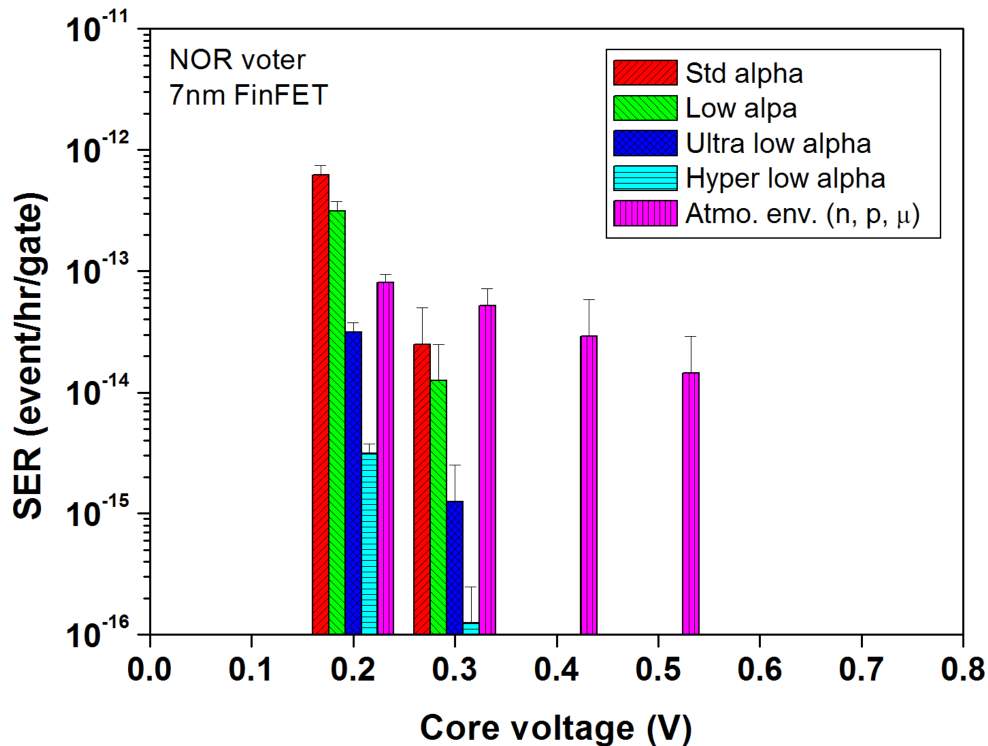
Figure 5.17 and Figure 5.18 shows the SER obtained for the NAND-based and NOR-based MJV circuits, respectively, both simulated for various alpha emissivity rate of the package and for the atmospheric environment at ground level. The atmospheric environment takes into account neutron, proton, and muon energy spectra. The SER has been calculated for a range of core voltage: from 0.7V down to 0.2V.

Figure 5.17: SER simulated for the NAND voter for the atmospheric constraint and for various alpha emissivity rate of the package as a function of core voltage



Source: (AGUIAR et al., 2017a).

Figure 5.18: SER simulated for the NOR voter for the atmospheric constraint and for various alpha emissivity rate of the package as a function of core voltage



Source: (AGUIAR et al., 2017a).

First, it is interesting to note the strong robustness of both majority voters. At nominal core voltage, i.e., 0.7V, no event has been observed even with alpha constraint. Note that one event has been considered with an error bar of 100%. Second, note that for higher core voltage than 0.3V, neutron, protons and muons particles are more critical than the alpha constraint. While at 0.2V the alpha constraint is significant in the SER for the two majority voters.

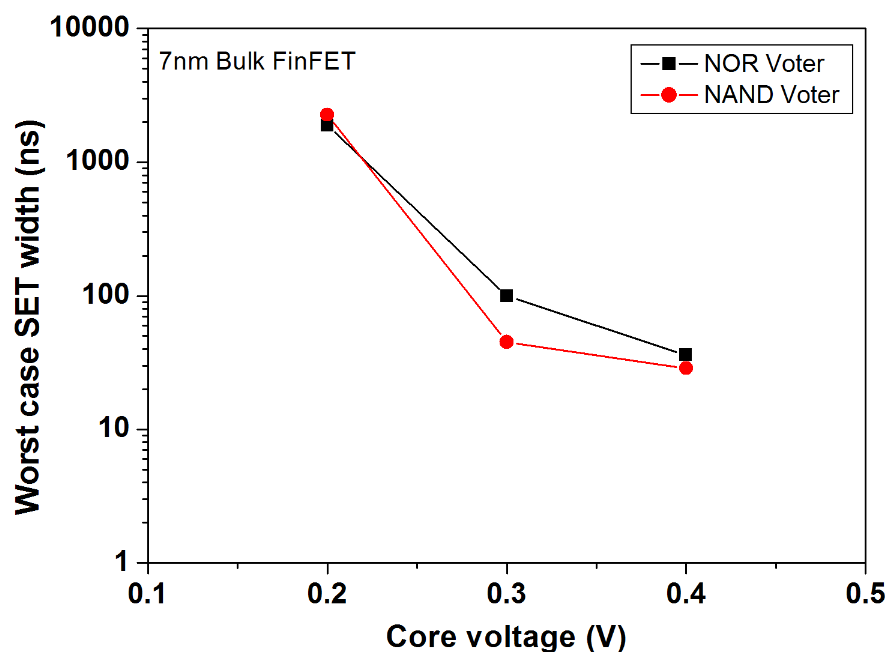
Further, the NOR-based voter seems to be slightly less sensitive than the NAND-based MJV as it provides lower SER. This point was not expected considering the higher sensitivity of standalone NOR gate observed in previous works (ARTOLA; HUBERT; ALIOTO, 2014). However, these previous simulation results have been obtained for an asymmetric design of NFET and PFET transistors (ARTOLA; HUBERT; ALIOTO, 2014). The asymmetric design performed in previous works has been done by a lower number of fins for NFET transistor of the NOR gate. It is not the case in this work. The elementary NOR and NAND gates have been designed with the same number of fins for NFET and PFET transistors. The symmetric design induced a higher drive current. It

improved the SEU robustness of the two majority voters and decreased the difference in the SER between the NOR and NAND gates.

5.2.4 Analysis of SET worst-case occurrences of majority voters at ground level

The final discussion of this work is focused on the worst case of the soft error occurrence in the two majority voters at ground level. The point is discussed by the analysis of the worst case of SET pulsewidth induced directly or indirectly by alpha and atmospheric particles. Figure 5.19 shows the widest SET pulse observed by simulation under atmospheric and alpha environment as a function of core voltage for the two majority voters.

Figure 5.19: Worst case of SET pulse width induced in atmospheric and alpha environment of NOR (red squares) and NAND (red dots) voter as a function of core voltage



Source: (AGUIAR et al., 2017a).

The simulations show a strong increase in the SET pulsewidth with the decrease in the core voltage for the two majority voters. This trend is in good correlation with previous works done on FinFET technologies (ARTOLA; HUBERT; ALIOTO, 2014). Note that, the largest SET pulse are observed for the NOR voter while its SER is lower than the NAND voter. This point is confirmed for the core voltages, except at 0.2V.

The worst case SET pulsewidth is a very important metric because of its utility to define the most relevant timing of clock tree used with the Flip-Flops system. Although the NOR-based MJV seems to be less radiation sensitive due to a lower SER, it presents wider transient pulses which must be taken into consideration in the early designs stages.

6 CONCLUSION AND FUTURE WORK

The ongoing scaling of technology has provided significant improvement in terms of processing power and performance of electronic systems. However, it is directly related to the decrease of reliability of designs. Scaling increases process, voltage, and temperature variability as well as the susceptibility to the effects of noise from the environment as radiation effects and/or electromagnetic interference. Fault-tolerant techniques are usually used to improve the robustness of electronic systems which require high reliability. However, the implications of the scaling of technology have interfered in the assurance of the effectiveness of fault-tolerant approaches. As variability effects take place in the electrical characteristics of the advanced devices, statistical analysis is necessary to understand and evaluate the reliability of designs. For this reason, this work has evaluated the radiation robustness of different circuits in FinFET technology under variability effects. In order to discover the best design options to implement fault-tolerant techniques such as, for example, the Triple-Module Redundancy (TMR) and/or Duplication with Comparison (DWC) schemes, the set of analyzed circuits were composed of ten different exclusive-OR (XOR) logic gate topologies and two majority voter (MJV) circuits.

Regarding the XOR topologies, two widely logic implementation concepts are used: CMOS complementary and Pass-Transistor logic families. It was found that not necessarily the output node of a logic gate is characterized as the most sensitive node. The topologies with multiple logic stages might have the most sensitive node as an internal node, depending on the drive strength of each stage. FinFET devices can be designed as a double-gate (DG FinFET) device which the channel is formed exclusively by the sidewalls of the fins, or as a tri-gate (TG FinFET) device which the channel is formed by the sidewalls plus the top side of the fin. Accordingly, the XOR designs were evaluated in the two configurations in order to determine which one exhibit a greater radiation robustness. From the simulation experiments, it can be concluded that TG FinFET circuits have an advantage compared to DG FinFET circuits in terms of radiation robustness. Overall, the XOR_V6 has shown to be the least sensitive to radiation effects for all three technologies in this study, considering both devices. Further, at $7nm$ and $20nm$, XOR_V4 is the most sensitive in both devices while XOR_8 is the most sensitive at $14nm$. Considering the variability, XOR_V5 was the most sensitive circuit to the supply voltage variation while XOR_V2 or XOR_V3 were the most robust.

Additionally, this work investigated the implications of Work-Function Fluctuation (WFF) to the radiation robustness of the XOR topologies at $7nm$ FinFET. The results demonstrated a considerable increase in the radiation-induced transient pulsewidth. The impact of WFF was also evaluated to a wide range of temperatures (from -10ºC to 125ºC). Different from most of the analyzed circuits, the XOR_V6 has shown a steady relative standard deviation under temperature variation, while the rest of topologies demonstrated an increase as the temperature is reduced. Different sizing approaches and voltage scaling are also evaluated to provide a broader understanding of the WFF impact. As the number of fins is increased, the SET pulsewidth is reduced. However, the relative standard deviation σ/μ is expected to increase, compromising the effectiveness of temporal radiation redundant techniques, for example. Further, the increased interest in low power designs will also lead to an increase in the standard deviation of SET pulsewidth as the supply voltage is reduced. It highlights the need to consider the variability impact to evaluate the radiation robustness of different designs to provide effective fault-tolerant techniques.

Regarding the MJV circuits, two implementations based on basic logic cells were analyzed: NAND-based and NOR-based MJV circuits. Initially, both circuits were designed in SPICE level and evaluated under WFF with two different sizing. The simulation experiments revealed that when the MJV circuits are designed with NFIN=1, the most sensitive to the WFF effect is the NOR-based MJV due to a higher relative standard deviation on the SET pulsewidth. However, when the circuits are designed with NFIN=3 this scenario changes as the larger deviation is observed for the NAND-based MJV.

In order to examine the contribution of the layout design and the BEOL and FEOL layers of an advanced technology to the radiation sensitivity, the MJV circuits were also designed using the $7nm$ FinFET Predictive Process Design Kit (ASAP7). Then, from the layout characteristics extracted from the GDS file, it was able to estimate the SER of the MJV circuits regarding radiation constraints, alpha, and atmospheric environment. The MUSCA SEP3 tool was used for this purpose. Overall, it is observed a high radiation robustness of the two majority voters. In accordance with the SPICE simulations, the MUSCA SEP3 estimated that the SET pulsewidth is larger for the NOR-based than for the NAND-based MJV circuit. However, the NOR-based voter seems to be slightly less sensitive than the NAND voter as it provides lower SER. The sensitivity to the supply voltage was also evaluated using the MUSCA SEP3 considering a voltage scaling from the nominal voltage until 0.3V. At nominal supply voltage, i.e. 0.7V, no event has been observed for alpha and atmospheric environment. In the future, a stronger statistic analy-

sis coupled with experimental radiation campaigns with very high fluence could be done in order to find rare events for this core voltage range.

In summary, the results emphasize the impact of variability effects to the radiation robustness of designs in advanced technology as bulk FinFET devices. Indeed, the choice of the device architecture induces different robustness, as it was observed a better radiation response for tri-gate FinFET devices. Also, it can be concluded that different topologies for the same logic function can exhibit different behaviors regarding both the variability effects and the radiation effects. Additionally, the transistor sizing affects the radiation sensitivity under variability as it causes the circuits to behave differently for each sizing approach.

6.1 Future Works

As future work suggested to answer questions raised during this work:

1. To design the layout of XOR logic gates using FinFET PDK available in the literature and evaluate the radiation robustness using a Monte-Carlo predictive tool which takes into consideration the layout characteristics and the FEOL and BEOL layers of advanced technologies to provide a better understanding of the radiation sensitivity of such circuits.

2. To expand the majority voter analysis in this work by designing the layout of different implementations of the majority voter logic function, for example, by using complex-gates circuits, to provide a broader comparative analysis.

3. To design the layout of a set of basic logic cells with different sizing approach in order to extend the understanding regarding its impact on the radiation sensitivity of circuits designed in FinFET technology.

4. To evaluate a comparison analysis by replicating the experiments for the analyzed circuits by using different devices, such as FDSOI.

5. To manufacture the circuits in advanced technology nodes available in the industry and to perform radiation campaigns to gather experimental data from silicon.

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APPENDIX A — LIST OF PUBLICATION

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