UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM COMPUTAÇÃO

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Timing Vulnerability Factor Analysis in Master-Slave D Flip-Flops

Thesis presented in partial fulfillment of the requirements for the degree of Master of Computer Science

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Porto Alegre
5th February 2016

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

L. Zimpeck, Alexandra
Timing Vulnerability Factor Analysis in Master-Slave D Flip-Flops / Alexandra L. Zimpeck - 2016.
104 f.: il.
Advisor: Ricardo Augusto da Luz Reis
Co-advisor: Fernanda Lima Kastensmidt
Dissertation (master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Computação. Porto Alegre, BR – RS, 2016.
1.Microelectronics 2. Soft Errors 3. Window of Vulnerability 4. Timing Vulnerability Factor 5. Environmental Variability

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"Mas eu não vim até aqui para desistir agora. Minhas raízes estão no ar, minha casa é qualquer lugar, se depender de mim eu vou até o fim."

Engenheiros do Hawaii (Humberto Gessinger)

AGRADECIMENTOS

Em primeiro lugar gostaria de agradecer aos meus PAIS, Alexandre e Dulcinara, pelo amor incondicional e incentivo aos estudos recebido desde as primeiras etapas da minha vida. A eles que sempre me motivaram a ir atrás dos meus sonhos, minha eterna gratidão. Eu não chegaria até aqui sem o apoio deles.

Ao meu IRMÃO Lucas, tão pequeno, mas de sabedoria enorme, o maior e melhor presente que meus pais podiam ter me dado. Aquele que muitas vezes não entendeu a minha ausência, mas que sempre que precisei, esteve ao meu lado. A toda a minha FAMÍLIA e aos meus AMIGOS que sempre torceram por mim e que compreenderam os vários momentos importantes em que eu não pude estar presente. Ao AMOR André Furlan, pelo companheirismo, paciência e apoio durante a reta final deste trabalho.

Aos meus COLEGAS de laboratório e de disciplinas da UFRGS, Gracieli, Felipe, Geancarlo, Calebe, Walter, Jucemar, Mateus, Tiago, Tania, Guilherme, Vitor, Adriel, Jorge, Louise, Vladimir, Lucas, Vinícius, Jody, Augusto e Cícero, muito obrigada por toda a ajuda que me deram na realização deste trabalho e pela amizade ao longo deste tempo. Especialmente, agradeço a Cristina Meinhardt por todo incentivo a pesquisa científica desde a graduação até os dias de hoje, e também por me aconselhar em todas as dúvidas que tive durante todos esses anos.

Ao meu ORIENTADOR, professor Ricardo Reis, por sempre acreditar no meu potencial, por me incentivar a continuar na pós-graduação e por me auxiliar em todas as etapas durante o mestrado. Agradeço também a minha COORIENTADORA, professora Fernanda Kastensmidt, por todas as discussões e apoio que foi dado para a realização deste trabalho. E por fim, agradeço a todos os PROFESSORES que passaram pela minha vida, desde as séries iniciais até os dias de hoje e que contribuíram com os seus conhecimentos para minha formação.

ABSTRACT

Technology scaling has brought undesirable issues to maintain the exponential growth rate and it raises important topics related to reliability and robustness of electronic systems. Currently, modern super pipelined microprocessors typically contain many millions of devices with ever decreasing load capacitances. This factor makes circuits more sensitive to environmental variations and it is increased the probability to induce a soft error. Soft errors in sequential circuits occur when a single energetic particle deposits enough charge near a sensitive node. Master-slave flip-flops are the most adopted sequential elements to work as registers in pipeline and finite state machines. If a bit-flip happens inside them, they lose the previous stored information and may cause an incorrect system operation. To provide reliable systems that can cope with radiation effects, this work analysis the Timing Vulnerability Factor (TVF) of some master-slave D flip-flops topologies in pipeline stages under different operating conditions. The effective time window, which the bit-flip can still be captured by the next stage, is defined as Window of Vulnerability (WOV). TVF corresponds to the time that a flip-flop is vulnerable to radiation-induced soft errors according to WOV and clock frequency. In the first step of this work, it is determined the dependence between the TVF with the fault propagation to the next stage through a combinational logic with different propagation delays and with different nanometer technological models, including also high performance and low power versions. All these simulations were made under the pre-defined nominal conditions in technology files. The variability manifests with an increase or decreases to initial specification, where the main problem is the uncertainty about the value stored in sequential. In this way, the second step of this work evaluates the impact that environmental variability effect causes in TVF. Some simulations were redone considering supply voltage and temperature variations in different master-slave D flip-flop topologies configurations. To achieve better results, it is necessary to try to decrease the TVF values to reduce the vulnerability to bit-flips. The propagation delay between two sequential elements and higher clock frequencies collaborates to reduce TVF values. Moreover, all the information can be easily integrated into Electronic Design Automation (EDA) tools to help identifying the most vulnerable master-slave flip-flops before mitigating or replacing them by radiation hardened ones.

Keywords: Microelectronics, Soft Errors, Window of Vulnerability, Timing Vulnerability Factor, Environmental variability.

Análise do Fator de Vulnerabilidade Temporal em Flip-Flops Mestre-Escravo do tipo D

RESUMO

O dimensionamento da tecnologia trouxe consequências indesejáveis para manter a taxa de crescimento exponencial e levanta questões importantes relacionadas com a confiabilidade e robustez dos sistemas eletrônicos. Atualmente, microprocessadores modernos de superpipeline normalmente contêm milhões de dispositivos com cargas nos nós cada vez menores. Esse fator faz com que os circuitos sejam mais sensíveis a variabilidade ambiental e aumenta a probabilidade de um erro transiente acontecer. Erros transientes em circuitos sequenciais ocorrem quando uma única partícula energizada deposita carga suficiente perto de uma região sensível. Flip-Flops mestre-escravo são os circuitos sequencias mais utilizados em projeto VLSI para armazenamento de dados. Se um *bit-flip* ocorrer dentro deles, eles perdem a informação prévia armazenada e podem causar um funcionamento incorreto do sistema. A fim de proporcionar sistemas mais confiáveis que possam lidar com os efeitos da radiação, este trabalho analisa o Fator de Vulnerabilidade Temporal (*Timing Vulnerability Factor* - TVF) em algumas topologias de flip-flops mestre-escravo em estágios de *pipeline* sob diferentes condições de operação. A janela de tempo efetivo que o *bit-flip* ainda pode ser capturado pelo próximo estágio é definido com janela de vulnerabilidade (WOV). O TVF corresponde ao tempo que o *flip-flop* é vulnerável a erros transientes induzidos pela radiação de acordo com a WOV e a frequência de operação. A primeira etapa deste trabalho determina a dependência entre o TVF com a propagação de falhas até o próximo estágio através de uma lógica combinacional com diferentes atrasos de propagação e com diferentes modelos de tecnologia, incluindo também as versões de alto desempenho e baixo consumo. Todas as simulações foram feitas sob as condições normais pré-definidas nos arquivos de tecnologia. Como a variabilidade se manifesta com o aumento ou diminuição das especificações iniciais, onde o principal problema é a incerteza sobre o valor armazenado em circuitos sequenciais, a segunda etapa deste trabalho consiste em avaliar o impacto que os efeitos da variabilidade ambiental causam no TVF. Algumas simulações foram refeitas considerando variações na tensão de alimentação e na temperatura em diferentes topologias e configurações de flip-flops mestre-escravo. Para encontrar os melhores resultados, é necessário tentar diminuir os valores de TVF, pois isso significa que eles serão menos vulneráveis a *bit-flips*. Atrasos de propagação entre dois circuitos sequenciais e frequências de operação mais altas ajudam a reduzir o TVF. Além disso, estas informações podem ser facilmente integradas em ferramentas de EDA para ajudar a identificar os flip-flops mestre-escravo mais vulneráveis antes de mitigar ou substituí-los por aqueles tolerantes a radiação.

Palavras-chave: Microeletrônica, Soft Errors, Janela de Vulnerabilidade, Fator de Vulnerabilidade Temporal, Variabilidade Ambiental.

LIST OF ABBREVIATIONS AND ACRONYMS

AVF	Architecture Vulnerability Factor
CMP	Chemical-Mechanical Planarization
CMOS	Complementary Metal-Oxide Semiconductor
IC	Integrated Circuits
EDA	Electronic Design Automation
FA	Full-Adder
FF	Flip-Flop
FinFET	Fin-Shaped Field-Effect Transistor
GND	Ground
HA	Half-Adder
HP	High-Performance
ITRS	International Technology Roadmap for Semiconductors
LE	Logical Effort
LET	Linear Energy Transfer
LP	Low Power
LSTP	Low Standby Power
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MS	Master-Slave
MTS	Minimum Transistor Sizing
NBTI	Negative Bias Temperature Instability
NFET	N Field-Effect Transistor
NMOS	N-channel Metal-Oxide Semiconductor
OTS	Optimized Transistor Sizing
PDP	Power-Delay-Product
PFET	P Field-Effect Transistor
PMOS	P-channel Metal-Oxide Semiconductor
PTM	Predictive Transistor Model

PVT	Process, Voltage and Temperature
RDF	Random Dopant Fluctuation
SCE	Short-Channel Effects
SE	Soft Errors
SEB	Single Event Burnout
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEL	Single Event Latchup
SER	Soft Error Rate
SEU	Single Event Upset
SET	Single Event Transient
SMSFF	Standard Master-Slave D Flip-Flop
SPICE	Simulation Program with Integrated Circuits Emphasis
SR	Set-Reset
STA	Static Timing Analysis
TGMSFF	Transmission-Gate Master-Slave D Flip-Flop
TVF	Timing Vulnerability Factor
VDD	Supply Voltage
VLSI	Very Large Scale Integration
WFF	Workfunction Fluctuation
WOV	Window of Vulnerability
WPMSFF	Write-Port Master-Slave D Flip-Flop

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1 INTRODUCTION

As the transistor size shrinks, integrated circuits (IC) can contain tens millions of sequential logic elements, such as latches and flip-flops, as well as combinational logic elements in the same chip, satisfying the demand for higher density, more functionality and low power consumption (ANGHEL et. al, 2007b). However, technology scaling also brings undesirable issues to maintain the exponential growth rate and raises important topics related to reliability and robustness of electronic systems. The most common unwanted effects presented in nanometer technologies are aging effects, process and environmental variability. These effects significantly increase the leakage currents and radiation-induced Soft Errors (SE) (ANGHEL et. al, 2007a; ORSHANSKY et. al, 2008).

The manufacturing process in sub-micron technologies demands modifications in the physical design due to the miniaturization of components. It is defined more complex layout rules (MEINHARDT, 2014). These modifications collaborate directly with the increase of process and environmental variability on CMOS devices. Moreover, technology scaling has been reducing the load capacitances and supply voltages that impact on the minimal charge required to induce a soft error (HUBERT et. al, 2013). A relevant matter today in the semiconductor industry is to cope mainly with these variability factors.

Soft errors occur when a single energetic particle deposits enough charge near a sensitive node in a sequential or combinational circuit. In bulk CMOS technologies, any PN-junction of the PMOS or NMOS transistors is considered a sensitive region (BAUMANN, 2005). The main sources of energetic particles that contribute to radiation effects are protons and electrons trapped in the Van Allen belts, heavy ions trapped in the magnetosphere, galactic cosmic rays and solar flares (VELAZCO et. al, 2007).

Fig. 1.1 shows the complete sequence of events from ionization until a failure, and the fault tolerance technique more suitable for each stage to guarantee the design of reliable circuits. The ionization (1) happens when an energetic particle strikes in the PN-junction of a transistor. The path formed due to ionization, results in a set of electron-hole pairs that generate a transient current due to the collected charge from the junction (2). If the collected charge is high enough to exceed the critical charge (Qcrit), where the on-transistor cannot balance the current, the transient voltage pulse appears and it causes a fault (3). The fault consists in an unexpected behavior that can change

the data state of logic gates, memory cells, registers, latches or flip-flops (DODD et. al, 2003).

This phenomenon is known as Single Event Effects (SEE) and it produces a wide range of effects that can be divided into permanent, intermittent or transient faults. Permanent faults remain for long periods till a corrective action is taken, whereas transient faults appear and disappear in a short time interval (MUKHERJEE, 2008).

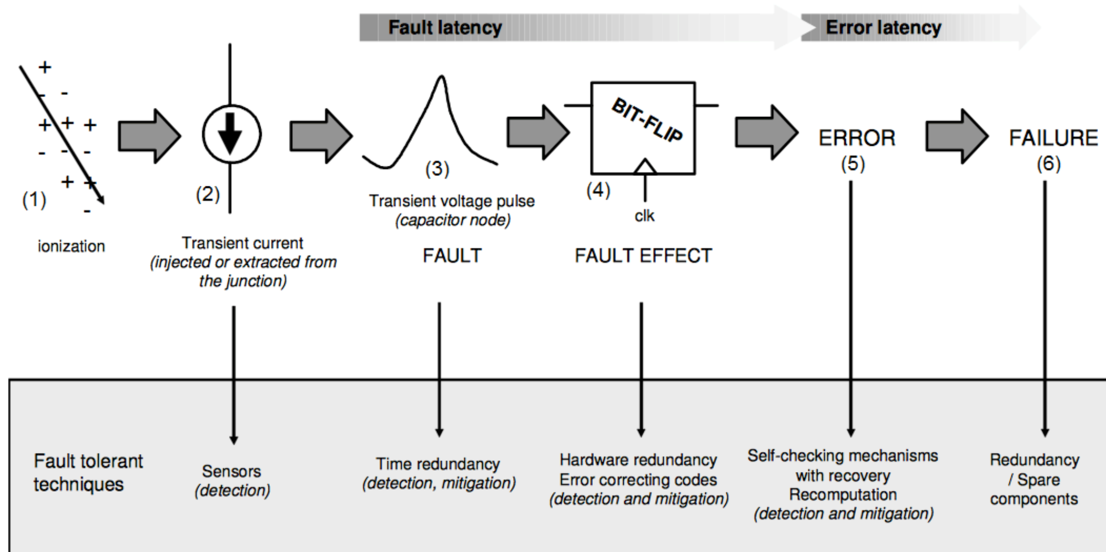


Figure 1.1: Complete sequence of events from ionization until a failure (KASTENSMIDT, 2007)

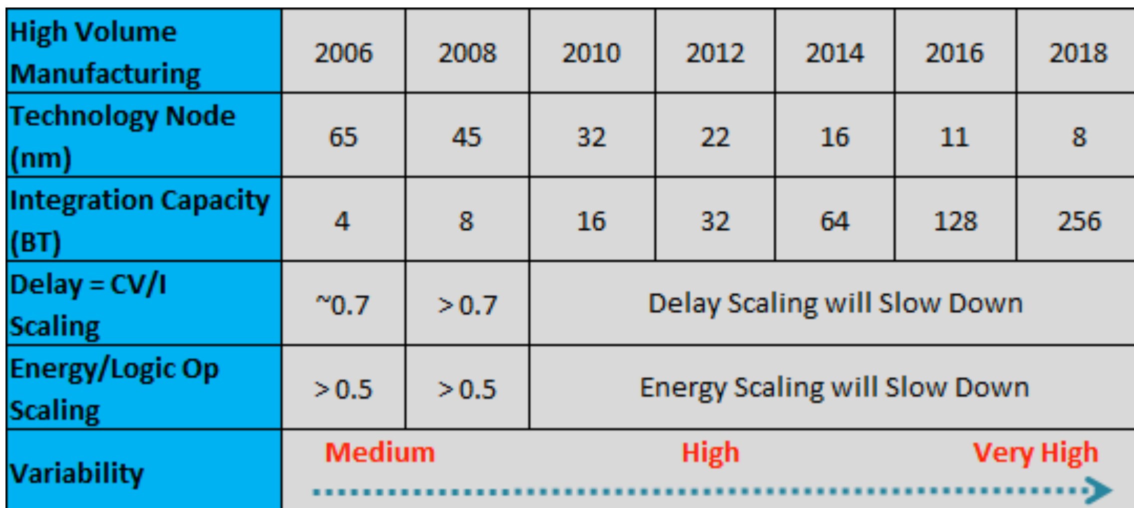
Two most common single events due to soft errors are Single Event Upset (SEU) and Single Event Transient (SET), which have been gaining prominence due the critical charge decreases with technology scaling. SEU or bit-flip occurs when an ionized particle hit inside a sequential logic while SETs happen when an ionized particle hits in a combinational logic (BRAMNIK et. al, 2013). Fault effects always will depend on the type of SEE. For example, the fault effect of SEUs is the inversion of an original stored data (4). If the SET has been propagated and the next sequential element latched in time this effect, the SET will become an SEU (BENEDETTO et. al, 2004).

Faults may or not lead a system to an error. An error is the manifestation of a fault and it generates value changes in internal operations (5). Permanent faults can cause permanent/hard errors; intermittent faults can cause intermittent errors, and transient faults can cause transient/soft errors. If the faults and errors cannot be masked or tolerated, the system malfunction will be visible to the user. This is commonly known as a failure (6). Faults detected early in designs can use simpler and cheaper techniques to tolerate them. The time period that a fault occurs until the moment that manifests itself as an error is defined as fault latency. Similarly, the time period that the error occurs until the moment that itself manifests as a failure is defined as error latency (WEBER, 2002).

Technology scaling introduced another important concern related to variability effects. Variability is the manufacturing-induced variations in a component. The main problem associated with them is the uncertainty about the correct circuit operation. Each circuit may present a different behavior, as a high deviation on performance or abnormal power consumption (SAHA, 2010). Moreover, variability generates many modifications along the lifetime of a circuit due to unexpected behaviors. It can accelerate the circuit degradation and make the circuit inappropriate for its initial purpose (GSS, 2010).

The variability can be divided into three factors (NASSIF, 2008): environmental, reliability and physical. Environmental factors appear during the operation of a circuit. The most common examples are the power supply and temperature variations. Reliability factors are related to transistor aging due the high electrical fields presented in modern circuits. Electromigration and Negative Bias Temperature Instability (NBTI) are classical problems in the reliability area. Finally, the physical factors are associated to variations of geometric or electrical parameters. In the majority of cases, physical variations are caused during the lithography step of the fabrication process.

Fig. 1.2 shows the evolution of variability perspective in recent years. The technology scaling has already presented a significant raise of variability effects since the 65nm technology node. The performance commitment is one of the disadvantages brought by variability effects. According to Fig. 1.3, the performance prediction cannot be reached in last decades. The red curve indicates the maximum frequency achieved in each year, and it is possible to see that the performance gain started to stabilize between 2006 and 2008. This behavior happens due to the variability effects and also it has relation with other challenges brought by technology scaling.



High Volume Manufacturing	2006	2008	2010	2012	2014	2016	2018
Technology Node (nm)	65	45	32	22	16	11	8
Integration Capacity (BT)	4	8	16	32	64	128	256
Delay = CV/I Scaling	~0.7	>0.7	Delay Scaling will Slow Down				
Energy/Logic Op Scaling	>0.5	>0.5	Energy Scaling will Slow Down				
Variability	Medium			High			Very High

Figure 1.2: Evolution of variability perspective in bulk CMOS nanotechnologies (BORKAR, 2009)

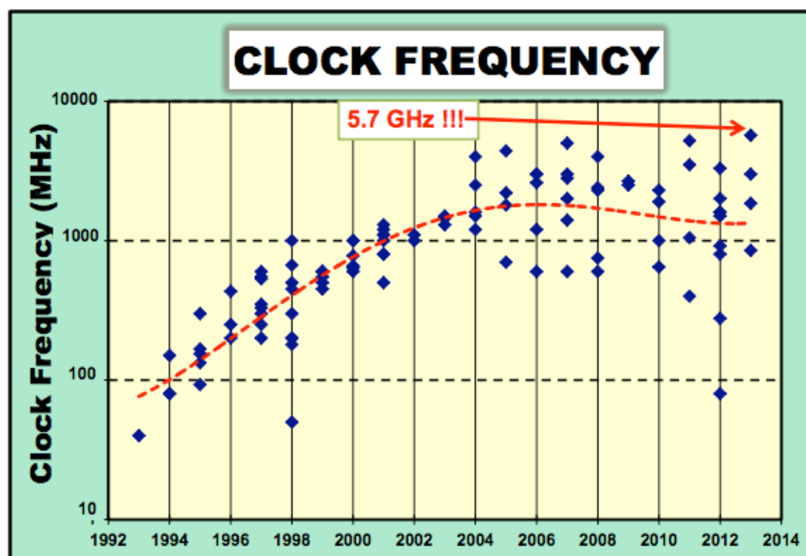


Figure 1.3: Clock frequency trends in the last decades (ISSCC, 2013)

Although bulk CMOS technology have been used in integrated circuits designs for several decades. At each new technology node, it suffers from undesirable leakage currents and Short-Channel Effects (SCE) (KING, 2005). According to the ITRS analysis (ITRS, 2011), FinFET (Fin-Shaped Field Effect Transistor) technology is pointed as the main multigate device to replace bulk CMOS in sub-22nm technology nodes to continue with technology scaling. The appendix shows a brief report of the research related to this subject that was done in parallel with this dissertation. The research has consisted in the analysis of the impact of process, voltage and temperature (PVT) variations on timing and total power in FinFET technology nodes.

Master-Slave Flip-Flops (MSFF) are the most adopted sequential elements in Very Large Scale Integration (VLSI) designs to storage data in registers and in finite state machines. If a bit-flip occurs inside them, they may lose the previous stored information, followed by an incorrect system operation. In order to provide reliable systems to cope with radiation and variability effects, this work analyses the Window of Vulnerability (WOV) and the Timing Vulnerability Factor (TVF) in different MS D Flip-Flops topologies in pipeline stages.

The effective time window, which the bit-flip can still be captured by the next stage, is defined as Window of Vulnerability (WOV) (NGUYEN et. al, 2005). TVF corresponds to the time that a flip-flop or a latch is vulnerable to radiation-induced soft errors according to WOV and clock frequency (SEIFERT et. al, 2004). In addition to the clock frequency, the TVF also depends of process technology, the logic propagation delay between two sequential elements and environmental variations. To achieve better results, it is necessary to try to decrease the TVF values to reduce the vulnerability to bit-flips. The next subchapters describe related researches, motivations and contributions of this work.

1.1 Related Researches

Many studies have compared FFs topologies regarding to performance, power consumption and timing characteristics in nanotechnologies, but neither of these showed a detailed analysis about the window of vulnerability of MSFF in a pipeline design. In (GIACOMOTTO et. al, 2007), a set of memory elements was analyzed in a real application, and it was proved that the most efficient flip-flops are identified through a pipeline structure. (ALIOTO, 2010) proposed a design flow for MS flip-flops to reach the better relation between power consumption and propagation delays. The interconnection delays also were considered in this flow. (ALIOTO, 2011) showed a comparison for a large quantity of FFs topologies in the energy-delay-area domain of nanometer CMOS flip-flops.

(SEIFERT and TAM, 2004) described a method for computing TVF of MS flip-flops and flow-through latches of a high-performance microprocessor, capturing the impact of sequential elements in your typical operating environment. This paper demonstrated that TVF has a high dependency with a propagation delay between two sequential circuits in a pipeline, and it varies between 0% and 50%. (HEIJMEN, 2008) created an approach to make an accurate estimation of the contribution of flip-flops to the Soft Error Rate (SER) of an IC. His approach is based on a set of expressions to calculate the TVF of master and slave latches, but it is only applicable to frequencies below 1GHz. (BRAMNIK et. al, 2013) introduced a novel technique for computing TVF in modern complex synchronous designs, where all key inputs are based on static timing data readily available in most design databases.

A complete explanation of variability concerns in bulk CMOS technologies sub-90nm is shown in (MASUDA et. al, 2005). (KUMAR, 2010) and (BORKAR, 2003) explore the performance of devices and interconnections when the temperature suffers variations. These works also describe the increase in fault susceptibility when temperature oscillations occur. Various analysis and comparisons have been carried out to evaluate variability effects in flip-flops, (NEUBERGER et. al, 2007), (REBAUD et. al, 2008) and (LOTZE et. al, 2008) showed the impact of variations on timing characteristics in different flip-flops topologies. (ALIOTO et. al, 2015) investigated the impact of all fundamental sources of variations on performance and robustness against hold time violations in some MS flip-flops. The analysis has considered process, voltage, temperature and clock slope variations in 65nm CMOS technology.

1.2 Motivation and Contributions

Latches and flip-flops are widely adopted in VLSI systems due the ability to control flow and storage data. Moreover, sequential elements are the most instantiated cell in digital integrated circuits, representing from 30% to 50% of the total circuit area (OKLOBDZIJA et. al, 2003). Radiation effects in ICs can range from low magnitude noises or large transient pulses that are able to generate transient upsets or soft errors affecting the data integrity.

Using radiation-hardened devices will often solve the radiation effects problem, but these circuits have some disadvantages. The hardened circuits are more expensive than non-hardened circuits and not all circuits are available in a hardened version. Hardened circuits are usually fabricated using mature technologies, and they have sale limitations (KASTENSMIDT, 2007). So, it is very important to study techniques to mitigate the radiation effects in non-hardened circuits. The prediction of the time quantity that non-hardened sequential circuits are vulnerable to upsets is crucial to guarantee the integrity of stored data.

Previous works calculate the window of vulnerability without considering the setup time of master and slave latches, but electrical simulations have been made and it was proved that the setup time of latches is also sensitive to bit-flips. For this, all analysis in our research were made respecting the definition provided in references, but the setup time was taken into account to calculate the WOV of MS Flip-Flops.

This work analyzes three different MSFF topologies under bit-flip in a pipeline design to determine the window of vulnerability and the timing vulnerability factor of master and slave latches. The first goal is to verify how much the variation of some parameters impact the WOV and TVF of FFMS listed below at nominal conditions:

1. Standard Master-Slave D Flip-Flop (SMSFF)
2. Transmission-Gate Master-Slave D Flip-Flop (TGMSFF)
3. Write-Port Master-Slave D Flip-Flop (WPMSFF)

The parameters analyzed in this work determines the dependence between TVF with operational frequency, with the fault propagation to the next stage through a combinational logic with different propagation delays and with different nanometer technological models, also considering High Performance (HP) and Low Power (LP) versions. All the simulations were made using the HSPICE electrical simulator.

The variability can manifest itself causing an increase or a decrease to the initial specification (SAHA, 2010). The main problem is the uncertainty about the value stored in sequential elements. For example, there are circuits that present operational frequency oscillations due to variability effects. In this way, the second goal is to evaluate the TVF of MSFF topologies against environmental variability effects with supply voltage and temperature variations.

The proposed study is important to demonstrate how to analyze the WOV and TVF of MSFFs, as well as to show the real impact of the choice of technology and operating frequency in designs under radiation. The dependency to TVF between diverse path delays and environmental variability also is crucial to determine the design vulnerability.

1.3 Work Organization

This dissertation is divided as follows. Chapters 2 and 3 introduce the theoretical foundation for full comprehension of this work. The methodology utilized to validate the contributions of this work can be seen in chapter 4. Finally, results are shown in chapters 5 and 6 with a methodological sequence to highlight the main results. A brief description of each chapter is presented below:

Chapter 2: Radiation Effects in Integrated Circuits - This chapter shows the main sources of radiation, the explanation of charge collection mechanism, case-studies of Single Event Effects, how transient faults are modeled electrically as well as the challenges faced in nanometer technologies.

Chapter 3: Sequential Logic Circuits - This chapter presents the basic concepts related with sequential circuits, including timing analysis and clock issues for MS D flip-flops. Furthermore, this chapter also explores how the WOV and TVF are measured, and how the propagation delay and clock frequency can contribute to reduce them.

Chapter 4: Methodology - This chapter describes the characteristics of three topologies of MS D flip-flops studied in this work and the pipeline design utilized in this research. Moreover, information about the nanometer technological models, operational frequencies, path delays and environmental variability utilized to obtain the experiment results also are present in this chapter.

Chapter 5: Experimental Results at Nominal Conditions - This chapter contains the TVF results for the three topologies FFMS considering different operational frequency, path delays and technologies models with nominal values corresponding to each examined technology.

Chapter 6: Experimental Results under Environmental Variability - This chapter also contain the TVF results and it is very similar to chapter 5. The difference is that the analysis is made under environmental variability, with supply voltage and temperature variations.

Chapter 7: Conclusions - This chapter has a set of conclusions that validate and reinforce the importance of contributions presented in this work. Potential future works and the main publications in conferences and journals during the master course also are presented.

2 RADIATION EFFECTS IN INTEGRATED CIRCUITS

Radiation consists in electromagnetic activity or particle incidence with high energy, which in contact with a particular material produces effects on it. Radiation effects can be very simple as low magnitude pulses or they can generate large magnitude pulses able to change the data in sequential or combinational logic elements. The Earth's atmosphere acts like a radioactive filter and it decreases the radiation intensity that impacts the Earth (BOUDENOT, 2007). However, the radiation incident continues to affect integrated systems even operating at sea level.

Reported problems due to particle strikes in commercial systems are unusual because the major companies do not like to reveal problems in their chips. Some reports that radiation could affect electronic devices are shown in Table I. May and Woods described in their landmark paper about the first evidence of soft errors from alpha particles in chip packaging modules (MAY et. al, 1979). Ziegler and Lanford predicted the occurrence of soft errors due to cosmic rays radiation at sea level (ZIEGLER et. al, 1979). Then, the first real evidence of soft errors from cosmic rays in semiconductors came in 1984, but it was not released by IBM Corporation.

Table 2.1: Main evidences of soft errors in commercial systems

Year	*Company/University*	*Reports*
1962	NASA/AT&T	Electrons in Van Allen belt cause degradation in some Telstar Satellite components.
1978	Intel Corporation	Chip packing modules got contaminated due to the impact of alpha particles.
1984	IBM Corporation	Soft errors in the systems due to cosmic radiation.
1987	IBM Corporation	Chip manufacturing process got contaminated due to the impact of alpha particles.
2000	Sun Microsystems	Error protection scheme implemented for Ultra SPARCII servers was insufficient to handle soft errors.
2004	Cypress Semiconductor	Single soft error crashed an interleaved system farm.
2005	Los Alamos National Laboratory	2048-CPU server system frequently crashed because of cosmic ray.
2008	AIRBUS	The aircraft made two abrupt descents due to the soft error that caused fault onboard computer system.

Source: Adapted from (MUKHERJEE, 2008)

2.1 Main Sources of Radiation-Induced Faults

There are different sources to induce transient faults in semiconductor devices. In general, the most common sources are process variability, thermal cycling, erratic fluctuations of minimum voltage and radiation external to the chip (MUKHERJEE, 2008). Various particles generated by sun activity contribute to radiation effects. They can be divided between energetic particles such as electrons, protons and heavy ions, and electromagnetic radiation, which can be X-ray, gamma ray or ultraviolet light (BARTH, 1997). The energetic particles that induce soft errors in silicon chips due to ionization of atomic electrons are known as alpha particles or neutrons.

Alpha particles are emitted from solder bumps or interactions with radioactive impurities such as uranium, thorium or radium present in the packaging materials through alpha decay process (MUKHERJEE, 2008). The structure of these particles consists of two protons and two neutrons bound together into a particle identical to a helium nucleus. Alpha particles lose its kinetic energy through interactions with the electrons when penetrates into the material, and thus leaves an ionization trail (BAUMANN, 2005). There are some materials that aim to minimize the emission of these particles, but these materials are very expensive. Furthermore, it is very difficult to eliminate them completely (DUPONT et. al, 2002).

Neutrons are the most frequent cause of upset at ground level and they are related to cosmic ray events (NORMAND, 2001). Soft errors caused by neutrons arise from interactions between cosmic ions and oxygen/nitrogen in the upper atmosphere (KASTENSMIDT, 2007). When atoms break apart, protons persist for long durations before decaying and it forms the majority of primary cosmic rays in earth's outer atmosphere. When primary cosmic rays collide with atmospheric atoms it is produced complex cascades of secondary particles, which constitutes the secondary cosmic rays. Primary and secondary cosmic rays are known as high-energy cosmic rays. If low-energy cosmic rays interact with the boron existing in some p-type dopants in semiconductor chips, other particles can be created (BAUMANN et. al, 2000).

Primary cosmic rays are composed of galactic and solar particles. Galactic particles arise from stellar flares, supernova explosions or other cosmic activity whereas solar particles arise from the sun. Galactic particles have more probability of reaching the sea level because its energy to penetrate the earth is bigger. Secondary cosmic rays are composed of secondary particles as pions, muons, protons and neutrons that if collided with other atmospheric atoms can create a new shower of particles. The neutron flux is strongly dependent on altitude, longitude and latitude. At terrestrial altitudes, less than 1% of primary cosmic rays reach the sea level (ZIEGLER et. al, 1981).

It is important to highlight that the kinetic energy of alpha particles is lower than typical neutrons that affect CMOS technology, but alpha particles generate more problems when they hit transistors. This happens because the impact of alpha particles immediately generates a track of electron-hole pairs in the substrate that deposits a significant amount of charge at a node while neutrons do not create it directly.

2.2 Charge Collection Mechanism

The charge generated by the impact of particles varies depending on the ion type, incident angle and impact site. The way as energetic particles interacts with silicon is different when the impact is due to neutrons or alpha particles. Alpha particles interact directly with electrons present on the substrate while neutrons interact through inelastic or elastic collisions. Experimental results show that inelastic collisions are the main cause of soft error due to neutrons, because they create secondary particles (SRINIVASAN, 1996).

The collision of energetic particles causes a strong field perturbation and it creates a track of electron-hole pairs with a high carrier concentration that deposits energy in the material (MESSENGER, 1982). This track contains equal number of electrons and holes. If ionization track transverses the depletion region, the electric field collects the carries generating a transient current pulse at the node, which can be negative or positive. Fig. 2.1 illustrates the moment that a particle strikes a node in a semiconductor device and it generates a pulse. The pulse can be positive or negative according to the transistor. NMOS transistors may present negative pulses, in other words, a discharge in the node, while PMOS transistors may present positive pulses or a charge in the node.

The disturbance caused for the impact depends on energy lost per unit track length known as linear energy transfer (LET). For every 3.6eV (electron volts) of energy loss by the particle, one electron-hole pair is created in the silicon substrate. The LET depends on the mass/energy of the particle and the material in which it is traveling. The highest LET values are obtained when more massive and energetic particles impact denser materials (BAUMANN, 2005). In this way, the width of the transient voltage pulse is dependent on the energy of the particle, the charge stored at a node and the charge collection of the affected junction. The duration and amplitude of transient voltage pulse depend on electrical characteristics of the struck node like resistance and capacitance. In nanometer technologies, the duration of transient voltage is around few hundreds of pico seconds to few nano seconds (LISBOA et. al, 2007).

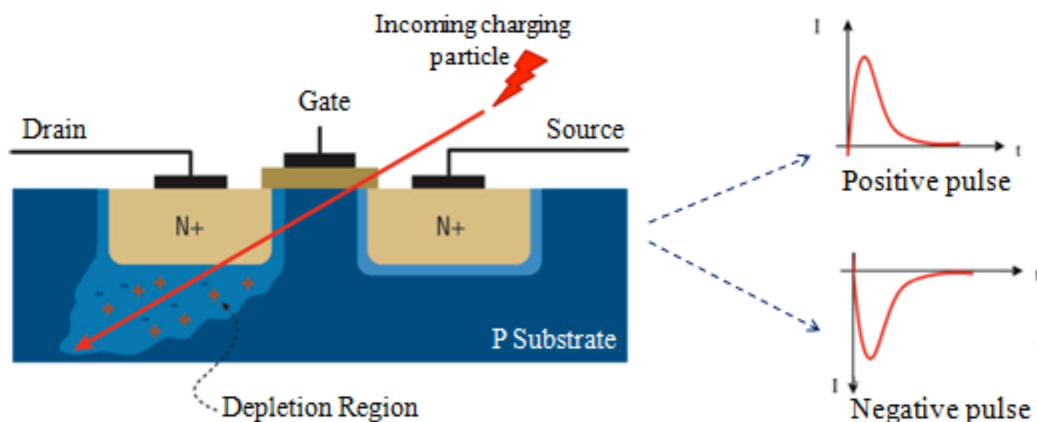


Figure 2.1: Silicon substrate ionization due to impact of energetic particles and the pulse generated by this effect. Adapted from (SAWANT, 2012)

The impact of neutrons occurs similarly to alpha particles one. The difference is that the impact of neutrons in the silicon substrate does not directly create electron-hole pairs. Instead, neutrons collide with the nuclei in the semiconductor resulting in the emission of energetic secondary particles. These new particles cause ionization tracks and they generate electron-hole pairs enough to cause a transient current pulse. The probability to create secondary particles is slight. A number of neutrons greater than a number of alpha particles are necessary to produce a transient fault with the same impact on a semiconductor device. (MUKHERJEE, 2008).

In bulk CMOS technologies, any PN-junction of the PMOS or NMOS transistors is considered a sensitive region (BAUMANN, 2005). Depending on the charge that is collected, a short occurs for a little time period in the impacted PN-junction, producing a transient pulse. There are cases that the pulses have a low magnitude and the initial value of the node is not modified. However, if the pulse exceeds the critical charge (Qcrit) and it turns on the gate of the opposite transistor, it will cause a circuit malfunction.

The nodes are more sensitive to upsets due the voltage supply (V_{DD}) and nodal capacitance (C_{node}) reductions to improve performance and power consumption at new technologies. These reductions are directly related to the charges stored at circuit nodes (Q_{node}), as shows Eq. 1.1. In this way, the stored charge in each node also becomes smaller and it affects the critical charge, reducing the quantity of charge required to corrupt the stored information at circuit nodes (JAHINUZZAMAN et. al, 2009). Consequently, soft errors susceptibility increases due to advanced technology.

$$Q_{node} = C_{node} * V_{DD} \quad (1.1)$$

Fig. 2.2 shows the charge collection mechanism in a drain terminal of PMOS transistor of an inverter gate. The current flows through the struck PN-junction of PMOS transistor and the expected value of the output of inverter gate is ‘0’. The transistor in on-state also conducts a current trying to balance the current generated by particle strike. If the collected charge is low and the transistor in on-state balances the current before the node capacitance is charged, the fault is not seen. On the other hand, if the collected charge is high enough and it exceeds the critical charge, a voltage change at the node occurs. This behavior happens similarly for the NMOS transistor. Depending on the transistor in on-state, the collected charge is eliminated through VDD or GND, making the node to return to its correct state (WANG et. al, 2008).

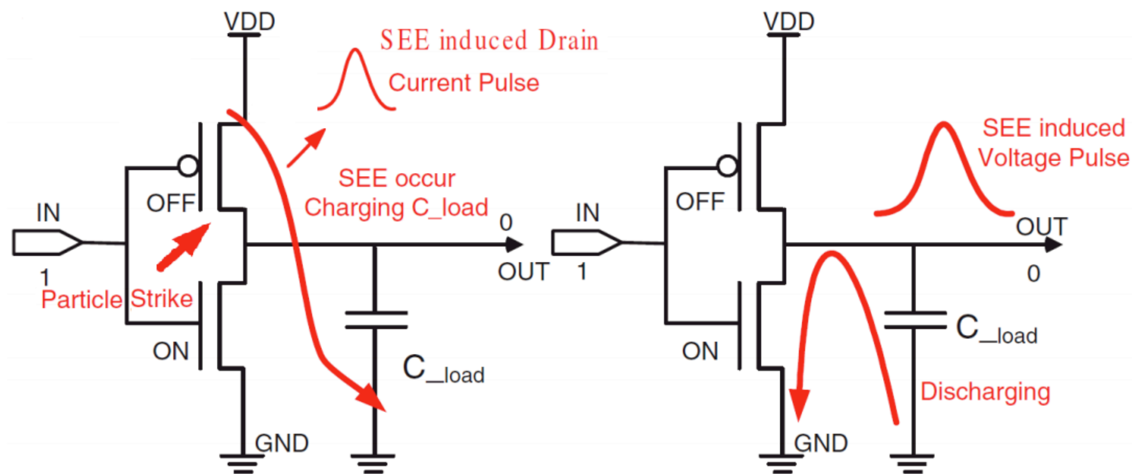


Figure 2.2: Charge collection mechanism when a soft error occurs at PN-junction (WANG et. al, 2008)

2.3 Single Event Effects

Faults caused by a single energetic particle, which can take on many forms, are called Single Event Effects (SEE) (O'BRYAN, 2000). With technology scaling, the device dimensions are suffering reductions, and the circuit speed is increasing. These factors have collaborated with the increase of SEE occurrence in the ICs (DODD et. al, 2004). The charge deposited by a single ionizing particle can produce a wide range of effects like Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latchup (SEL) and Single Event Burnout (SEB). Fig. 2.3 shows a simple diagram to represent the sequence of events from incident particle until an SEE, as well as the classification of SEE divided into soft errors and hard errors. In some cases, SEB and SEL are also classified as hard error.

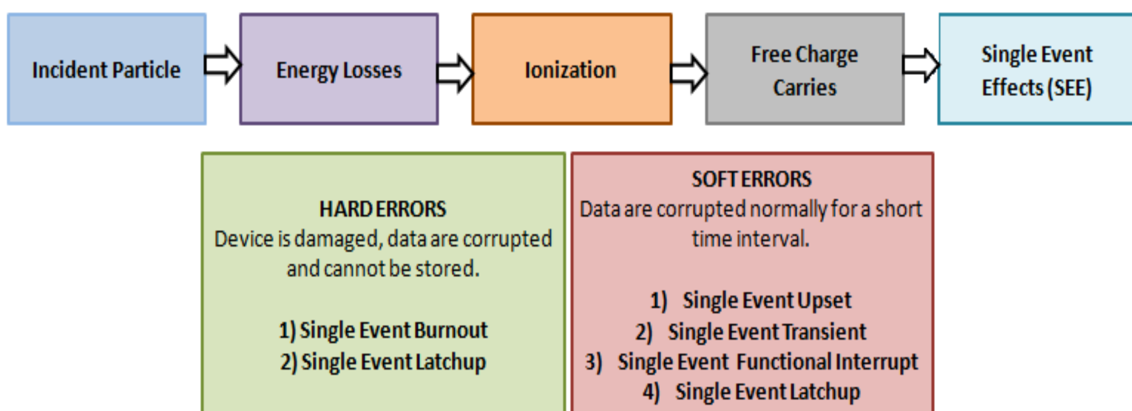


Figure 2.3: Classification of Single Event Effects in ICs

When a single energetic particle interacts with silicon, the upset can reach the combinational logic or the sequential logic as shown in Fig. 2.4. (CRAIN et. al, 2001; ALEXANDRESCU et. al, 2002). The data from the first sequential cell is released to the combinational logic only when a clock edge occurs and at this moment, the logic operations are performed. The results of combinational logic normally reach the next sequential sometime before the next clock edge. At this clock edge, whatever is the data in the input of the second sequential, which is in agreement with the setup and hold times, it will be stored in a sequential circuit.

If a charged particle strikes a memory element, such as a latch or flip-flop, it may invert the stored original value, producing a Single Event Upset or in other words, a bit-flip (BAUMANN, 2002). When a charged particle hits the combinational logic block, it also generates a transient current pulse. This circumstance is known as Single Event Transient (LEAVY et. al, 1991). If the fault propagates up to an input of the next sequential and if this data comply with timing constraints, an incorrect value will be stored. Moreover, an SET will become an SEU in the circuit.

Figure 2.4: Upsets possibilities: combinational or sequential logic circuits. Adapted from (KASTENSMIDT et. al, 2006)

Fig. 2.5 exemplifies the most common single event effects that happen on the circuits. First, the SET occurs in a sensitive node in a NOR gate and it generates a pulse in the combinational logic (a). This pulse was propagated and it reached the sequential logic to the right, which stored the incorrect value '0'. Memory cells have two stable states, one that represents a stored value '0' and one that represents a stored value '1'. In each state, there are two transistors in on-state and two transistors in off-state. In the second case (b), an energetic particle hits in the sequential logic in one of the two sensitive nodes. So, an SEU occurs (reverse the transistor state) and it affects the rest of the circuit because the incorrect value also is stored in the sequential logic to the right.

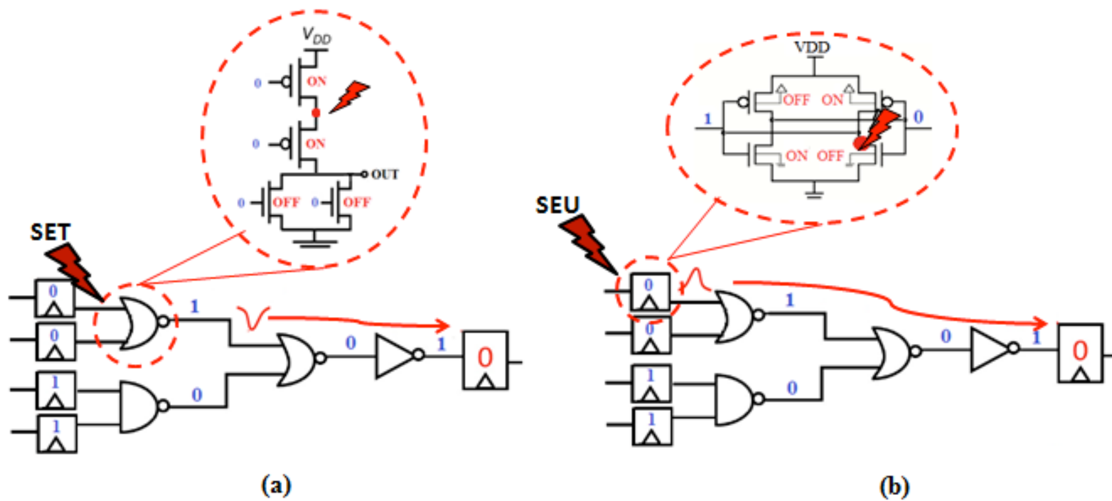


Figure 2.5: (a) Single Event Transient and (b) Single Event Upset on a circuit

There are some cases where a transient pulse will be masked, and it will not be captured by the sequential elements. In this case, the fault will not lead to errors or failures visible to the user. Moreover, the circuit keeps a correct value in the output because the faults are masked still in origin. There are three kinds of masking commonly observed in logic blocks: logical masking, electrical masking and latch window masking (LIDEN et. al, 1994; SHIVAKUMAR, 2002).

The logical masking happens when a particle strike affects a portion of the circuit. However, the hit node is not relevant to determine the final output. In this way, the output can be determined only by inputs not affected by a particle. For example, the first input of NAND gate in Fig. 2.6 is '0', and then, the second input is not important because the final result will always be '1'. So, if a particle impacts one of inputs, the error will not be seen in the last output. According to truth table, the same happens with a NOR gate, if one input is equal to '1', the final result will always be '0'.

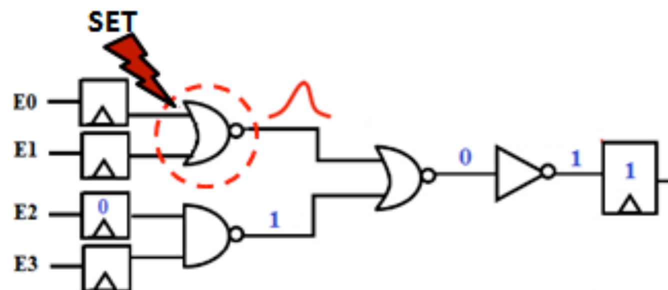


Figure 2.6: Logical masking in a combinational circuit

The electrical masking happens when the fault impacts the circuit node, but the current pulse generated is attenuated through the combinational logic and it disappears before being stored by a forward latch. For example, in Fig. 2.7, NOR gate has an SET in the first input, but the effect that it causes is mitigated when is propagated until the output of an inverter. The fault reaches the forward latch, but the pulse has a small

amplitude that is interpreted as a logical value. So, the latch will store the correct value, which in this case, is equal to '0'.

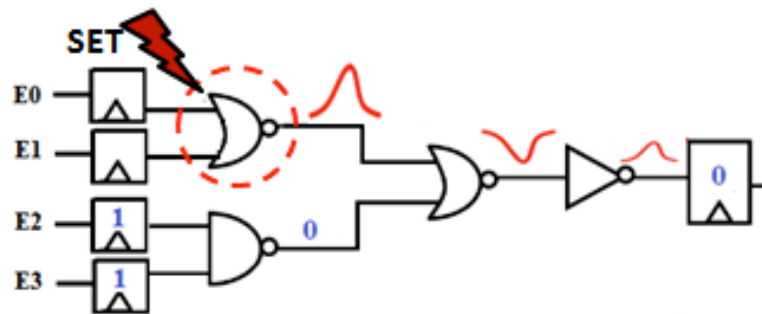


Figure 2.7: Electrical masking in a combinational circuit

When a transient pulse cannot be masked logically or electrically, it propagates until it reaches a sequential circuit. Latch-window masking happens when the pulse is not captured by a latching window of a sequential logic. In Fig. 2.8, if the pulse at the NOR gate was not masked by one of the methods that were already been presented, the memory element can mask it according to the latch-window. On the right of Fig. 2.8, it is shown a clock cycle with its latching window. If the SET is captured when a clock transition happened, a wrong value will be stored. Finally, the rate that SETs get latched as errors depends on the clock frequency and the topology of sequential circuits.

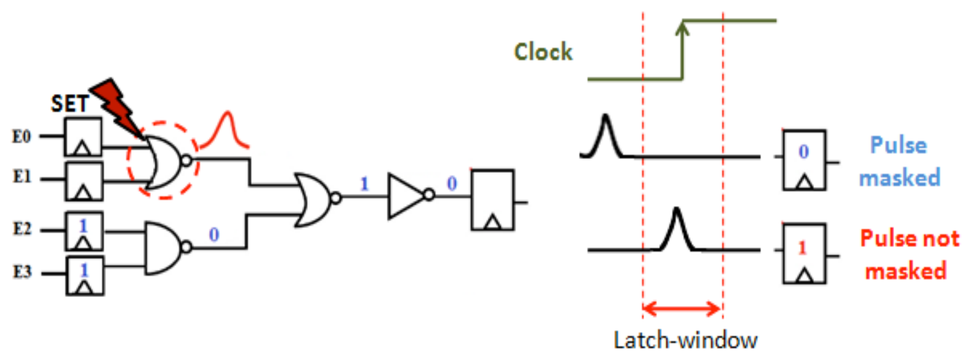


Figure 2.8: Latch-window masking in a combinational circuit

2.4 Transient Pulse Modeling

Depending on fabrication process and the sensitive nodes, different shapes of transient currents can be observed (DODD, 2005; FERLET-CAVROIS, 2006). After the silicon particle ionization, the charge collection proceeds through two mechanisms: drift and diffusion. When the resultant ionization track traverses the depletion region, carriers are rapidly collected by the high electric field. This charge collection is known as drift. The crossing of particles through the depletion region is responsible for temporary deformation in a funnel shape. This effect is called funneling and it causes an increase in the collected charge efficiency due to the increase of the depletion region area (BAUMANN, 2005). Finally, diffusion process collects all the other carries generated

besides the depletion layer. The typical current waveform resulting from the additional collect charge induced by particle incidence can be seen in Fig. 2.9.

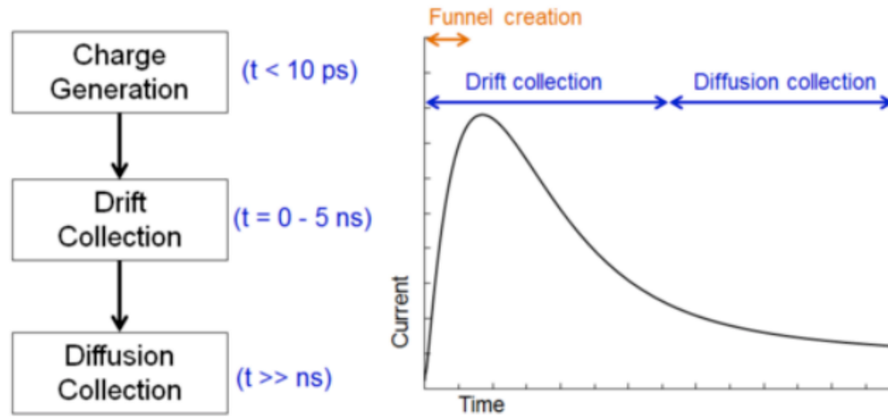


Figure 2.9: Typical current waveform of one single event (CUMMINGS, 2010)

Charge deposition mechanism is widely used and it is modeled by a double exponential current pulse, which is given by Eq. 2.1, Eq. 2.2 and Eq. 2.3 (MESSENGER, 1982). These equations are based on the current node algorithm, which aims to convert the circuit described in a matrix and solving a linear equation that is generated from Kirchhoff's current law (HO et al., 1975).

$$I_P(t) = I_0 \left(e^{-t/\tau\alpha} - e^{-t/\tau\beta}\right) \tag{2.1}$$

$$I_0 = Q_{coll}/(\tau\alpha - \tau\beta) \tag{2.2}$$

$$Q_{coll} = 10.8 * L * LET \tag{2.3}$$

The terms of equations above represent:

I_0 = the maximum charge collection current;

Q_{coll} = the collected charge;

$\tau\alpha$ = the collection time constant of the junction;

$\tau\beta$ = the time constant for initially establishing the ion track;

L = the charge collection depth;

In bulk silicon, a typical charge collection depth for a heavy ion is approximately 2µm. For every 1MeV.cm²/mg, an ionizing particle deposits about 10.8fC of electron-hole pairs along each micron of its track (MAVIS et. al, 2002).

3 SEQUENTIAL LOGIC CIRCUITS

Logic circuits for digital systems can be of two types: combinational circuits and sequential circuits. A combinational circuit is composed by a set of logic gates, which determine the output values directly from the current input values. On the other hand, sequential circuits depend on the current input values, and they also depend on preceding input value (RABAEY et. al, 2003). Sequential circuits act as memories, remembering data storage in the system. In addition to logic gates, the main elements used in sequential circuits are latches and flip-flops to store one bit of information. Fig. 3.1 shows the symbol and the timing diagram of two main elements of sequential circuits.

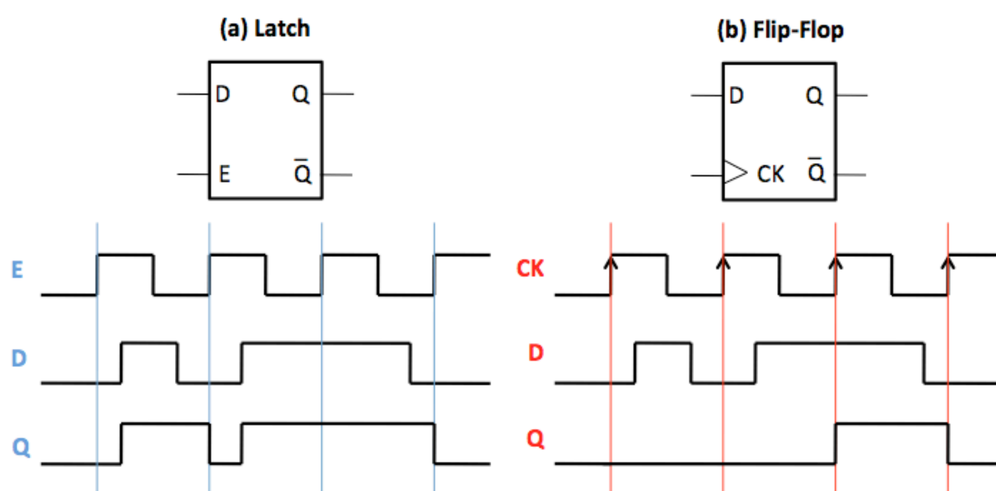


Figure 3.1: Symbol and timing diagram for a positive (a) latch and (b) flip-flop

A latch is a level-sensitive circuit with two main operating modes: transparent mode and hold mode. Latches are in transparent mode, if they are enabled to receive data such that the D input passes its value to the Q output during all phases. Latches are in hold mode, if they are not enabled to receive data such that the last value stored in Q output is maintained until the next level change occur. Moreover, latches can be classified as positive or negative depending on the phase of clock period that they are in transparent mode. For example, a positive latch passes the D input values to the Q output when the clock signal is high as shown in the timing diagram of Fig. 3.1 (a). A latch is essential in the construction of an edge-triggered flip-flop.

Flip-Flops are edge-triggered circuits that also have the transparent and hold modes. Contrary to latches, flip-flops only copy the D input value to Q output on a clock transition remaining with this value until other clock transition occurs. Flip-flops can be also classified as positive or negative, it depends if the circuit captures the data on a positive or a negative edge-triggered. For example, a positive flip-flop passes the D input value to the Q output when a 0 → 1 clock transition occurs as shown the timing diagram in Fig. 3.1 (b). The inputs must be stable for a short period around the clock edge to meet setup and hold requirements.

In real circuits, the flip-flops are designed as a master-slave structure composed of positive and negative latches in cascade controlled by complementary clock signals. Fig. 3.2 shows the structure of master-slave D flip-flop sensible to rising edge. The operation is very simple: when the clock signal is low, the master latch is in transparent mode and the slave latch is storing the previous value. If a positive clock transition happens, the master latch only stores the value between two latches while the slave latch in transparent mode puts the D input values on the Q output.

According to the timing diagram in Fig. 3.2, the master latch is negative and all data in the D input will be transfered to Q_M when the clock is low. Similarly, all data present in Q_M input will be transfered to Q_S when the clock is high because the slave latch is positive. In the figure below, it is assumed that Q_S and Q outputs are equal as well as Q_M is equal to D_2 too. To create a master-slave D flip-flop sensible to falling edge it is only necessary to reverse the clock signal that feeds the two latches. These flip-flops form the basic elements of shift registers, which are an essential part of several electronic devices.

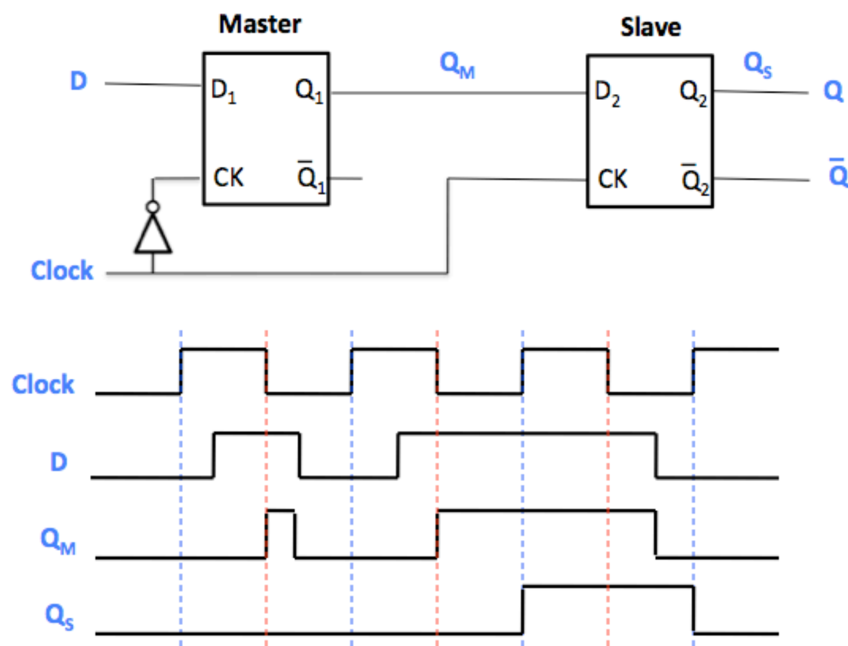


Figure 3.2: Structure and timing diagram of master-slave D flip-flop

3.1 Timing analysis and clock issues

Due to parasitic elements, like channel resistance and gate capacitance, when an input changes, the output is not going to change instantaneously (NUNES, 2014). The time that the output takes to answer a stimulus in the input is defined as propagation delay (Tp/Tprop). To compare combinational logic circuits regarding performance, it is important to know the propagation times called high-low delay (Tp_{HL}) and low-high delay (Tp_{LH}). The propagation times are measured by convention from the 50% of the signal, assuming that the switching threshold is located in the middle of the waveform, as shows Fig. 3.3 on the left. So, the propagation delay of circuits is given by the average of propagation times.

Furthermore, propagation delays have relation to slopes of the input and output signals. Transition delays are introduced to quantify these slopes and they express how fast a signal transits between the different levels (RABAEY et. al, 2003). The time required for a signal transition from 0 to 1 or from 1 to 0 are defined as the rise (Trise) and fall times (Tfall), respectively. These times are measured between 10% and 90% of the output waveform, as shows Fig. 3.3 on the right. In summary, these times indicate the amount of time needed to reflect a stable value at output until another input change occurs.

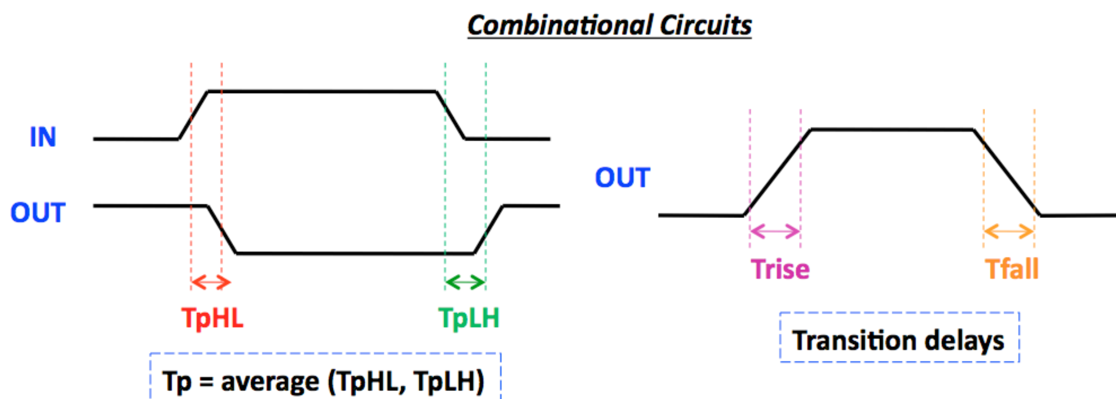


Figure 3.3: Propagation and transition delays for combinational logic circuits

Propagation delay in flip-flops is commonly measured as the time that the data in D input takes to appear in the Q output from the moment that clock edge trigger happens (Tclk-Q), as shows the Fig. 3.4 on the left. In the case of latches, timing characteristics are measured in relation to the D input and Q output ($T_{D\text{-}Q}$). By convention, the propagation delay of a sequential circuit is also measured from the 50% of the signal assuming that the switching threshold is located exactly in the middle of the waveform.

There are two important timing constraints that if they are violated for any flip-flop in the circuit, the circuit cannot operate correctly. These restrictions are shown in Fig. 3.4 on the right. Setup time (Tsetup) indicates the time that the data input must be stable before the clock transition trigger. The hold time (Thold) is the amount of time that the data input must be valid after the clock transition trigger. All circuits must be designed respecting the restricted region. The data signal needs to arrive at least before the clock

edge of the setup time and it remains without changes until at least till the hold time after the clock edge.

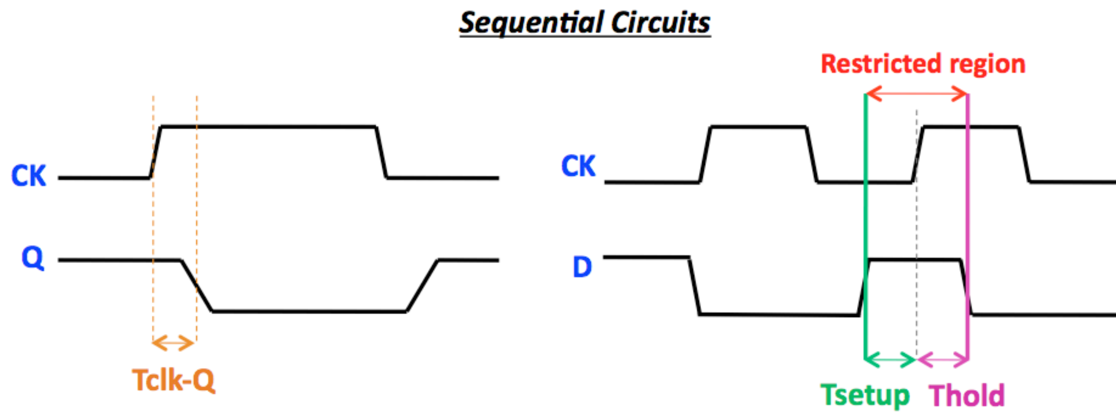


Figure 3.4: Propagation delay, hold and setup times for sequential logic circuits

In the literature, it is normally assumed that the clock signal is a perfect one. However, this is not a safe assumption because in real applications, the clock signal suffers some changes. There are two main factors known as clock skew and clock jitter that can cause harm to a clock signal. Cells in a core are placed in different regions and the clock signal is distributed from a single source to all sequential elements of the circuit. The clock skew is defined as the difference in the arrival time of clock signal to any two flip-flops fed by the source. On the other hand, the clock jitter is defined as the undesired variation of a signal in relation to the ideal position in time. Both effects can be seen with more details in Fig. 3.5.

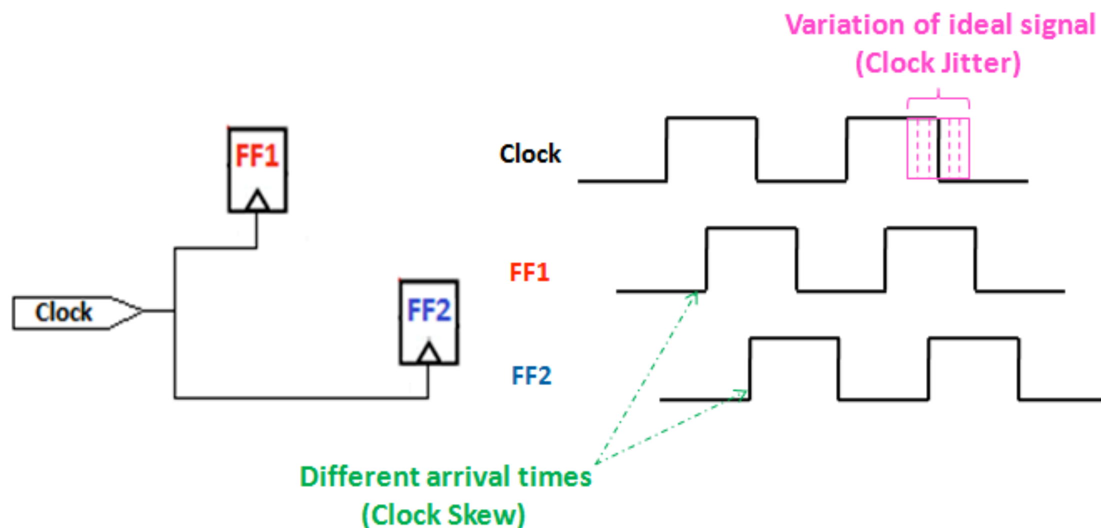


Figure 3.5: Clock skew and clock jitter causes harm to a clock signal

Timing analysis and clock issues presented above are directly related to the clock frequency of sequential circuits. In a typical circuit, pipeline designs are composed of

two flip-flops and a combinational logic between them, as shown Fig. 3.6. Each one these structures has a data arrival time and a data required time. Eq. 3.1 gives the data arrival time, where Tclk-Q is the propagation delay of the first flip-flop, Tp is the propagation delay of combinational logic and Tsetup is the setup time of the second flip-flop. It is crucial to minimize the data arrival time to obtain the maximum clock possible frequency. The data required time corresponds to a full clock period as shown by Eq. 3.2.

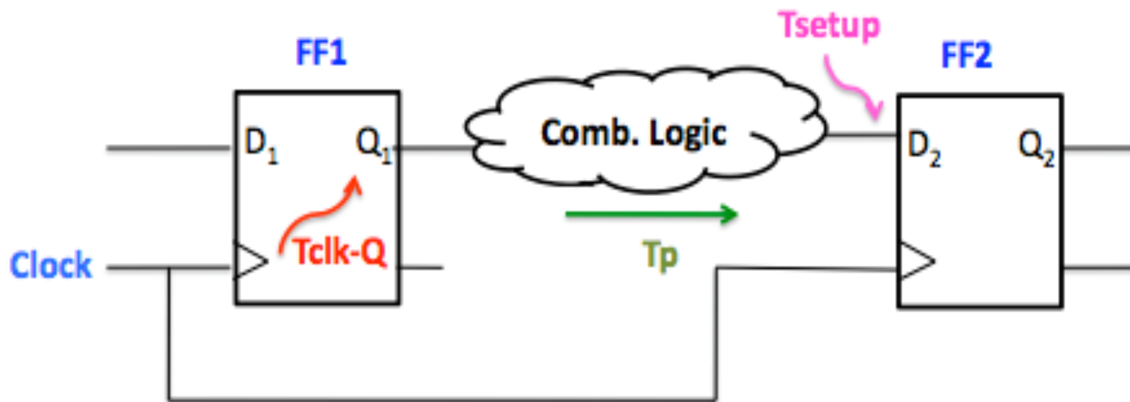


Figure 3.6: Pipeline design of typical circuits

$$\text{Data arrival time} = \text{Tclk-Q} + \text{Tp} + \text{Tsetup} \quad (3.1)$$

$$\text{Data required time} = \text{Tclock} \quad (3.2)$$

Static Timing Analysis (STA) tools consider the data arrival time to compare it to the clock period defined in the constraints file. This time must be smaller than the clock period defined previously to meet the timing enclosure. If the circuit does not operate exactly in the defined frequency, a slack is created. Slack is defined as the difference between the data arrival time and the data required time for a timing path, and it determines if the pipeline design is working at the specified frequency. Zero setup slack indicates that the pipeline design works exactly at the specified frequency, and there is no margin available in the circuit. However, it is possible that a pipeline design operates at frequencies lower than one pre-defined previously. In this case, this gap between the frequencies generates a positive setup slack that can be shown in Fig. 3.7. Negative slack implies that the pipeline design does not operate in the pre-defined frequency.

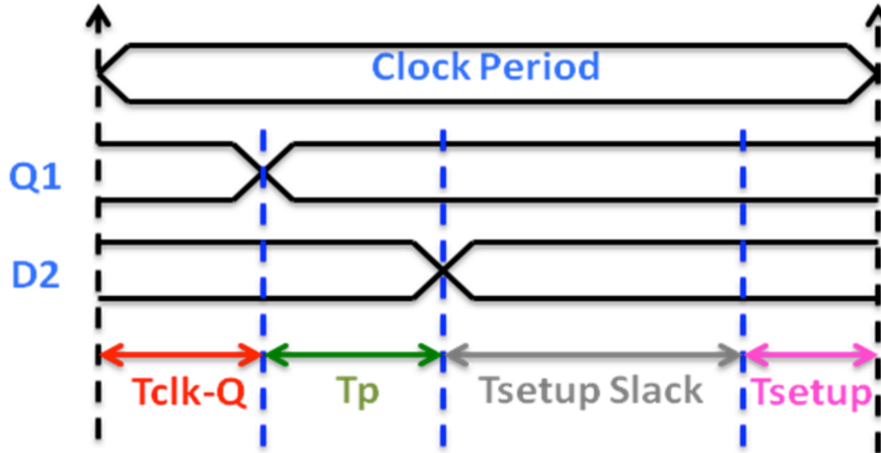


Figure 3.7: Timing diagram analysis for setup time slack

3.2 Soft Error Rate (SER)

Technology scaling also decreases the probability of electrical masking in combinational logic circuits. This happens because a high transistor density generates small combinational logic depth and it reduces the propagation delays between memory elements. In this way, the pulse cannot be attenuated enough by combinational logic and the quantity of SETs that can get latched as errors in sequential circuits becomes higher. Since the delay of circuits is smaller, the clock frequency is becoming larger, allowing that circuits to process more data in less time (DODD et. al, 2004). Currently, the curve of SEU in Fig. 3.8 does not represent a constant because the number of SEU also increases as well as the technology advanced. For this reason, it is important to study the behavior of sequential circuits under radiation since both single event effects (SET and SEU) contribute significantly to the Soft Error Rate. SER is the rate at which a device encounters soft errors during a system operation.

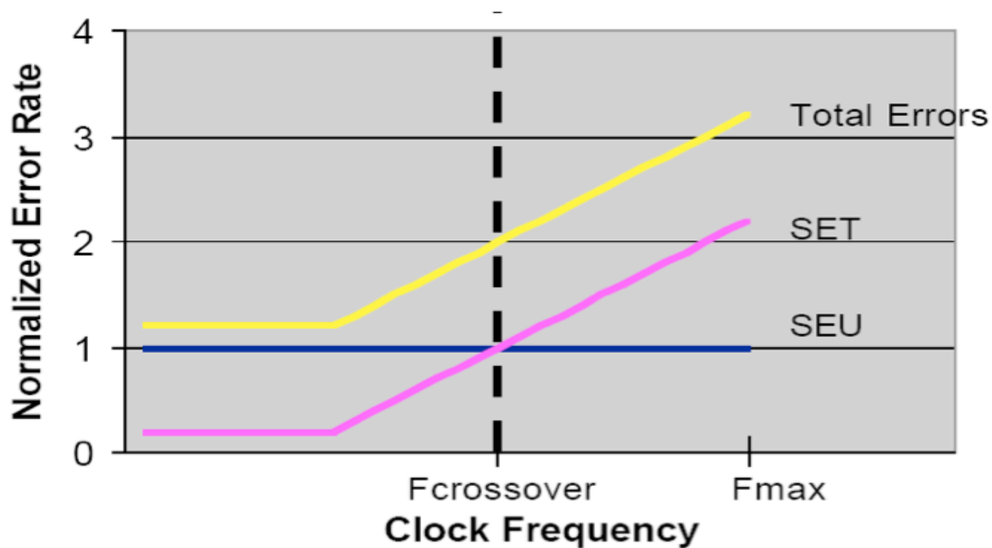


Figure 3.8: Soft Error Rate in last decades (DODD et. al, 2004)

The Soft Error Rate of a circuit can be estimated by Eq. 3.3 (NGUYEN et. al, 2003):

$$SER^{Circuit} = \sum_{i \text{ over all nodes}} (SER^{Nominal}_i * TVF_i * AVF_i) \quad (3.3)$$

where the nominal SER ($SER^{Nominal}_i$) refers to the underrated SER that is independent of the circuit environment. The impact that the circuit environment and the architecture have on SER are accounted by the Timing Vulnerability Factor (TVF_i) and by the Architecture Vulnerability Factor (AVF_i). AVF is the probability that a fault in a device *i* will be observed by the system or by the user. Since TVF and AVF are two independent concepts, this work is focused on the calculation of TVF under different operating conditions. The explanation of TVF is presented in subchapter 3.4. A complete methodology to compute the AVF can be seen in (MUKHERJEE et. al, 2003).

3.3 Window of Vulnerability (WOV)

The effective time window wherein the bit-flip in master or slave latch of the first MS D flip-flop can still be captured by the MS D flip-flop output of the next stage is defined as Window of Vulnerability (NGUYEN et. al, 2005). MS D Flip-Flops is not sensitive to soft errors during an entire clock period. Master and slave latches are vulnerable to bit-flips when they are in hold mode, and with this, it keeps the value of the previous state. It is important to emphasize that bit-flips that occur outside the WOV limits of sequential circuits do not propagate in time to be seen in the next stage of pipeline design. Moreover, it should not contribute to increase the SER.

Seifert and Tam (SEIFERT et. al, 2004) describe a method for computing WOV of sequential circuits. Their research also considers the impact of the circuit environment that sequential circuits are typically placed in. The circuits used to validate their experiments were MS Flip-Flops and flow-through latches inside a high-performance microprocessor. Fig. 3.9 shows the Window of Vulnerability of MS Flip-Flops according to (SEIFERT et. al, 2004). In this measure, the authors do not consider the setup time of master and slave latches to calculate the WOV.

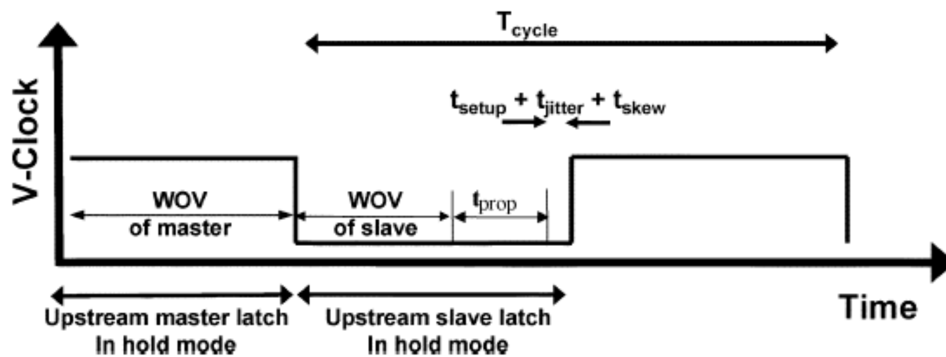


Figure 3.9: Window of Vulnerability according to (SEIFERT et. al, 2004)

In this work, simulations were made and they proved that master and slave latches are also sensitive to bit-flip during its setup time. For this reason, all analysis here respect the definition provided in (SEIFERT et. al, 2004), but it is taken into account the setup time to calculate the WOV for latches of MS D Flip-Flops. In a generic way, Fig. 3.10 shows the WOV that master and slave latches are vulnerable to bit-flips considering the setup time. Master latches are susceptible to bit-flips when the clock is high and the slave latches are susceptible to bit-flips when the clock is low. Both cases correspond to a time that latches are in a hold mode.

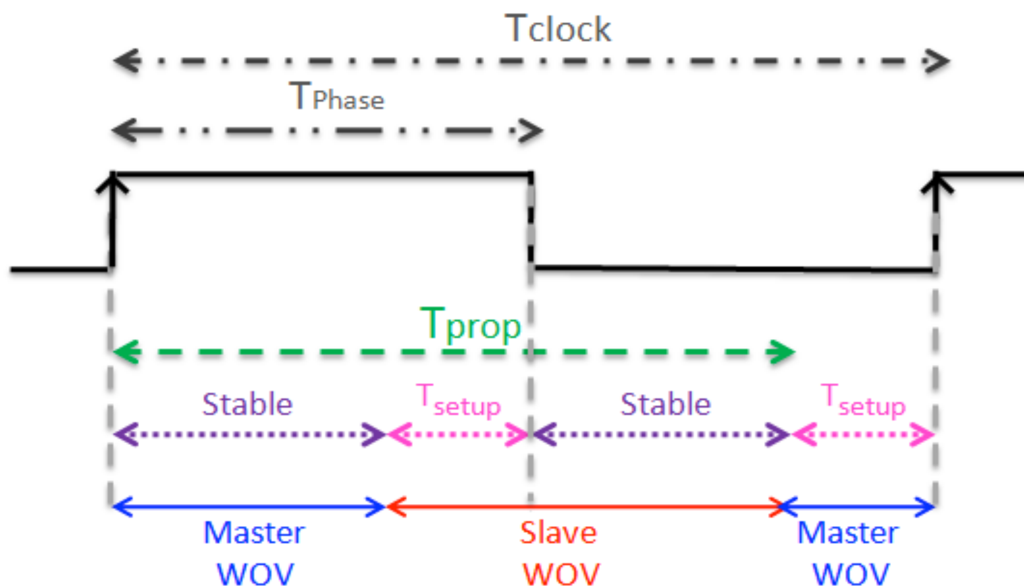


Figure 3.10: Window of Vulnerability for master and slave latches working on a rising edge MS flip-flop

The window of vulnerability strongly depends on the number of combinational gates in the logic path between two sequential elements. In a shifter register pipelines, typically there is no combinational logic between flip-flops. In this case, the propagation delay is zero considering negligible the delay of a wire, that is not the case in recent nanoCMOS tehnologies. The WOV of each latch is composed by the time that it is in hold mode in addition to its setup time as shown Fig. 3.10. This configuration represents the worst-case scenario such that the total WOV of MS D Flip-Flop is almost equal to entire clock period (Tclock).

There is always any combinational logic with different propagation delays in pipeline design with arithmetic operations. If there is a combinational logic between two MS D Flip-Flops, the propagation delay can contribute to reduce the WOV of master and slave latches. Propagation delays can represent a large or a small percentage of the clock period, and the bit-flip takes a greater amount of time to propagate until the next MS D flip-flop depending on combinational logic.

Fig. 3.11 illustrates some cases with different propagation delays at same clock period. If the propagation delay is equal to zero (a), the TVF of master and slave latches are approximately equaled. When the propagation delay is just a small percentage of a

clock period (b), the WOV of a slave latch is reduced and the WOV of a master latch is entirely preserved. For intermediate propagation delays (c), the WOV of slave latches can reach a value very close to zero. In some cases, the propagation delay represents a very large percentage of the clock period (d), which becomes the WOV of a slave equal to zero and the WOV of a master is reduced drastically.

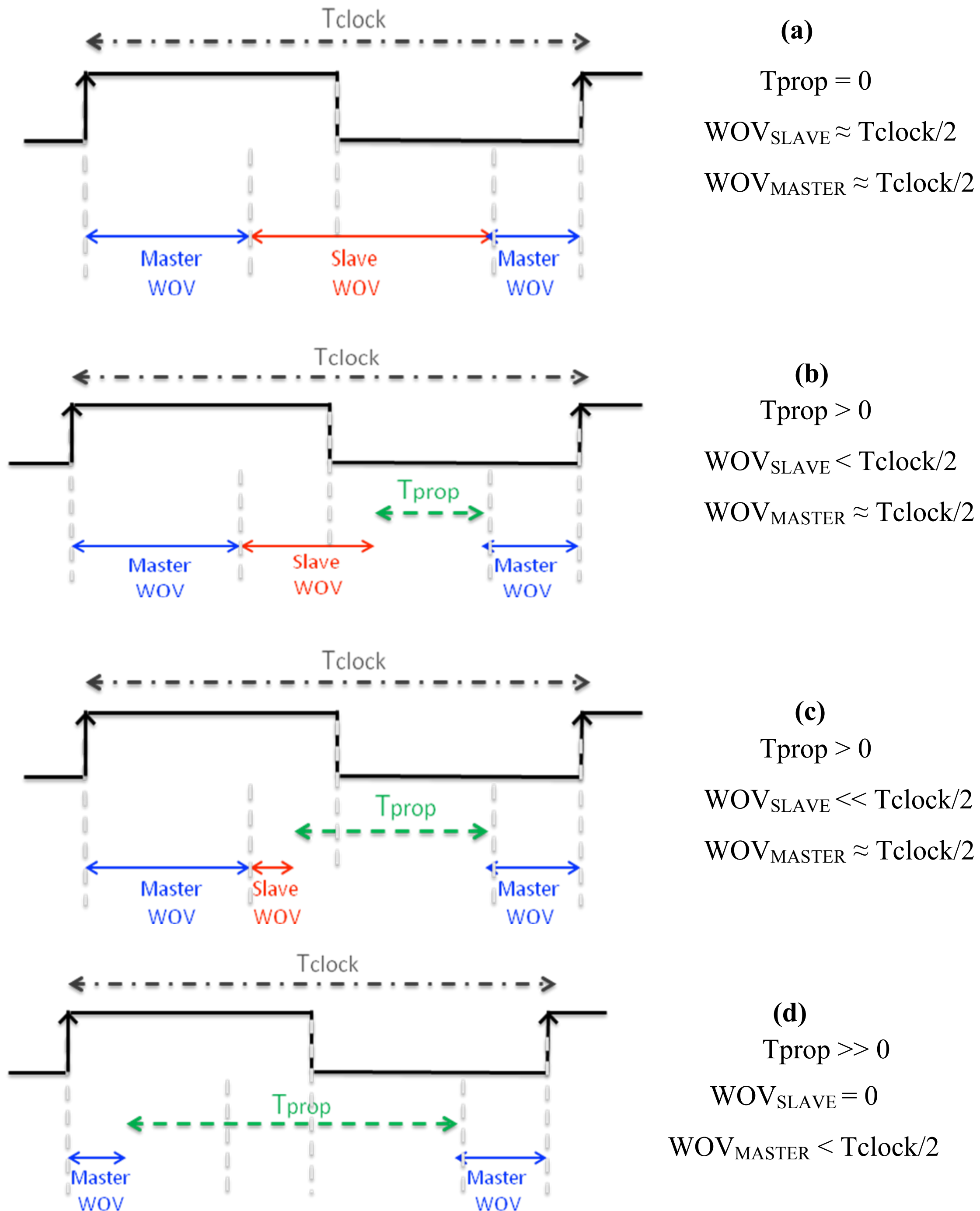


Figure 3.11: Effect of the WOV for different propagation delays (Tprop) at same clock period

3.4 Timing Vulnerability Factor (TVF)

Timing Vulnerability Factor corresponds to the time that a flip-flop or a latch is vulnerable to radiation-induced soft errors according to WOV and clock frequency (SEIFERT et. al, 2004). Eq. 3.4 describes an equation for computing the total TVF of MS D Flip-Flops according to Seifert and Tam:

$$TVF_{Sequential} \approx \frac{(Tcycle - (Tprop + Tsetup + Tlclk \pm Tskew))}{Tcycle} \quad (3.4)$$

where, Tprop is the sum of the propagation delay through the combinational logic and the intrinsic delay within the sequential, Tsetup denotes the setup time, Tclk corresponds to the clock rise and fall times, and also accounts of clock jitter. Finally, Tskew denotes the clock skew. In this equation, authors only consider the setup time of the MS D Flip-Flop and not consider the setup time of master and slave latches separately. For this reason, this work calculates the TVF for sequential elements utilizing the new measurement methodology, which respect the previous definition, but considers the setup time for two latches. Clock rise times, clock fall times, clock skew and clock jitter are considered negligible in this work. In cases of MS D Flip-Flops in a pipeline design, even master and slave can present different TVF values for the same propagation delay (Tprop > 0) (BRAMNIK et. al, 2013). With a logical combinational between MS D Flip-Flops, the TVF of master and slave latches can vary from ~0% to 50%.

A set of equations was created to determine the TVF of master and slave latches considering the propagation delay and the setup time. Eq. 3.5 and Eq. 3.6 shows as the TVF of master and slave latches are calculated when there are not combinational delays between MS D Flip-Flops. TVF of master and slave latches are always the same and very close to half of the clock period. Eq. 3.7 and Eq. 3.8 demonstrates the situation that the combinational logic delay is less or equal to the window of vulnerability of a slave latch. So, TVF of slave latch decreases while TVF of master latch remains unchanged. Eq. 3.9 and Eq. 3.10 also considers that the combinational logic delay is greater than the window of vulnerability of slave latch, so that it is equal to zero. Thereby, the TVF of a master latch is also reduced and it represents the better scenario to decrease the vulnerability to a bit-flip in the next stage of a pipeline design.

IF Tprop = 0

$$TVF_{SLAVE} \approx \frac{WOV_{SLAVE}}{Tclock} \quad (3.5)$$

$$TVF_{MASTER} \approx \frac{WOV_{MASTER}}{Tclock} \quad (3.6)$$

IF Tprop $\leq ((T_{clock}/2 - T_{setup_Master}) + T_{setup_Slave})$

$$TVF_{SLAVE} = \frac{((T_{clock}/2 - T_{setup_Master} - T_{prop}) + T_{setup_Slave})}{Tclock} \quad (3.7)$$

$$TVF_{MASTER} \approx \frac{WOV_{SLAVE}}{Tclock} \quad (3.8)$$

IF Tprop $> ((T_{clock}/2 - T_{setup_Master}) + T_{setup_Slave})$

$$TVF_{SLAVE} = 0 \quad (3.9)$$

$$TVF_{MASTER} \downarrow \quad (3.10)$$

The total TVF of MS D flip-flop has a strong dependency on its clock frequency too. Fig. 3.12 shows the effects on TVF when the clock period increases for the same propagation delay. Applications that work with lower frequencies and consequently a larger clock period, present higher TVF. This makes sense, since a large clock period presents a small contribution of the combinational logic to reduce the TVF. In this way, the WOV that a bit-flip in the first MS D Flip-Flop can be latched by the next stage decreases for higher frequencies.

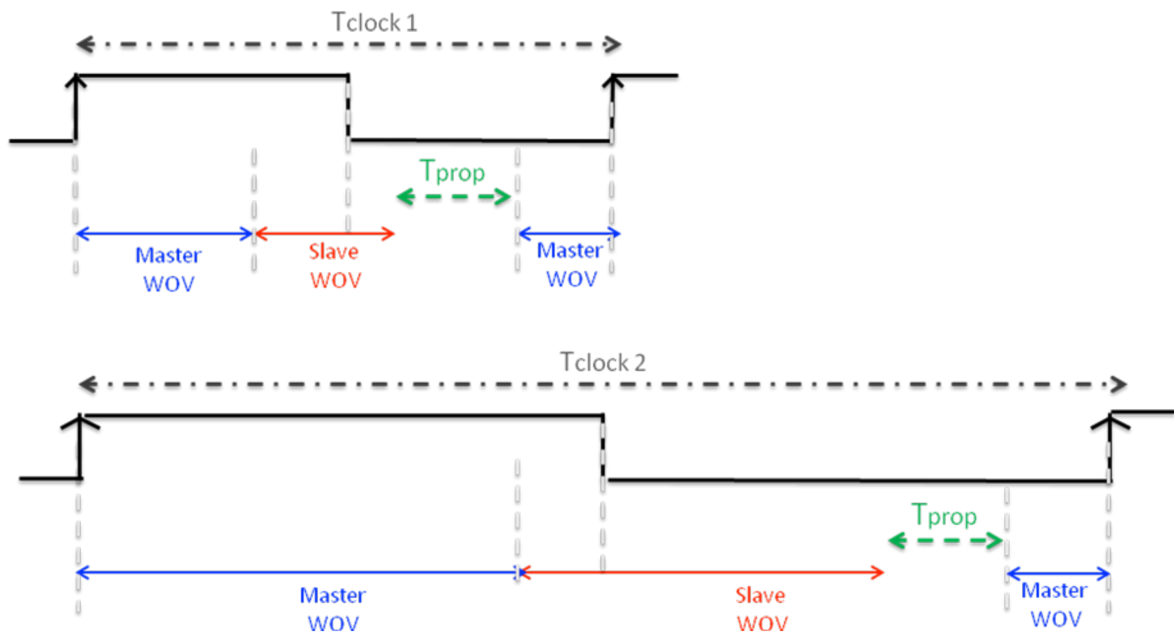


Figure 3.12: Effect of the TVF when clock frequency increases for the same propagation delay

Fig. 3.13 shows the insertion fault in master and slave latches considering a timing diagram without propagation delay between MS D Flip-Flops. In this case, the master and slave latches have its window of vulnerability entirely preserved. Wrong values due to the bit-flip are shown in red. Analyzing the last MS D Flip-Flop output, it is possible to notice that the fault effects are only seen in the next clock period. Moreover, the TVF values change according to propagation delay, technology model and clock frequency.

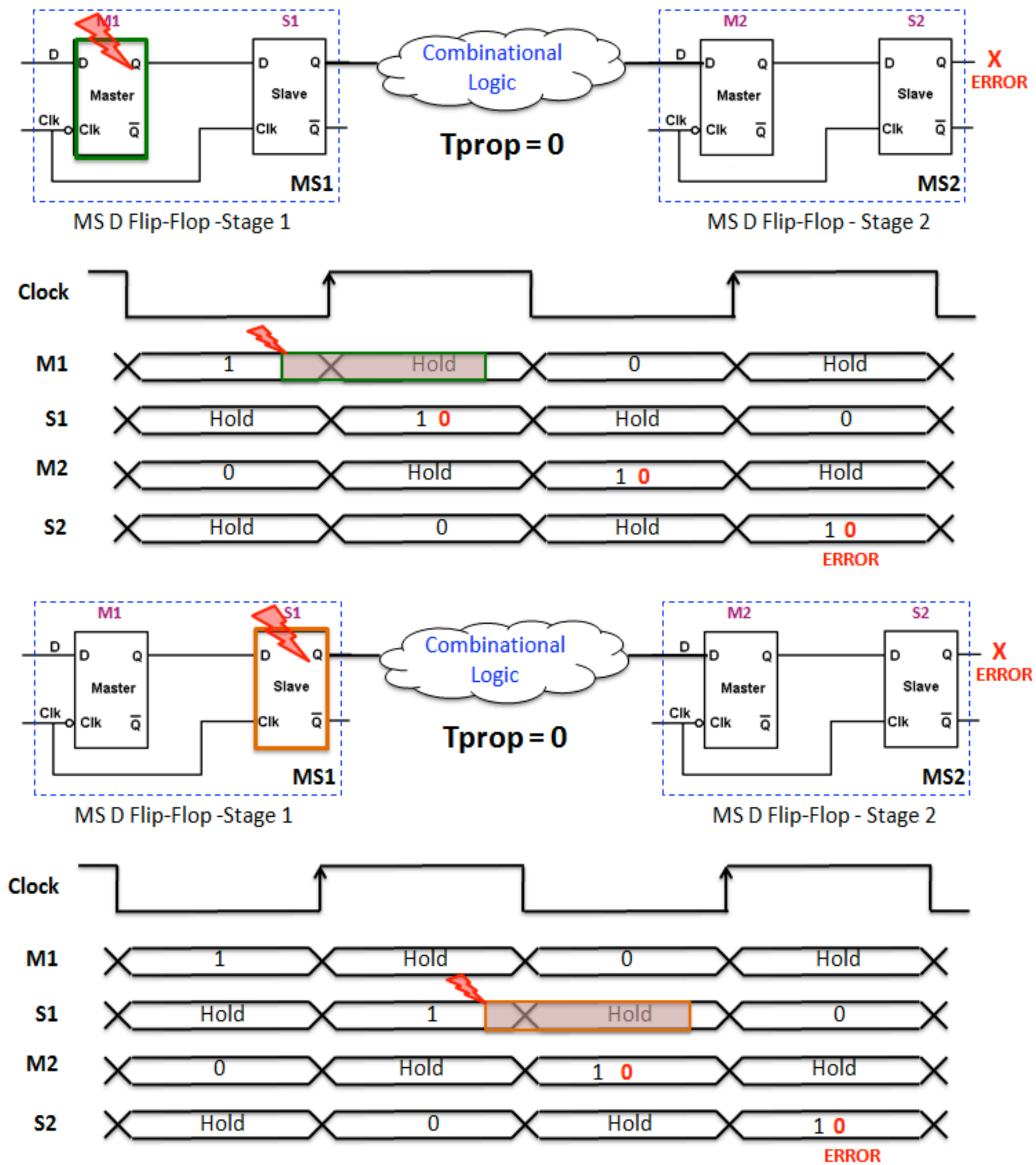


Figure 3.13: Insertion fault in (a) master and (b) slave latches considering a timing diagram without propagation delay between MS D Flip-Flops

Fig. 3.14 shows the insertion fault in master and slave latches considering a timing diagram with a large propagation delay between MS D Flip-Flops. When a fault is inserted in a slave latch, it is not propagated to the last MS Flip-Flop output due to a propagation delay of the combinational logic. As propagation delay is higher than WOV of the slave, the TVF of master decreases significantly, although it can still be seen in the output of pipeline stage.

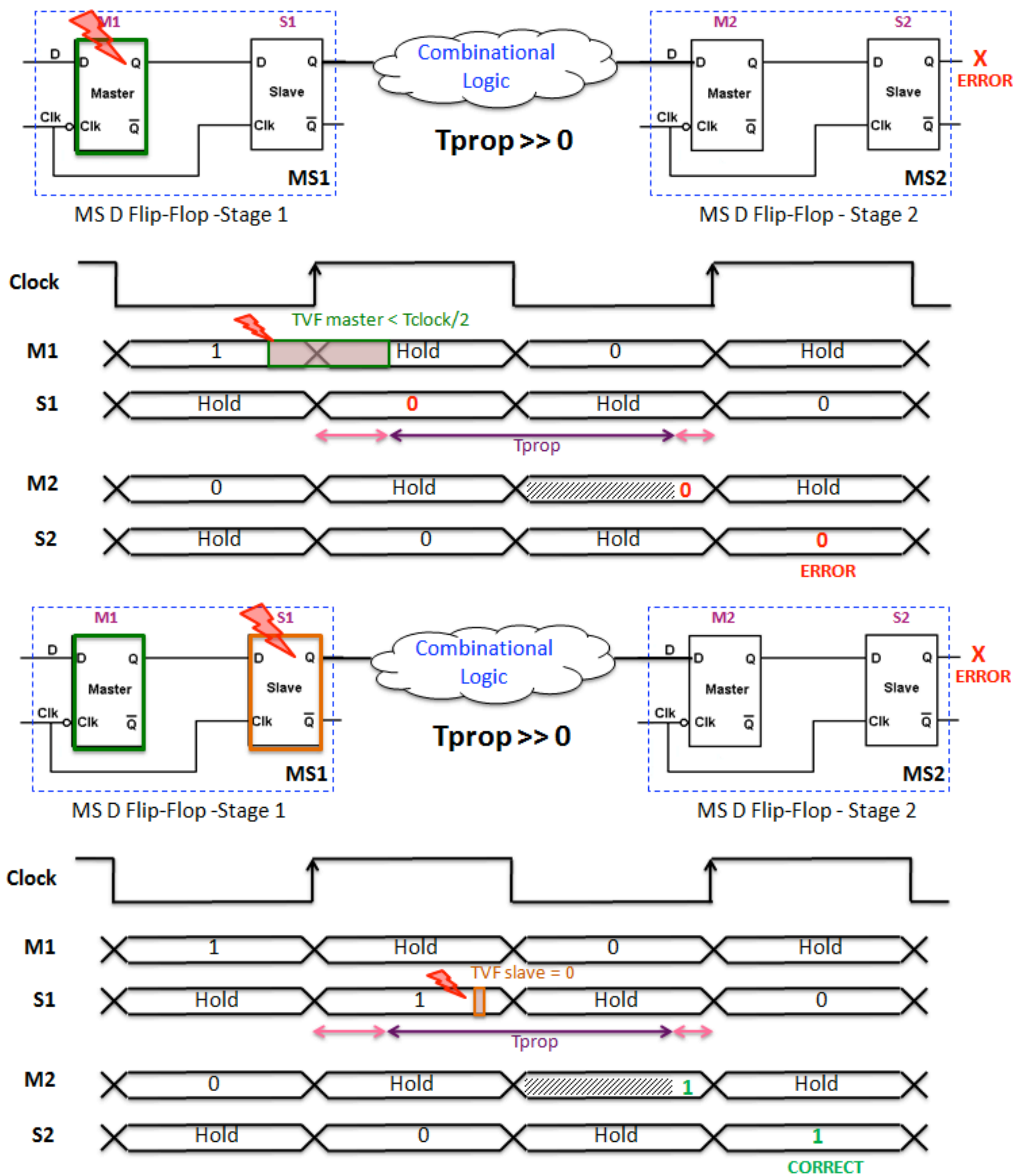


Figure 3.14: Insertion fault in master and slave latches considering a timing diagram with a large propagation delay between MS D Flip-Flops

4 METHODOLOGY

For the experiments, three different MS D Flip-Flop topologies in pipeline stages were considered to evaluate the Window of Vulnerability and the Timing Vulnerability Factor under different operating conditions. However, the methodology described here applies to any sequential. The implementation used in MS D Flip-Flops considers that they are triggered on the rising edge of the clock. MS D Flip-Flops were chosen to be analyzed, and it is listed below:

1. Standard Master-Slave D Flip-Flop (SMSFF)
2. Transmission-Gate Master-Slave D Flip-Flop (TGMSFF)
3. Write-Port Master-Slave D Flip-Flop (WPMSFF)

Standard Master-Slave D Flip-Flop is one of the most utilized topologies in the literature to teach the basic concepts of flip-flops (RABAEY et. al, 2003). This topology consists of two clocked RS (Reset-Set) flip-flops cascaded constructed with NOR gates. SMSFF schematic is shown in Fig. 4.1. When the clock is low, the master flip-flop is disabled by a pair of AND gates and remains in its set stable. When the clock goes high, the slave flip-flop is set to the value at D input, which gives the value at the output. SMSFF was implemented in a complementary CMOS logic with a total of 44 transistors divided in 22 transistors NMOS and 22 transistors PMOS. The sizing was made using the logical effort technique (SUTHERLAND, 1999).

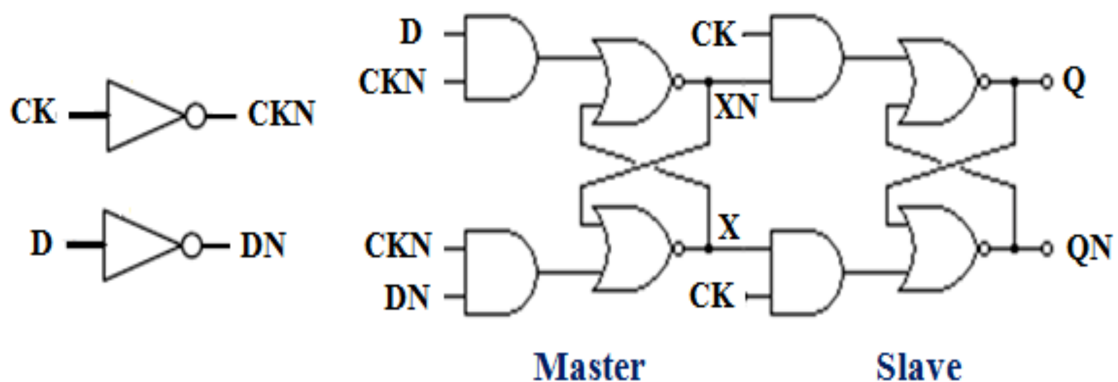


Figure 4.1: Standard Master-Slave D Flip-Flop (SMSFF)

Transmission Gate Master-Slave D Flip-Flop (RAMAKRISHNAN et al., 2008) is composed of transmission gates that will selectively block or pass a signal level from the input to the output. The control gates are biased in a complementary manner comprised of PMOS and NMOS transistors. TGMSFF schematic is shown in Fig. 4.2. The N5/P5 and N9/P9 transmission gates act as feedback loops in this topology while another versions of this flip-flop use tri-state inverters. When the clock signal is high, the transmission gate N2/P2 is in transparent mode, allowing that D input pass to the intermediate node M1. The transmission gate N5/P5 ensures that the previous output value will be maintained. When the clock is low, the logic value stored in M2 node is transmitted to Q output through of transmission gate N9/P9. TGMSFF has implemented with 18 transistors divided in 9 transistors NMOS and 9 transistors PMOS. The sizing was done according to (NUNES, 2014).

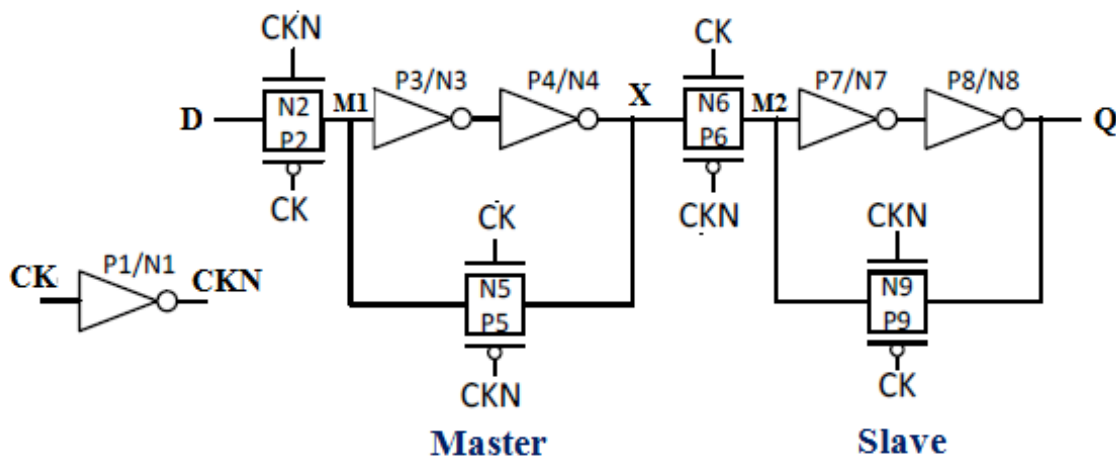


Figure 4.2: Transmission Gate Master-Slave D Flip-Flop (TGMSFF)

Write-Port Master-Slave D Flip-Flop is the least common structure presented here. WPMSFF schematic is shown in Fig. 4.3 and it was implemented with 24 transistors (16 transistors NMOS and 8 transistors PMOS). The access of the intermediate nodes is done through N4 and N11 NMOS transistors. The intermediate nodes are kept through the logical paths P3/P4/N6/N7/N8 and P6/P7/N13/N14/N15, when the clock is low and high, respectively. When the intermediate node is low, the loop that keeps the flip-flop stable is independent of the clock signal (MARKOVI et. al, 2003).

Due to threshold voltage drop inherent to the operation of NMOS transistors, it is necessary to reinforce the high value in intermediate nodes. In this way, P4/N3/N5 and P7/N10/N12 transistors serve to guarantee voltage equal to VDD in intermediate nodes. The sizing in WPMSFF received a special attention because the P4 and P7 transistors needed a smaller sizing to allow the correct operation of the flip-flop. All other transistor sizings were done according to (NUNES, 2014).

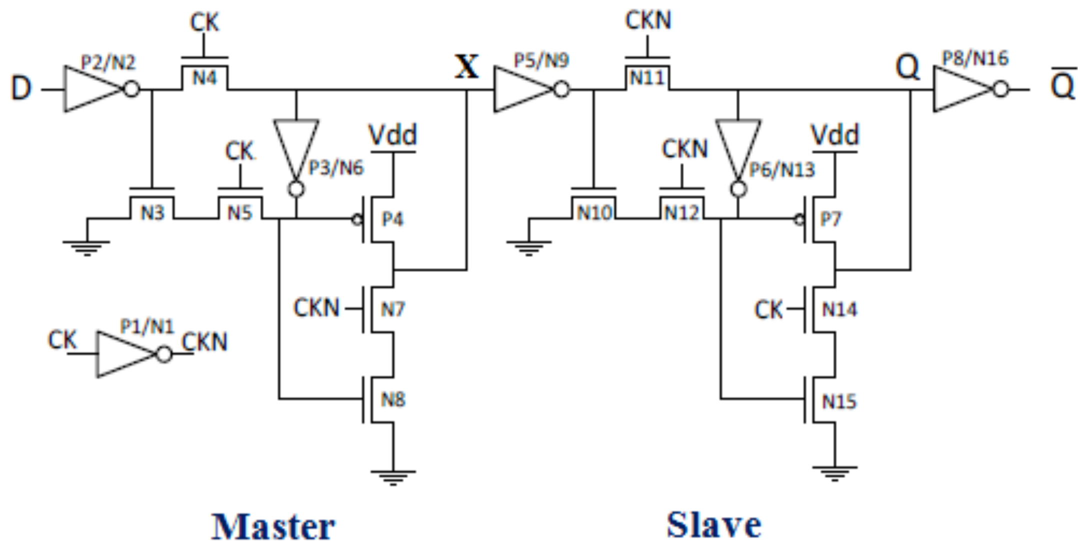


Figure 4.3: Write-Port Master-Slave Flip-Flop (WPMSFF)

Each one of the MS D Flip-Flops shown above was described using the SPICE language to allow the electrical simulations. The setup for all simulations is very similar for comparison purpose, with a total simulation time equal to 14ns and the same D input value for all topologies. The major changes in the descriptions are related with the technological model chosen in each experiment. The experiments adopted 32nm, 22nm or 16nm CMOS process technologies from Berkeley Predictive Transistor Model (PTM) in High Performance (HP) and Low Power (LP) versions. Simulations were carried out by using HSPICE tool from Synopsys Company. Tab. 4.1 shows the nominal values for each technology model utilized in this work. These parameters represent the obligatory changes in SPICE description every time a circuit with a new technology was simulated.

Table 4.1: Nominal Parameters from PTM technologies

Models	*Technology (nm)*	*Supply Voltage (V)*	*Gate Lenght (nm)*	*Temperature (ºC)*
HP	16	0.70	16	27
	22	0.80	22	27
	32	0.90	32	27
LP	16	0.90	16	27
	22	0.95	22	27
	32	1.00	32	27

Source: (PTM, 2015)

In order to analyze the TVF of MS D Flip-Flops, it is necessary to implement a pipeline design with combinational logic between the stages, as shown Fig. 4.4. In this work, each simulation has been composed by two MS D Flip-Flops with a chain of inverters varying from 4 to 24 inverters between them. Inverters were chosen as combinational logic because a large enough transient will always propagate through an inverter, whereas with a multiple input logic gate not always the propagation happens (GADLAGE et. al, 2004). For example, in an NAND gate, the state of the other input can determine if the transient pulse will propagate or not. All pipeline design was analyzed at 2GHz, 1GHz, 500MHz and 250MHz clock frequencies.

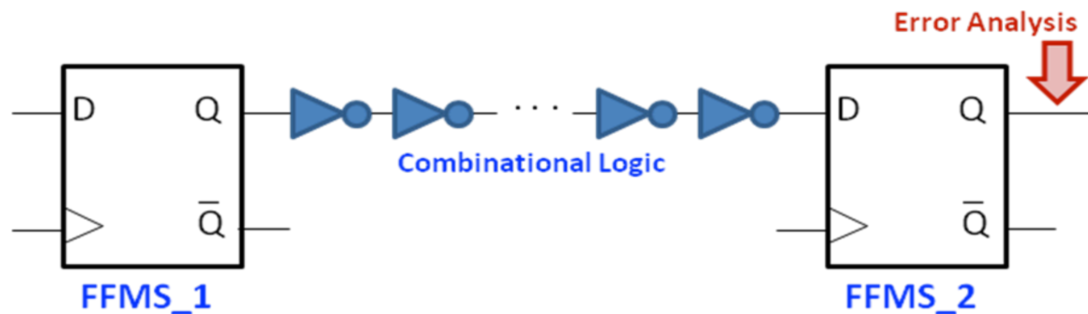


Figure 4.4: Pipeline design with inverters between flip-flops

4.1 Transient Fault Simulation

Soft error injections were done through a transient current source addition in the harmed node. Charge deposition mechanism is modeled by a double exponential current pulse according to Messenger's equation, which was presented in subchapter 2.4. At the SPICE electrical level, this equation is added to the circuit nodes according to Fig. 4.5 (GADLAGE et. al, 2004).

Names in red means the keywords in SPICE description, where Iset is the source name and EXP represents the double exponential. *Net+* and *net-* corresponds the positive and negative pulse at a node, respectively. The pulse polarity depends if the impacted node is initially in '0' or in '1'. For example, if the previous value of a node is equal to '1', the transient current must produce a negative pulse. The *initial_value* is the starting value of the pulse; the *pulsed_value* is the maximum charge collection (I_0); *tau_beta* and *tau_alpha* are constants very dependent on several process-related factors; *rise_delay* and *fall_delay* are the exponential rise and fall delays.

```
Iset ('net+' 'net-') EXP = ( 'initial_value'  'pulsed_value'
                             'rise_delay'     'tau_beta'
                             'fall_delay'     'tau_alpha')
```

Figure 4.5: Double exponential current source in SPICE

Fig. 4.6 shows an example of an SET that propagates until to reach the sequential circuit input. An SET occurs on the first NOR logic gate (OUT_NOR_1) and the circuit cannot mask logically or electrically the transient pulse generated by it. Also, the transient pulse propagates through the second NOR logic gate (OUT_NOR_2) and it reaches the inverter output (OUT_INV). In this case, it does not occur the latch-window masking, because the pulse is inside the latch-window limits and it is captured by the falling edge of a clock cycle. With the SET propagation, an incorrect value is stored in the memory element (OUT_FF) by a short time period (only 0.5ns). The output of NAND gate remains unchanged (OUT_NAND), because the fault not affects this arrangement.

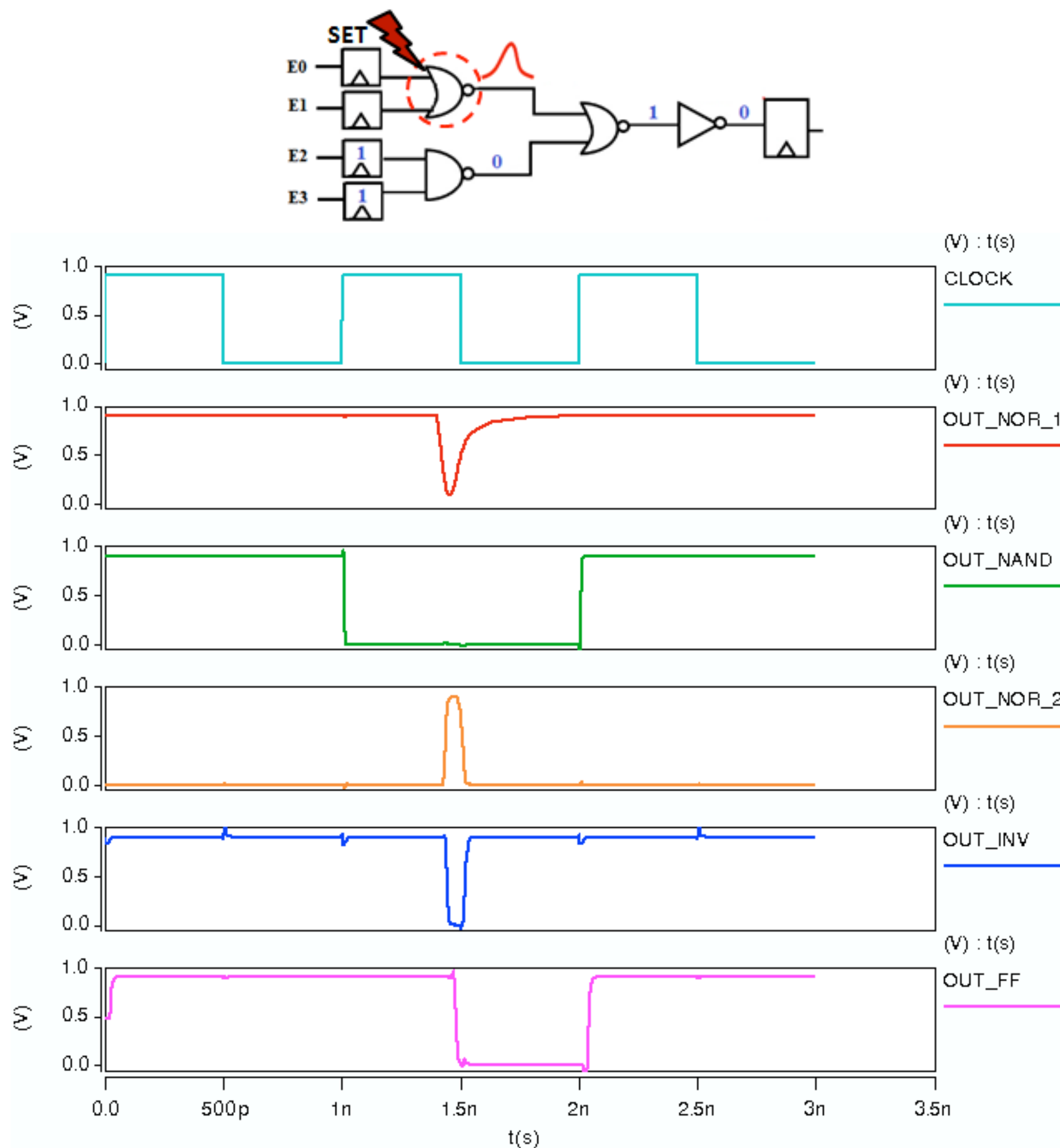


Figure 4.6: SET propagation until to reach a sequential circuit output

To compute the TVF of MS D Flip-Flops, a script was implemented to inject charge during a full clock period, which was divided up into 0.01ns time-steps. For all simulations in this work, some important considerations were taken into an account:

1) Only one fault was inserted at each simulation.
2) Fault insertion has been made in the first flip-flop of the pipeline design.

   This topic was divided into two steps: Fault insertion in the master latch and fault insertion in the slave latch. Each fault insertion provides a result that corresponds to a master TVF and to a slave TVF.
3) To all topologies of MS D Flip-Flops, the fault insertion was made at X node in the master latch and at the Q node in the slave latch, as shown Fig. 4.1, Fig. 4.2 and Fig. 4.3.
4) Error analysis is always made in the last flip-flop of the pipeline design independent of in which latch the fault was inserted, as shown Fig. 4.4.

4.2 Environmental Variability Simulation

Voltage supply and temperature variations consider only the High-Performance version of the 16nm and 32nm CMOS process technology for all MS D Flip-Flops topologies. In environmental variability simulation, the same structure shown above is used varying only voltage and temperature parameters. The impact of voltage variation in TVF is evaluated through the sensitivity of the Window of Vulnerability and Timing Vulnerability Factor to the variations around ±10% of the nominal power supply (VDD). These variations are commonly used as the typical targeted in many applications. The supply ranges for the two analyzed technologies are shown in Tab. 4.2.

Table 4.2: Variations of ±10% of the nominal power supply

Technology (nm)	*Nominal Supply Voltage (V)*	*Supply Range (V)*
16	0.70	0.61 - 0.79
32	0.90	0.81 - 0.99

The impact of temperature variation was evaluated regarding temperature coefficient around the nominal operating value of 27ºC. Hence, in the temperature evaluation, it was changed from 27ºC to 125ºC also considering the values commonly used as typical targeted in many applications. A script also was implemented to simulate the environmental variations for all clock frequencies and chain of inverters between sequential elements as they were mentioned above.

5 EXPERIMENTAL RESULTS AT NOMINAL CONDITIONS

In the last decades, many Electronic Design Automation (EDA) tools have been developed to help in the design flow steps and to predict electrical characteristics of circuits, for example. Currently, electrical simulations provide invaluable analysis because besides allowing the modeling of circuit operation, it is also possible to realize tests to predict unexpected behaviors before the manufacturing process. So, the project becomes cheaper because many problems are still detected by doing electrical simulations.

This chapter evaluates the Timing Vulnerability Factor of master and slave latches for the three topologies of MS D Flip-Flop considering different clock frequencies, combinational path delays and technologies models through electrical simulations. The first set of results consist in determine the dependency between SEU occurrences in a flip-flop with its clock frequency besides analyzing the fault propagation to the next stage through a combinational logic with different propagation delays. The second set of results provides the impact for different technological nodes, including High-Performance and Low Power version, cause on TVF values.

The methodology utilized in all experiments is the same. However, when the technology node changes, many geometrical and electrical parameters suffer modifications in their technology description file. Due to these modifications, the combinational logic path between the MS D Flip-Flops also changes. Moreover, the circuit topology can also modify the setup time of master and slave latches. For this reasons, the TVF of sequential circuits present different values. The proposed study is very important to show in details how to analyze the vulnerability of MS D Flip-Flops under SEU. It shows the real impact of the technology and of the chosen clock frequency in the sensitivity of the design under radiation.

Combinational delays can be a large or a small percentage of the clock period. Depending on the path delay, the circuit can be considered more or less sensible to bit-flips. Fig. 5.1 shows a generic example, with the same technology and topology, to analyze the impact that different clock frequencies and propagation delays on TVF of a slave latch according to what has been explained in subchapters 3.3 and 3.4. Small propagation delays (160ps and 280ps) between the sequential circuits and lower frequencies as 0.25GHz and 0.5GHz have a minor reduction if compared to initial TVF

values. However, with an intermediate propagation delay (400ps) at 2GHz, the reduction on TVF of a slave latch is significant, and it already can reach near zero.

Longer propagation delays (600ps and 720ps) at lower frequencies reduce the TVF values on average 15% for 0.25GHz and 30% for 0.5GHz, but when the circuit operates at 1GHz, for example, the TVF of a slave latch reduces sharply. The columns that do not appear in graphs mean that the circuit does not work at that frequency because the combinational delay is longer than the clock period.

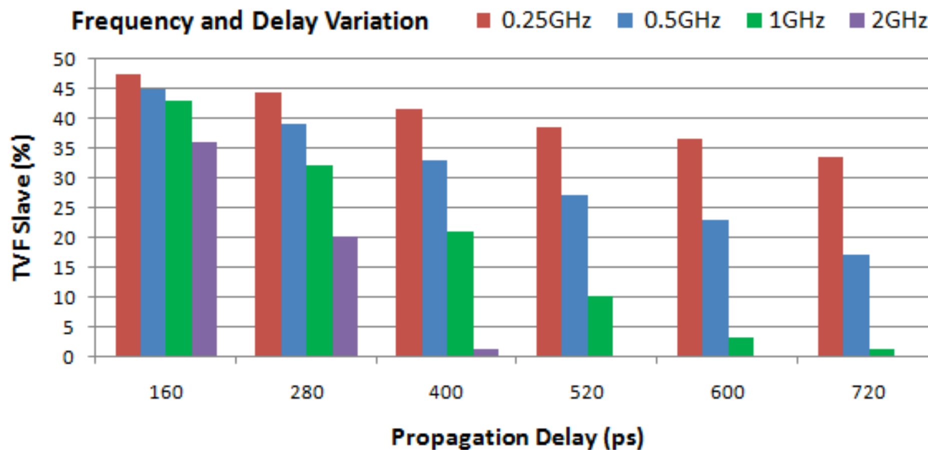


Figure 5.1: Impact on TVF with frequency and propagation delay variations

5.1 Standard Master-Slave D Flip-Flop

The measured TVF for the slave latch of SMSFF are presented in Fig. 5.2 for a 32-nanometer technology in High-Performance version. It is possible to confirm that each slave latch in different case-study circuits present variations on TVF according to the delay of combinational logic that it is connected to and to the clock frequency. At 0.25GHz, even with a large propagation delay, the TVF of a slave latch can decrease only to 33.5%. For the SMSFF to have 0% of TVF for a slave latch at 0.25GHz, it is necessary that the combinational logic path delay is equal to or greater than 2060ps. However, if the pipeline design operates at 2GHz with a propagation delay equal to 280ps, it is possible to reduce the TVF for the slave latch to 10%. To achieve a TVF equal to 0%, all the slave latches must be connected to combinational path delays with 310ps or more.

Fig. 5.3 and Fig. 5.4 show the TVF for a slave latch of a SMSFF using 22nm and 16nm technologies in High-Performance version. With the technology scaling down, the TVF for slave latches increase. For example, the TVF for slave latch considering the same combinational logic is equal to 42%, 40% and 38.5% at 0.25GHz for 16nm, 22nm and 32nm technologies, respectively. In this case, the variation of the technology model does not reduce significantly the TVF. On the other hand, at 1GHz and propagation delays between 420ps and 520ps, the effect of technology model variation is the most significant with TVF of a slave latch equal to 18%, 10% and 3% for 16nm, 22nm and 32nm technologies, respectively.

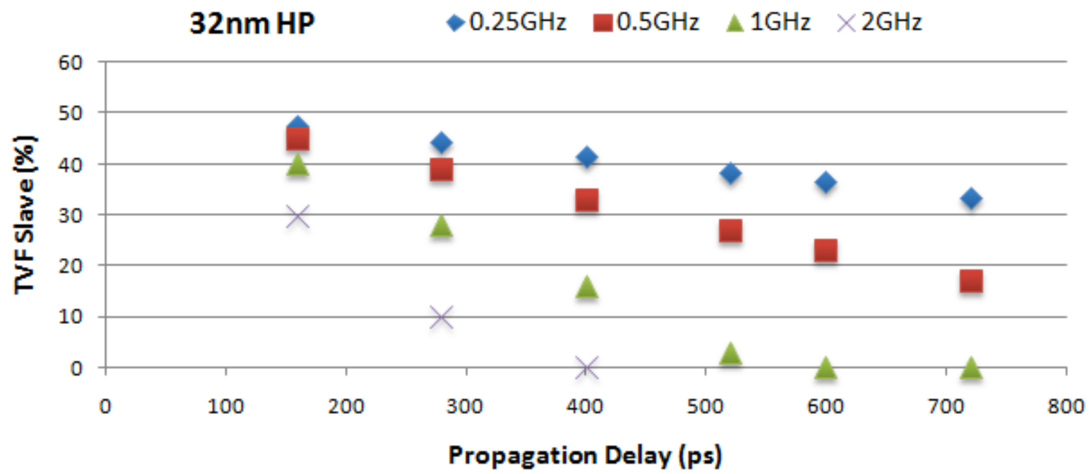


Figure 5.2: TVF for the slave latch of SMSFF for 32nm/HP

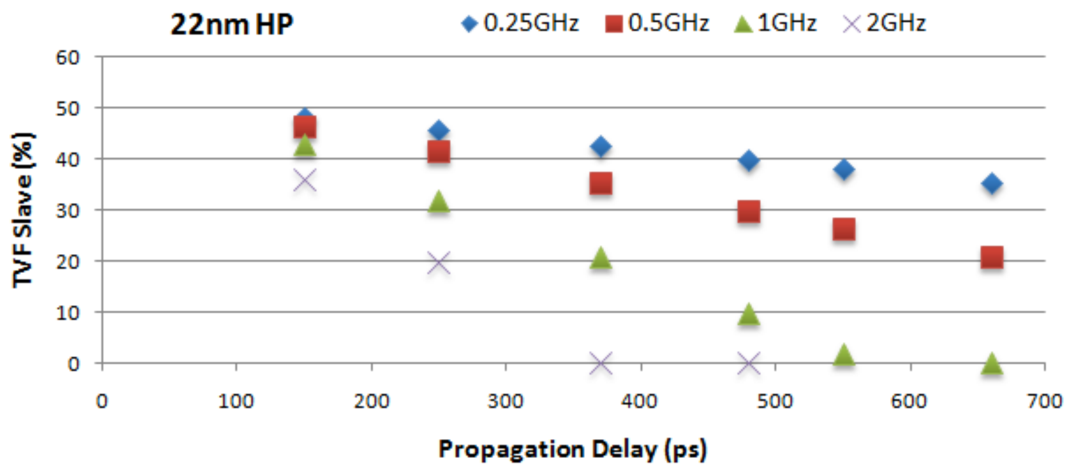


Figure 5.3: TVF for the slave latch of SMSFF for 22nm/HP

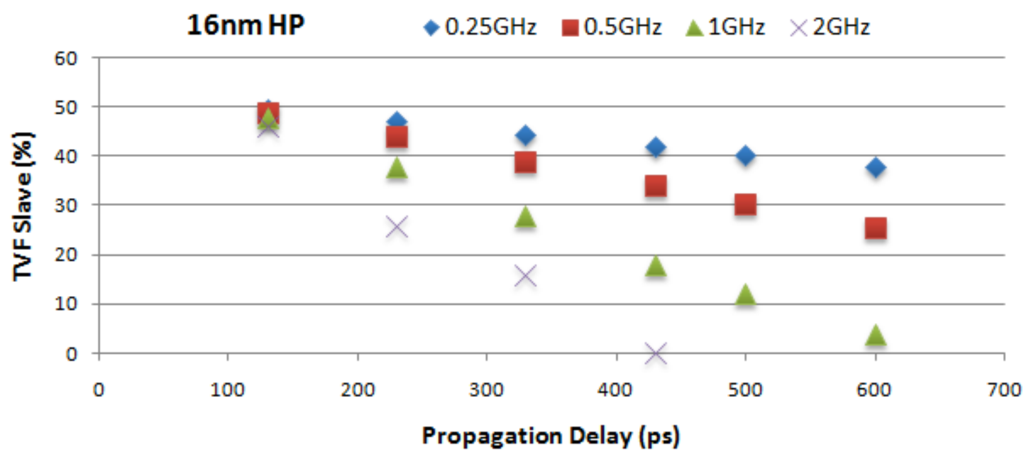
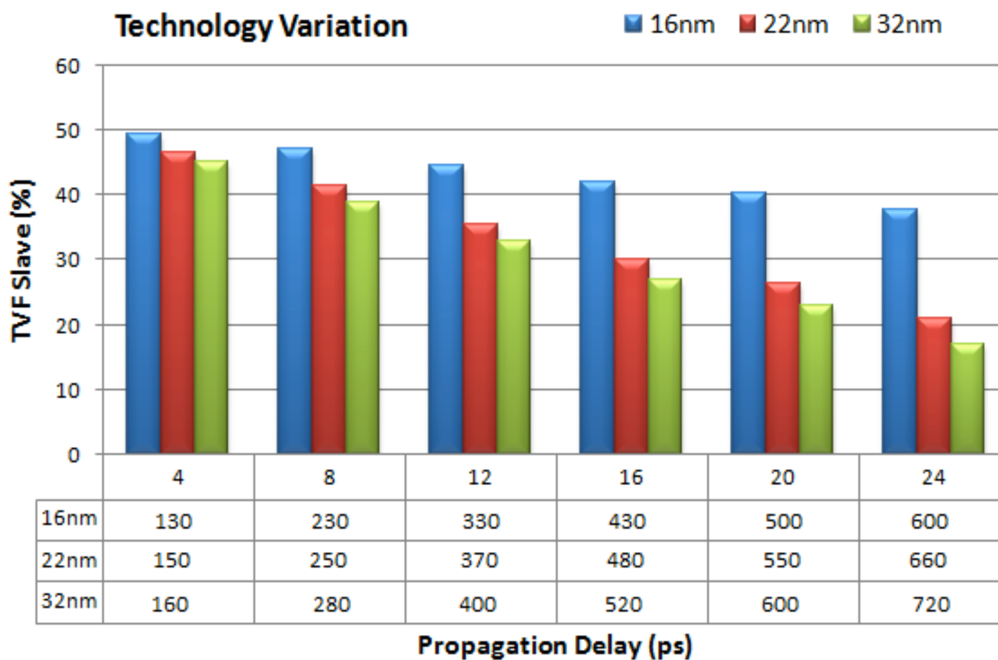


Figure 5.4: TVF for the slave latch of SMSFF for 16nm/HP

Fig. 5.5 shows the detailed analysis on TVF of a slave latch considering different technology models at a same clock frequency. The same combinational logic path was used in all experiments, but with the technology scaling down, these paths present different propagation delays as shown in the table in Fig. 5.5. Note that by changing the technology from 32nm to 22nm, there is no significant reduction in the TVF of a slave latch, where the maximum difference in TVF values is equal to 4% at a high combinational logic path. However, there is a large difference when we compare the technology from 32nm to 16nm, where the difference in TVF values can reach 20.75% for a long combinational logic path. This behavior asserts that lower node technology models are more sensitive to bit-flips. These set of results were recently published and it can be seen in (ZIMPECK et. al, 2014) and (ZIMPECK et. al, 2015).



	4	8	12	16	20	24
16nm	130	230	330	430	500	600
22nm	150	250	370	480	550	660
32nm	160	280	400	520	600	720

Figure 5.5: TVF of slave latch as function of the different technology nodes at 0.5GHz

As the TVF values of MS D Flip-Flops depend on the propagation delay between them and the decrease of the fault probability begins at the slave, the TVF of master latch only is modified when the TVF of a slave reaches 0%. At low frequencies of 0.25GHz and 0.5GHz, the TVF of slave latches do not reach 0% as it can be seen in Fig. 5.2, Fig. 5.3 and Fig. 5.4. For this, the TVF of master latches are completely preserved. In higher frequencies, there are some cases that beyond the slave TVF become zero and the TVF of master latch also suffers decrease. Tab. 5.1 shows the TVF for the master latches that suffer reduction due to propagation delays higher than half of the clock period. The spaces present in the table represent that given a technology, the TVF of slave latch does not reach 0% or that the pipeline design do not operate in pre-defined frequency.

Table 5.1: TVF for the master latch of SMSFF for 32nm/22nm/16nm/HP technologies

Frequency	*Inverters Number*	*Technology*					
		32nm		*22nm*		*16nm*	
		Delay (ps)	TVF (%)	Delay (ps)	TVF (%)	Delay (ps)	TVF (%)
1GHz	20	600	42	550	-	500	-
	24	720	30	660	38	600	-
2GHz	12	400	24	370	36	330	-
	16	520	-	480	16	430	30

The impact on TVF of a slave latch values when the pipeline design has the same technology node (16nm), but different application versions are shown in Fig. 5.6 and Fig. 5.7. In applications related to low power consumption, the combinational logic presented very large propagation delays in the majority of cases. The positive side is that TVF of master and slave latches decrease significantly making the SMSFF less sensitive to a bit-flip. But the negative point is that these pipeline designs only operates at low frequencies.

In Fig. 5.6, the reduction between the two application versions on TVF of slave latch is slightly smaller for short propagation delays. A chain of inverters with 4 or 8 inverters only reduce the TVF of a slave latch to 5.75% and 14.75%, respectively. If we consider a propagation delay equal to 20 inverters at 0.25GHz, TVF of a slave latch has a reduction of 35.5% at 16nm Low Power version. For a combinational logic path with 24 inverters, the TVF of a slave latch can reach zero. So, the TVF of a master latch also suffers a reduction in its vulnerability, presenting a new value equal to 40.25%.

In Fig. 5.7, the same analysis is made with a pipeline design working at 0.5GHz. With the increasing of the clock frequency, the difference between two application versions is even more significant as the combinational logic path increases. When the propagation delay is equal to 4 inverters, the reduction of TVF of a slave latch for a Low Power application version is 13.5%. However, with a chain composed by 12 or 16 inverters, the TVF of slave latch can already become zero. In this case, the TVF of master latch also decreases with these large delays and it present new values equal to 35% and 15%, respectively. A chain of inverters with 20 and 24 inverters do not present results because the propagation delay is bigger than the clock period.

The results of TVF of a slave latch for SMSFF in 16nm considering LP and HP application versions at 1GHz and 2GHz were omitted. The reason is that the pipeline designs with LP version do not work at 2GHz because all propagation delays studied are bigger than the clock period. The same happens when the pipeline design operates at 1GHz where only results with 4 and 8 inverters can be considered as valid.

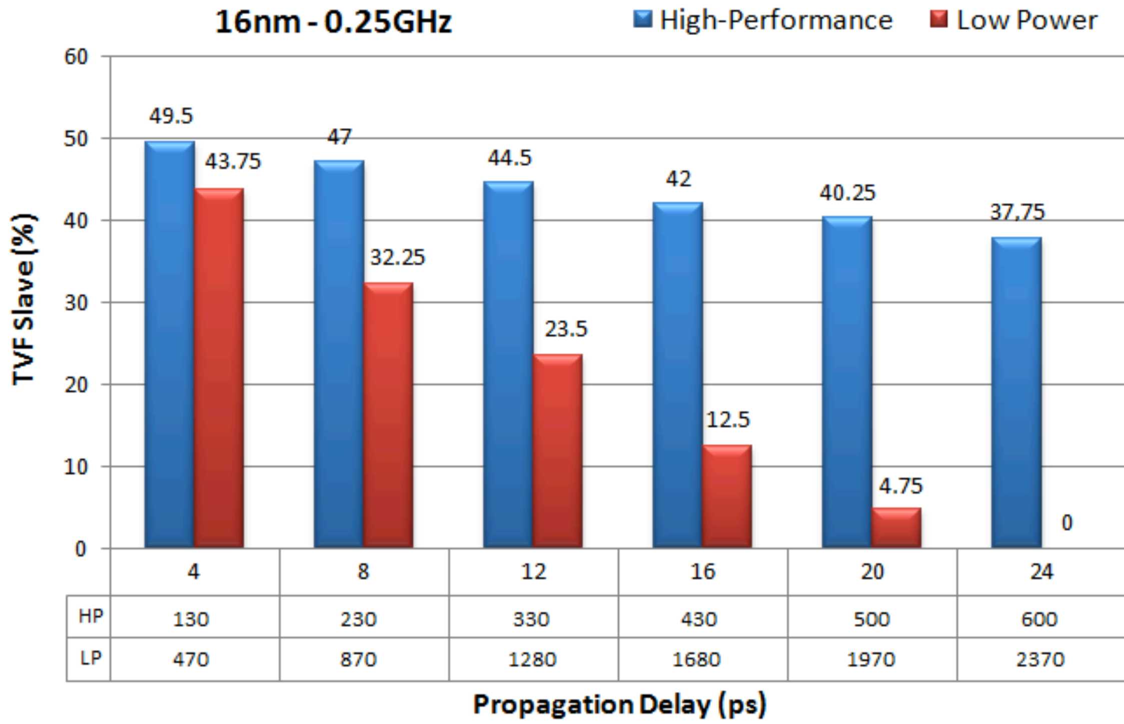


Figure 5.6: TVF for slave latch of SMSFF at 0.25GHz for 16nm High-Performance and Low Power versions

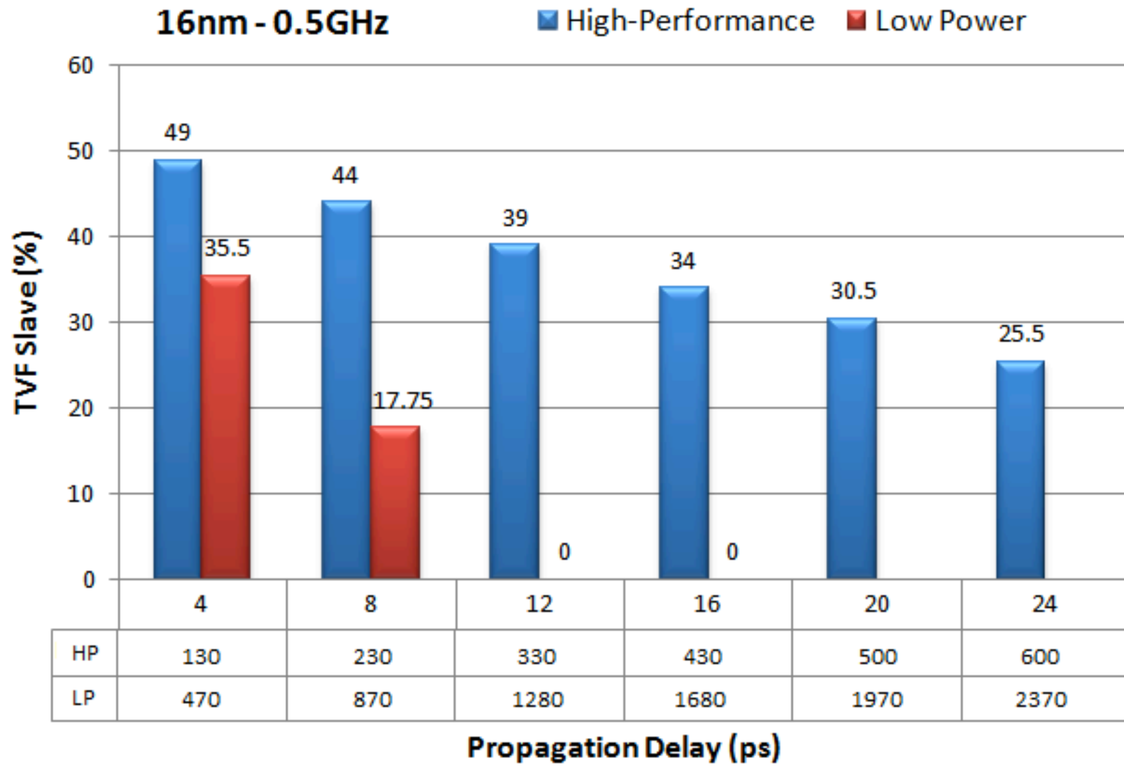


Figure 5.7: TVF for slave latch of SMSFF at 0.5GHz for 16nm High-Performance and Low Power versions

Fig. 5.8 and Fig. 5.9 also consider the impact on TVF of a slave latch when the pipeline design operates in two different clock frequencies and two different technology versions. But in this experiment, it was considered the 32nm technology node. In Fig. 5.8, the pipeline design operates at 0.25GHz and it is possible to note that the TVF of a slave latch is lower than the 16nm technology node operating with the same frequency. This means that higher technologies nodes are more robust to bit-flips. If we consider a propagation delay equal to 16 inverters, the TVF of slave latch has a reduction of 30.25% in the 32nm Low Power version. For a combinational logic path with 20 and 24 inverters, the TVF of a slave latch can reach to zero. So, the TVF of a master latch reduces its vulnerability to faults and it present new values equal to 45.25% and 34% respectively.

In Fig. 5.9, the pipeline is working at 0.5GHz and the difference between the TVF of a slave latch with propagation delays remains more significant. When the propagation delay is equal to 4 inverters, the reduction of TVF of a slave latch for a Low Power application version is 10%. With propagation delays equal to 12 and 16 inverters, the TVF of a slave is totally free of bit-flips and the TVF of master was reduced to values equal to 45.25% and 34%, respectively. A chain of inverters with 20 and 24 inverters also do not present results because the propagation delay is bigger than the clock period.

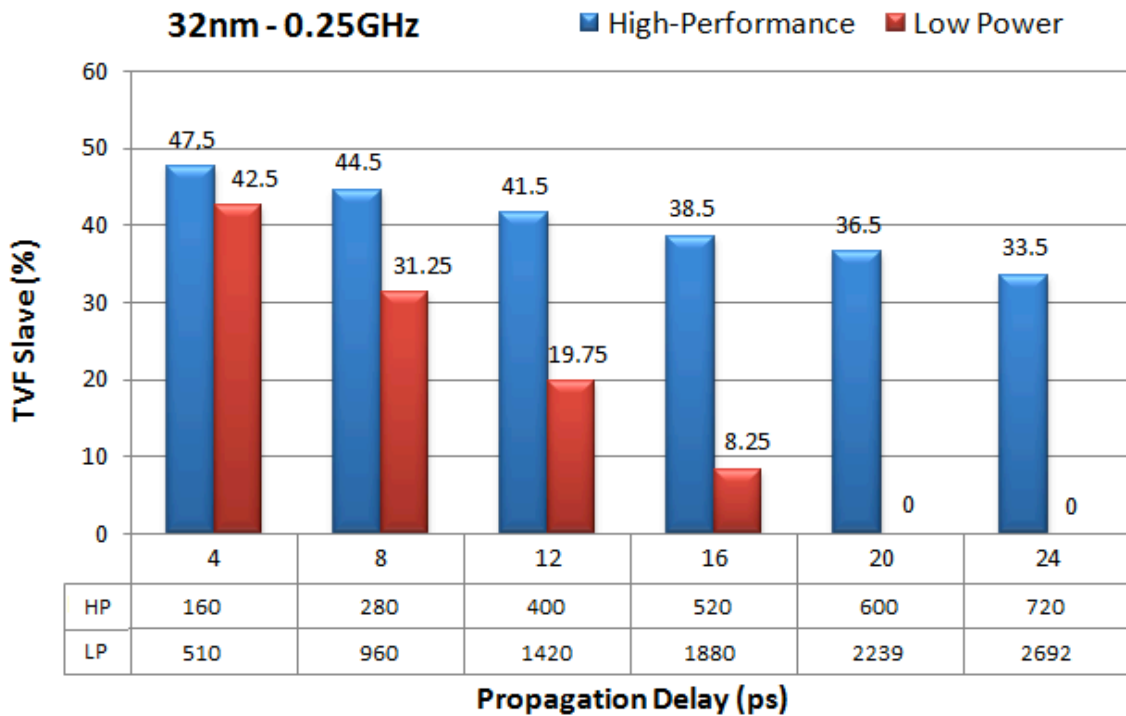


Figure 5.8: TVF for slave latch of SMSFF at 0.25GHz for 32nm High-Performance and Low Power versions

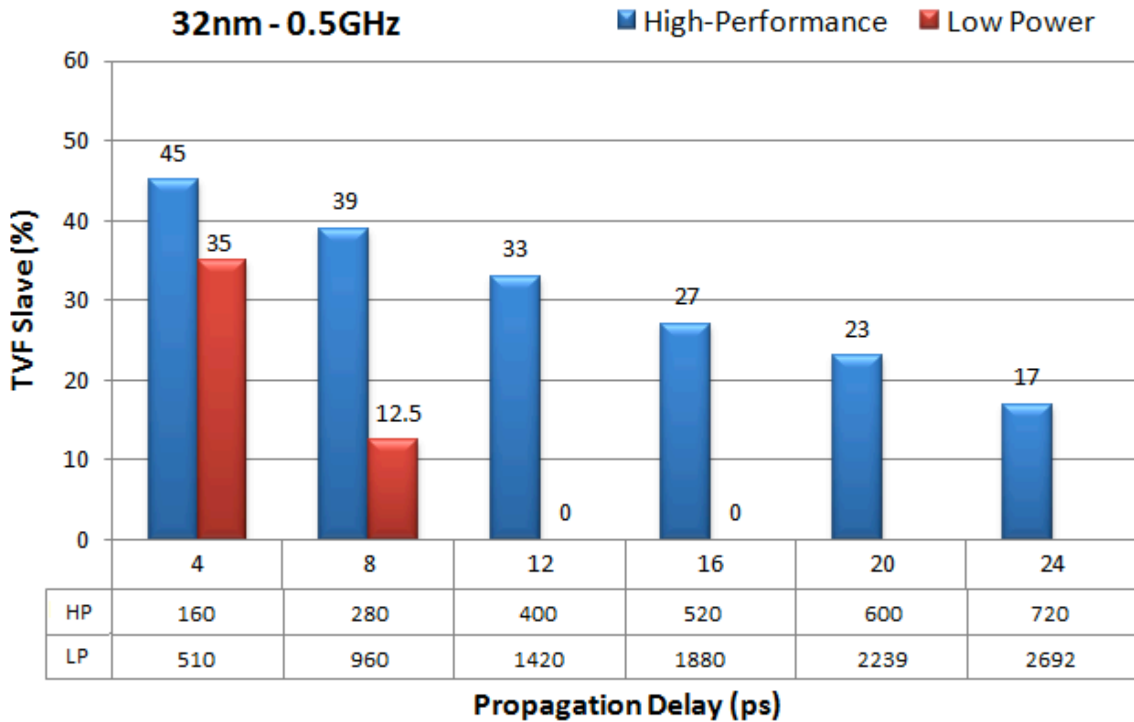


Figure 5.9: TVF for slave latch of SMSFF at 0.5GHz for 32nm High-Performance and Low Power versions

5.2 Transmission Gate Master-Slave D Flip-Flop

The measured TVF for a slave latch of a TGMSFF are presented in Fig. 5.10 for 32 nanometer technology in High-Performance version. Considering the maximum propagation delay analyzed in this work (24 inverters) and clock frequency equal to 0.25GHz, the TVF of a slave latch is reduced around to 17.5% in relation to the initial value. For the TGMSFF to have 0% of TVF for the slave latch, it is necessary that the combinational path delay is equal to or greater than 2030ps. However, if the same pipeline design operates at 2GHz with propagation delay equal to 280ps, it is possible to reduce the TVF for the slave latch to 22%.

Fig. 5.11 and Fig. 5.12 show the TVF for a slave latch of TGMSFF for 22nm and 16nm technologies in High-Performance version. The impact that the technology scaling down generates in TVF values also can be seen on the results of TGMSFF topology. Considering the lower frequency (0.25GHz) and 16 inverters as combinational logic, the TVF for slave latches are equal to 41.5%, 39.5% and 37.5% for 16nm, 22nm and 32nm technologies, respectively. The variation of technology node with small propagation delay in this topology does not present a significant difference on TVF values. At higher frequencies (1GHz) and propagation delays between 430ps and 530ps, the effect of technology model variation is bigger because the TVF for slave latches is equal to 16%, 8% and 2% for 16nm, 22nm and 32nm technologies, respectively.

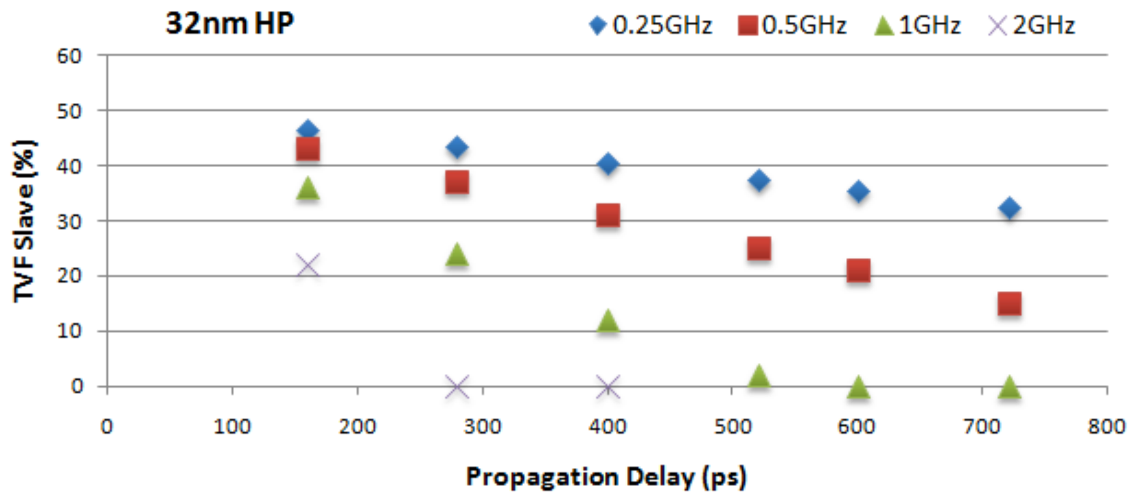


Figure 5.10: TVF for the slave latch of TGMSFF for 32nm/HP

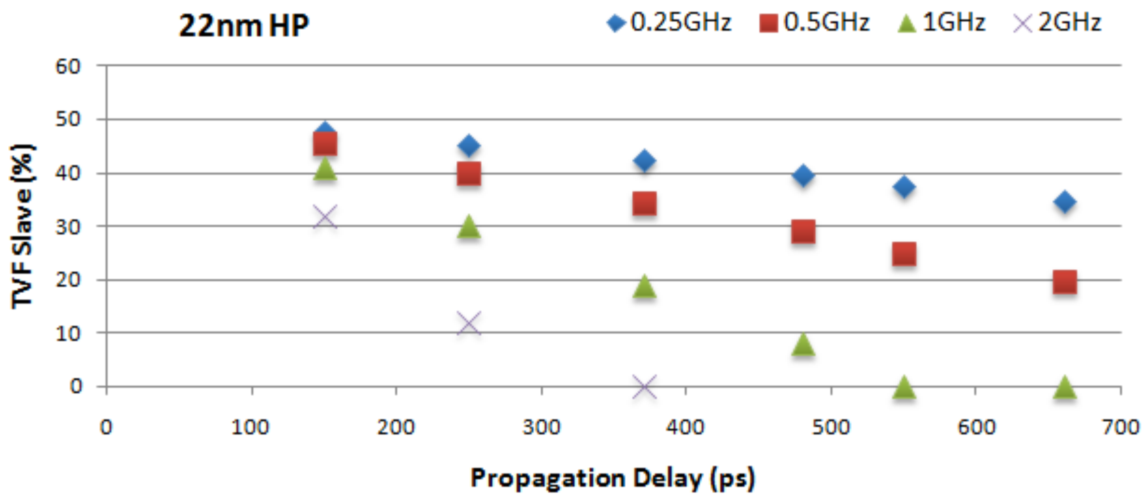


Figure 5.11: TVF for the slave latch of TGMSFF for 22nm/HP

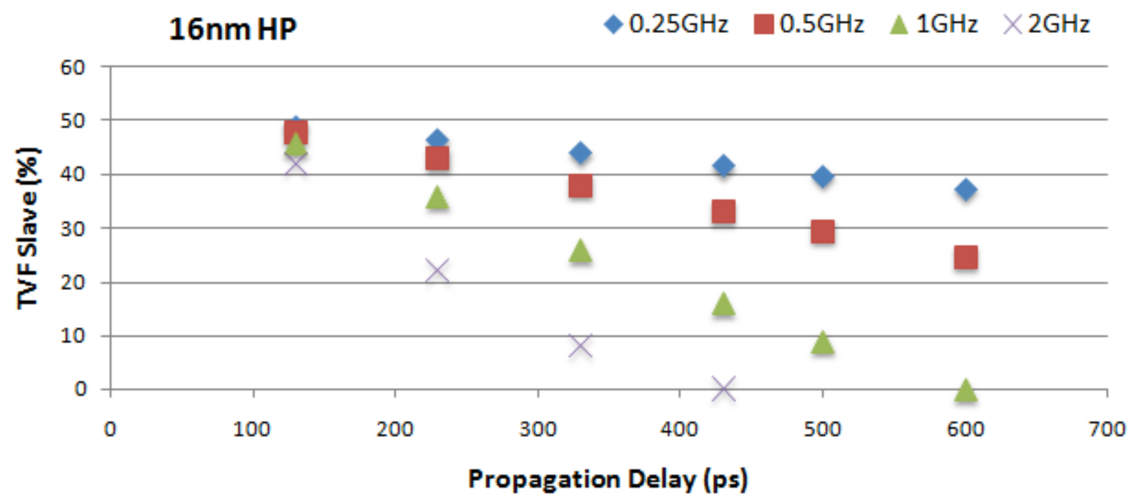


Figure 5.12: TVF for the slave latch of TGMSFF for 16nm/HP

As the TVF values of a MS D Flip-Flops depend on the propagation delay between them and the decrease of the fault probability begins at the slave, the TVF of a master latch only is modified when the TVF of a slave reaches 0%. In higher frequencies, there are some cases that beyond the slave TVF become zero, the TVF of master latch also suffers a decrease. Tab. 5.2 shows the TVF for the master latch that suffer reduction due to propagation delays higher than half of the clock period. The spaces presented in the table represent that given a technology, the TVF of slave latch does not reach to 0% or the pipeline design do not operate in pre-defined frequency. At 2GHz, only with 8 inverters already is possible to achieve TVF of slave latch equal to zero. Moreover, different on results for SMSFF, this topology present more situations that TVF of a master latch suffers a considerable reduction. This means that TGMSFF is more robust to bit-flips than a SMSFF is.

Table 5.2: TVF for the master latch of TGMSFF for 32nm/22nm/16nm/HP technologies

Frequency	*# of Inverters*	*Technology*					
		32nm		*22nm*		*16nm*	
		Delay (ps)	TVF (%)	Delay (ps)	TVF (%)	Delay (ps)	TVF (%)
1GHz	20	600	39	550	48	500	-
	24	720	27	660	37	600	47
2GHz	8	290	42	260	-	230	-
	12	400	18	370	-	330	-
	16	520	-	480	28	430	34

The impact on TVF of slave latch values when the pipeline design has the same technology node (16nm), but with different application versions are shown in Fig. 5.13 and Fig. 5.14 for the TGMSFF topology. Propagation delay equal to 1650ps at 0.25GHz reduces the TVF of a slave latch from 39.75% to 9.5% in a 16nm Low Power version as shown in Fig. 5.13. However, the reduction of TVF of a slave latch between the two applications versions can be considered negligible when propagation delay is equal to 4 inverters (7.25%). For combinational logic path with 20 and 24 inverters, the TVF of slave latch reach to zero and so, the TVF of a master latch gains new values equal to 45.25% and 33.75%, respectively.

In Fig. 5.14, the same analysis is done for a pipeline design working at 0.5GHz. With the increasing clock frequency, the difference between the TVF of a slave latch with different propagation delays deserves more prominence. When the propagation delay is equal to 4 inverters, the reduction of the TVF of a slave latch for Low Power application version is 15.75%. A chain of inverters with 12 or 16 inverters resets the TVF of a slave latch and the TVF of a master latch presents new values equal to 30% and 7%, respectively.

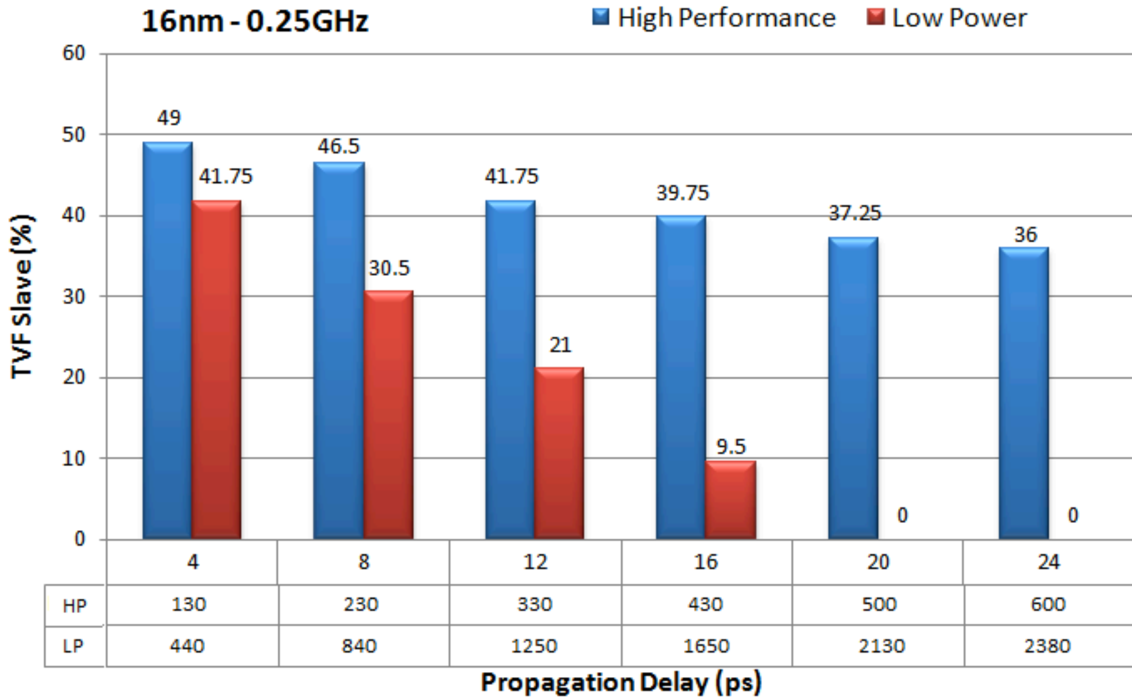


Figure 5.13: TVF for slave latch of TGMSFF at 0.25GHz for 16nm High-Performance and Low Power versions

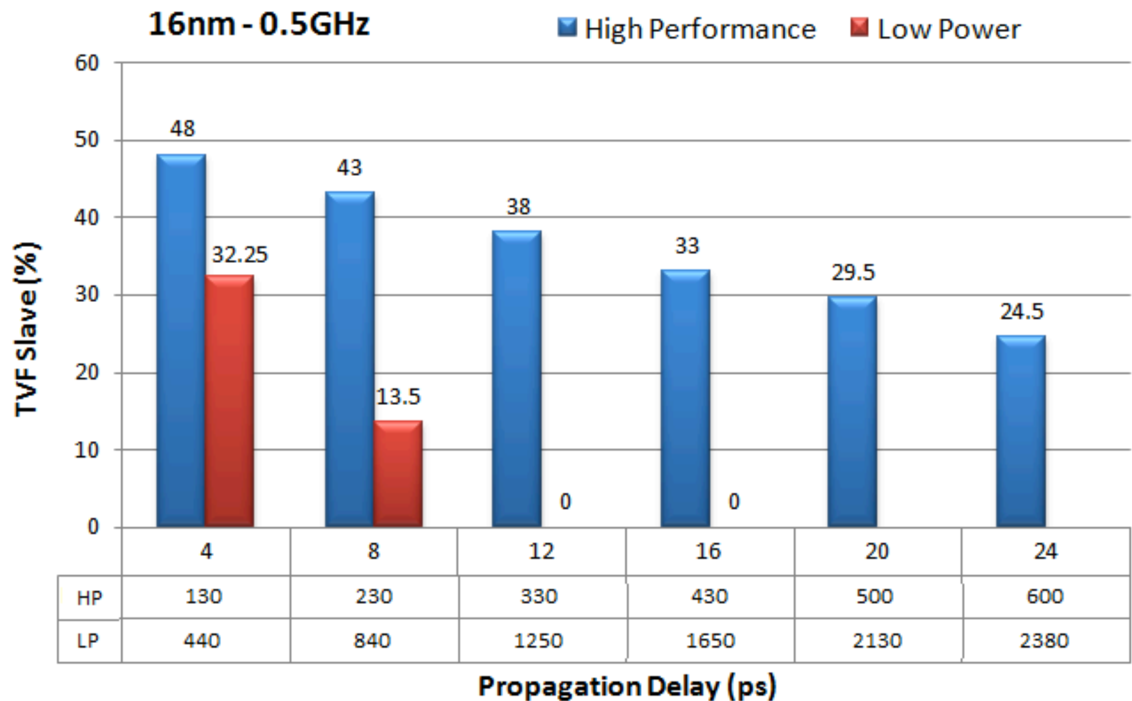


Figure 5.14: TVF for slave latch of TGMSFF at 0.5GHz for 16nm High-Performance and Low Power versions

Fig. 5.15 and Fig. 5.16 also consider the impact on TVF of a slave latch when the pipeline design operates at two different clock frequencies and two different technology application versions, but in this experiment was considered a 32nm technology node. In Fig. 5.15, the pipeline design operates at 0.25GHz. The TVF of a slave latch is lower than with a 16nm technology node operating with the same frequency. A significant decrease on TVF of a slave latch, when it is considered a 32nm Low Power version and 16 inverters, is easily noticed, varying it from 37.5% to 6.5%. For the TVF of slave latch that reach to zero, the TVF of a master latch with 20 and 24 inverters gain a reduction that is equal to 48.5% and 41.75%, respectively.

In Fig. 5.16, the pipeline is working at 0.5GHz and the difference between the TVF of a slave latch with propagation delays remains more significant. When the propagation delay is equal to 4 inverters, the reduction of TVF of a slave latch for Low Power application version is 12.75%. With propagation delays equal to 12 and 16 inverters, the TVF of a slave is totally free of bit-flips and the TVF of a master was reduced to values equal to 38.5% and 18.5%, respectively. Chain of inverters equal to 20 and 24 inverters also do not present results because the propagation delay between two sequential circuits is bigger than the clock period.

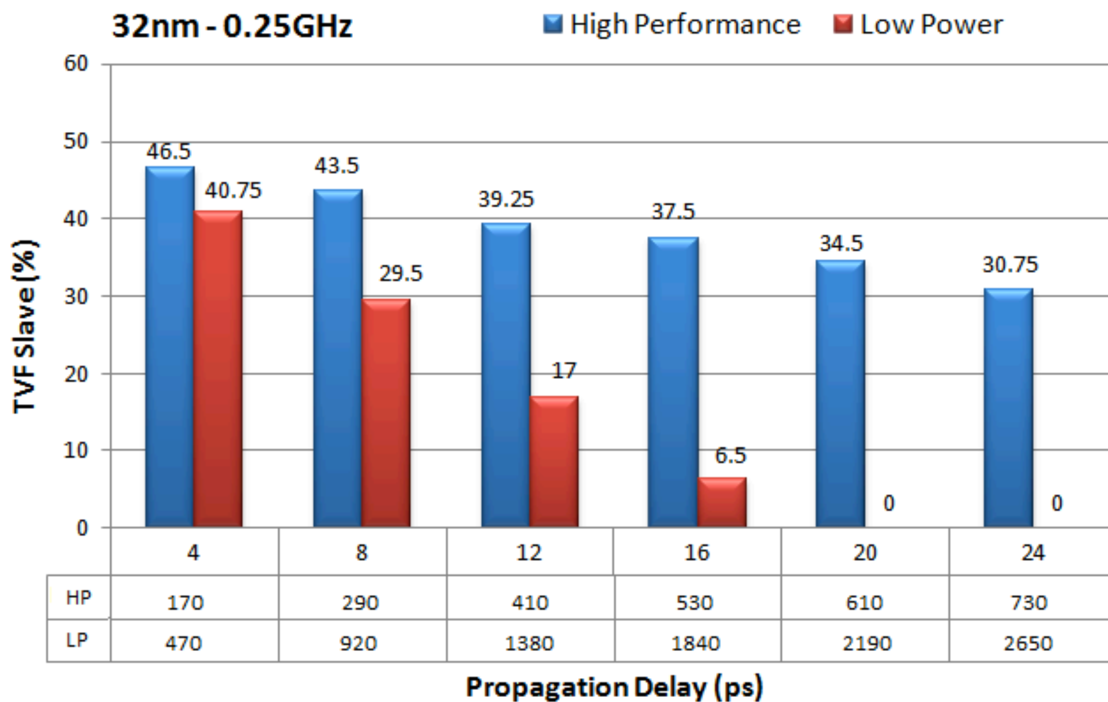


Figure 5.15: TVF for slave latch of TGMSFF at 0.25GHz for 32nm High-Performance and Low Power versions

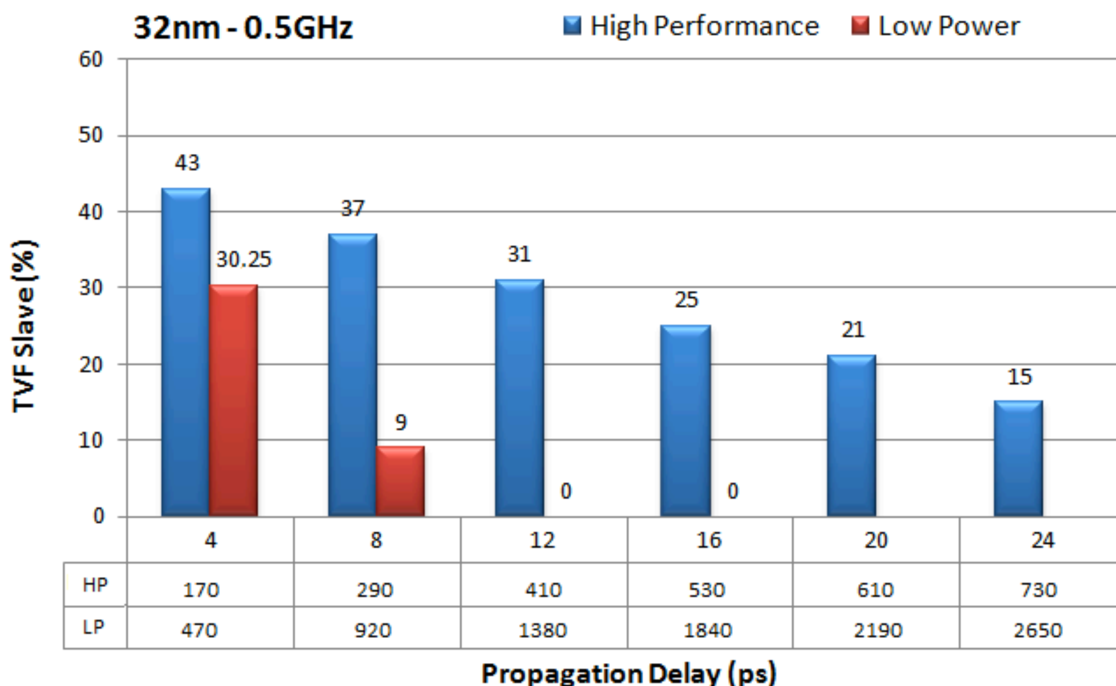


Figure 5.16: TVF for slave latch of TGMSFF at 0.5GHz for 32nm High-Performance and Low Power versions

5.3 Write-Port Master-Slave D Flip-Flop

The last topology that was studied is the Write-Port MS D Flip-Flop. Fig. 5.17 shows the measured TVF for the slave latch of a WPMSFF in 32nm technology node. When the pipeline design operates at 2GHz with a propagation delay equal to 290ps, it is possible to reduce the TVF for the slave latch to 12.75%. To achieve TVF equal to 0%, all the slave latches must be connected to combinational path delays of 1070ps or more. In order to achieve the lowest TVF for the slave latches, it is better to operate in 1GHz where all latches connected to paths longer than 570ps have 0% TVF, while if the same circuit operates at 0.25GHz, only latches connected to path delays over 2070ps will have 0% TVF.

Fig. 5.18 and Fig. 5.19 show the TVF for the slave latch of a WPMSFF using 22nm and 16nm technology nodes in High-Performance version. For example, considering the frequency of 0.25GHz, the TVF for slave latches are equal to 42.5%, 41.25% and 40.5% for 16nm, 22nm and 32nm technologies for the same combinational logic, respectively. At higher frequencies (1GHz) and propagation delays between 420ps and 520ps, the effect of the technology model variation is bigger because the TVF for slave latches is equal to 22%, 13.5% and 4% for 16nm, 22nm and 32nm technologies, respectively.

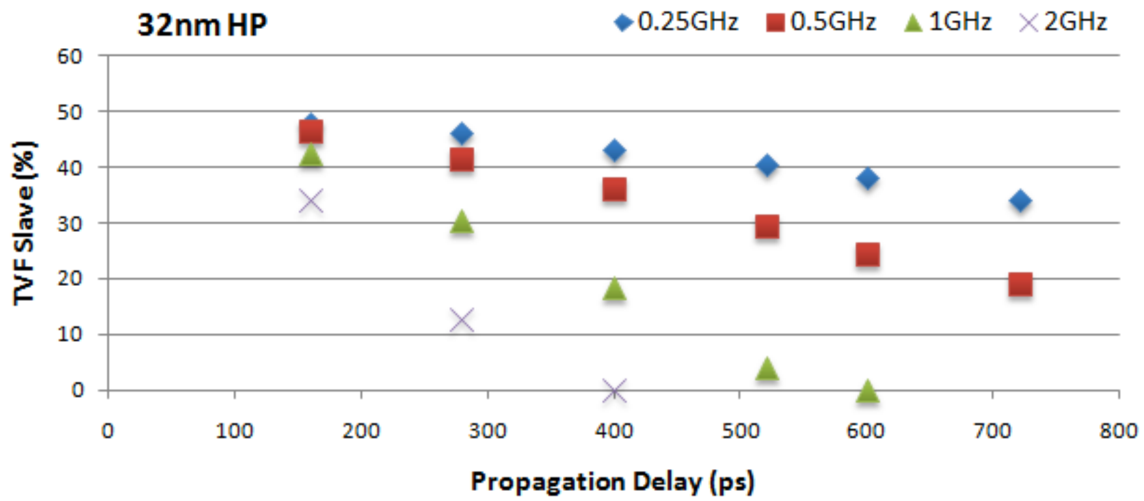


Figure 5.17: TVF for the slave latch of WPMSFF for 32nm/HP

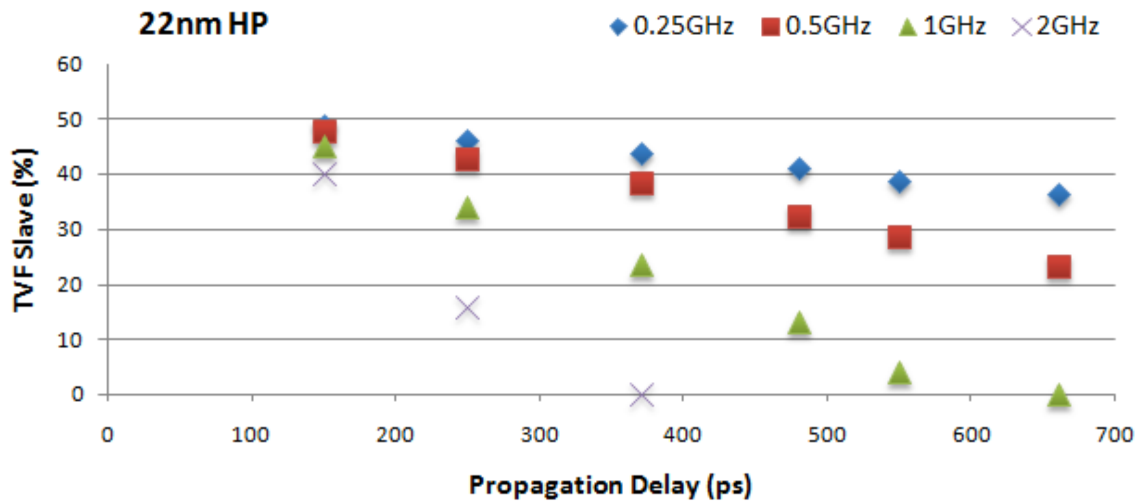


Figure 5.18: TVF for the slave latch of WPMSFF for 22nm/HP

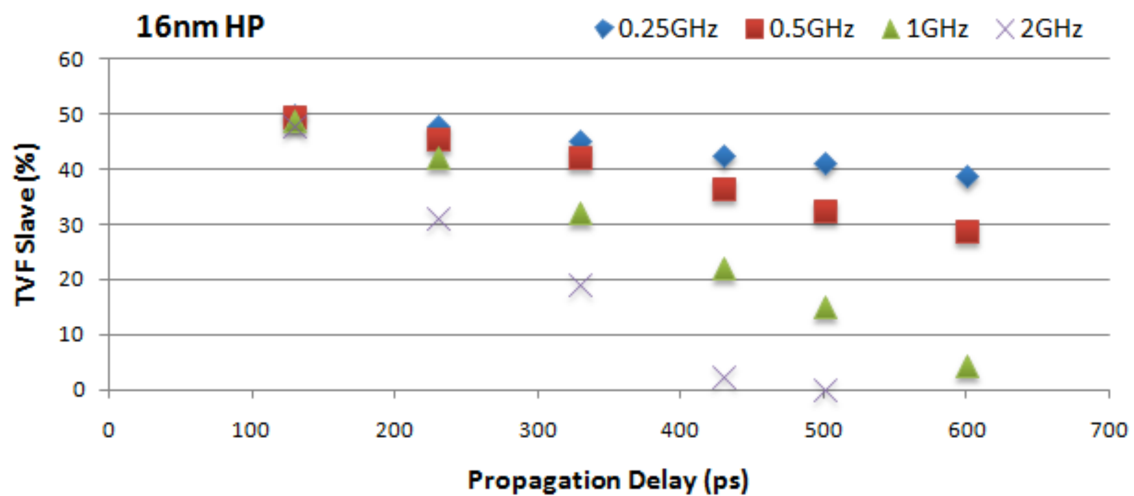


Figure 5.19: TVF for the slave latch of WPMSFF for 16nm/HP

The TVF values depend on the propagation delay of combinational logic and the decrease of the fault probability begins at the slave, the TVF of master latch is only modified when the TVF of a slave reaches 0%. In higher frequencies, there are some cases that beyond the slave TVF become zero, the TVF of master latch also suffers a decrease. Tab. 5.2 shows the TVF for the master latch that suffer reduction due to propagation delays higher than half of the clock period. At 2GHz, only with 12 inverters it is already possible to achieve TVF of a slave latch equal to zero. Moreover, different on results for SMSFF and TGMSFF, this topology presents the maximum reduction in master latches equal to 28%. So, according to values obtained, this topology is more sensitive to bit-flips than the SMSFF and TGMSFF.

Table 5.3:TVF for the master latch of WPMSFF for 32nm/22nm/16nm/HP technologies

Frequency	*Inverters Number*	*Technology*					
		32nm		*22nm*		*16nm*	
		Delay (ps)	TVF (%)	Delay (ps)	TVF (%)	Delay (ps)	TVF (%)
1GHz	20	600	45.5	550	-	500	47
	24	720	33	660	35	600	-
2GHz	12	400	28	370	34	330	-
	16	520	-	480	-	430	36

The impact on TVF of slave latch when the pipeline design uses 16nm or 32nm technology models considering high-performance and low power applications versions are shown in Fig. 5.20, Fig. 5.21, Fig. 5.22 and Fig 5.23. In a 16nm technology node, the more significant is a reduction between the applications versions as large the propagation delays are, as shown Fig. 5.20 and Fig. 5.21. When the combinational logic is small, the reduction of TVF of a slave latch can be considered more negligible at 0.25GHz (5.75%) and a little bit significant when the pipeline design operates at 0.5GHz (12%). At 0.25GHz, the TVF of a slave reach to zero only with a chain containing 24 inverters and the TVF of master receives the new value equal to 35.75%.

For 32nm technology model, the reduction that has been brought by the use of different node versions is milder as shown Fig. 5.22 and Fig. 5.23. This happens because at higher technology nodes, the propagation delay of logic gates increases and consequently, it decreases the TVF of slave latches. At 0.25GHz, the TVF of a slave reach to zero already with a chain containing 20 inverters and it can reduce a little the TVF of a master latch to 47.25%. Similarly with the 16nm technology, at 0.5GHz the TVF of a slave latch already reach zero with combinational logic with 12 and 16 inverters.

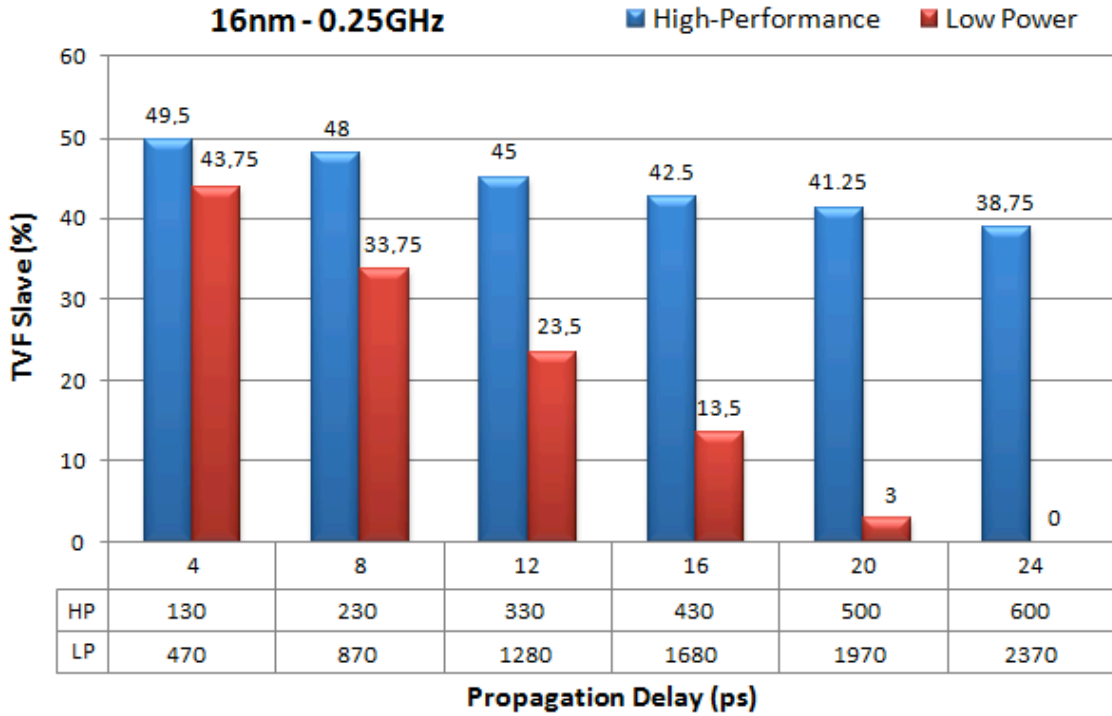


Figure 5.20: TVF for slave latch of WPMSFF at 0.25GHz for 16nm High-Performance and Low Power versions

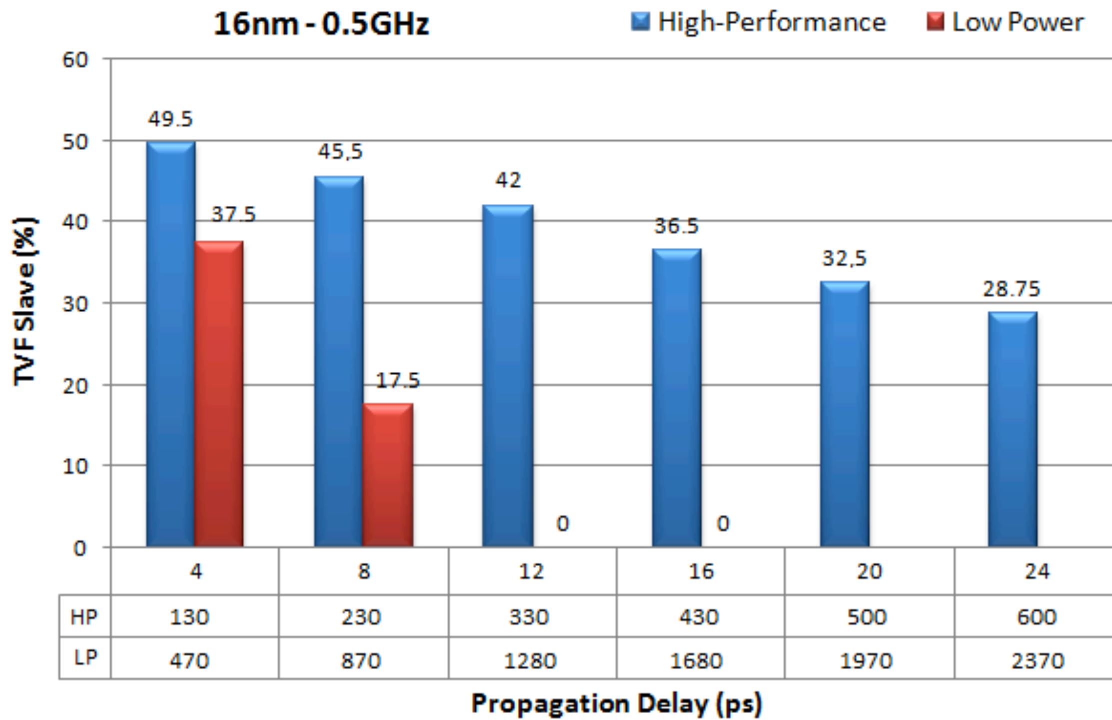


Figure 5.21: TVF for slave latch of WPMSFF at 0.5GHz for 16nm High-Performance and Low Power versions

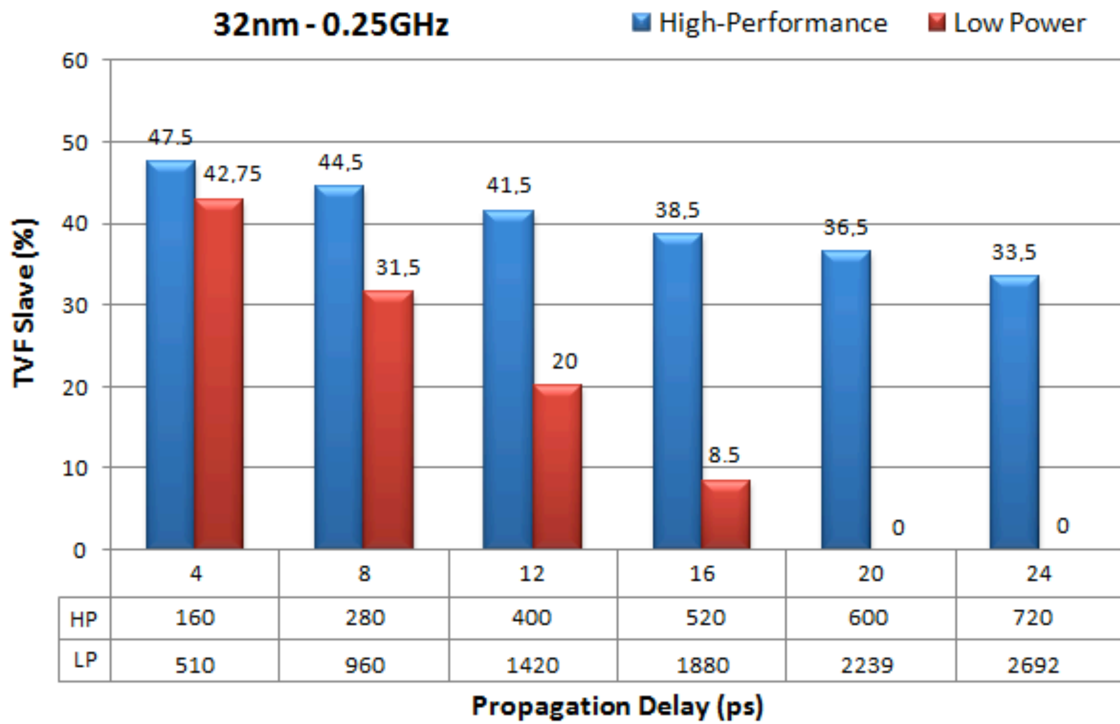


Figure 5.22: TVF for slave latch of WPMSFF at 0.25GHz for 32nm High-Performance and Low Power versions

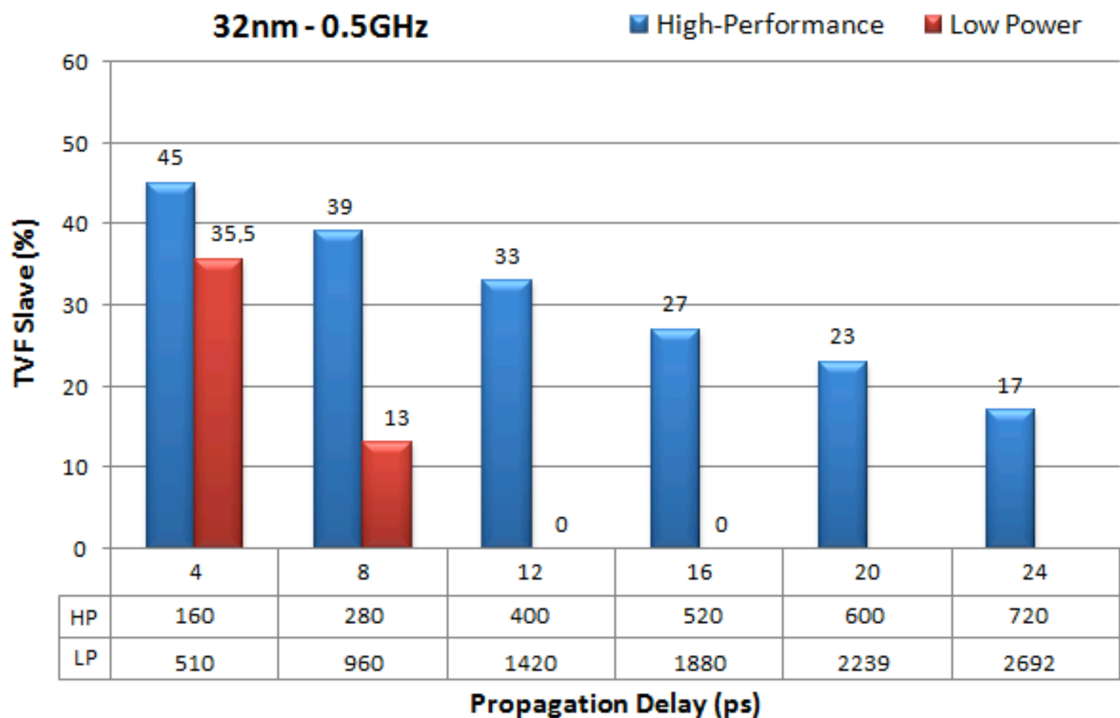


Figure 5.23: TVF for slave latch of WPMSFF at 0.5GHz for 32nm High-Performance and Low Power versions

6 EXPERIMENTAL RESULTS UNDER ENVIRONMENTAL VARIABILITY

This chapter evaluates, also through electrical simulations, the Timing Vulnerability Factor of the same three MS D Flip-Flops topologies in a pipeline design under environmental variability. The first set of results consists in determining the impact that supply voltage oscillations around 10% of nominal values causes on TVF of master and slaves latches. The second set of results shows the impact that temperature variation from 27ºC to 125ºC causes in TVF of master and slave latches of MS D Flip-Flops. Temperature and voltage variations are investigated for 32nm and 16nm technologies nodes in High-Performance version, highlighting the relation between TVF values with environmental variations and a good choice of technology and clock frequency when the circuit operates under radiation effects.

In this chapter, the methodology utilized in all experiments is also the same. However, in addition to considering the updates that diverse parameters suffer in each technology description file, environmental variability also causes variations on the propagation delay of a combinational logic. Furthermore, devices and interconnections may have performance and power consumption affected due to temperature and supply voltage variations. The subchapters of this chapter show the TVF results under environmental variability.

6.1 Voltage Variations

The power supply is usually associated with the system power consumption and supply voltage variations affect directly the propagation delays of logic gates. To obtain the best TVF for the slave latches, it is necessary to work with low supply voltage in order to increase the propagation delay of combinational logic. However, the supply voltage is not constant on a chip. The variations happen due to nonzero resistances in the network connections of power lines.

Tables 6.1 and 6.2 shows the propagation delay approximations for different supply voltages at 16nm and 32nm technology models, respectively. Note that, each combinational logic has a different propagation delay according to technology utilized and the supply voltage variations. These values were utilized in all experiments that involved voltage variations.

Table 6.1: Propagation delay approximations for different supply voltages at 16nm technology

Voltage (V)	*Propagation Delay (ps)*					
	4	*8*	*12*	*16*	*20*	*24*
0.61	170	310	460	600	700	840
0.65	150	270	390	510	590	710
0.70	130	230	330	430	500	600
0.75	120	200	290	370	440	520
0.79	110	190	260	340	400	480

Table 6.2: Propagation delay approximations for different supply voltages at 32nm technology

Voltage (V)	*Propagation Delay (ps)*					
	4	*8*	*12*	*16*	*20*	*24*
0.81	190	330	480	630	730	880
0.85	170	310	440	570	660	790
0.90	160	280	400	520	600	720
0.95	150	260	370	480	550	660
0.99	130	250	350	450	520	620

Voltage variations effects are independent of the technology model, the propagation delay of logical path or clock frequencies, i. e., a MS D Flip-Flops with lower supply voltages always obtain the biggest TVF value for the slave latch. However, the absolute value of each slave latch in different case-study circuits present variations on TVF according to the delay of the combinational logic that it is connected to, the clock frequency and delays.

6.1.1 Standard Master-Slave D Flip-Flop

Fig. 6.1 shows the TVF of slave latch for SMSFF at 16nm technology node in different clock frequencies under voltage variations. It is possible to see that at lower frequencies, the TVF value remains higher than 30%, mainly for pipeline designs with small propagation delay and low supply voltages. At 1GHz, with supply voltages lower than nominal value can reach to zero with combinational logic of 20 inverters.

Fig. 6.2 considers the same methodology utilized above, but analyzes the SMSFF at 32nm technology node. Voltage variation impact in TVF for small propagation delay is considered negligible when compared with nominal values. At 0.25GHz and 0.5GHz, a large propagation delay causes an increase in the TVF value if the voltage is bigger than the nominal value. On the other hand, for values lower than the nominal condition operation, the TVF decreases to 3% and 6%, respectively. Analyses at 2GHz were omitted because, in the majority of the pipeline designs, the MS D Flip-Flop does not operate in this frequency.

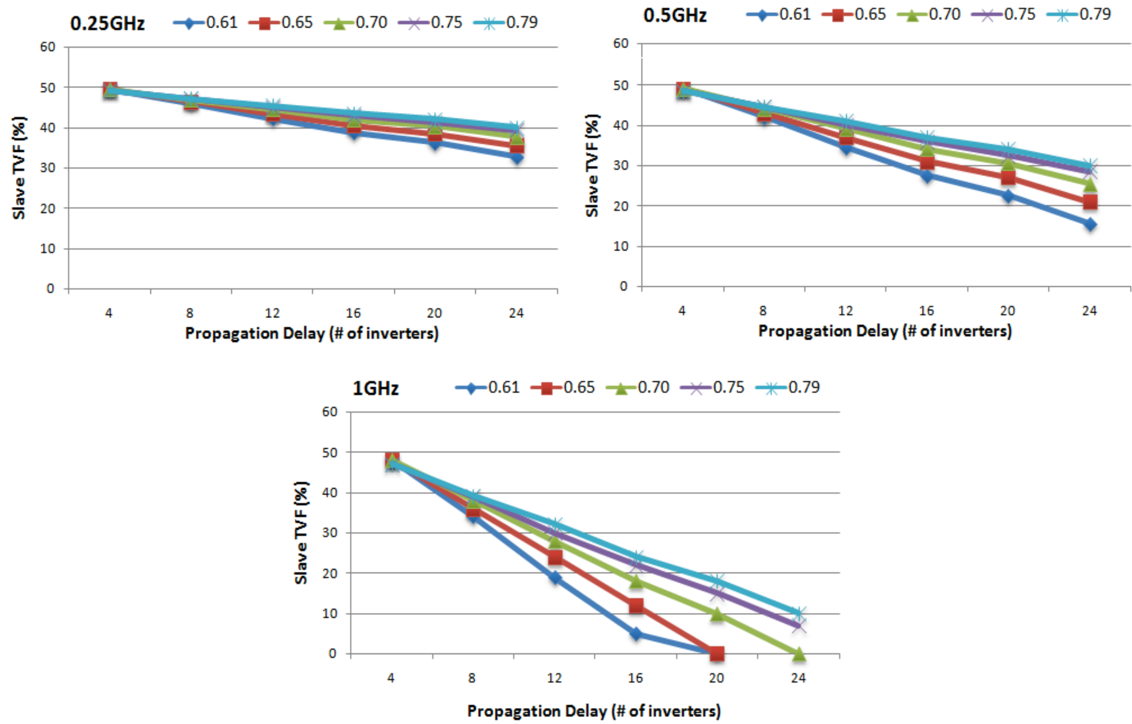


Figure 6.1: TVF of slave latch for SMSFF at 16nm technology node in different clock frequencies under voltage variations

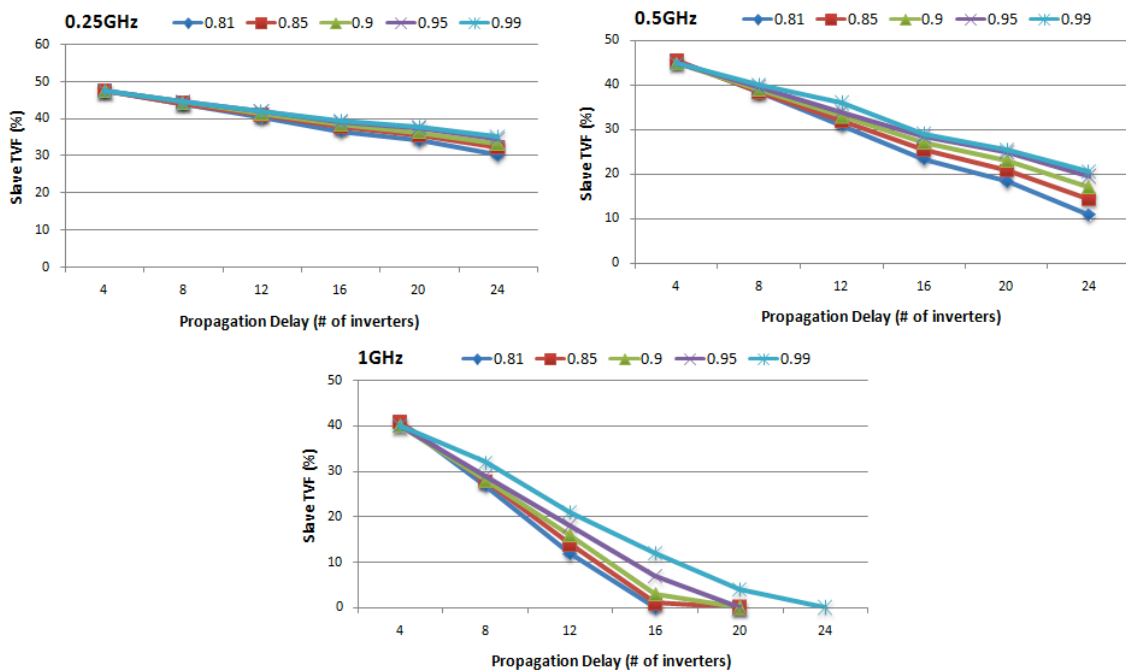


Figure 6.2: TVF of slave latch for SMSFF at 32nm technology node in different clock frequencies under voltage variations

6.1.2 Transmission Gate Master-Slave D Flip-Flop

Fig. 6.3 shows the TVF of a slave latch in a TGMSFF using a 16nm technology node under voltage variations. At 0.25GHz, propagation delays until 12 inverters do not represent a significant decrease in TVF values reaching a maximum reduction of 8.5%. But with a large combinational delay in the pipeline design it is possible to reach reduction until 20%. Moreover, voltage variations generate very similar TVF of slave latches mainly with combinational logic with 4 and 8 inverters. With the clock frequency increase, the voltage variations impact more the TVF values, making the circuit more robust to bit-flips. In addition, the TGMSFF topology also proved to be less sensitive to faults than the SMSFF one under voltage variations.

Fig. 6.4 considers the same methodology utilized above, but analyzes the TGMSFF at a 32nm technology node. As seen in the previous chapter, higher technology nodes generate lower TVF values due to the propagation delay of combinational logic. Supply voltage variations at 0.25GHz and 0.5GHz with large propagation delays impacts more significantly the TVF in relation to nominal values. TVF variations due to voltage oscillations are between 3-6% when the voltage is lower and between 2.5-5% when the voltage is higher than nominal values. At 1GHz, regardless of the supply voltage, all pipeline design can achieve TVF of slave latch equal to zero with 16 or 20 inverters.

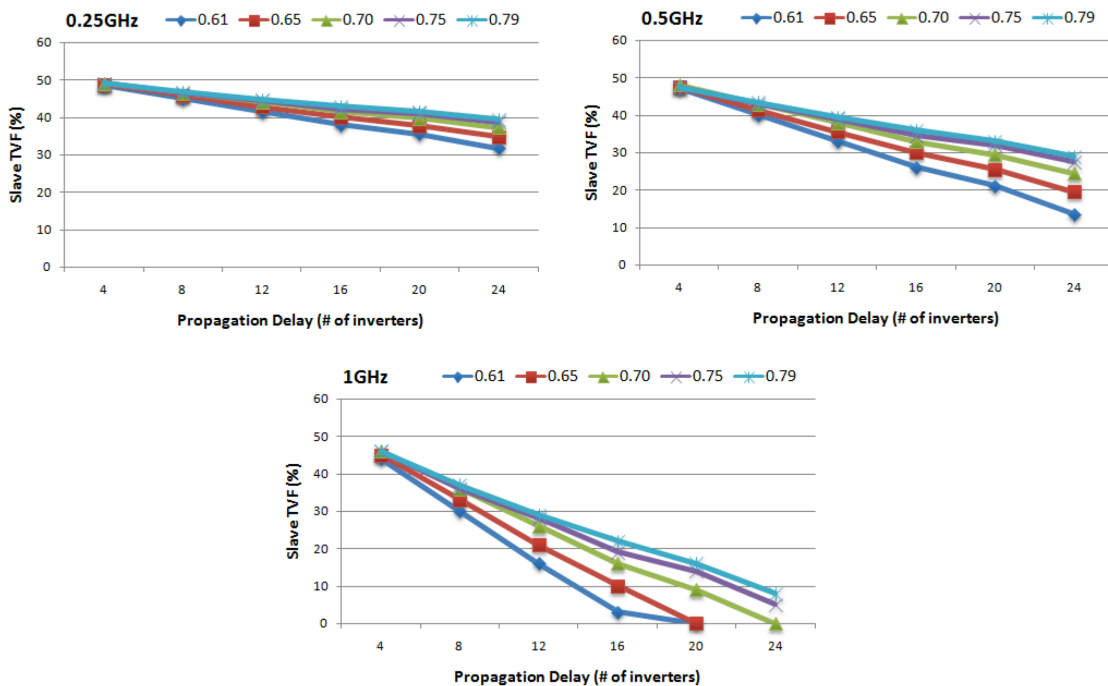


Figure 6.3: TVF of slave latch for TGMSFF at 16nm technology node in different clock frequencies under voltage variations

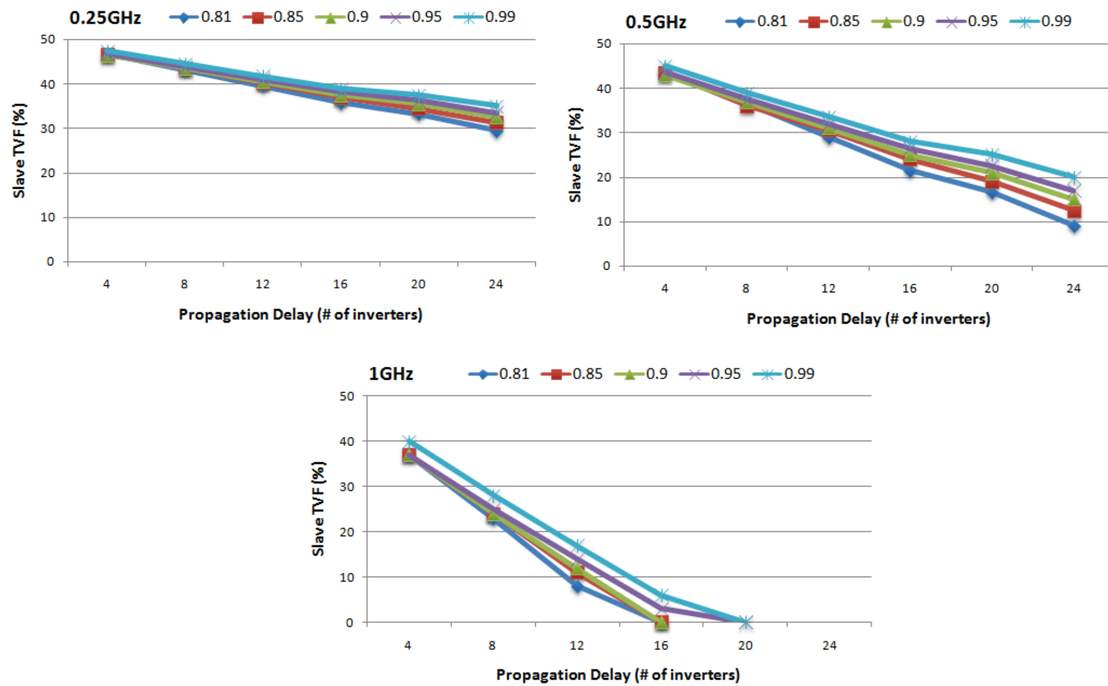


Figure 6.4: TVF of slave latch for TGMSFF at 32nm technology node in different clock frequencies under voltage variations

6.1.3 Write-Port Master-Slave D Flip-Flop

Finally, Fig. 6.5 and Fig. 6.6 presents the TVF of a slave latch for WPMSFF at 16nm and 32nm technology nodes under voltage variations, respectively. For 16nm technology nodes, when the supply voltage is equal to 0.61V, the TVF of a slave latch suffers an increase of around 13% compared with the TVF values found in nominal conditions for larger combinational logics. Also, for supply voltage equal to 0.65V, the different between the nominal TVF and TVF under variability is 6.75%. To supply voltage above the nominal voltage (0.7V), the decrease of TVF is not significant.

For 32nm technology node, at 0.25GHz the TVF values practically not change with different propagation delays and voltage variations. The maximum reduction on TVF with the higher propagation delay and the lower voltage supply is only 15.75%. When the supply voltage is equal to 0.81V, the TVF of a slave latch suffers an increase around 8.5% compared with the TVF values found in nominal conditions. The opposite not generates a significant decrease on TVF because when the supply voltage is equal to 0.99V, the TVF suffers only an increase of 1% compared with the nominal value.

According to the results, we conclude that the impact of voltage variations on TVF values is more significant in higher node technologies. We also conclude that the topology more affected due to voltage changes is the one of a WPMSFF in 32nm and 16nm technology nodes.

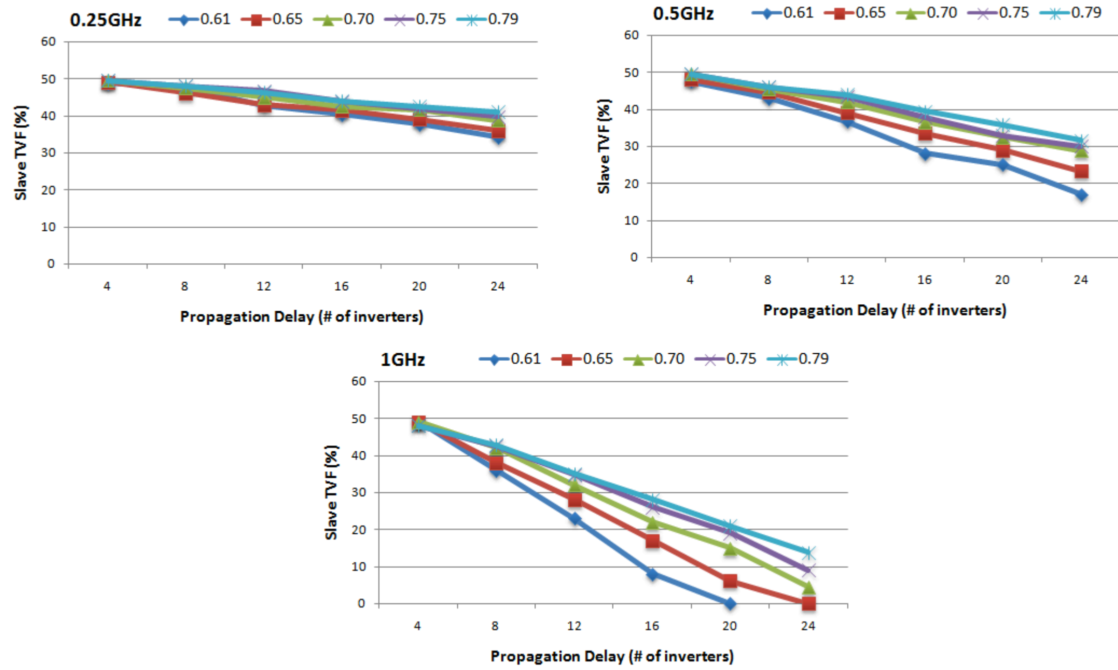


Figure 6.5: TVF of slave latch for WPMSFF at 16nm technology node in different clock frequencies under voltage variations

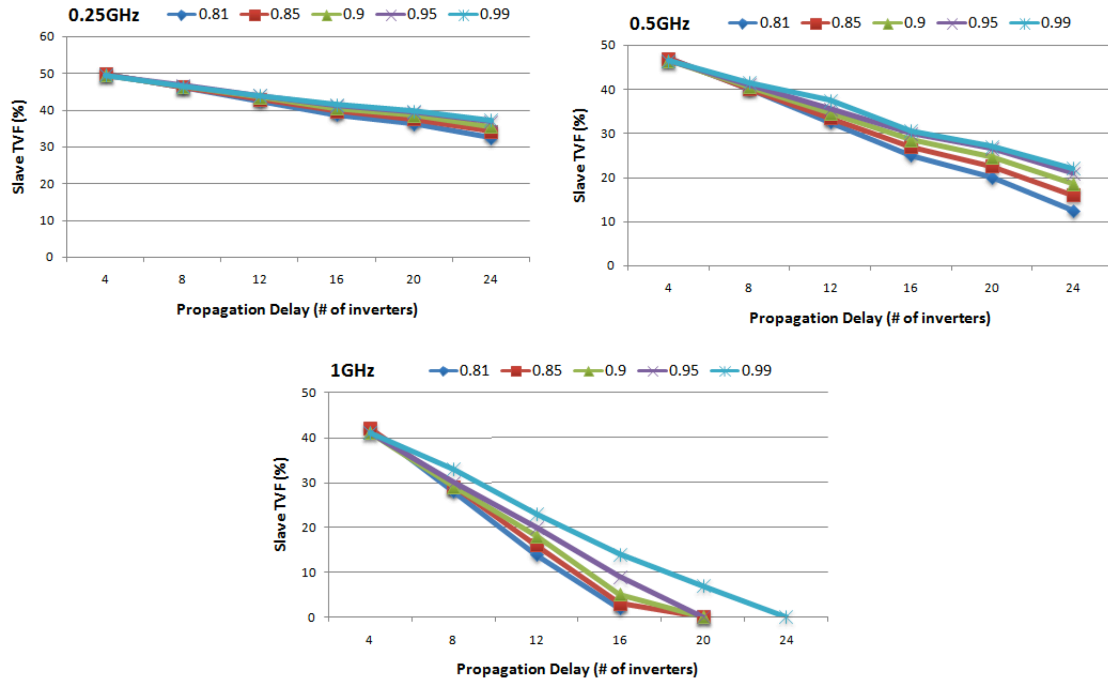


Figure 6.6: TVF of slave latch for WPMSFF at 32nm technology node in different clock frequencies under voltage variations

6.2 Temperature Variations

The performance of the devices and interconnections is directly related to the temperature. The temperature of the semiconductor junctions forming the transistors can significantly exceed the room temperature when the circuits are placed in real applications. The transistor drain current decreases when the temperature increases, increasing the delay of the logic gate and thereby, reducing system performance.

Tables 6.3 and 6.4 shows the propagation delay approximations for different temperatures at 16nm and 32nm technology models, respectively. Note that, each combinational logic has a different propagation delay according to the technology utilized and temperature variations. These values were utilized in all experiments that involved temperature variations.

Table 6.3: Propagation delay approximations for different temperatures at 16nm technology

Temperature (ºC)	*Propagation Delay (ps)*					
	4	*8*	*12*	*16*	*20*	*24*
27	130	230	330	430	500	600
50	140	260	370	480	560	680
75	160	290	420	550	640	770
100	180	330	470	620	720	870
125	200	360	530	690	810	980

Table 6.4: Propagation delay approximations for different temperatures at 32nm technology

Temperature (ºC)	*Propagation Delay (ps)*					
	4	*8*	*12*	*16*	*20*	*24*
27	170	290	410	530	610	730
50	180	310	440	580	670	810
75	190	330	490	640	750	900
100	210	380	550	720	840	1010
125	220	420	610	800	940	1140

Temperature variations effects are independent of the technology model, the propagation delay of a logical path or clock frequencies, i. e., a MS D Flip-Flops with lower temperatures always obtain the biggest TVF value for the slave latch. However, the absolute value of each slave latch in different case-study circuits present variations on TVF according to the delay of combinational logic that it is connected to, the clock frequency and delays.

6.2.1 Standard Master-Slave D Flip-Flop

Fig. 6.7 shows the TVF of a slave latch for SMSFF at a 16nm technology node in different clock frequencies under temperature variations. At 0.25GHz, the TVF value remains higher than 35% for all cases of propagation delays and range of temperature. Lower frequency contributes little to become a SMSFF less sensible to bit-flips. On the other hand, when the same circuit operates at 0.5GHz, the TVF of a slave latch can achieve a reduction greater than 30% of initial values with 16 inverters as combinational logic and temperature equal to 75ºC. In this technology, the maximum reduction that TVF of slave latch can obtain is equal to 38% with 24 inverters and 125ºC.

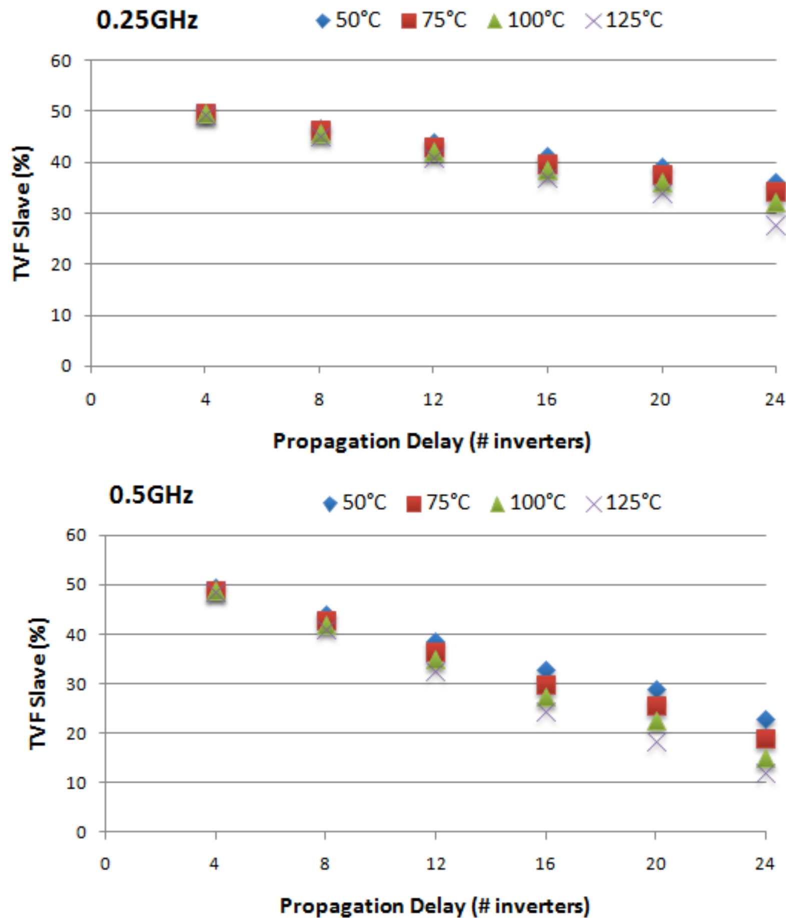


Figure 6.7: TVF of slave latch for SMSFF at 16nm technology node in higher clock frequencies under temperature variations

Tab. 6.5 shows the results for 16nm technology at 1GHz. It is possible to see that with 24 inverters as combinational logic, the TVF of master latches can be reduced considerably. With 24 inverters and temperature equal to 125ºC, the total TVF of a SMSFF is equal to 19% in 16nm technology. Good values of total TVF were already been achieved with 16 inverters in the combinational logic. Analyses at 2GHz were omitted because the TGMSFF only operates with propagation delays equal to 4 or 8 inverters.

Table 6.5: TVF for the master and slave latches of SMSFF at 1GHz in 16nm technology

# inverters	*Slave TVF (%)*				*Master TVF (%)*			
	50ºC	*75ºC*	*100ºC*	*125ºC*	*50ºC*	*75ºC*	*100ºC*	*125ºC*
4	49	48.5	48	47	50	50	50	50
8	37	35	33	31	50	50	50	50
12	26	22	19	14	50	50	50	50
16	15	9	4	0	50	50	50	41
20	7	0	0	0	50	50	38	29
24	0	0	0	0	41	32	23	19

In a 32nm technology node, the SMSFF is less vulnerable to radiation effects as shown in Fig. 6.8. At 0.25GHz, the difference of reduction between combinational logic equal to 4 inverters and 24 inverters is equal to 20% for TVF of a slave latch. At 0.5GHz, the TVF of a slave latch is more robust. With 20 inverters, independent of the temperature analyzed, the TVF already obtain values below 22.5%. With a higher temperature and propagation delay, the TVF almost reaches a zero (5.5%).

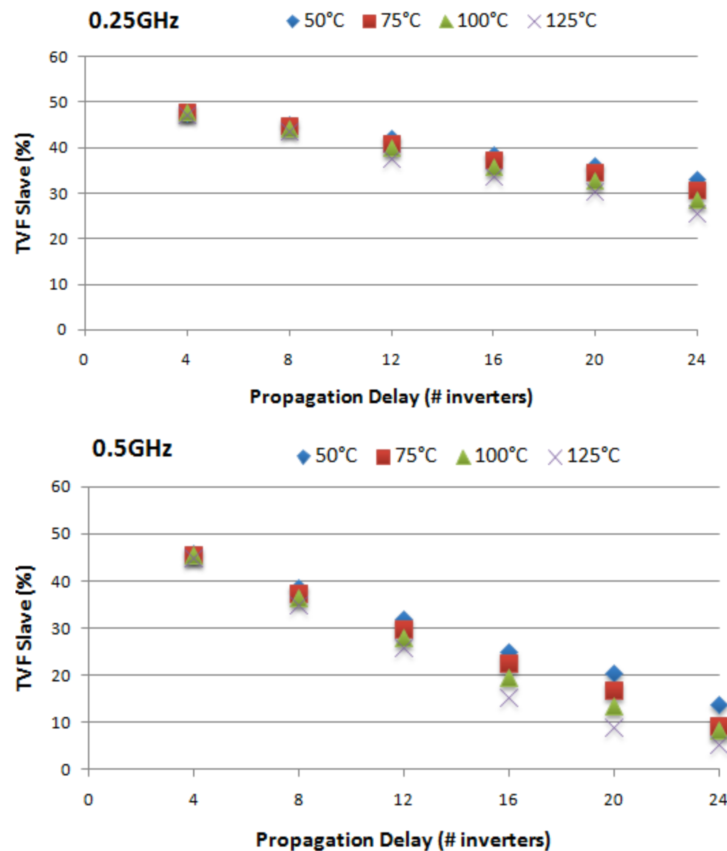


Figure 6.8: TVF of slave latch for SMSFF at 32nm technology node in higher clock frequencies under temperature variations

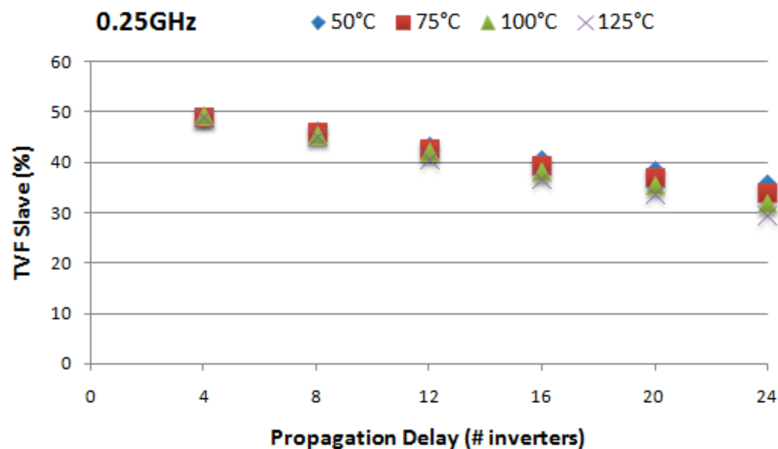
Tab. 6.6 shows the results for a 32nm technology at 1GHz. It is possible to see that in many cases, the TVF of master latches can be reduced significantly. With 24 inverters and temperature equal to 75ºC, the total TVF of a TGMSFF is equal to 17.5%. The gaps in the table mean that the circuit does not operate under those conditions. Analyses at 2GHz were omitted because the TGMSFF only operates with propagation delays equal to 4 or 8 inverters.

Table 6.6: TVF for the master and slave latches of SMSFF at 1GHz in 32nm technology

# inverters	*Slave TVF (%)*				*Master TVF (%)*			
	50ºC	*75ºC*	*100ºC*	*125ºC*	*50ºC*	*75ºC*	*100ºC*	*125ºC*
4	40	41	41	40	50	50	50	50
8	27	25	23	21	50	50	50	50
12	14	10	6	0	50	50	50	44
16	0	0	0	0	46	39	34	27
20	0	0	0	-	37	31	22.5	-
24	0	0	-	-	25	17.5	-	-

6.2.2 Transmission Gate Master-Slave D Flip-Flop

Fig. 6.9 shows the TVF of a slave latch for TGMSFF at 16nm technology node in different clock frequencies under temperature variations. At 0.25GHz, the TVF value remains higher than 30% for all cases of propagation delays and range of temperatures, and it not contributes significantly to become a TGMSFF more robust to bit-flips. On the other hand, when the same circuit operates at 0.5GHz, the TVF of a slave latch can already be half the value than with 16 inverters. The better values of TVF are obtained with higher temperatures and propagation delays.



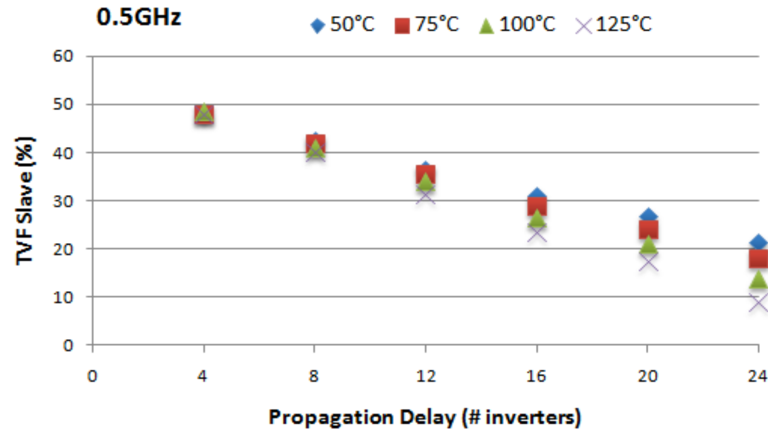


Figure 6.9: TVF of slave latch for TGMSFF at 16nm technology node in higher clock frequencies under temperature variations

Tab. 6.7 shows the results for a 16nm technology at 1GHz. It is possible to see that with 24 inverters as combinational logic, the TVF of master latches can be reduced considerably. With 24 inverters and temperature equal to 125ºC, the total TVF of a TGMSFF is equal to 16% in 16nm technology. Analyses at 2GHz were omitted because the TGMSFF only operates with propagation delays equal to 4 or 8 inverters.

Table 6.7: TVF for the master and slave latches of TGMSFF at 1GHz in 16nm technology

# inverters	*Slave TVF (%)*				*Master TVF (%)*			
	50ºC	*75ºC*	*100ºC*	*125ºC*	*50ºC*	*75ºC*	*100ºC*	*125ºC*
4	46	46	47	46	50	50	50	50
8	35	34	32	30	50	50	50	50
12	23	21	18	12	50	50	50	50
16	12	7	2	0	50	50	50	43
20	3	0	0	0	50	45	39	31
24	0	0	0	0	50	33	24	16

Fig. 6.10 considers the same methodology utilized above, but analyzes the TGMSFF at a 32nm technology node. It is possible to see that TVF of slave latches for 32nm technology present better values, making the circuit less vulnerable to radiation effects. At 0.25GHz, with high temperature and very large propagation delay, the TVF of slave latch can reach a reduction of 25%. For smaller propagation delays (4 and 8 inverters), the TVF can reduce a maximum of 8% for the higher temperature. At 0.5GHz, the TVF of a slave latch is more robust. With 20 inverters, independent of temperature analyzed, the TVF already obtain values below 20%. With higher temperature and propagation delay the TVF reaches a zero, and the TVF of a master latch suffers a reduction of 4.5%.

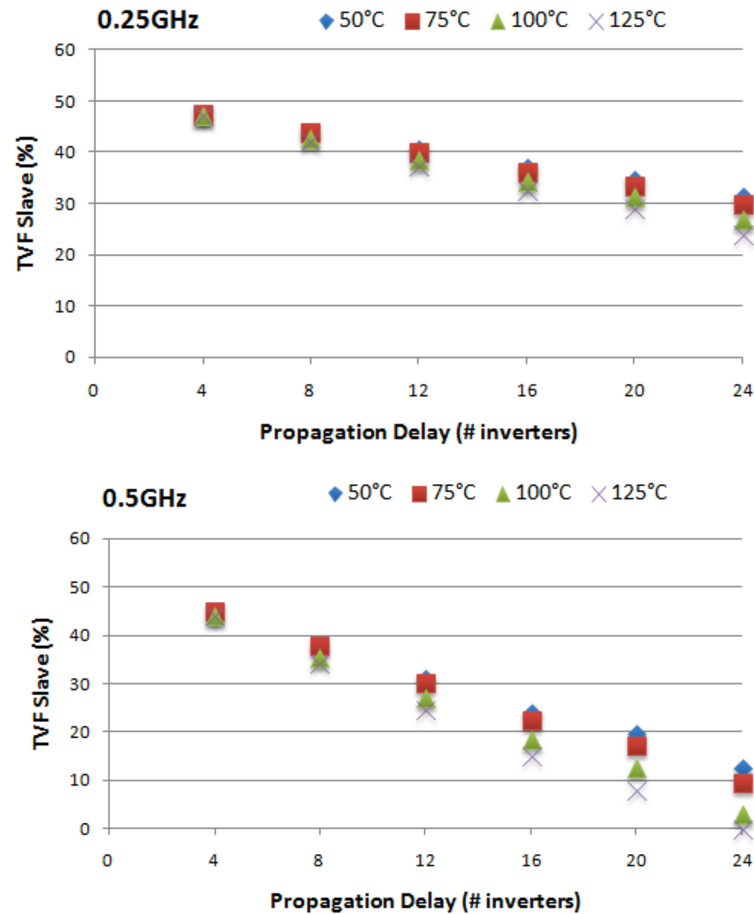


Figure 6.10: TVF of slave latch for TGMSFF at 32nm technology node in higher clock frequencies under temperature variations

Tab. 6.8 shows the results for 32nm technology at 1GHz. In many cases, the TVF of master latches can be reduced significantly. With 24 inverters and temperature equal to 75ºC, the total TVF of a TGMSFF is equal to 15%. This represents the more robust to radiation effects case. Analyzes at 2GHz were omitted because the TGMSFF only operates with propagation delays equal to 4 or 8 inverters.

Table 6.8: TVF for the master and slave latches of TGMSFF at 1GHz in 32nm technology

# inverters	*Slave TVF (%)*				*Master TVF (%)*			
	50ºC	*75ºC*	*100ºC*	*125ºC*	*50ºC*	*75ºC*	*100ºC*	*125ºC*
4	38	40	38	38	50	50	50	50
8	25	26	21	18	50	50	50	50
12	12	10	4	0	50	50	50	50
16	2	0	0	0	50	47	33	25
20	0	0	0	0	36	30	21	11
24	0	0	-	-	23	15	-	-

6.2.3 Write-Port Master-Slave D Flip-Flop

Fig. 6.11 shows the TVF of a slave latch for WPMSFF at a 16nm technology node in different clock frequencies under temperature variations. At 0.25GHz, the TVF value does not suffer significant variations in relation to SMSFF and TGMSFF topologies. When the same circuit operates at 0.5GHz, the TVF of a slave latch can already be half the value than with 16 inverters, but with small propagation delays, the TVF reduces only 9.5% for the higher temperature. Although the difference is small between the topologies, WPMSFF presents the worst case of TVF under temperature variations.

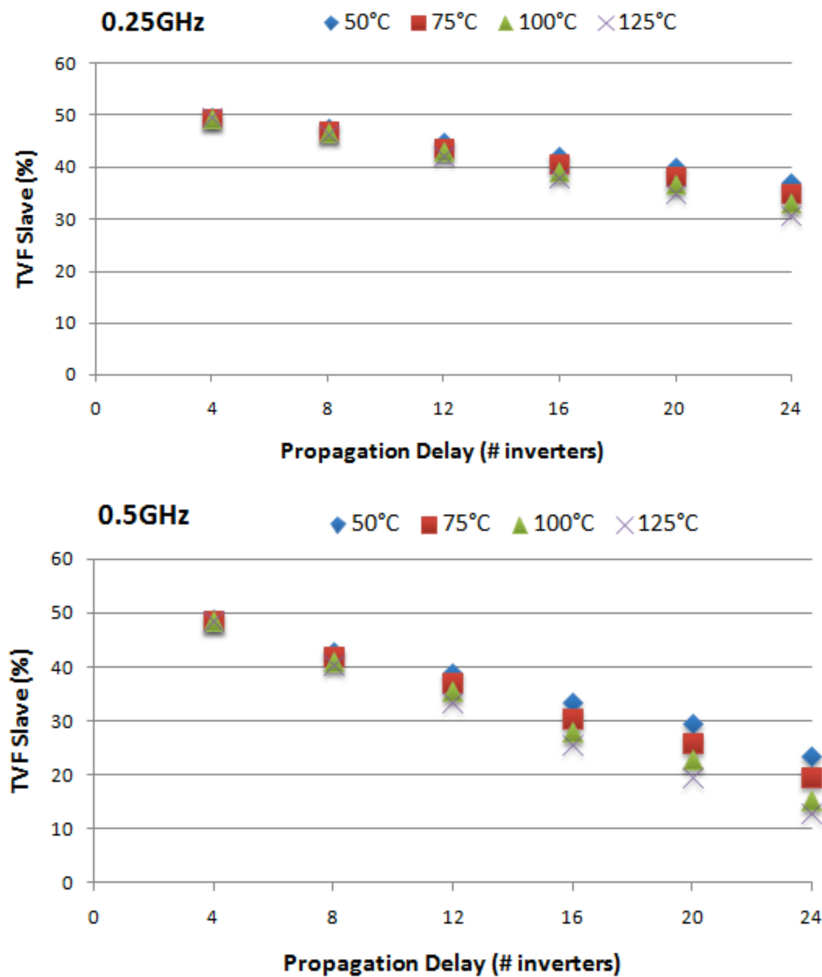


Figure 6.11: TVF of slave latch for WPMSFF at 16nm technology node in higher clock frequencies under temperature variations

Tab. 6.9 shows the results for a 32nm technology at 1GHz. It is possible to see that with only 20 inverters as combinational logic and 100ºC that the TVF of slave latches can be equal to zero. With 24 inverters and temperature equal to 125ºC, the total TVF of a WPMSFF is equal to 22% in a 16nm technology. Analyses at 2GHz were omitted because the TGMSFF only operates with propagation delays equal to 4 inverters.

Table 6.9: TVF for the master and slave latches of WPMSFF at 1GHz in 16nm technology

# inverters	*Slave TVF (%)*				*Master TVF (%)*			
	50ºC	*75ºC*	*100ºC*	*125ºC*	*50ºC*	*75ºC*	*100ºC*	*125ºC*
4	48	47.5	47	46	50	50	50	50
8	38	36	34	33	50	50	50	50
12	27	23	21	13	50	50	50	50
16	16	11	5	2	50	50	50	50
20	8	2	0	0	50	50	40	33
24	0	0	0	0	42	34	27	22

In a 32nm technology node, the WPMSFF is more vulnerable to radiation effects as shown Fig. 6.12. At 0.25GHz, as explained previously, TVF of a slave latch does not suffers variations with significant differences (±2%) in relation to results obtained for a SMSFF and a TGMSFF, as explained previously. At 0.5GHz, with a large propagation delay, the TVF of a slave latch can suffer variations of 36% or more from initial values. The better values of TVF are obtained with higher temperatures and propagation delays.

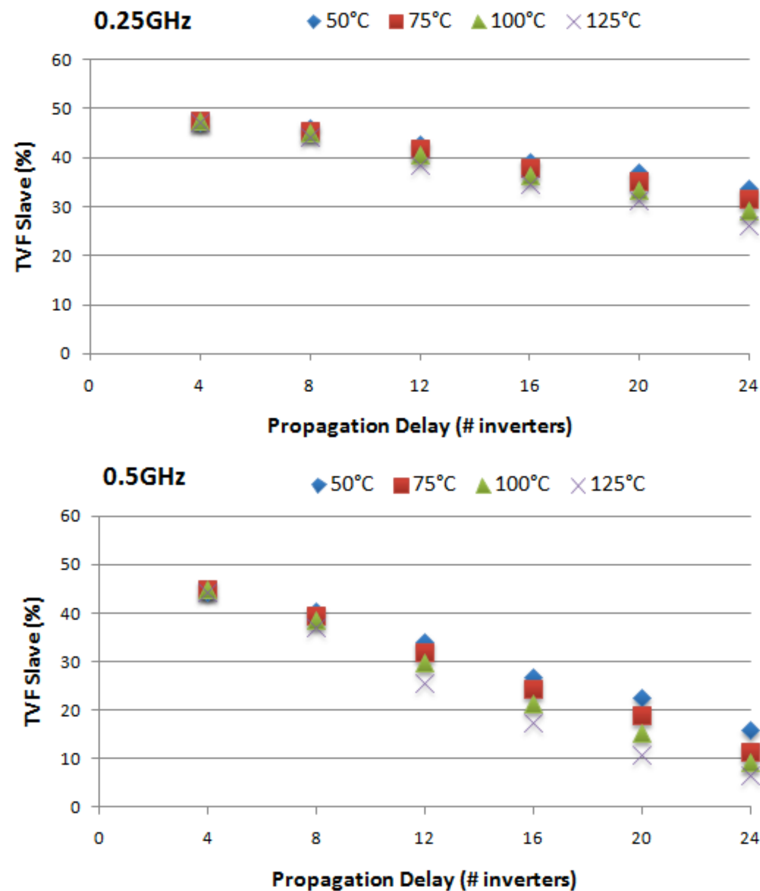


Figure 6.12: TVF of slave latch for WPMSFF at 32nm technology node in higher clock frequencies under temperature variations

Tab. 6.10 shows the results for a 32nm technology at 1GHz. With 18 inverters and 75ºC, the TVF of master latches can be reduced significantly. With 24 inverters and temperature equal to 75ºC, the total TVF of WPMSFF is equal to 24%. Analyzes at 2GHz were omitted because the TGMSFF only operates with propagation delays equal to 4 inverters.

Table 6.10: TVF for the master and slave latches of WPMSFF at 1GHz in 32nm technology

# inverters	*Slave TVF (%)*				*Master TVF (%)*			
	50ºC	*75ºC*	*100ºC*	*125ºC*	*50ºC*	*75ºC*	*100ºC*	*125ºC*
4	40	39.5	39	38	50	50	50	50
8	29	27	25	22	50	50	50	50
12	18	14	10	7	50	50	50	50
16	4	0	0	0	50	46	41	38
20	0	0	0	0	39	34	32	24.5
24	0	0	-	-	29	24	-	-

7 CONCLUSIONS

In this work, three different MS D Flip-Flop topologies in pipeline stages were considered to evaluate the Timing Vulnerability Factor under different operating conditions. The first set of results consisted in determining the dependency between SEU occurrences in a flip-flop with its clock frequency besides analyzing the fault propagation to the next stage through a combinational logic with different propagation delays. The second set of results shows the impact that different technological nodes, including High-Performance and Low Power version, cause on TVF values. Finally, the TVF of master and slave latches of MS D Flip-Flop topologies was studied under environmental variability as supply voltage and temperature variations. When analyzing the results of this work some important conclusions can be highlighted.

Master and slave latches have different TVF values, and all results indicate that master latches are more vulnerable to soft errors than slave latches. Thus, it is more important to develop master latches more robust to bit-flips than slave latches because the TVF of the slave latch can be easily reduced due to the combinational path delay. If a circuit must be redesigned to improve reliability, the master latches must incorporate techniques to provide a radiation hardened design, as the inclusion of redundant transistors, and the logical paths must have the minimal possible slack.

The dependency between the SEU occurrences with the clock frequency is significant. According to the analyzed technologies, we conclude that the circuit must operate at the highest possible frequency according to the critical path delays in order to obtain the lowest TVF values for the slave latches and a significant decrease on TVF for the master latches. The results also show that reducing frequency to reduce power for instance is a bad choice for reliability as it may increase the TVF for the slave latches.

Results have shown that each slave latch presents a different TVF according to the combination path delay connected to. The shorter combinational logic paths are more sensitive than larger combinational logic paths. The main reason for this is because a bit-flip generated in the first MS D Flip-Flops still has to arrive at least till the setup time before the clock edge at the second MS D flip-flop. For long delays, the bit-flip does not arrives in time to be latched at the next stage and consequently it does not become a soft error at the next stage of the pipeline.

All results have shown that the impact of frequency, path delays and slack gets slightly more intense with more advanced technology. For longer combinational paths, the TVF can be reduced even more with technology scaling down. In applications related to low power consumption, the combinational logic presents very large propagation delays in the majority of cases. The positive side is that TVF of master and slave latches decrease significantly making the MSFF less sensitive to bit-flips but consequently the pipeline designs only operates at lower frequencies.

Supply voltage variations affect directly the propagation delays of logic gates. In this way, higher supply voltages reduce the propagation delay, and the MS D Flip-Flops becomes faster. According to the range of power supply analyzed, we conclude that the MS D Flip-Flops that works with lower supply voltages obtain the largest TVF values for the slave latches, and so, the circuit is more susceptible to bit-flips. To obtain the best TVF for the slave latches, it is necessary to work with lower supply voltages in order to increase the propagation delay of the combinational logic.

The drain current of the transistor decreases when the circuits work at higher temperatures, and consequently it increases the propagation delay of the logic gates. For the range of temperatures analyzed, this behavior was confirmed. We concluded that the MS D Flip-Flops that work at highest possible temperatures guarantees the correct circuit operation, presents the best TVF values for the slave latches and they contribute to a significant decrease on TVF of master latches. So, at lower temperatures the MS D Flip-Flops are more sensitive to radiation effects.

Three MS D Flip-Flops topologies were analyzed under different operating conditions. We conclude that the most robust topology presented here was the Transmission Gate Master-Slave D Flip-Flop because the best TVF values of slave latches were obtained with this topology. Moreover, TGMSFF also gets to decrease many TVF values of master latches. According to the results, the topology more susceptible to bit-flip is the Write-Port Master-Slave D Flip-Flop. The reasons that led a topology to be better than the other one are not included in the scope of this work.

In summary, designers can take into account different propagation delays and clock frequencies according to the process technology used to reduce the TVF of the flip-flops. In some designs, the clock frequency has been stagnant in order to the decrease the power consumption. In this case, the increase of the propagation delay between the sequential circuits, complying with the maximum critical path delay allowed, is a good way to obtain a smaller TVF and to obtain a greater tolerance to radiation effects.

It is very common that commercial circuits do not operate exactly on nominal conditions. During the operation time, many oscillations may occur in temperature and supply voltage. For this reason, designers also need to take into account environmental variability to get flip-flops more robust to bit-flips. All the information of TVF values of each MS D Flip-Flop can be easily integrated into design tools to help identifying the most vulnerable flip-flops in circuits before mitigating or replacing the flip-flops by radiation hardened ones.

7.1 Future Works

As future works, we intend to expand the Timing Vulnerability analysis in MS D Flip-Flops to increase the precision of current research. So, we would like to check how much energetic particles with different LETs (Linear Energy Transfer) impact the TVF values of sequential circuits considering different frequencies, propagation delays and nanotechnologies, and also environmental variability. So far, we have analyzed the simple topologies of MS D Flip-Flops without considering the means that the circuit is inserted. We would like to analyze also how the setup time slack of the logical paths can impact the TVF values of MS D Flip-Flops.

7.2 Scientific Production

The papers listed on Tab. 7.1 were partial results of the studies about radiation effects on integrated circuits. The first two papers are directly related to the dissertation theme and they analyzes the impact of frequency, different combinational logic path and technological nodes in the TVF of a Standard Master-Slave D Flip-Flop. The last paper was made in partnership with FURG University.

Table 7.1: List of publications related to radiation effects on integrated circuits

Title	*Publication*	*Year*
Analyzing Impact of Frequency and Diverse Path Delays in the Timing Vulnerability Factor of Master-Slave D Flip-Flop	IEEE ISVLSI	2015
Análise do Timing Vulnerability Factor em Flip-Flop D Mestre-Escravo em Nanotecnologias	IBERCHIP	2016
NFAS-tool: Avaliação da Confiabilidade de Células Combinacionais sob Falhas de Radiação do tipo SET	IBERCHIP	2016

The papers listed on Tab. 7.2 were partial results of the studies about variability in FinFET devices also realized during the master course.

Table 7.2: List of publications related to variability in FinFET devices

Title	*Publication*	*Year*
An analysis of FinFET devices under environment and process variability	SIM	2014
Predictive Evaluation of electrical characteristics of sub-22nm FinFET Technologies under device Geometry Variations	Microelectronics Reliability (Journal)	2014
Impactof Gate Workfunction Fluctuationon FinFET Standard Cells	IEEE ICECS	2014
Evaluating the Impact of Environment and Physical Variability on the I_{ON} current of 20nm FinFET Devices	PATMOS	2014
Análise do Impacto da Variabilidade Física nas Correntes I_{ON} e I_{OFF} de dispositivos FinFET sub-20nm	IBERCHIP	2015
Sub-22nm FinFETs: An Evaluation of the Physical Variability Impact	SIM	2015
Impact of PVT Variability on 20nm FinFET Standard Cells	Microelectronics Reliability (Journal)	2015
Process Variability in FinFET Standard Cells with Different Transistor Sizing Techniques	IEEE ICECS	2015
Efeitos da Variabilidade PVT em células FinFET com diferentes dimensionamentos	IBERCHIP	2016
FinFET Cells with Different Transistor Sizing Techniques against PVT Variations	IEEE ISCAS	2016

REFERENCES

ALEXANDRESCU, D., ANGHEL, L.; NICOLAIDIS, M., New Methods for Evaluating the Impact of Single Event Transients in VDSM ICs. In: IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems Workshop, DFT, 17, 2002. **Proceedings...** [S.I.]: IEEE Computer Society, 2002. p. 99-107.

ALIOTO, M., General Strategies to design nanometer flip-flops in the energy-delay space. In: IEEE Transactions on Circuits and Systems, vol. 57, no. 7, pp. 1583-1596, 2010.

ALIOTO, M., Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: part I - methodology and design strategies. In: IEEE Transactions on Very Large Integration (VLSI) Systems, vol. 19, no. 5, pp. 725-736, 2010.

ALIOTO, M.; CONSOLI, E.; PALUMBRO, G., Comparative Analysis of the Robustness of Master-Slave Flip-Flop against Variations. In: IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2015. **Proceedings...** [S.I.]: IEEE, 2015.

ANGHEL, L.; NICOLAIDIS, M., Defects Tolerant Logic Gates for unreliable Future Nanotechnologies. In: Lecture Notes in Computer Science, v. 4507, Berlin, pp. 422-429, 2007a.

ANGHEL, L., REBAUDENGO, M., REORDA, M. S., VIOLANTE, M., Multi-level Fault Effects Evaluation. In: VELAZCO, R.; FOUILLAT, P.; REIS, R. (Ed.). Radiations Effects on Embedded Systems. [S.l.]: Springer, p.69 – 88, 2007b.

BARTH, J., Applying Computer Simulation Tools to Radiation Effects Problems. In: IEEE Nuclear Space Radiation Effects Conference Short Course, NSREC, 1997. **Proceedings…** [S.I.] : IEEE Computer Society, 1997, p. 1-83.

BAUMANN, R. C., SMITH, E. Neutron-induced boron fission as a major source of soft errors in deep submicron SRAM devices. In: IEEE International Reliability Physics Symposium, 38, 2000. **Proceedings…** [S.I]: IEEE Computer Society, 2000.

BAUMANN, R. C., The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction. In: International Electron Devices Meeting (IEDM '02), 2002. **Proceedings…** [S.I]: IEEE Computer Society, 2002, p. 329-332.

BAUMANN, R. C., Radiation-induced soft errors in advanced semiconductor technologies. In: IEEE Transaction on Device and Materials Reliability, 2005. **Proceedings…** [S.I]: IEEE, 2005, p. 305-316.

BENEDETTO, J., EATON, P., AVERY, K., MAVIS, D., GADLAGE, M., TURFLINGER, T., DODD, P. E. ; VIZKELETHYD, G., Heavy ion-induced digital single-event transients in deep submicron processes. In: IEEE Transaction Nuclear Science., vol. 51, no. 6, pp. 3480–3485, Dec. 2004.

BORKAR, S. et al., Parameter Variations and Impact on Circuits and Microarchitecture. In: Design Automation Conference, DAC, 40, 2003. **Proceedings…** [S.I]: ACM/IEEE, 2003, p. 338-342.

BORKAR, S., Design perspectives on 22nm CMOS and beyond. In: Design Automation Conference, DAC, 46, 2009. **Proceedings…** [S.I]: ACM/IEEE, 2009, p. 93-94.

BOUDENOT, J.-C., Radiation space Environment. In: VELAZCO, R.; FOUILLAT, P.; REIS, R. (Ed.). Radiations Effects on Embedded Systems. [S.l.]: Springer, p. 1–9, 2007.

BRAMNIK, A.; SHERBAN, A.; SEIFERT, N., Timing Vulnerabiblity Factors of Sequential Elements in Moderns Microprocessors. In: IEEE 19th International On-line Test Symposium (IOLTS) Conference, 2013. **Proceedings…** [S.I]: IEEE, 2013, pp. 55-60, 2013.

CRAIN, S. et. al., Analog and Digital Single-event Effects Experiments in Space. In: IEEE Transactions in Nuclear Science, New York, v. 48, n. 6, Dec. 2001.

DODD, P. E., MASSENGILL, L. W., Basic Mechanism and Modeling of Single-Event Upset in Digital Microelectronics. In: IEEE Transaction on Nuclear Science, vol. 50, pp. 583-602, Jun. 2003.

DODD, P. E., SHANEYFEKT, M. R., FELIX, J. A., SCHWANK, J. R., Production and Propagation of Single-Event Transients in high speed digital logic ICs. In: IEEE Transactions Nuclear. Science, vol. 49, pp. 3038-3944, 2004.

DODD, P., Physics-Based Simulation of Single-Event Effects. In: IEEE Transactions On Device And Materials Reliability", vol. 5, n. 3, pp.343-457, Sept. 2005.

DUPONT, E., NICOLAIDIS, M. ROHR, P., Embedded robustness IPs for transient-error-free ICs. In: IEEE Design & Test of Computers, New York, v. 19, n. 3, pp. 54-58, 2002.

FERLET-CAVROIS, V. et al., Statistical Analysis of the Charge Collected in SOI and Bulk Devices Under Heavy Ion and Proton Irradiation - Implications for Digital SETs. In: IEEE Transactions on Nuclear Science, Vol 53, n. 6, p. 3242-3252, Dec. 2006.

GADLAGE, M. J.; SCHRIMPF, R. D.; BENEDETTO, J. M.; EATON, P. H.; MAVIS, D. G.; SIBLEY, M.; AVERY, K.; TURFLINGER, T. L., Single Event Transient Pulsewidths in Digital Microcircuits. IEEE Transactions on Nuclear Science, vol. 51, No. 6, 2004.

GIACOMOTTO, C.; NEDOVIC, N.; OKLOBDZIJA, V., The effect of the system specification on the optimal selection of clocked storage elements. IEEE Journal Solid-State Circuits, vol. 42, no. 6, p. 1392-1404, 2007.

GSS – Gold Standard Simulations Ltd. Case Study: Statistical Variability in an Example 22nm FinFET. 2010. Available in: http://www.goldstandardsimulations.com/GSS_22nm_FinFET_case_study.pdf

HEIJMEN, T., Soft-Error Vulnerability of sub-100nm Flip-Flops. In: 14th IEEE Internacional On-line Test Symposium (IOLTS'08) Conference, p. 247-252, Jul. 2008.

HO, C.-W.; RUEHLI, A.; BRENNAN, P., The modified nodal approach to network analysis. In: IEEE Transactions on Circuits and Systems, [S.l.], v.22, n.6, p.504 – 509, jun. 1975.

HUBERT, G.; ARTOLA, L., Single-event transient modeling in a 65nm bulk CMOS technology based-on multi-physical approach and electrical simulations. IEEE Transactions Nuclear Science, 60 (6), p. 4421-4429, 2013.

ISSCC. IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE. Available in: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6487631. Access: May 2015.

ITRS. THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS. Available in: http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf, 2011. Access: Aug. 2015.

JAHINUZZAMAN, S. M., RENNIE, D. J., SACHDEV, M., A soft error tolerant 10T SRAM bit-cell with differential read capability. In: IEEE Transactions Nuclear Science, vol. 56, vol. 6, p .3768-3773, 2009.

KASTENSMIDT, F. L.; CARRO, L.; REIS, R., **Fault-tolerance Techniques for SRAM-based FPGAs**. [S.I.] : Springer, 2006.

KASTENSMIDT, F. L., SEE Mitigation Strategies for Digital Circuit Design Applicable to ASIC and FPGAs. In: Hugh Barnaby. (Org.). IEEE NSREC Short Course. 1ed. Los Alamos: IEEE, p. 1-75, 2007.

KING, T.-J., FinFETs for Nanoscale CMOS Digital Integrated Circuits. In: International Conference on Computer-Aided Design, 2005. **Proceedings…** [S.I]: IEEE, 2005, p. 207–210.

KUMAR, V. R. et al., Submicron 70nm CMOS Logic Design with FinFETs. International Journal of Engineering Science and Technology, v.2, n.9, p. 4751-4758, 2010.

LEAVY, J., HOFFMANN, L.F., SHOVAN, R.W., JOHNSON, M.T., Upset due to a Single Particle Caused Propagated Transient in a Bulk CMOS Microprocessor. In: IEEE Transactions on Nuclear Science, New York, v. 38, n. 6, p. 1493-1499, Dec. 1991.

LIDEN, P., DAHLGREN, P., JOHANSSON, R., KARLSSON, J., On Latching Probability of Particle Induced Transient in Combinational Networks. In: 24th Symposium on Fault-tolerant Computing (FTCS), 1994. **Proceedings…** [S.I]: IEEE, 1994, p. 340-349.

LISBOA, C. A., ERIGSON, M. I., CARRO, L., System Level Approaches for Mitigation of Long Duration Transient Faults in Future Technologies. In: Proceedings of the 12th IEEE European Test Symposium ETS, 2007. **Proceedings…** [S.I]: IEEE, 2005, p. 165-172.

LOTZE, M; ORTMANNS, M.; MANOLI, Y., Variability of Flip-Flop Timing at Sub-Threshold Voltages. In: International Symposium on Low Power Electronics and Design (ISLPED), 2009. **Proceedings…** [S.I]: IEEE/ACM, 2009, p. 221-224.

MARKOVIC, D.; NOKOLIC, B.; BRODERSEN, R., Analysis and design of low-energy flip-flops. In: International Symposium on Low Power Electronics and Design (ISLPED), 2001. **Proceedings…** [S.I]: ACM, 2001, p. 52-55.

MASUDA H., OHKAWA, S., KUROKAWA, A., AOKI, E M., Challenge: Variability characterization and modeling for 65–90 nm process. In: IEEE Custom Integrated Circuits Conference, 2005. **Proceedings…** [S.I]: IEEE, 2005, p. 593-599.

MAVIS, D. G.; EATON, P. H., Soft Error Rate Mitigation Techniques for Modern Microcircuits. In: Proc. 40th Annual Reliability Physics Symposium, 2002. **Proceedings…** [S.I]: IEEE, 2002, p. 216-225.

MAY, T. C.; WOODS, M. H., Alpha-Particle-Induced Soft Errors in Dynamic Memories. In: IEEE Transactions on Electronics Devices, Vol. 26, Issue 1, pp. 2-9, Jan. 1979.

MEINHARDT, C., Variabilidade em FinFETs, 2014c. Tese (Doutorado em Ciência da Computação) – Instituto de Informática, Programa de Pós-Graduação em Computação, UFRGS, Porto Alegre.

MESSENGER, G. C., Collection of Charge on Junction Nodes from Ion Tracks. In: IEEE Transactions of Nuclear Science, [S.l.], v. NS-26, n.6, Dec. 1982.

MOORE, G. E., Cramming more Components onto Integrated Circuits, pp. 114-117, 1965.

MUKHERJEE, S. et. al., A Systematic methodology to Compute the Architectural Vulnerability Factors for a High-Performance Microprocessor. In: Annual International Symposium on Microarchitecture (MICRO-36), 2003. **Proceedings…** [S.I]: ACM, 2003, p. 29-40.

MUKHERJEE, S., **Architecture Design for Soft Errors.** [S.I.] : Morgan Kaufmann, 2011.

NASSIF, S. R., Process variability at the 65nm node and beyond. In: IEEE Custom Integrated Circuits Conference, 2008. **Proceedings…** [S.I]: IEEE, 2008, p. 1-8.

NEUBERGER, G. et. al., Statistical Analysis of Systematic and Random Variability of Flip-Flop Race Immunity in 130nm and 90nm CMOS Technologies. In: International Conference on Very Large Scale Integration (VLSI-SoC), 2007. **Proceedings…** [S.I]: IEEE, 2007, p. 78-83.

NGUYEN, H.; YAGIL, Y., A Systematic Approach to SER Estimation and Solutions. In: IEEE International Reliability Physics Symposium, 2003. **Proceedings…** [S.I]: IEEE, 2003, p. 60-70.

NGUYEN, H. T.; YAGIL, Y.; SEIFERT, N.; REITSMA, M., Chip-level Soft Error Estimation Method. In: IEEE Transactions on Device and Materials Reliability, vol. 5, no. 3, pp. 365-381, 2005.

NORMAND, E., Correlation of in-flight neutron dosimeter and SEU measurements with atmospheric neutron model. In: IEEE Transactions on Nuclear Science, NewYork, v.48, n.6, p. 1996-2003, Dec. 2001.

NUNES, C. S., Metodologia para Avaliação do Impacto de Efeitos de Envelhecimento em Flip-Flops. 2014. Dissertação (Mestrado em Microeletrônica) – Instituto de Informática, Programa de Pós-Graduação em Microeletrônica, UFRGS, Porto Alegre.

O'BRYAN, M. V., Radition Effects & Analysis - Single Event Effects. Nov. 2000. Available in: <http://radhome.gsfc.nasa.gov/radhome/see.htm>. Acess: Sept. 2015.

OKLOBDZIJA, V., et al. **Digital system clocking: high-performance and low-power aspects.** New York : Wiley-IEEE, 2003.

ORSHANSKY, M.; NASSIF, S.; BONING, D., **Design for Manufacturability and Statistical Design**. [S.I.] : Springer, 2008.

PTM - Predictive Technological Model. Available in: <http://ptm.asu.edu/>. Access: Apr. 2015.

RABAEY, J. M.; CHANDRAKASAN, A.; NIKOLIC, B., **Digital Integrated Circuits: A Design Perspective.** 2 ed. Upper Sladdle River: Prentice Hall, 2003.

RAMAKRISHNAN, K. et al., Comparative analysis of NBTI effects on low power and high performance flip-flops. In: International Conference on Computer Design (ICCD), 2008. **Proceedings…** [S.I]: IEEE, 2008, p. 200-205.

REBAUD, B. et. al., A Comparative Study of Variability Impact on Static Flip-Flop Timing Characteristics. In: International Integrated Circuit Design and Technology and Tutorial (ICICDT), 2008. **Proceedings…** [S.I]: IEEE, 2008, p. 167-170.

SAHA, S.K., Modeling Process Variability in Scaled CMOS Technology. IEEE Design and Test of Computers, v.27, p.8–16, Mar. 2010.

SAWANT, M., Single Event Effects Complicate Military Avionics System Design. The Journal of Military Electronics & Computing, COTS Journal, january, 2012. Available in: <http://www.cotsjournalonline.com/articles/view/102279>. Access: Aug. 2015.

SEIFERT, N.; TAM, N., Timing Vulnerability Factors of Sequentials. In: IEEE Transactions on Device and Materials Reliability, vol. 4, no. 3, pp. 516-522, 2004.

SHIVAKUMAR, P., KISTLER, M. ; KECKLER, S.W. ; BURGER, D. ; ALVISI, L., Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic. In: International Conference on Dependable Systems and Networks, 2002. **Proceedings…** [S.I.]: IEEE, 2002, p. 389-398.

SRINIVASAN, G. R., Modeling the Cosmic-Ray-Induced Soft-Error Rate in Integrated Circuits: An Overview. In: IBM Journal of Research and Development, Vol. 40, No. 1, pp. 77-89, 1996.

SYNOPSYS. Available in: http://www.synopsys.com. Access: Sep. 2015.

VELAZCO, R.; FOUILLAT, P.; REIS, R. A. L. (eds.), **Radiation Effects on Embedded Systems**. [S.I.] : Springer, 2007.

WANG, F.; AGRAWAL, V. D., Single event upset: An embedded tutorial. In VLSI Design, 2008. VLSID 2008. 21st International Conference on, pages 429–434. IEEE, 2008.

WEBER, T. S., **Um roteiro para exploração dos conceitos básicos de tolerância a falhas**. Textos didáticos em tolerância a falhas. Porto Alegre: Instituto de Informática. UFRGS, 2002.

ZIEGLER, J. F.; LANFORD, W. A., The effect of sea level cosmic rays on electronic devices. In: IEEE International Solid-State Circuits Conference, 1982. **Proceedings…** [S.I.]: IEEE, 1981, vol. 52, no. 6, p. 4305-4318.

ZIMPECK, A. L.; KASTENSMIDT, F. L.; REIS, R., Analyzing the Impact of Frequency and Diverse Path Delays in the Timing Vulnerability Factor of Master-Slave D Flip-Flops. In: IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2015. **Proceedings…** [S.I.]: IEEE, 2015, p. 521-526.

ZIMPECK, A. L.; KASTENSMIDT, F. L. REIS, R., Análise do Timing Vulnerability Factor em Flip-Flop D Mestre-Escravo em Nanotecnologias. In: XXII Iberchip Workshop, 2016. **Proceedings…** [S.I.]: Iberchip Proceedings, 2015, p. 1-4.

APPENDIX

VARIABILITY IN FINFET DEVICES

MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) device technology limits are being achieved ant it will not be trivial to continue with that in technologies below 22nm (FRANK et. al, 2001). FinFET (Fin-Shaped Field Effect Transistor) devices are taking a strong position to replace the MOSFETs because of its excellent short channel effect (SCE) controllability compared with traditional planar devices. The fin-like geometry of FinFETs, where the depletion regions reach the gates entirely into the body region, implies that no free charge carriers are available, making the suppression of SCE possible (KING, 2005). Moreover, FinFET technology stands out because it provides perfect isolation, reducing leakage current and giving high driving capability, both for high-speed and low-power applications (HENDERSON, 2013; ITRS, 2011).

However, there are a number of scaling challenges with FinFETs, as geometric variability, mitigate Random Dopant Fluctuation (RDF), fringe capacitance to contact, low-k spacer, fin and gate fidelity, conformal coverage in gate wrap-around devices, Chemical-Mechanical Planarization (CMP) polish and contact resistances (ENDO et. al, 2009). In addition, Process, Voltage and Temperature (PVT) also significantly affect the FinFET technology. It can accelerate circuit degradation and make the circuit inappropriate for its initial purpose.

Process variations are caused, in the majority of cases, during the lithography step of the fabrication process. Voltage is usually associated with the system power consumption. However, the system performance is also affected by the supply voltage deviations. It occurs because transistor saturation current depends on the power supply and the gate delay is dependent on the saturation current. This relation is exponential for a wide voltage range. Devices and interconnects may have performance and power consumption affected due to temperature dependence (KUMAR et. al, 2005). Temperature variations across communicating blocks on a same chip may cause performance mismatches, logic or functional failures (BORKAR et. al, 2003).

FinFET double gate devices consist of vertical silicon fins to form the channel region and to connect the source and drain regions at each end. The gate region is wrapped around this vertical fin and MOS channels are formed at the two sidewalls plus top-side of the fin. The fin-like geometry, where the depletion regions reach the gates entirely

into the body region, implies that no free charge carriers are available, making the suppression of SCE possible in FinFETs (KING, 2005). Fin engineering (balancing height, fin thickness, oxide thickness, and channel length) is essential in minimizing the leakage current, I_{OFF}, and maximizing the on current, I_{ON} (SWAHN et. al, 2006). The main geometrical parameters suffering from process variability for a FinFET considering single-fin and multi-fin are presented in Fig. A.1 (ALIOTO, 2010):

i. Gate length (L_G) – the distance between drain and source;

ii. Fin height (H_{FIN}) – uniform for all fins on chip;

iii. Fin thickness (T_{SI}/W_{FIN}) – wrapped around by gate electrodes.

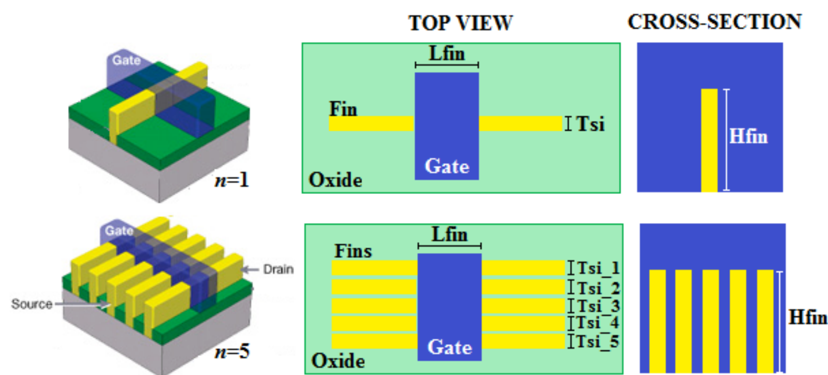


Fig. A.1: FinFET structure for single-fin and multi-fin – Top view and cross-section. Adapted from (CHRISTIANSEN, 2015)

Metal gate workfunction fluctuation (WFF) is an electrical parameter that is also considered as sensitive to process variations in FinFET technologies. WFF is caused by the dependency of metal workfunction on the orientation of its grains, as depicted in Fig. A.2. In the ideal fabrication process, metal gates devices have the gates produced with metal uniformly aligned. Nevertheless, in real fabrication process, metal gate devices are generally produced with metals with different workfunctions (ϕ_m) randomly aligned, which causes higher variations.

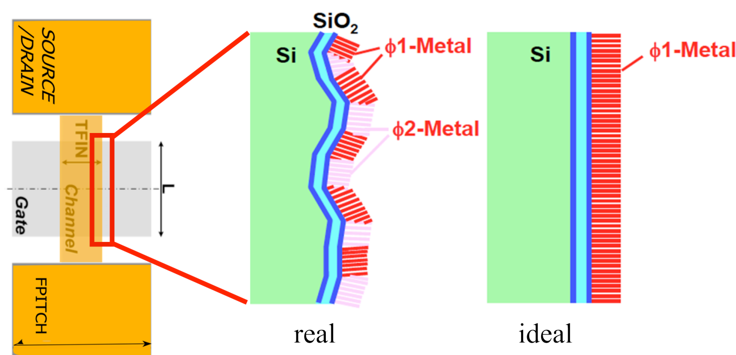


Fig. A.2: Metal gate fabrication in ideal and real aspects. Adapted from (DADGOUR, 2008)

Process variability was taken by Monte Carlo SPICE simulations with a total of ten thousand variations of each parameter in HSPICE tool. The mean (μ) and standard deviation (σ) are then compared. The normalized standard deviation (σ/μ) of the metrics was compared because it makes possible to compare the variability of the parameter with different means. The impact of voltage variation is evaluated through the sensitivity of the power consumption and performance to the variations around ±10% of the nominal power supply (VDD). In the temperature evaluation done in this work, the temperature was changed from -25ºC to 125ºC. Both analyses generally consider the values commonly used in industry.

A.1 Process variability and temperature variations in PFET and NFET transistors

This research analyzes the effects that the process variability causes on I_{ON} and I_{OFF} currents in PFET and NFET transistors for a set of predictive FinFET technologies from 20nm to 7nm by electrical device simulations. For it, it was adopted two FinFET device models with different threshold voltages: the high-Performance (HP) and the Low Standby Power (LSTP) version of the PTM-MG models. The parameters analyzed are gate length (Lg), fin height (H_{FIN}), fin width (W_{FIN}) and workfunction fluctuation (WFF) and their references values for technologies used are showed in Tab. A.1.

Table A.1: Reference values for the main parameter of HP and LSTP FinFET devices

Technology (nm)	*Supply Voltage (V)*	*Lg (nm)*	*H_{FIN} (nm)*	*W_{FIN} (nm)*	*WFF HP (eV)*		*WFF LSTP (eV)*	
					N	*P*	*N*	*P*
20	0.90	24	28	15	4.38	4.80	4.56	4.62
16	0.85	20	26	12	4.41	4.76	4.58	4.59
14	0.80	18	23	10	4.42	4.75	4.60	4.57
10	0.75	14	21	8	4.42	4.75	4.60	4.56
7	0.70	11	18	6.5	4.42	4.74	4.61	4.56

Source: (PTM, 2015)

Results of I_{ON} and I_{OFF} currents were obtained from simulations for 3σ deviation of 10% from nominal values of the geometric parameters analyzed under variations. Fig. A.3 shows the average impact on I_{OFF} of geometric parameters variation for NFET and PFET devices in HP and LSTP versions. Results showed that fin height has a small standard deviation while gate length and fin thickness have an intermediate value of the difference. The parameter that suffers the most significant impact is WFF on current I_{ON}. The same behavior occurred when the current I_{ON} was analyzed, but the experiments were omitted for compactness.

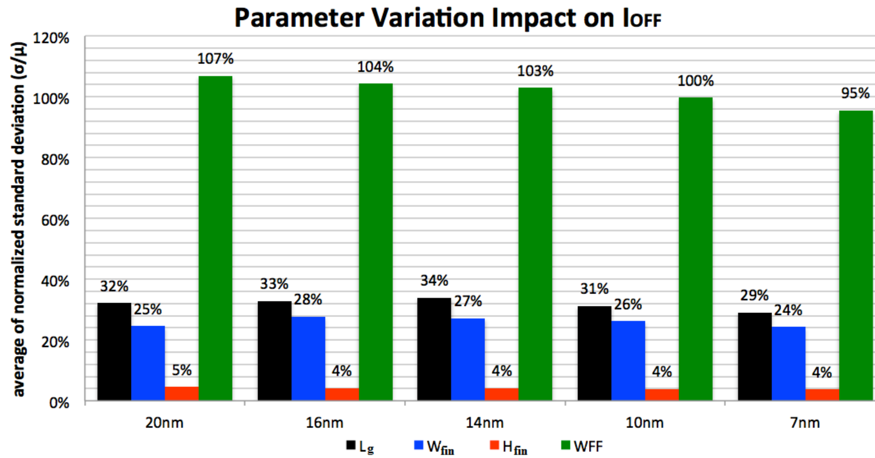


Fig. A.3: HP and LSTP devices average I_{OFF} impact due to process variability (MEINHARDT et. al, 2014a)

For all FinFET devices evaluated, workfunction fluctuation shows to be the most significant parameter because WFF experiments show large standard deviation results. This impact will affect the specifications of large and complex circuits using these technologies. Understanding the behaviour of the workfunction fluctuations in new technologies is key to the development of designs and tools. In this context, the next step of this experiment evaluates only the effect of the WFF in predictive FinFET technologies.

For the electrical parameter WFF, the simulations assume a more conservative approach with the 3σ deviation of 10% from nominal values initially. For 10% of WFF, circuits in these predictive technologies will have to deal with about 50% of I_{ON} normalized deviation and more than 100% of I_{OFF} deviation normalized deviation, as Fig. A.4 and A.5 showed, respectively. The impact appears to be decreasing with the technology scaling, mainly for PFET devices on I_{OFF} current, but still high enough to be neglected in digital designs, particularly in low-power applications.

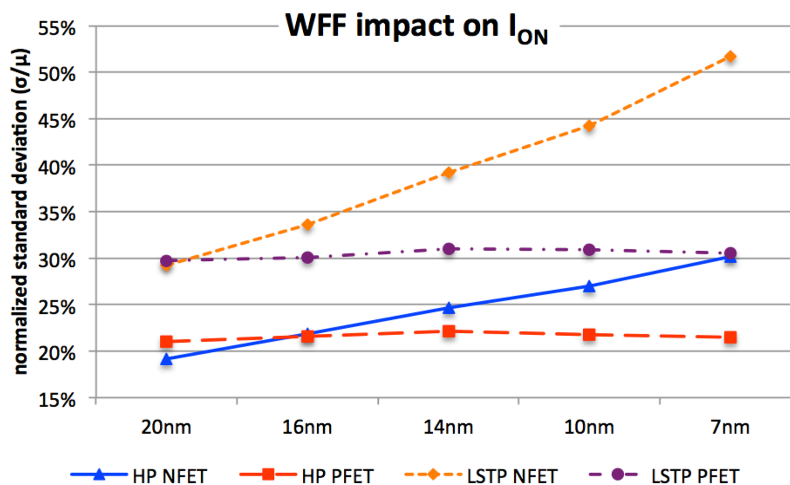


Fig. A.4: Sub-20nm 10% of WFF tendency of deviation impact on I_{ON} for HP and LSTP devices (MEINHARDT et. al, 2014a)

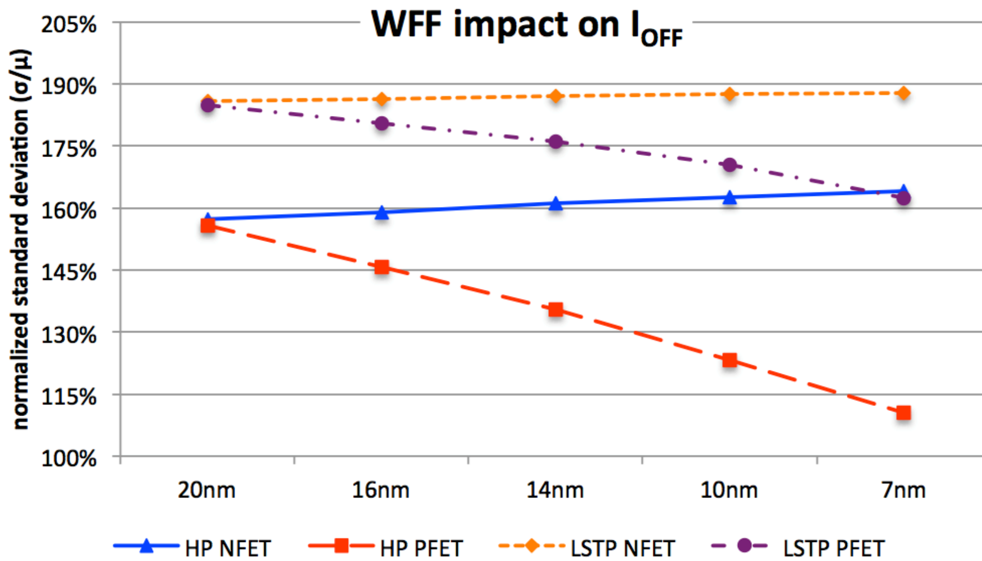


Fig. A.5: Sub-20nm 10% of WFF tendency of deviation impact on I_{OFF} for HP and LSTP devices (MEINHARDT et. al, 2014a)

A second experiment analyses the consequence of different degrees of WFF deviation on I_{ON} and I_{OFF} currents. This experiment considers workfunction as a Gaussian distribution with 3σ deviation of 4% to 10% from nominal values. The experiments showed that more than 5% of WFF, the current I_{ON} starts to have more than 10% of deviation even for the 20nm technology, as shows the Fig. A.6. This investigation is more alarming about I_{OFF} current. WFF introduces a large deviation from nominal values and brings elevated standard deviation even for small values of WFF variability, as it is possible to see in Fig. A.7.

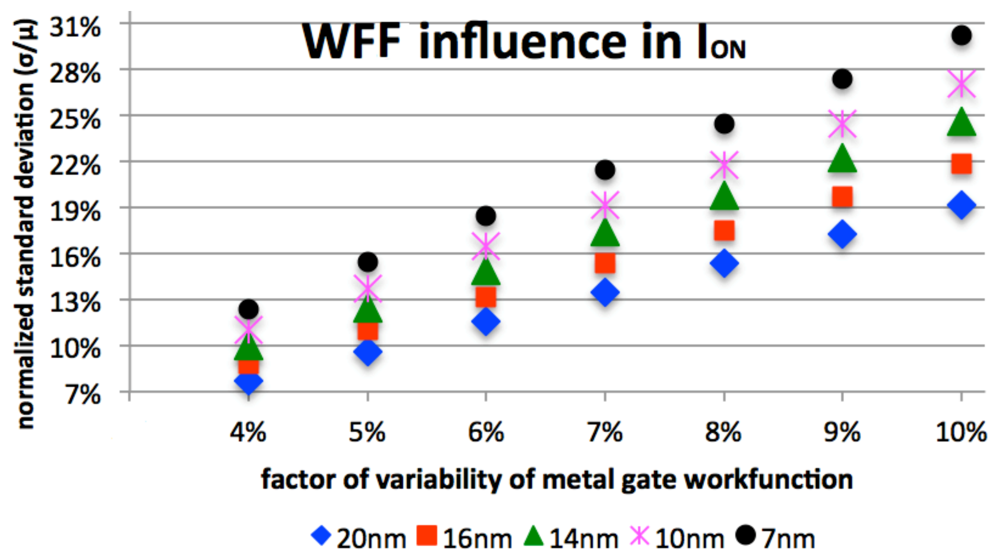


Fig. A.6: Factor of fluctuation on workfunction and the effect on the I_{ON} (MEINHARDT et. al, 2014a)

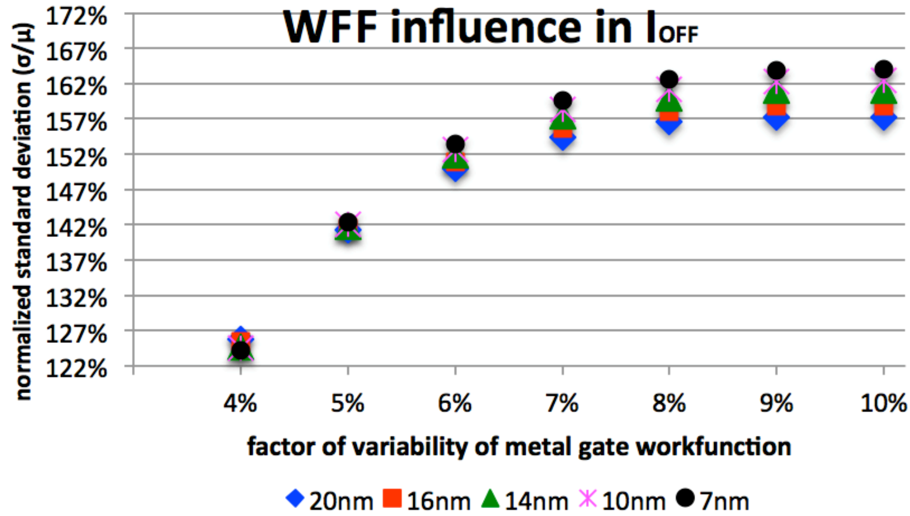


Fig. A.7: Factor of fluctuation on workfunction and the effect on the I_{OFF} (MEINHARDT et. al, 2014a)

The second analysis consists in the verification of the current device behavior with the temperature varying on 20nm FinFET devices models in HP and LSTP. Table A.2 presents the absolute values for the evaluated FinFET devices. In the last row, the ΔI factor indicates how many times the current increases at 125°C compared with the reference temperature. This factor allows us to see that LSTP devices are more sensitive to the effects of temperature oscillation.

Fig. A.8 shows the expected increase in the current with the temperature increase. PFET devices are more impacted by the temperature, with an increase of 7.27μA and 7.82μA in the I_{ON} to HP and LSTP devices, respectively. LSTP devices are up to 25% more sensible to temperature variations. Another point is that PFET devices are approximately 30% more sensible to temperature effects. To highlight the difference of sensibility for each device in the HP and LSTP technologies, Fig. A.8 (on the right) shows the normalized results of the increase in I_{DS} for the considered technologies, always adopting the reference temperature at 25°C.

Table A.2: Maximum I_{DS} deviation due to temperature variations in 20nm FinFET technology

Temperature (°C)	*Maximum I_{DS} (μA)*			
	HP		*LSTP*	
	PFET	*NFET*	*PFET*	*NFET*
25	78.29	88.42	45.91	51.48
50	80.36	90.28	47.96	53.23
75	82.25	91.90	49.94	54.87
100	83.98	93.30	51.87	56.40
125	85.56	94.51	53.73	57.82
ΔI	**7.27**	**6.09**	**7.82**	**6.34**

Source: Adapted from (ZIMPECK et. al, 2014)

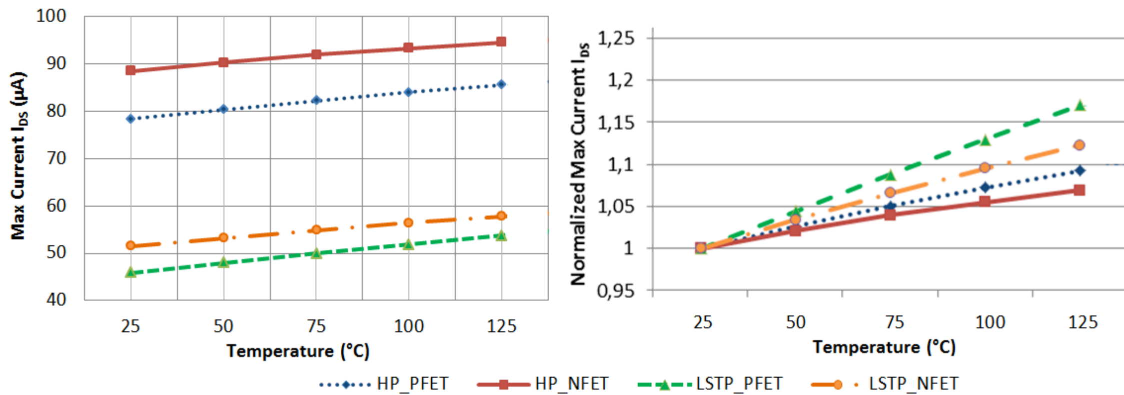


Fig. A.8: Temperature impact on I_{ON} of 20nm FinFET devices on the left and results normalized to reference temperature at 25ºC on the right (ZIMPECK et. al, 2014)

A.2 PVT Variability Impact in FinFET Cells

To analyze the impact of PVT variability, this work considers a subset of circuits that represents the 1-to-4-inputs combinational cells most frequently available in traditional commercial standard cell libraries in NanoCMOS. As vendor tools for standard cells using FinFET are not yet available in the market, this experiment generates a predictive library where all cells were adapted to the 20nm FinFET technology node, respecting the aspects ratio of the commercial library in 45nm. The predictive evaluation adopts the 20nm High-Performance application version from PTM-MG.

These evaluations help to predict the influence of PVT variations in future technology nodes and to identify relevant behavioral standards on the use of FinFET technologies in digital designs, highlighting the need to consider all electrical characteristics in the development of IC designs and EDA tools. The WFF parameter was modeled as a Gaussian function with 3σ deviation of 5% from nominal values. Timing measurements consider the worst case of propagation time and total power is the power consumed during the execution of the timing arcs simulation. The comparison in these experiments was made regarding mainly the Power-Delay-Product (PDP).

Fig. A.9 shows a comparison between the nominal values of timing, as a form of reference values to the variability analyses, and the results considering WFF. The standard deviation from this experiment is showed in the errors bars. It highlights that NOR3 and NOR4 gates are also timing sensible to WFF. About the standard deviation, power results show a low-density function for all cells, with large deviation, above 17% of nominal deviation. Error bars in Fig. A.10 show that WFF provokes a considerable deviation in total power that has to be considered in VLSI designs. It is possible to see that WFF have more impact on the power consumption (24% on average) than timing (8% on average).

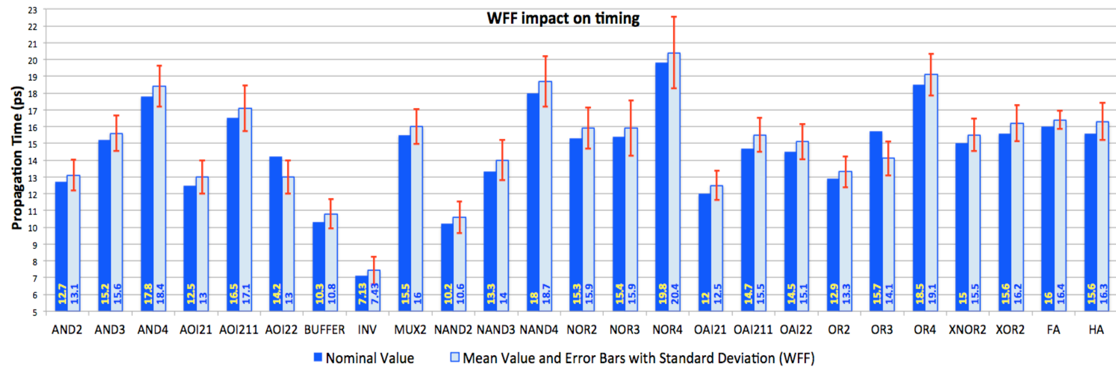


Fig. A.9: Nominal timing results compared with mean and standard deviation timing results for the Standard Cell gates under WFF (MEINHARDT et. al, 2014b)

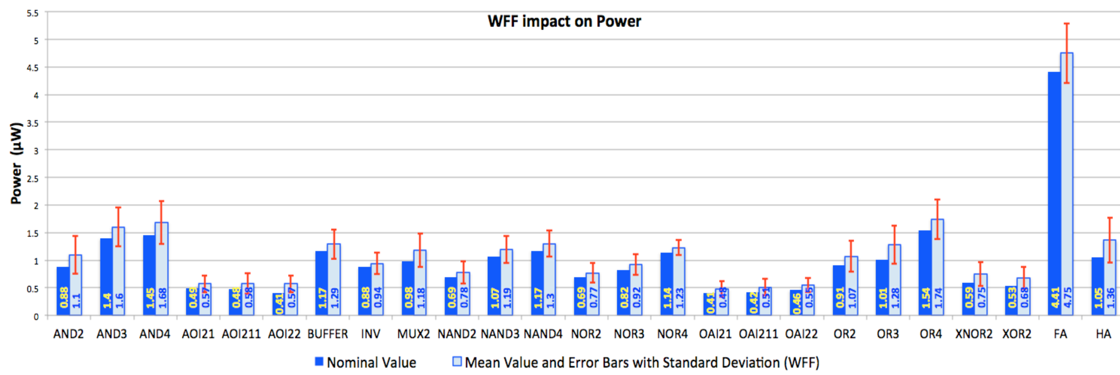


Fig. A.10: Nominal total power results compared with mean and standard deviation power results for the Standard Cell gates under WFF (MEINHARDT et. al, 2014b)

Fig. A.11 shows a comparison between PDP nominal values and under WFF variations. The results of the comparison highlights that Full-Adder (FA), AND4 and Half-Adder (HA) are more sensible to variations of WFF. These cells present deviation of 10.33%, 19.76% and 35.36% above the PDP nominal values, respectively. On the other hand, the cells less sensible to variations of WFF are INV, NAND2 and AOI21 with deviation of 11.11%, 18.57% and 22.44% more than the PDP nominal values, respectively.

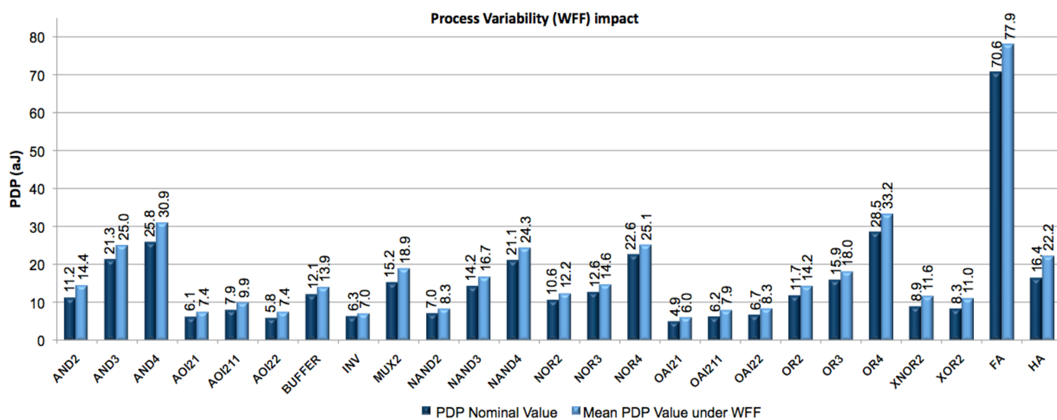


Fig. A.11: Nominal PDP results compared with mean values results for the Standard Cell gates under WFF (ZIMPECK et. al, 2015a)

Fig. A.12 shows that timing percentage increase reaches at 0.3V compared to the nominal voltage for all timing arcs of each cell from the library. Analyzing the results, the cells that present more sensitive to variations are FA, NOR3 and NAND4 with deviation of 60.79%, 26.86% and 25.84%, respectively. For the cells AND3, NOR4, OR4 and FA, the frequency of activity was reduced to allow the near-threshold operation in the voltage experiments. Thus, these circuits consume less power at nominal values of temperature and voltage, because these cells will remain more time in the static behavior at high voltages than in the temperature experiment.

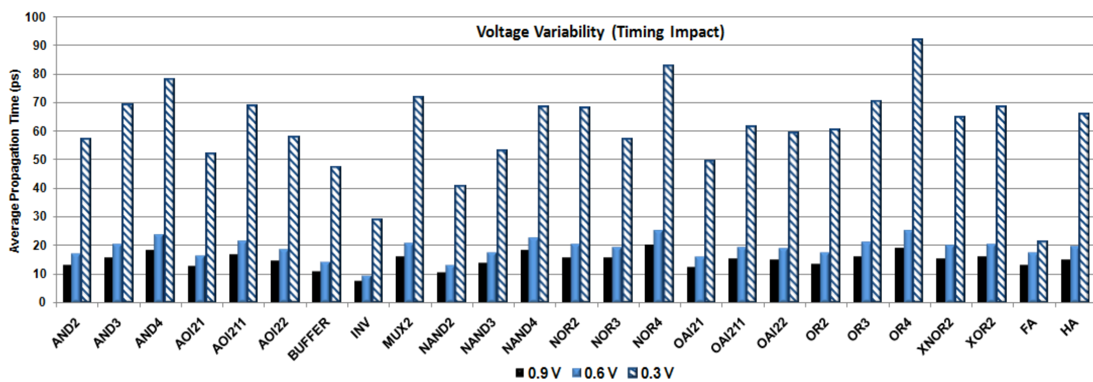


Fig. A.12: Voltage variability results for the Standard Cell gates under WFF (ZIMPECK et. al, 2015a)

Fig. A.13 highlights the cells that consume more power in the analyzed set of cells. The full adder is the cell that presents the largest power consumption at room temperature, and the temperature increase makes this cell reaching even higher energy values. It is important to note that these cells reach power results in the order of dozens of µW. AND4 cell shows the larger sensibility to temperature oscillation, with an increase of 4% for each degree temperature increase. As the temperature was varied, results show that the average timing remains practically constant, with a slight increase when the temperature rises. However, total power consumption is impacted by the temperature increase. We know that it is not advisable to vary the temperature above 125ºC, but we did experiments only to confirm that above this temperature, the correct circuit behavior is not guaranteed.

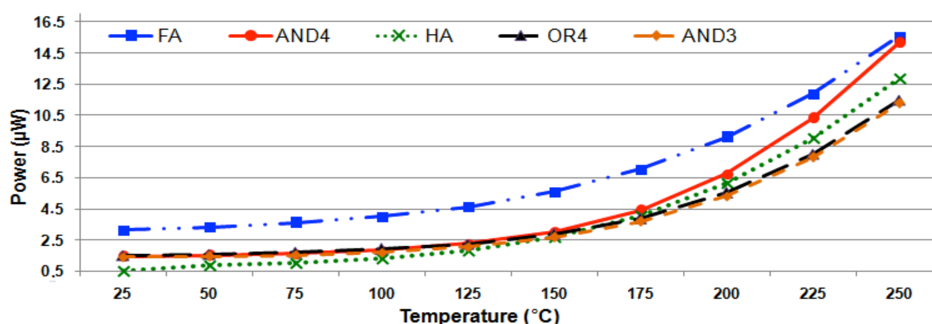


Fig. A.13: Top 5 cells more sensible to temperature variation (ZIMPECK et. al, 2015a)

A.3 PVT Variability Impact in FinFET Cells with Different Transistor Sizing Techniques

It was analysed the impact of PVT variations on performance and power consumption for different transistor sizing techniques applied to a fixed sub-set of gates from each benchmark circuit presented in (POSSER et. al, 2014) considering 14nm FinFET technology. Different than for MOSFET devices, transistor sizing for FinFET devices is discrete, i.e., the transistor sizing is given by the number of parallel arrangement of fins. It was considered as transistor sizing techniques: Minimum Transistor Sizing (MTS), which corresponds to all cells with number of fins equal to 1; Logical Effort (LE); and Optimized Transistor Sizing (OTS) using the sizing presented in (POSSER et. al, 2014).

Transistor sizing by logical effort is based in a simple delay model where each combinational logic has a different logical effort based on minimum sizing of an inverter. We calculated the logic effort and obtained the discrete transistor sizing individually for a set of cells and it is adopted the well-known fan-out-of-4 delay metrics *FO4*. For OTS technique, transistor sizing is obtained from a geometric programming (GP) optimization for delay/area minimization. This optimization generates a continuous W_{TOTAL} and the number of fins is defined by $n = W_{TOTAL}/W_{MIN}$. As the FinFET size has to be discrete, a simple rounding is applied to discretize the transistor sizes. We selected the transistor sizes for a set of cells with the largest occurrence in the experimental circuit results related in (POSSER et. al, 2014).

Fig. A.14 shows the power results for the circuits evaluated under process variability. The three transistor sizing strategies present a similar behavior for the most of the cells. However, cells with transistor sizing by Logical effort present more sensibility to process variability, with high values of normalized standard deviation. Optimized Transistor Sizing results improve the process variability robustness in practically all the cases.

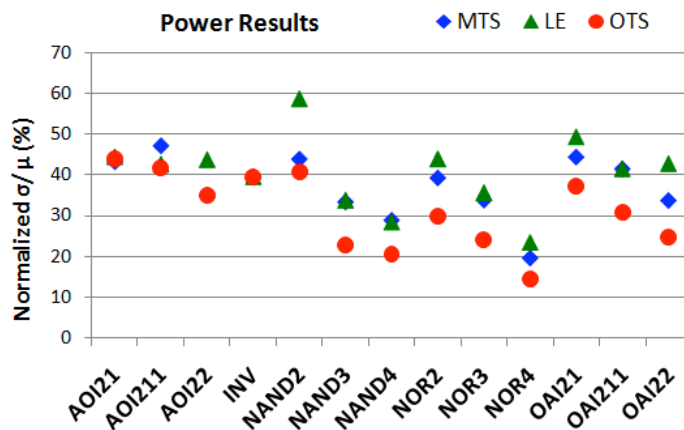


Fig. A.14: Power Normalized Standard Deviation (σ) by Mean (µ) results obtained by Monte Carlo simulation of the standard cells evaluated (ZIMPECK et. al, 2015b)

Furthermore, Fig. A.15 presents the timing results obtained for cells under process variability. Inverter cell presents the largest deviation (approximately 13%) compared to the other cells in the three strategies analyzed. However, Logical Effort technique presents more sensibility to process variations impact on delay, in a very high level, when compared to the other techniques. For example, OAI211 and OAI22 cells present more than 150% deviation from nominal values considering this approach. OTS presents higher nominal values and, hence, the normalization could be lower although the values are higher.

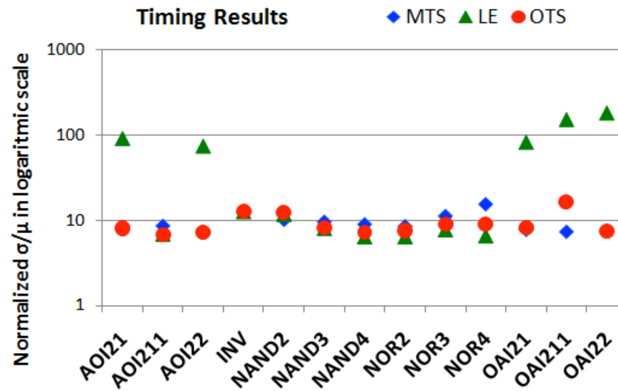


Fig. A.15: Delay Normalized Standard Deviation (σ) by Mean (μ) results obtained by Monte Carlo simulation of the standard cells evaluated (ZIMPECK et. al, 2015b)

PDP results help to evaluate together the process variability impact on power and delay of each cell analyzed. Fig. A.16 shows the difference obtained between PDP nominal values and PDP under WFF variations for the three transistor sizing techniques. It is possible to see that NAND2 cell shows a high sensibility to WFF, with deviations of 19.8%, 22.6% and 19.4% for MTS, LE and OTS techniques, respectively. In average, LE shows the largest deviation on the normalized PDP. The OTS technique presents the best relationship between nominal PDP and PDP under process variability, considering normalized standard deviation and mean. A preliminary hypothesis for this is that OTS presents higher nominal values and, hence, the normalization could be lower although the values are higher.

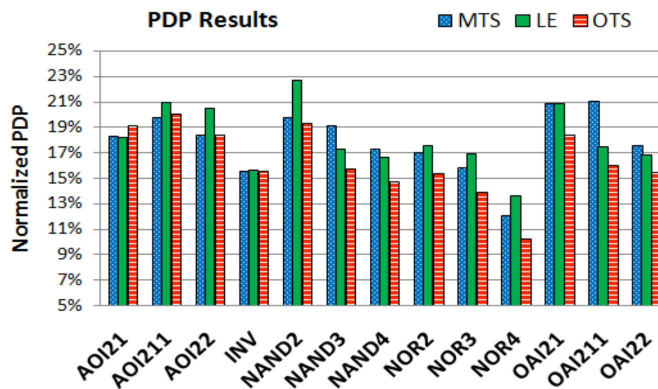


Fig. A.16: Difference between nominal PDP and mean values results for different cells sizing under process variability (ZIMPECK et. al, 2015b)

Voltage variations effects are most visible in the PDP results and the behavior is slightly different for the average and worst case, as shown in Fig. 4, for the three transistor sizing techniques. LE and MTS curves in the worst case are practically equal in average, but in OTS the results are almost twice as higher than in the worst case. PDP variations due to voltage oscillation are up to 22.1% when the voltage is lower and up to 27.6% when the voltage is higher than nominal values, in the worst and average cases. Though, OTS worst case presents higher energy consumption and it is also more sensible to voltage oscillation as compared to the others worst cases.

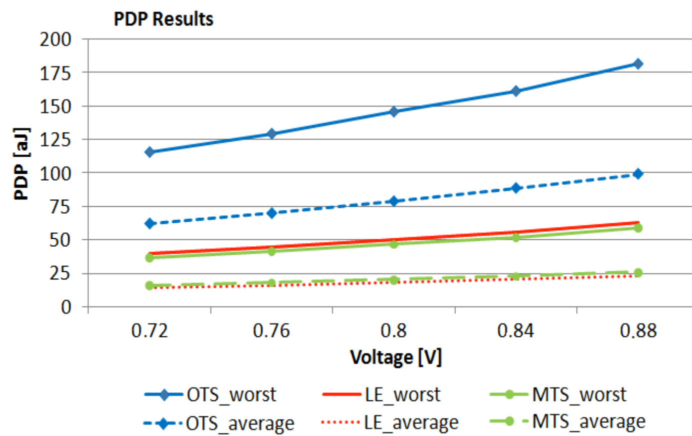


Fig. A.17: PDP results for different cells sizing under voltage variations (ZIMPECK et. al, 2016)

LE and MTS sizing techniques are robust to variations below the nominal temperature. However, from 100ºC to 125ºC the total power is three to four times larger than the nominal value, respectively, for all techniques. OTS technique shows worst PDP results and a large deviation from negative and high temperature. Evaluating the impact in each cell, shown in Fig. A.18, LE presents the on average the largest deviation on the normalized PDP. AOI22 cell shows a high sensibility to temperature variations, with high deviations of 77%, 85% and 76% for MTS, LE and OTS techniques, respectively. OTS is the technique less impacted by temperature variations in all the cases, considering the standard deviation.

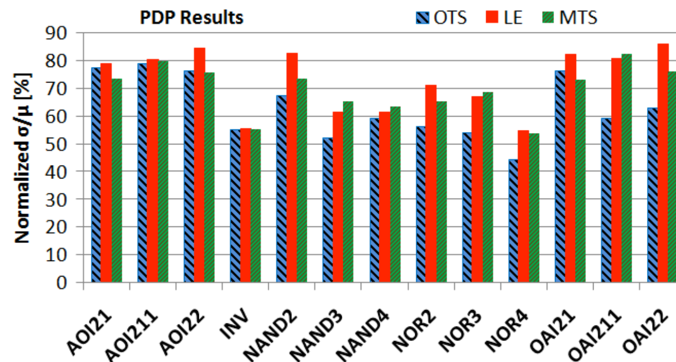


Fig. A.18: PDP Normalized Standard Deviation by Mean results considering temperature variations (ZIMPECK et. al, 2016)

REFERENCES

ALIOTO, M., Analysis of layout density in finfet standard cells and impact of fin technology. In: International Symposium on Circuits and Systems (ISCAS), 2010. **Proceedings…** [S.I]: IEEE, 2010, p. 3204–3207.

BORKAR, S. et al., Parameter Variations and Impact on Circuits and Microarchitecture. In: Design Automation Conference, DAC, 40, 2003. **Proceedings…** [S.I]: ACM/IEEE, 2003, p. 338-342.

CHRISTIANSEN, M., Design for Success: USB IP for FinFET Process. DesignWare Technical Bulletin. Synopsys, 2015.

DADGOUR, H.; DE, V.; BANERJEE, K., Statistical Modeling of Metal-Gate Work-Function Variability in Emerging Device Technologies and Implications for Circuit Design. In: International Conference on Computer-Aided Design (ICCAD), 2008. **Proceedings…** [S.I]: ACM/IEEE, 2008, p. 270-277.

ENDO, K. et. al., Variation Analysis of TiN FinFETs, ISDRS, December 9-11, College Park, USA, 2009.

FRANK, E. J. et. al., Device Scaling Limits of Si MOSFETs and their Application Dependencies. In: Proc. IEEE, 89(3): 259-288, Mar. 2001.

HENDERSON, C. L., Failure analysis techniques for a 3D world, In: Microelectronics Reliability, Vol. 53, i. 9-11, pp. 1171-1178, 2013.

ITRS. THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS. Available in: http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf, 2011. Access: Aug. 2015.

KING, T.-J., FinFETs for Nanoscale CMOS Digital Integrated Circuits. In: International Conference on Computer-Aided Design, 2005. **Proceedings…** [S.I]: IEEE, 2005, p. 207–210.

KUMAR, R.; KURSUN, V., Voltage Optimization for Temperature Variation Insensitive CMOS Circuits. In: Midwest Symposium on Circuits and Systems (MWCAS), 2005. **Proceedings…** [S.I]: IEEE, 2005, p. 476-479.

MEINHARDT, C.; ZIMPECK, A. L.; REIS, R., Predictive evaluation of electrical characteristics of sub-22nm FinFET technologies under device geometry variations. Microelectronics Reliability Journal, v. 54, n. 9–10, 2014a, p. 2319-2324.

MEINHARDT, C., ZIMPECK, A. L., REIS, R. Impact of Gate Workfunction Fluctuation on FinFET Standard Cells. In: IEEE 21th International Conference On Electronics, Circuits, And Systems (ICECS), 2014b. **Procedings...** [S.l:]: IEEE, 2014b, p. 574-577.

POSSER, G. et al., Performance Improvement with Dedicated Transistor Sizing for MOSFET and FinFET devices. In: IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2014. **Proceedings…** [S.I.]: IEEE, 2014, p. 418-423.

SWAHN, B.; HASSOUN, S., Gate-sizing: finfets vs 32nm bulk mosfets in DAC, San Francisco, CA, United States, 2006, pp. 528-531.

ZIMPECK, A. L; MEINHARDT, C.; REIS, R., Evaluating the Impact of Environment and Physical Variability on the I_{ON} current of 20nm FinFET Devices. In: 24th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2014. **Proceedings…** [S.I.]: IEEE, 2014, p. 1-8.

ZIMPECK, A. L; MEINHARDT, C.; REIS, R., Impact of PVT Variability on 20nm FinFET Standard Cells. Microelectronics Reliability Journal, v. 55, n. 9-10, 2015a.

ZIMPECK, A. L; MEINHARDT, C.; POSSER, G.; REIS, R., Process Variability in FinFET Standard Cells with Different Transistor Sizing Techniques. To be published in: 22st IEEE International Conference on Electronics Circuits and Systems, Cairo-Egypt, 2015b.

ZIMPECK, A. L; MEINHARDT, C.; POSSER, G.; REIS, R., FinFET Cells with Different Transistor Sizing Techniques against PVT variations. To be published in: IEEE International Symposium on Circuits and Systems (ISCAS), Montreal-Canada, 2016.