UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA

PEDRO FILIPE LEITE CORREIA DE TOLEDO

MOSFET Zero-Temperature-Coefficient (ZTC) Effect Modeling and Analysis for Low Thermal Sensitivity Analog Applications

Thesis presented in partial fulfillment
of the requirements for the degree of
Master of Microeletronics

Advisor: Prof. Dr. Hamilton Duarte Klimach
Coadvisor: Prof. Dr. Eric Fabris

Porto Alegre
August 2015

CIP – CATALOGING-IN-PUBLICATION

de Toledo, Pedro Filipe Leite Correia

MOSFET Zero-Temperature-Coefficient (ZTC) Effect Modeling and Analysis for Low Thermal Sensitivity Analog Applications / Pedro Filipe Leite Correia de Toledo. – Porto Alegre: PGMICRO da UFRGS, 2015.

147 f.: il.

Thesis (Master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica, Porto Alegre, BR–RS, 2015. Advisor: Hamilton Duarte Klimach; Coadvisor: Eric Fabris.

1. ZTC Bias Point. 2. GZTC Bias Point. 3. CMOS Analog Integrated Circuits. 4. Low Temperature Sensitivity Transconductors. 5. Voltage Reference. 6. Current Reference. I. Klimach, Hamilton Duarte. II. Fabris, Eric. III. Título.

UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
Reitor: Prof. Carlos Alexandre Netto
Vice-Reitor: Prof. Rui Vicente Oppermann
Pró-Reitor de Pós-Graduação: Prof. Vladimir Pinheiro do Nascimento
Diretor do Instituto de Informática: Prof. Luis da Cunha Lamb
Coordenador do PGMICRO: Prof. Gilson Inácio Wirth
Bibliotecária-chefe do Instituto de Informática: Beatriz Regina Bastos Haro

“Probabilidade é grau de certeza e difere da certeza absoluta assim como a parte difere do todo.”

— SIR JAMES BERNOULLI, 1713

ACKNOWLEDGMENTS

During the development of this thesis, I started a new family with my wife, **Claudia Camerini Correa de Toledo** and my son, **Pietro Camerini Correa de Toledo**. That changed my life goals and boosted the completion of this work. I would like especially to thank my wife for all the motivation, support and patience during my whole graduate studies at the Federal University of Rio Grande do Sul. Mainly during conference periods where she had to take care of our child alone while I was presenting works related to this thesis.

I would like to thank to my parents, **Bernardino Marques Toledo** and **Sineide Leite da Silva**, and my beautiful sisters **Thais Toledo** e **Adriana Toledo**, for all support given to my master's studies and life in Porto Alegre.

My advisors, **Prof. Hamilton Klimach** and **Prof. Eric Fabris**, for the excellent discussions that helped me mature and learn so much in the field of microelectronics. The same remarks apply to **Prof. Sergio Bampi**.

My friends of NSCAD group, Renê Timbo, Diogo Santana, Helga Dornelas, Alonso Schmidt, Jhon Caicedo, and in particular **David Cordova**, for all discussions in the lab and meetings. **David Cordova** made a tremendous contribution to this thesis since two of the circuits presented in this work were designed and measured by him.

My friends of lab 110 Analog/RF group, Arthur Liraneto, Filipe Baumgratz, Renato Campana , Sandro Binsfeld, Oscar Mattia, Márlon Lorenzetti, Rafael Schultz, Luís Rodovalho, Bruno Canal, Moacir Monteiro, Arthur Oliveira, Roger Zamparette, Gabriel Guimarães,Pedro Toledo, David Cordova, Fernando Carrion, Marcelo Pedrini, Thales Ribeiro and Yi Chen Wu for the discussions in the lab and meetings.

All administrative people, who have been working hard to keep all the infrastructure of the Instituto de Informática and Graduate Program in Microelectronics fully available to me.

PRONEX/CNPq and Capes for the funding support given to this research. The IC-Brazil program, NSCAD support to Cadence tools and MOSIS for the MOSIS Educational Program (MEP), which gave the opportunity to fabricate some circuits presented here.

ABSTRACT

Continuing scaling of Complementary Metal-Oxide-Semiconductor (CMOS) technologies brings more integration and consequently temperature variation has become more aggressive into a single die. Besides, depending on the application, room ambient temperature may also vary. Therefore, procedures to decrease thermal dependencies of eletronic circuit performances become an important issue to include in both digital and analog Integrated Circuits (IC) design flow. The main purpose of this thesis is to present a design methodology for a typical CMOS Analog design flow to make circuits as insensitivity as possible to temperature variation. MOSFET Zero Temperature Coefficient (ZTC) and Transconductance Zero Temperature Coefficient (GZTC) bias points are modeled to support it. These are used as reference to deliver a set of equations that explains to analog designers how temperature will change transistor operation and hence the analog circuit behavior. The special bias conditions are analyzed using a MOSFET model that is continuous from weak to strong inversion, and both are proven to occur always from moderate to strong inversion operation in any CMOS fabrication process. Some circuits are designed using proposed methodology: two new ZTC-based current references, two new ZTC-based voltage references and four classical Gm-C circuits biased at GZTC bias point (or defined here as GZTC-C filters). The first current reference is a Self-biased CMOS Current Reference (ZSBCR), which generates a current reference of 5 μA. It is designed in an 180 nm process, operating with a supply voltage from 1.4V to 1.8 V and occupying around $0.010mm^2$ of silicon area. From circuit simulations the reference shows an effective temperature coefficient (TC_{eff}) of 15 ppm/^{o}C from -45 to $+85^o$C, and a fabrication process sensitivity of $\sigma/\mu = 4.5\%$, including average process and local mismatch. Simulated power supply sensitivity is estimated around $1\%/V$. The second proposed current reference is a Resistorless Self-Biased ZTC Switched Capacitor Current Reference (ZSCCR). It is also designed in an 180 nm process, resulting a reference current of 5.88 μA under a supply voltage of 1.8 V, and occupying a silicon area around $0.010mm^2$. Results from circuit simulation show an TC_{eff} of 60 ppm/^{o}C from -45 to +85 ^{o}C and a power consumption of 63 μW. The first proposed voltage reference is an EMI Resisting MOSFET-Only Voltage Reference (EMIVR), which generates a voltage reference of 395 mV. The circuit is designed in a 130 nm process, occupying around 0.0075 mm^2 of silicon area while consuming just 10.3 μW. Post-layout simulations present a TC_{eff} of 146 ppm/^{o}C, for a temperature range from -55 to $+125^o$C. An EMI source of 4 dBm (1 V_{pp} amplitude) injected into the power supply of circuit, according to Direct Power Injection (DPI) specification results in a maximum DC Shift and Peak-to-Peak ripple of -1.7 $\%$ and 35.8m V_{pp}, respectively. The second proposed voltage reference is a 0.5V Schottky-based Voltage Reference (SBVR). It provides three voltage reference outputs, each one utilizing different threshold voltage MOSFETs (standard-V_T, low-V_T, and zero-V_T), all available

in adopted 130 nm CMOS process. This design results in three different and very low reference voltages: 312, 237, and 51 mV, presenting a TC_{eff} of 214, 372, and 953 ppm/^{o}C in a temperature range from -55 to 125°C, respectively. It occupies around 0.014 mm^2 of silicon area for a total power consumption of 5.9 μW. Lastly, a few example Gm-C circuits are designed using GZTC technique: a single-ended resistor emulator, an impedance inverter, a first order and a second order filter. These circuits are simulated in a 130 nm CMOS commercial process, resulting improved thermal stability in the main performance parameters, in the range from 27 to 53 ppm/^{o}C.

Keywords: ZTC Bias Point, GZTC Bias Point, CMOS Analog Integrated Circuits, Low Temperature Sensitivity Transconductors, Voltage Reference, Current Reference.

MODELAMENTO E ANÁLISE DO EFEITO DE COEFICIENTE NULO DE TEMPERATURA (ZTC) DO MOSFET PARA APLICAÇÕES ANALÓGICAS DE BAIXA SENSIBILIDADE TÉRMICA

RESUMO

A contínua miniaturização das tecnologias CMOS oferece maior capacidade de integração e, consequentemente, as variações de temperatura dentro de uma pastilha de silício têm se apresentado cada vez mais agressivas. Ademais, dependendo da aplicação, a temperatura ambiente a qual o CHIP está inserido pode variar. Dessa maneira, procedimentos para diminuir o impacto dessas variações no desempenho do circuito são imprescindíveis. Tais métodos devem ser incluídos em ambos fluxos de projeto CMOS, analógico e digital, de maneira que o desempenho do sistema se mantenha estável quando a temperatura oscilar. A ideia principal desta dissertação é propor uma metodologia de projeto CMOS analógico que possibilite circuitos com baixa dependência térmica. Como base fundamental desta metodologia, o efeito de coeficiente térmico nulo no ponto de polarização da corrente de dreno (ZTC) e da transcondutância (GZTC) do MOSFET são analisados e modelados. Tal modelamento é responsável por entregar ao projetista analógico um conjunto de equações que esclarecem como a temperatura influencia o comportamento do transistor e, portanto, o comportamento do circuito. Essas condições especiais de polarização são analisadas usando um modelo de MOSFET que é contínuo da inversão fraca para forte. Além disso, é mostrado que as duas condições ocorrem em inversão moderada para forte em qualquer processo CMOS. Algumas aplicações são projetadas usando a metodologia proposta: duas referências de corrente baseadas em ZTC, duas referências de tensão baseadas em ZTC, e quatro circuitos gm-C polarizados em GZTC. A primeira referência de corrente é uma Corrente de Referência CMOS Auto-Polarizada (ZSBCR), que gera uma referência de 5 μA. Projetada em CMOS 180 nm, a referência opera com uma tensão de alimentação de 1.4 à 1.8 V, ocupando uma área em torno de $0.010mm^2$. Segundo as simulações, o circuito apresenta um coeficiente de temperatura efetivo (TC_{eff}) de 15 ppm/^{o}C para -45 à +85 ^{o}C e uma sensibilidade à variação de processo de $\sigma/\mu = 4.5\%$ incluindo efeitos de variabilidade dos tipos processo e descasamento local. A sensibilidade de linha encontrada nas simulações é de $1\%/V$. A segunda referência de corrente proposta é uma Corrente de Referência Sem Resistor Auto-Polarizada com Capacitor Chaveado (ZSCCR). O circuito é projetado também em 180 nm, resultando em uma corrente de referência de 5.88 μA, para uma tensão de alimentação de 1.8 V, e ocupando uma área de $0.010mm^2$. Resultados de simulações mostram um TC_{eff} de 60 ppm/^{o}C para um intervalo de temperatura de -45 à +85 ^{o}C e um consumo de potência de 63 μW. A primeira referência de tensão proposta é uma Referência de Tensão resistente à pertubações eletromagnéticas contendo apenas MOSFETs (EMIVR), a qual gera um valor de referência de 395 mV. O circuito é projetado no processo CMOS 130 nm, ocupando em torno de 0.0075 mm^2 de área de silício, e consumindo apenas 10.3 μW. Simulações pós-leiaute apresentam um TC_{eff} de 146 ppm/^{o}C, para um intervalo de temperatura de -55 à $+125^o$C. Uma fonte EMI de 4 dBm (1 V_{pp} de amplitude) aplicada na alimentação do circuito, de acordo

com o padrão Direct Power Injection (DPI), resulta em um máximo de desvio DC e ondulação Pico-à-Pico de -1.7 $\%$ e 35.8m V_{pp}, respectivamente. A segunda referência de tensão é uma Tensão de Referência baseada em diodo Schottky com 0.5V de alimentação (SBVR). Ela gera três saídas, cada uma utilizando MOSFETs com diferentes tensões de limiar (standard-V_T, low-V_T, e zero-V_T). Todos disponíveis no processo adotado CMOS 130 nm. Este projeto resulta em três diferentes voltages de referências: 312, 237, e 51 mV, apresentando um TC_{eff} de 214, 372, e 953 ppm/^{o}C no intervalo de temperatura de -55 à 125°C, respectivamente. O circuito ocupa em torno de 0.014 mm^2, consumindo um total de 5.9 μW. Por último, circuitos gm-C são projetados usando o conceito GZTC: um emulador de resistor, um inversor de impedância, um filtro de primeira ordem e um filtro de segunda ordem. Os circuitos também são simulados no processo CMOS 130 nm, resultando em uma melhora na estabilidade térmica dos seus principais parâmetros, indo de 27 à 53 ppm/^{o}C.

Palavras-chave: Ponto de Operação ZTC, Ponto de Operação GZTC, Circuitos Integrados Analógicos CMOS, Transcondutores com baixa sensibilidade térmica, Referências de Tensão, Referências de Corrente.

LIST OF FIGURES

1.1	Thermal map of an integrated microprocessor highlighting on-chip temperature variation. Temperature gradient between a microprocessor core and an on-chip cache.	21
1.2	Impact of technology scaling on power density. α features each technological node (μm).	22
1.3	CPU cooling system.	22
1.4	TCP/IP offload accelerator engine fabricated in 90nm CMOS.	23
1.5	Trends in integration strategies.	24
1.6	Ultra-low-power 2.4-GHz wireless transmit efficiency. The arrow shows the desired trends. All symbols except the red squares represent ISSCC papers. The ISSCC 2015 paper numbers are indicated next to the red circles.	24
2.1	NMOSFET ZTC point for (a) 180nm and (b) 350 nm processes.	28
2.2	Planar MOSFET transistor.	29
2.3	Connections among external voltages, interfaces characteristics and drain current.	30
2.4	$V_{S(D)B}$ vs. $\psi_{SS(D)}$.	31
2.5	I_D Drift and diffusion current comprise ids.	32
2.6	V_{GB} vs. $\psi_{SS(D)}$.	33
2.7	$Q'_{I(D)S}$ vs. $V_{S(D)B}$.	34
2.8	Connections among external voltages, interfaces characteristics, and drain current using UICM model.	34
2.9	(a) V_{T0} versus temperature for different values of V_{SB} (0 to 100 mV) and $V_{GB} = 900mV$ in a 180nm CMOS process (b) $\alpha_{V_{T0}}$ vs. N_A for different t_{ox}.	36
2.10	μ vs. temperature for different N_A.	37
2.11	Threshold voltage (left), slope factor (center), and Mobility in saturation (right), as a function of channel length and temperature, NMOS (upper) and PMOS (lower) devices of a 110 nm CMOS technology.	38
2.12	(a) Oscillation frequency (f_{osc}) vs. supply voltage (V_{DD}) for different temperature and (b) Oscillation frequency (f_{osc}) vs. temperature. These are simulated data of 130 nm CMOS technology using an inverter with L = 130nm, W_n = 130 nm and W_p = 520 nm. L is length, W_n and W_p are the widths of NMOS and PMOS transistor, respectively.	40

2.13 (a) Measured characteristics for DMESFET of form factor W/L = 50/2 in linear region and saturation region (b) TC_{eff} for Diode Zenner for different terminal voltage. (c) Experimental I_D vs. V_G and g_m characteristics of n-channel DTMOS in the linear region over a temperature range of 25^oC to 125^oC. Note that the ZTC point is 0.85 V when V_{DS} = 0.1 V in the linear region. (d) Theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor in both the linear and saturation regions. 44
2.14 Measured and simulated gate bias (V_{GZ}) and drain current (I_{DZ}) at the ZTC point with drain bias (V_{DS}) in both linear and saturation regions for NMOS ($\frac{W}{L} = \frac{30\mu m}{10\mu m}$) and PMOS($\frac{W}{L} = \frac{30\mu m}{5\mu m}$). 45
2.15 Gate capacitance versus gate voltage for (a) different body doping (at Vds = 0) and (b) different gate-oxide thickness (at Vds = 2 V), at 27 °C (solid line), 150 °C (dotted line), and 300 °C (dashed line) from an ideal MOS transistor, with the corresponding ZTC points extracted from the numerical data (symbols). Drain current versus gate voltage in (c) linear (Vds = 0.1 V) and (d) saturation (Vds = 2 V) modes for different body doping as indicated, at 27 °C (solid line), 150 °C (dotted line), and 300 °C (dashed line) from an ideal MOS transistor, with the corresponding ZTC points extracted from the numerical data (symbols). 46
2.16 (a) Contour plots of constant $V_{ztc,ds}$ (solid line) and V_{GZ} (dotted line) extracted from the compact ZTC charge and current models, respectively, due to body doping and gate oxide thickness variations. The box illustrates a process window around the nominal values of N_A = 10^{18} cm^{-3} and t_{ox} = 2 nm, which predicts a potential $V_{ztc,ds}$ variation from 0.5 V to 0.7 V and V_{GZ} variation from 0.85 to 1.3 V, respectively, if the variations in N_A and t_{ox} are given within the box. (b) Contour plot of constant V_{GZ} extracted from the compact ZTC drain current model at any V_{DS} due to body doping variations for devices operating in partial, dynamic, and full depletion modes. 47
2.17 ZTC forward inversion level Surface (ZTCS). Graphic made with the script of appendix C. 52
2.18 V_{OVZ} - the ZTC overdrive voltage. Graphic made with the script of appendix C. 53
2.19 $(\frac{g_{mg}}{I_D})_Z$ or g_{mg} over I_D biased on i_{fz}. Graphic made with the script of appendix C. 54
2.20 $V_{GB}(T)$ for $\Delta I_d > 0$, $\Delta I_d = 0$ and $\Delta I_d < 0$. Simulated data from 180 nm CMOS technology. 56
2.21 β_z in function of $|\alpha_{V_{T0}}|$. Note that, for adopted assumption $\alpha_\mu \approx -2$, β_z is always negative since it is only dependent of $\alpha_{V_{T0}}$. Graphic made with the script of appendix C. 56
2.22 (a) simulations data for a diode-connected NMOS transistor (W/L = $2.5\mu m/1\mu m$) in 180 nm CMOS technology with five different bias current (5, 20, 26.25, 35, 50 μA), yielding distinct V_{GB} temperature dependence. (b) V_{GB} versus temperature enforcing right TC_I that cancels PTAT or CTAT behavior. (c) Zoom for $I_D = 5\mu A$. (d) Zoom for $I_D = 20\mu A$. 57

2.23 (a) Zoom for $I_D = 35\mu A$. (b) Zoom for $I_D = 50\mu A$. (c) Zoom for $I_D = 26.25\mu A$. (d) TC_{eff} for each vicinity condition. 58
2.24 i_{f0} in function of TC_I and $\alpha_{V_{T0}}$. Graphic made with the script of appendix C. 59
2.25 Overdrive voltage change around ZTC point (TC_I = 0) for different values of current temperature coefficients (TC_I). Graphic made with the script of Appendix C. 60
2.26 (a) The MOSFET operating plane illustrating tradeoffs in performance for the selected inversion coefficient and channel length. Copyright John Wiley and Sons Limited. (b) MOSFET operating plane translated to UCIM presented before including temperature behavior of MOSFET transistor. 61
2.27 (a) ZTC forward inversion level surface (ZTCS) and GZTC forward inversion level surface (GZTCS) (b) overdrive voltage for the ZTC (V_{OVZ}) and GZTC bias point (V_{OVGZ}) as a function of the values for α_μ and $\alpha_{V_{T0}}$. Graphics made with the script of Appendix C. 64
2.28 ZTC and GZTC condition for a PMOS transistor in a 130 nm process with $V_{T0} = 250$ mV. These curves have been plotted using V_{DS} = V_{GS}. 65
2.29 Necessary TC_I, or TC_{IGZ}, to keep the MOSFET transconductance temperature independent in function of $|\alpha_{V_{T0}}|$ and α_μ. Graphic made with the script of appendix C. 65

3.1 Idea of proposed Self-biased CMOS Current Reference based on ZTC Operation Condition. 67
3.2 Self-biased CMOS Current Reference based on ZTC Operation Condition 68
3.3 Numerical Sizing with Wicked^{TM}. 69
3.4 Layout - 100μm X 100μm 70
3.5 Idea of proposed Resistorless Self-Biased ZTC Switched Capacitor Current Reference. 72
3.6 (a) The ZTC Switched Capacitor Current Reference (ZSCCR). (b) ZSCCR Layout - 100μm X 100μm in 180 nm CMOS process. 73
3.7 Basic concept of a bandgap voltage reference. 76
3.8 (a) Proposed EMI resisting CMOS voltage reference schematic circuit. (b) Layout Area: 81 μm X 88 μm 77
3.9 The thermal cancellation strategy used in proposed EMI Resisting MOSFET-Only Voltage Reference 78
3.10 Poles and Zeros related to nodes and feedback capacitance in proposed EMI Voltage reference, respectively. 80
3.11 Proposed 0.5-V CMOS voltage reference schematic circuit. 82
3.12 Low-voltage supply PTAT current reference. 83
3.13 Proposed 0.5-V CMOS voltage reference layout. 84
3.14 PMOS differential pair with active load. 85
3.15 (a) single-ended resistor emulator (b) impedance inverter (c) first order filter (d) second order filter. 87

4.1 (a) Test die inside of MLM2013 reticle (b) Micrograph of IBM 130 nm die. 89

4.2 Self-biased CMOS Current Reference based on ZTC Operation Condition . . . 90
4.3 Current Reference vs. temperature . . . 91
4.4 Normalized Power Supply Sensitivity . . . 91
4.5 (a) I_{REF} Monte Carlo simulation including process and mismatch. (b) I_{REF} Monte Carlo simulation only for mismatch. (c) TC_{eff} Monte Carlo simulation including process and mismatch. (d) TC_{eff} Monte Carlo simulation only for mismatch. . . . 93
4.6 ZTC Switched Capacitor Current Reference (ZSCCR). . . . 94
4.7 I_{REF} in time domain . . . 95
4.8 I_{REF} vs. Temperature . . . 95
4.9 Gain loop transfer function. (a) Magnitude (b) Phase. PSS+PSTB analyzes were performed for this result. . . . 96
4.10 Proposed EMI resisting CMOS voltage reference schematic circuit. . . . 98
4.11 V_{REF} vs Temperature. (b) Power Supply Rejection Ratio of V_{REF} . . . 98
4.12 V_{REF} Power Supply Rejection Ratio . . . 99
4.13 V_{REF} Power Supply Rejection Ratio . . . 99
4.14 Micrograph of a small area of the chip, fabricated in IBM 130nm, where the proposed V_{REF} is highlighted. . . . 100
4.15 V_{REF} vs. V_{DD}, dies # 1-5 . . . 101
4.16 (a) DC shift as a function of the EMI frequency and temperature. (b) Peak-to-peak ripple on V_{REF} as a function of the EMI frequency and temperature. EMI level = 4 dBm . . . 102
4.17 (a) DC shift process sensitivity as a function of the EMI frequency and temperature. (b) Peak-to-peak ripple process sensitivity on V_{REF} as a function of the EMI frequency and temperature. EMI level = 4 dBm . . . 103
4.18 Proposed 0.5-V CMOS voltage reference schematic circuit. . . . 105
4.19 PTAT current reference variation over temperature. . . . 105
4.20 Voltage reference (standard-V_T) variation over temperature. . . . 106
4.21 Voltage reference (low-V_T) variation over temperature. . . . 107
4.22 Voltage reference (zero-V_T) variation over temperature. . . . 107
4.23 Power supply rejection ratio of the proposed voltage reference. . . . 108
4.24 Micrograph of our proposed 0.5 V Voltage Reference in IBM 130 nm die . . . 109
4.25 (a) Measurements line sensitivity for 5 samples (b) V_{REF} for each sample (c) All Line Regulation (LR) measurements for each output (d,e,f) V_{REF} versus temperature for $V_{REF,SVT}$, $V_{REF,LVT}$ and $V_{REF,ZVT}$ reference voltages, respectively. . . . 110
4.26 (a) single-ended resistor emulator (b) impedance inverter (c) first order filter (d) second order filter. . . . 112
4.27 (a) Input impedance of single-ended resistor emulator (b) Equivalent Resistance vs. Temperature. Effective Temperature Coefficient is given by $TC_{eff} = \frac{I_{REF_{max}} - I_{REF_{min}}}{(T_{max} - T_{min}) I_{REF(T_0)}}$. . . . 112
4.28 (a) Equivalent Inductance vs. Temperature (b) Dominant Pole vs. Temperature. . . . 113
4.29 Quality Factor vs. Temperature. . . . 114

4.30 Dominant pole Monte Carlo simulations for a temperature range of -45 to 85^oC. For each temperature (-45,-15, 27, 55 and 85 ^oC), 1000 samples were performed. 114

5.1 Second order effects on ZTC bias point 117
5.2 Short channel effects on ZTC bias point 117

A.1 Classical two-stage Miller amplifier. 128
A.2 Miller Amplifier: (a) GBW (b) Integrated Noise (c) PM (d) Slew Rate. 129

C.1 Script Structure 133

LIST OF TABLES

2.1 MOSFET Parameters extraction for 110 nm CMOS technology. . . . 38
2.2 ZTC Operating Point with $\frac{W}{L} = \frac{10\mu m}{1\mu m}$ 43
2.3 MOSFET ZTC Operating Point 43

3.1 Device Sizing of proposed ZSBCR 71
3.2 Device Sizing of proposed ZSCCR 75
3.3 Device Sizing of proposed EMIVR 81
3.4 Device Sizing of proposed SBVR 84

4.1 Comparison of CMOS Current References 92
4.2 Comparison of CMOS Current References 97
4.3 Simulated Performance of the voltage reference. 100
4.4 Comparison with other works. 104
4.5 Simulated Performance of the SUB-1V V_{DD} Schottky based reference. 108
4.6 Performance comparison for SUB-1V V_{DD} Schottky based reference 109

A.1 Miller amplifier specifications 129

LIST OF ABBREVIATIONS AND ACRONYMS

CMOS	Complementary metal-oxide-semiconductor
IC	Integrated Circuits
ZTC	Zero Temperature Coefficient
GZTC	Transconductance Zero Temperature Coefficient
MOSFET	Metal-oxide-semiconductor Field Effect Transistor
NMOSFET	N-channel MOSFET
PMOSFET	P-channel MOSFET
ZSCCR	Resistorless Self-Biased ZTC Switched Capacitor Current Reference
ZSBCR	ZTC Self-biased CMOS Current Reference
EMI	Electro-Magnetic Interference
EMIVR	EMI Resisting MOSFET-Only Voltage Reference
SBVR	Schottky-based Voltage Reference
TCP/IP	Transmission Control Protocol/Internet Protocol
SOC	System-on-Chip
IOT	Internet of Things
SDCR	Software Defined Cognitive Radio
WSN	Wireless Sensor Network
RF	Radio Frequency
PA	Power Amplifier
ISSCC	International Solid-State Circuits Conference
MESFET	Metal-Semiconductor Field Effect Transistor
SOI	Silicon on Insulator
3D	Three Dimensions
DC	Direct Current
AC	Alternate Current
UCCM	Unified Charge-Control Model

ADF	Analog Design Flow
UICM	Unified Current Control Model
BSIM	Berkeley Short-Channel IGFET Model
DIBL	Drain-Induced Barrier Lowering
ITD	Inverted Temperature Dependence
STA	Static Timing Analysis
DTMOS	Dynamic Threshold Voltage MOSFET
VLSI	Very-Large-Scale Integration
PD-SOI	Partially Depleted Silicon-on-Isolator
ZTCS	ZTC Forward Inversion Level Surface
PTAT	Proportional to Temperature Absolute Temperature
CTAT	Complementary to Temperature Absolute Temperature
TC	Temperature Coefficient
GZTCS	GZTC Forward Inversion Level Surface
OTA	Operational Transconductance Amplifier
KVL	Kirchoff's Voltage Law
GBW	Gain-bandwidth Product
FEA	Feasibility Optimization
DNO	Deterministic Nominal Optimization
YOP	Yield Optimization
MIM	Metal-Insulator-Metal
PSRR	Power Supply Rejection Ratio
SBCR	Self-Biased Current Reference
SCM	Self-Cascode MOSFET
PN	p-type and n-type
OA	Operational Amplifiers
RC	Resistor-Capacitor
CML	Current-Mode-Latch
CL-LDO	Capacitor-Less Low Drop-Out
PCB	Printed-Circuit Board
LNTA	Low Noise Transconductance Amplifier
LNA	Low Noise Amplifier
PVT	Process-Voltage-Temperature
IBM	International Business Machines Corporation

MLM	Multi-Layer Mask
MC	Monte Carlo
PSS	Periodic Steady-State
PSTB	Periodic Stability
KHz	KiloHertz
MHz	MegaHertz
GHz	GigaHertz
DPI	Direct Power Injection
dBm	decibel-milliwatts
dB	Decibel
VR	Voltage-Reference
LR	Line Regulation
SVT	Standard VT
LVT	Low VT
ZVT	Zero VT
IEEE	Institute of Electrical and Electronics Engineers

CONTENTS

1 INTRODUCTION 20
1.1 Thermal effects in CMOS digital circuits 20
1.2 Thermal effects in CMOS analog and mixed-signal circuits 23
1.3 Motivation 25
1.4 Contributions and Thesis Organization 25

2 THE ZERO TEMPERATURE COEFFICIENT (ZTC) CONDITION 27
2.1 Continuous all-regime MOSFET model 28
2.2 MOSFET thermal dependence 36
2.3 ZTC Condition 39
2.4 MOSFET Bias ZTC Condition Analysis 48
2.4.1 ZTC Bias from Strong Inversion MOSFET Model 48
2.4.2 ZTC Bias from UICM All-regime MOSFET Model 50
2.4.3 ZTC Bias Vicinity Condition from UICM Model 54
2.5 MOSFET Transconductance ZTC Condition 62

3 ANALOG APPLICATIONS USING ZTC CONDITION 66
3.1 Self-biased CMOS Current Reference based on ZTC Operation Condition - ZSBCR 66
3.1.1 Circuit Analysis 67
3.1.2 Circuit Design 69
3.1.3 Layout 70
3.2 Resistorless Self-Biased ZTC Switched Capacitor Current Reference - ZSCCR 71
3.2.1 Circuit Analysis and Design 72
3.2.2 Layout 74
3.3 Electromagnetic Interference (EMI) Resisting MOSFET-Only Voltage Reference - EMIVR 75
3.3.1 Circuit Analysis and Design 77
3.3.2 Layout 81
3.4 0.5 V Supply Schottky-diode based Voltage Reference - SBVR 81
3.4.1 Circuit Analysis and Design 82
3.4.2 Layout 84
3.5 GZTC Based Gm-C Filters 85
3.5.1 Circuit Analysis and Design 87

4 SIMULATIONS AND MEASUREMENTS RESULTS 89
4.1 Self-biased CMOS Current Reference based on ZTC Operation Condition - ZSBCR 90
4.2 Resistorless Self-Biased ZTC Switched Capacitor Current Reference - ZSCCR 94
4.3 Electromagnetic Interference (EMI) Resisting MOSFET-Only Voltage Reference - EMIVR 98
4.4 0.5 V Supply Schottky-diode based Voltage Reference - SBVR 105
4.5 GZTC Based Gm-C Filters 111

5 CONCLUSION 115
5.1 Future Work 116

REFERENCES 119

LIST OF PUBLICATIONS 126

APPENDIX A IMPACT OF TEMPERATURE VARIATIONS ON TWO-STAGE MILLER AMPLIFIER 128

APPENDIX B EXPRESSIONS 130
B.1 $\frac{\partial\mu}{\partial T} = \frac{\mu\alpha_\mu}{T}$ 130
B.2 $\frac{\partial\phi_t}{\partial T} = \frac{\phi_t}{T}$ 130
B.3 $\frac{\partial\phi_t^2}{\partial T} = \frac{2}{T}\phi_t^2$ 131
B.4 GZTC Condition - $(\partial g_{mg})/(\partial T)|_{T=T_1} = 0$ 131

APPENDIX C OCTAVE SCRIPTS 133
C.1 ZTCAnalysisTotal.m 134
C.2 ZTCAnalysis.m 134
C.3 SlopeZTCAnalysis.m 135
C.4 ZTCAnalysisgm.m 136
C.5 ZTCAnalysisTCigm.m 137
C.6 VinZTCAnalysis.m 138
C.7 fowardZTC.m 141
C.8 fowardZTCgm.m 141
C.9 VinFowardZTC.m 141

APPENDIX D SUMMARY IN PORTUGUESE 142
D.1 INTRODUÇÃO - CAPÍTULO 1 143
D.2 MODELAMENTO ZTC E SUAS APLICAÇÕES - CAPÍTULO 2, 3 E 4 143
D.2.1 MODELAMENTO ZTC - CAPÍTULO 2 143
D.2.2 APLICAÇÕES BASEADAS EM ZTC - CAPÍTULO 3 E 4 144
D.3 CONCLUSÃO - CAPÍTULO 5 146
D.3.1 TRABALHOS FUTUROS 146

1 INTRODUCTION

Solid-state circuits and temperature have had a close relationship since the beginning of electrical physical and electronics developments. In 1600 CE, William Gilbert described how increasing temperature reduced the attraction between oppositely charged objects [GILBERT (1600)]. In 1821 CE, Sir Humphry Davy presented to the Royal Society of London the results of an experiment in which [SMITH; CO (1840)] "the conducting power of metallic bodies varied with the temperature, and was lower, in some inverse ratio, as the temperature was higher." One year later, in 1822 CE, Thomas Johann Seebeck noted that when the junction temperature of two dissimilar metals increased, a current was created. This phenomenon is the Seebeck or thermoelectric effect [SEEBECK (1840)]. One of the most important temperature-related material discoveries happened in 1833 when Michael Faraday noticed that silver sulphide was conductive at high temperatures and nearly insulating at low temperatures [FARADAY (1839)]. This was in direct contrast to the temperature dependence observed in metals, which become less conductive as the temperature is increased. Faraday had discovered the semiconductor, and the reasoning behind this new relationship between temperature and current was later linked to the thermal excitation of carriers.

Afterwards, a similar principle was discovered by Jean Charles Athanase Peltier in 1834 CE, who found that when current flows through such a junction, heat is absorbed from one end of the junction and moved to the other [PELTIER (1834)]. This effect is material dependent; the material's majority carrier determines whether heat flows in the same direction as the current or the opposite direction. The Peltier effect (or Peltier–Seebeck effect) is now commonly used in electronic heat transfer and cooling systems, including small electric refrigerators. The Peltier and Seebeck effects have also been examined for regulating chip temperature and recycling thermal energy back into electrical[GOULD et al. (2008)]. The findings of Davy, Seebeck, Peltier, and Faraday have laid the foundation for the impact of temperature on current electronic systems.

1.1 Thermal effects in CMOS digital circuits

In current literature, there are two definitions of temperature variation that can affect system performance: global temperature variations and local temperature variations. Changes in ambient temperature or cooling capacity cause global temperature variations (Cooler uses Seebeck-Peltier effect to control and minimize the impact of temperature on chip performance). For instance, the United States military IC requirements define the range of ambient temperature extend from -55 ^{o}C to 125 ^{o}C as operation regime [DEFENSE (2012)]. The intra-die disparity in power dissipation between active units and inactive units can result in severe hot spots on a chip. These disparities define local tem-

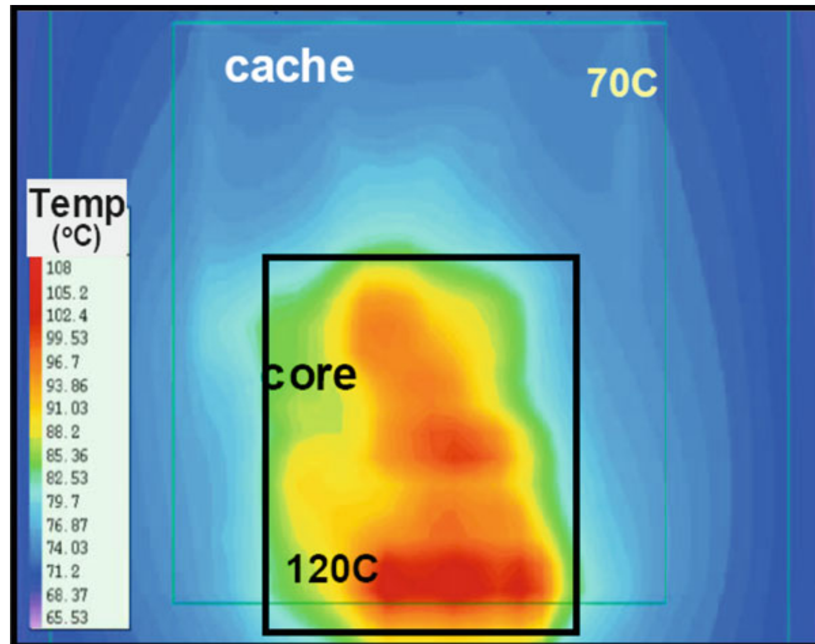


Figure 1.1: Thermal map of an integrated microprocessor highlighting on-chip temperature variation. Temperature gradient between a microprocessor core and an on-chip cache.

perature variation. Intra-die temperature variations exceeding 50 ^oC have been reported at [SATO et al. (2005)].

From current CMOS digital design point of view, power dissipation in silicon is related to temperature through the material's thermal conductivity, measured in Watts per meter Kelvin (W/(m·K)). This relation translates as where in the digital core the activity is concentrated, and the temperature is the highest. At the same time, variations in temperature affect the conductivity of the material, i.e., alters transistor performance inside of each logic gate, which affects the speed of computation in the systems. These changes in temperature inside digital circuits can have catastrophic effects on system performance and functionality, and are becoming increasingly problematic as technologies scale. In other words, as power dissipation increase beyond our ability to distribute and remove the generated heat, local temperatures will continue to rise. The potential for delay failure will grow consequently affecting the time slack of the whole system. To illustrate, Fig. 1.1 shows a typical thermal map between a cache memory and an integrated microprocessor [SATO et al. (2005)]. In more advanced technological nodes, thermal activity has been more aggressive as shown in Fig. 1.2. The cause is due to more powerful digital processing capability per area [SATO et al. (2005)].

The performance degradation in CMOS digital circuits due to changes in temperature (global temperature variation) and/or problem of power dissipation (local temperature variation) has brought about the development of better cooling systems (external temperature control) and immense improvements in optimizing on-chip power dissipation (internal temperature control). Fig. 1.3 shows a common implementation of a passive cooling system, including the chip, heat spreader, and heat sink [WOLPERT; AMPADU (2012)]. Thermal interface material is a high thermal conductivity substance used to improve the flow of heat between each separate component. This technique is a method to control the IC temperature externally.

Besides external thermal control (e.g. using cooler), on-chip mechanisms for thermal

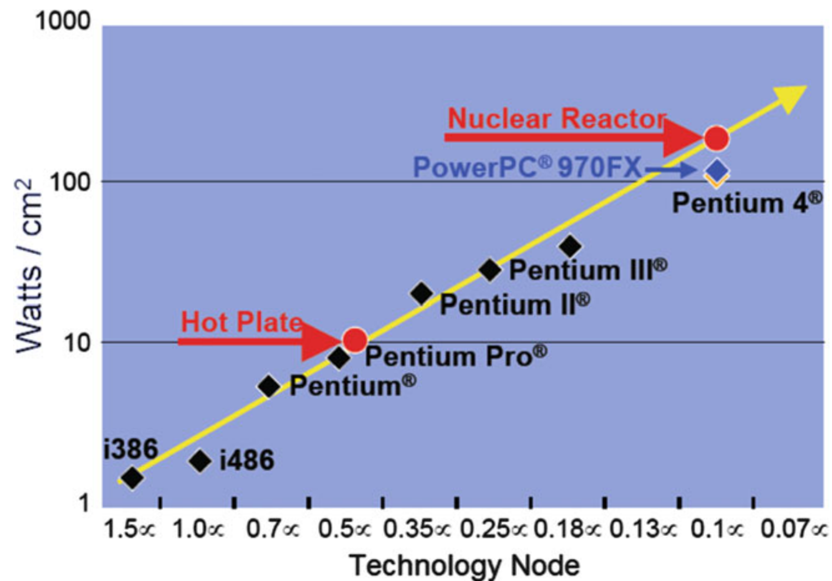


Figure 1.2: Impact of technology scaling on power density. α features each technological node (μm).

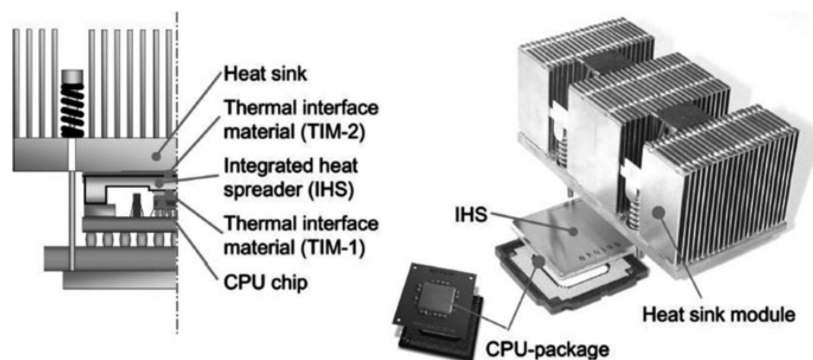


Figure 1.3: CPU cooling system.

control can be adopted as well. In applications with larger power densities, digital designers can try to reduce the occurrence of hotspots. They can, for example, be reduced at design level using thermally-aware floorplanning techniques [WOLPERT; AMPADU (2012)], in which units with large power dissipation are spread evenly across the chip. Another strategy is to use adaptive measures such as thermal throttling which improve reliability by adjusting the processor frequency and supply voltage when high-temperature spots are detected. For instance, Fig. 1.4 shows a TCP/IP offload accelerator engine fabricated in 90nm CMOS, which improves reliability by adjusting the processor frequency and supply voltage when high-temperature conditions are identified. These adaptive systems can be useful for mobile applications as well, detecting when a chip is brought into a hot environment and reducing its processor speed to avoid timing failures [TSCHANZ et al. (2007)].

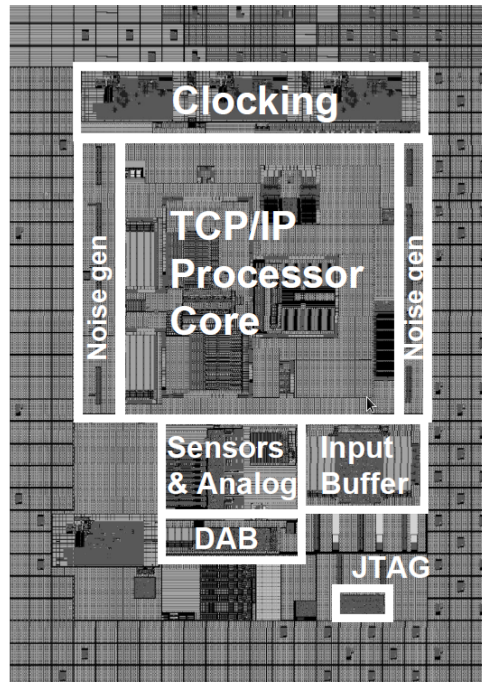


Figure 1.4: TCP/IP offload accelerator engine fabricated in 90nm CMOS.

1.2 Thermal effects in CMOS analog and mixed-signal circuits

In addition to ambient temperature variations, temperature changes due to internal power dissipation also affect analog circuits. Bias conditions and performances such as gain, bandwidth, slew rate, offsets, noise, impedance, stability are modified (See, for example, the temperature variation impact on classical CMOS two-stage Miller Amplifier in Appendix A). This effect has been more evident on the current trend of mixed-signal System-on-Chip (SoC) solutions. Internet of Things (IoT), Software Defined Cognitive Radios (SDCR), and Wireless Sensor Network (WSN) are few applications examples that enforce even more the current trend for SoC solutions: integration of digital and Analog/RF parts in a unique chip [NARENDRA; FUJINO; SMITH (2015)]. For these IC systems, variations on circuit performance changed by different temperature operation will be increasingly visible, thus justifying that techniques to mitigate these performances degradations is of great importance for analog circuits. Fig 1.5 depicts some current (2000-2015) state-of-art SoCs that have the digital and Analog/RF part integrated into the same die.

The digital core is not the only responsible for chip self-heating (Section 1.1). In wireless communications SoCs, for example, some Radio Frequency (RF) blocks are also power hungry. The Power Amplifier (PA) will also contribute to SoC temperature increase. Fig. 1.6 shows state-of-art Ultra-low-power 2.4-GHz wireless transmit efficiency (PA inside it), and it reveals that commercial chips consuming around 30-100 mW with efficiency between 3-30% can be found in the market. This power consumption level certainly contributes to the change of temperature profile spread all over SoC. Indeed, ambient temperature, digital core operation mode, and analog circuit consumption cause temperature variation within a mixed-signal SoC. This variation demands that, in addition to proper functioning of the digital part, the analog section must operate correctly fulfilling all required performances under the required temperature range.

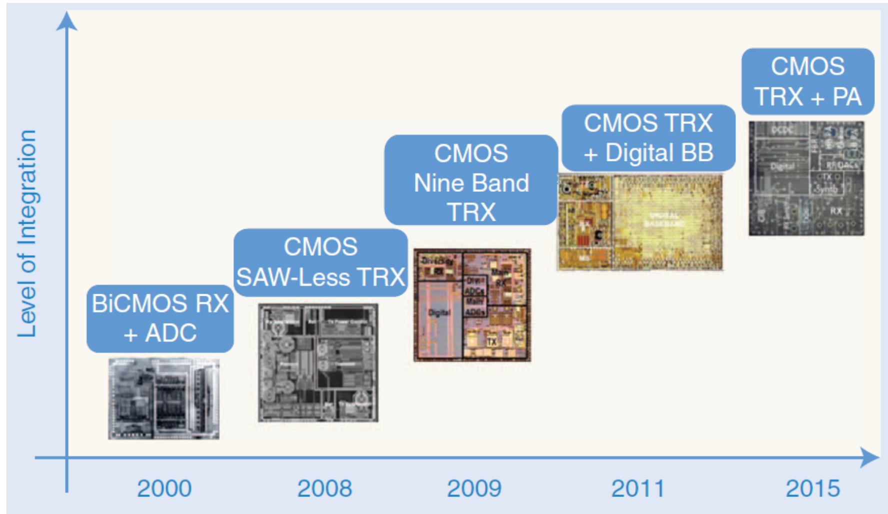


Figure 1.5: Trends in integration strategies.

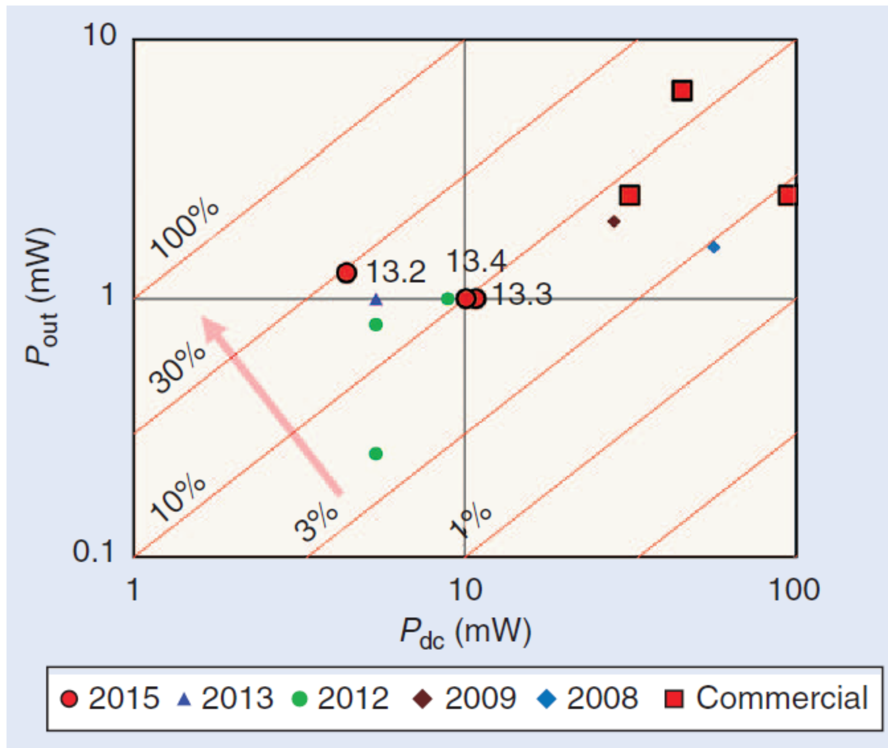


Figure 1.6: Ultra-low-power 2.4-GHz wireless transmit efficiency. The arrow shows the desired trends. All symbols except the red squares represent ISSCC papers. The ISSCC 2015 paper numbers are indicated next to the red circles.

1.3 Motivation

Continuing scaling of CMOS technologies brings more integration (the literature currently shows Mixed-Signal SoC attaching 5.6 Billion transistors in a single die [NARENDRA; FUJINO; SMITH (2015)]) and consequently temperature variation has become more aggressive. In addition, depending on application the room temperature ambient can vary. Therefore, procedures to decrease thermal dependencies in electronic circuit performances become an important issue to include in both digital and analog IC design flow.

The main objective of this thesis is to generate a set of equations that provides to the analog designer insights regarding temperature variations during a typical Analog CMOS design flow. In this way, some precautions can be adopted during an analog block sizing. As transistor sizing is inherent in analog block development, Bias MOSFET Zero Temperature Coefficient (ZTC) and Transconductance Zero Temperature Coefficient (GZTC) operating bias points are investigated. They are used as references to deliver equations that inform the designer how temperature changes transistor operation and consequently circuit behavior.

To demonstrate that (G)ZTC bias points are good candidates as reference points for low temperature sensitivity CMOS analog circuit, some circuits are designed: two new ZTC-based current references, two new ZTC-based voltage references, and four classical Gm-C filters biased at GZTC bias point.

1.4 Contributions and Thesis Organization

During whole MOSFET ZTC condition investigation and its application to analog circuit design, this thesis produced interesting contributions listed below.

- The ZTC modeling developed here used an all-region MOSFET modeling that is continuous from weak to strong inversion [SCHNEIDER; GALUP-MONTORO (2010)], showing that this condition always occurs from moderate to strong inversion operation in any CMOS fabrication process. It worth to mention that until this moment this effect had only been modeled in strong inversion regime.
- As consequence, the same transistor model was also used to model the ZTC behavior in MOS transconductance.
- To generate design insights regarding temperature variations on MOS transistor, the ZTC vicinity concept was addressed, showing that MOS transistor temperature behavior can be adjusted according to the interest of analog designer.
- Both concepts, ZTC, and its vicinity were used to generate two new current references and two new voltage references.
- Lastly, the ZTC condition in MOS transconductance was applied in transconductors inside of some Gm-C filters, providing circuits with low thermal dependence on their performance.

The text is organized as follows. Chapter 2 presents the ZTC concept using MOSFET transistor as a first example. A brief review of the ZTC condition in some other electronic devices such as Zenner Diode, MESFET, and Fully Depleted SOI MOSFET are discussed in chronological order. After, in the same chapter, a MOSFET ZTC modeling for both drain current and transconductance is analytically derived through a continuous MOSFET model that is valid from weak to strong inversion. The modeling determines

that these conditions will always happen in moderate to strong inversion. Also, a ZTC Vicinity behavior is studied, and some insights on how the transistor behaves in function of temperature are discussed. In chapter 3, two novel voltage and current references and some typical gm-C filter are designed using suggested all-region ZTC modelings in two different CMOS processes. Chapter 5 analyzes thorough simulation results and makes a fair comparison against state-of-art implementations. The thesis concludes pointing out to future directions for the further development of ZTC modeling and its applications.

2 THE ZERO TEMPERATURE COEFFICIENT (ZTC) CONDITION

The MOSFET ZTC condition derives from the mutual cancelation of mobility and threshold voltage dependencies on temperature [FILANOVSKY; ALLAM (2001)], at a particular gate-to-bulk voltage bias. This condition defines a bias point (V_{GZ}, I_{DZ}) where the drain current presents small temperature sensitivity, as Fig. 2.1 exhibits.

The ZTC drain current condition occurs for any MOSFET in every planar technology, for N and PMOS transistors, and this bias point depends on process parameters (mobility and threshold voltage dependencies on temperature). Remembering that the drain current increases when mobility increases and when threshold voltage decreases, and that mobility and threshold voltage both decrease when temperature increases, it can be proved that both effects can cancel each other at a certain bias point. Fig. 2.1 presents the drain current vs. gate-bulk voltage of NMOS transistors under three temperatures for two different fabrication process, and in both figures a convergence point can be seen for the three I-V curves drawn. Fig. 2.1 (a) shows the drain current (on a log scale) as a function of the gate-bulk voltage (V_{GB}) of a saturated long-channel NMOSFET. In the simulation, the temperature ranged from -45^oC to $+85^oC$, for a 180 nm process. The ZTC operation point can be seen around $V_{GB} \approx 760mV$ for a transistor with $V_T = 430mV$, resulting that ZTC point occurs for an overdrive voltage around 330mV, meaning the transistor operates in strong inversion. Fig. 2.1 (b) shows the same for an NMOS transistor in a 350 nm CMOS process.

The traditional analysis of this effect presented in the literature is based on the strong inversion quadratic MOSFET model [FILANOVSKY; ALLAM (2001)]. However, this effect can be found in moderate inversion regime as well (always above the threshold voltage). This statement is theoretically demonstrated as fact during this chapter and confronted with extracted ZTC bias points from simulations data of commercial CMOS processes, justifying the importance of a ZTC modeling taking into account all inversion regimes. Despite initial ZTC investigations have been made regarding the drain current, this effect can be analyzed in several other MOSFET characteristics such as transconductance and gate-bulk capacitance. This chapter will mention these ZTC occurrences for the drain current and model them. It will show that ZTC also occurs for transconductance, deriving its model as well.

This chapter is organized as follows: section 2.1 presents a continuous all-region MOSFET model, which the proposed ZTC modeling employ. During the whole chapter, this model will serve as basis for MOSFET Thermal dependencies study (Section 2.2) and after that for ZTC bias points definitions (Sections 2.3, 2.4 and 2.5).

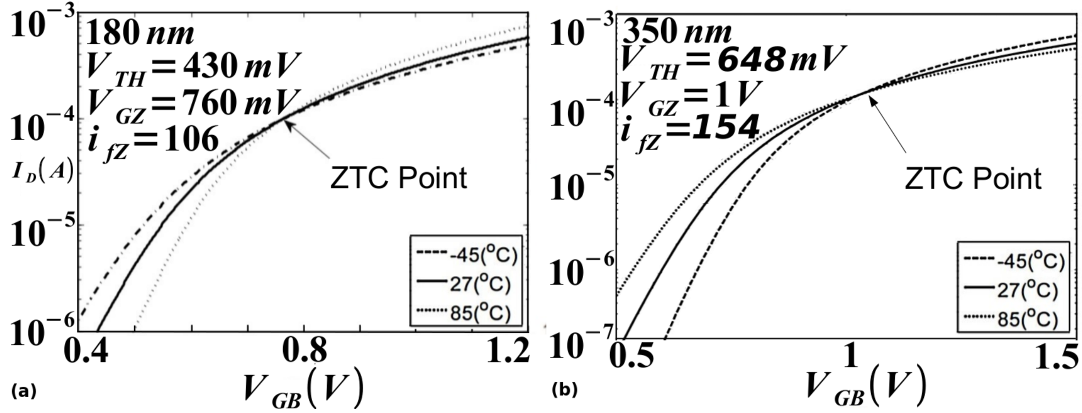


Figure 2.1: NMOSFET ZTC point for (a) 180nm and (b) 350 nm processes.

2.1 Continuous all-regime MOSFET model

"MOS Transistor is a four-terminal device where all voltage applied in each its terminal is responsible to either create or eliminate the inversion layer for digital applications or to modulate its conductance in a continuous manner for analog/RF applications" [TSIVIDIS; MCANDREW (2010)]. Fig 2.2 shows a perspective vision of planar MOS transistor, as well as the "quantum zoom" at source and drain terminals. These source and drain energy band diagrams relate to the degree of inversion charge that consequently determines DC MOSFET drain current (I_{DS}). Each parameter in Fig. 2.2 will be defined and discussed thoroughly in this section.

Classical MOSFET modeling found in the current literature is based on the set of assumptions listed below [TSIVIDIS; MCANDREW (2010)]. All of these criteria also will be taken into account in the modeling presented in this work.

- Long channel device: edge effects are negligible, e. g., the effective length is the same of geometric transistor length.
- The substrate is uniformly doped.
- pn junctions in the terminals Drain and Source are operating in reverse-biased condition. This region under channel is considered as perfectly insulating layer. Even at high temperatures, the drain-source-body junction can have a significant leakage current in the drain current but it will be also neglected.
- The external dc voltages have been applied for a long time, operating with charges in steady-state regime.
- The horizontal field component will be assumed to be much smaller than the vertical component. This approximation refers to the gradual channel approximation.
- There is no gate leakage. $I_G = 0$.
- High-frequency operation is not included in this ZTC modeling, so that this modeling uses lumped circuit abstraction, e, g., the current that arrives in the source is the same that leaves the drain.
- Inversion layer has an infinitesimal thickness, i.e., an infinitesimal depth from the surface concentrates all inversion charge. This assumption is called charge sheet approximation.
- Surface mobility is assumed to be equal along the whole channel.
- The relationship used to calculate the total inversion charge through the solution of

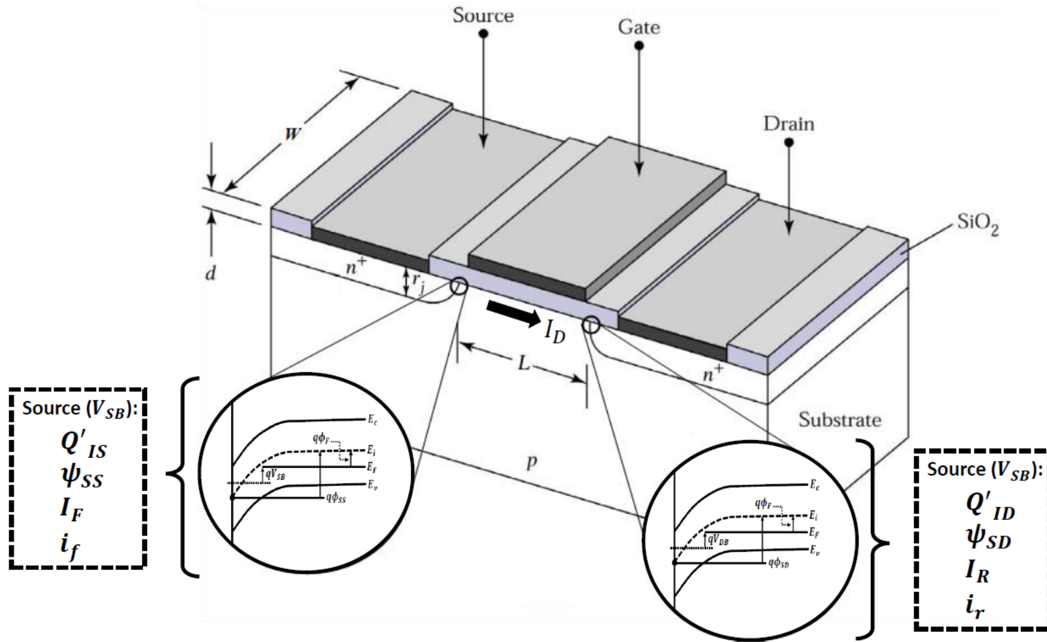


Figure 2.2: Planar MOSFET transistor.

Poisson's equation does not take into account accumulation regime.

- The quasi-equilibrium charge concentration assumption is used to define the number of electrons and holes at drain and source of the transistor, as shown in "quantum zoom" of the Fig. 2.2.

Both physical mechanisms, drift and diffusion, cause current under gate channel [TSIVIDIS; MCANDREW (2010)]. In this case, the current is evaluated spread over the whole length channel (L), i.e., x = 0 (source) to x = L (drain), as described in Eq. 2.1.

$$I_{DS}(x) = I_{drift}(x) + I_{diff}(x) \tag{2.1}$$

where

$$I_{drift}(x) = W\mu(Q'_I)\frac{d\psi_S}{dx} \tag{2.2}$$

and

$$I_{diff}(x) = W\mu\phi_t\frac{dQ'_I}{dx} \tag{2.3}$$

The parameters are: ψ_S is the potential surface, μ is defined as low field mobility, ϕ_t is the thermal voltage, W is transistor width and Q'_I inversion charge density. Along with the criteria previously listed, it is possible to achieve a total drain current of transistor just integrating throughout the channel and then,

$$I_{DS} = \mu\frac{W}{L}\left(\int_{\psi_{SD}}^{\psi_{SS}}(-Q'_I)d\psi_S + \phi_t\int_{Q'_{ID}}^{Q'_{IS}}Q'_I dQ'_I\right) \tag{2.4}$$

where $\psi_{SS(D)}$ and $Q'_{IS(D)}$ are source (drain) potential surface and source (drain) inversion charge density, respectively. From Eq. (2.4), it deserves to note that final I_{DS} is only

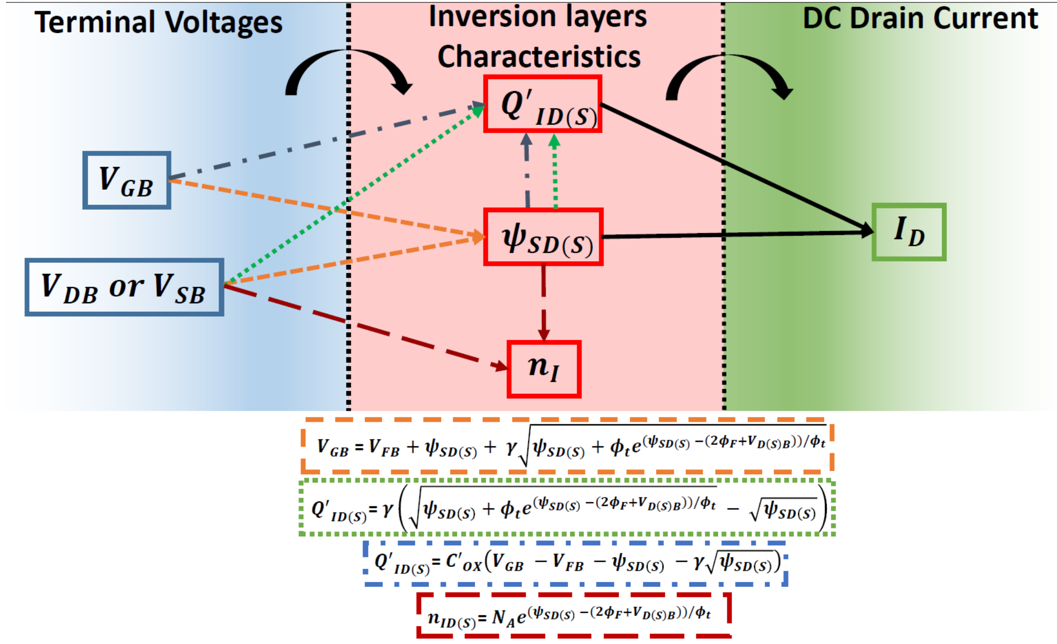


Figure 2.3: Connections among external voltages, interfaces characteristics and drain current.

dependent on terminal characteristics, i.e., knowing both $\psi_{SS(D)}$ and $Q'_{IS(D)}$ for a fixed geometry ($\frac{W}{L}$) a drain current can be defined.

The next step is to calculate the interface (inversion layer of an infinitesimal thickness, as previous mentioned) terminal characteristics. Applying quasi-equilibrium charge assumption into Poisson's equation along with potential and charge balance condition [TSIVIDIS; MCANDREW (2010)], a set of equations that link terminals voltages with drain and source interface characteristics can be found and is listed below

$$V_{GB} = V_{FB} + \psi_{SS(D)} + \gamma\sqrt{\psi_{SS(D)} + \phi_t e^{(\psi_{SS(D)} - (2\phi_F + V_{D(S)B}))/\phi_t}} \tag{2.5}$$

$$Q'_{I(D)} = \gamma(\sqrt{\psi_{SS(D)} + \phi_t e^{(\psi_{SS(D)} - (2\phi_F + V_{D(S)B}))/\phi_t}} - \sqrt{\psi_{SS(D)}}) \tag{2.6}$$

$$Q'_{IS(D)} = C'_{ox}(V_{GB} - V_{FB} - \psi_{SS(D)} - \gamma\sqrt{\psi_{SS(D)}}) \tag{2.7}$$

where V_{GB},V_{SB}, and V_{DB} are gate, source and drain to bulk voltages, V_{FB} is the flat band voltage, $\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C'_{ox}}$, q is magnitude of electron charge, C'_{ox} is the oxide capacitance per unit of area, N_A substrate doping concentration, ϵ_s is permittivity of silicon and, ϕ_F is called Fermi Potential given by $\phi_t ln(N_A/n_i)$. Combining Eq.s (2.5), (2.6), and (2.7) together with (2.4), is possible to define I_{DS} behavioral in all operating regions of MOS transistor. This modeling is defined as *"complete sheet model"*. Fig. 2.3 helps to see all connections among external voltages, interfaces characteristics and drain current using Eq.s (2.4) to (2.7). Note that, from this modeling, it is always needed to calculate both charge and surface potential to achieve the drain current. Similar format Lines in Fig. 2.3 shows possible ways to reach I_{DS}.

Also, it is possible to plot some of these equations and analyze the transistor operation. For instance, plotting the Eq. (2.5) for a fixed gate-bulk bias (V_{GB}) Fig. 2.4 is depicted.

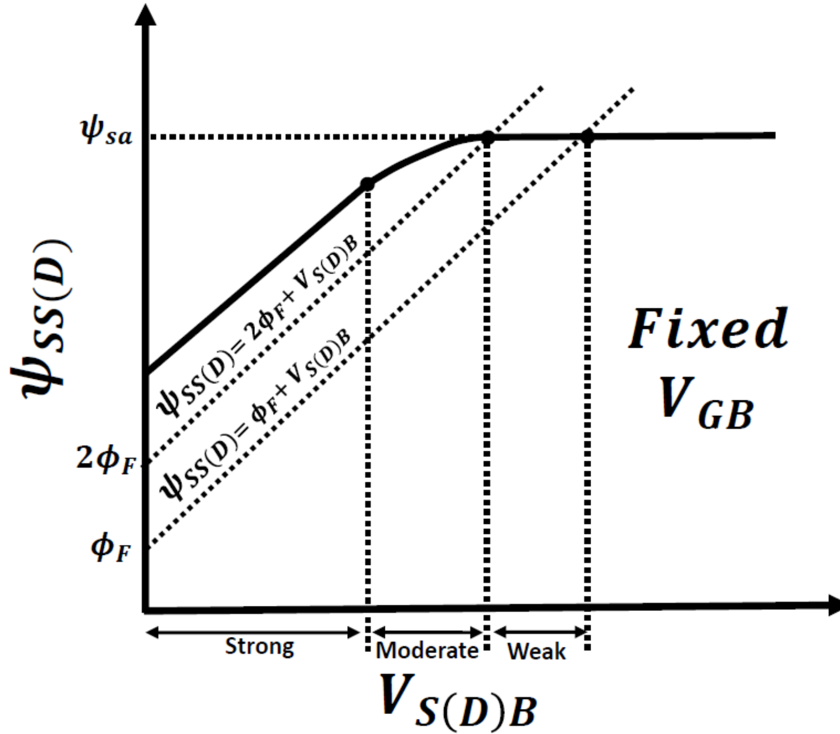


Figure 2.4: $V_{S(D)B}$ vs. $\psi_{SS(D)}$.

One direct conclusion is that when $\psi_{sa} = 2\phi_F + V_{D(S)B}$ (intersection point between the curves Eq. (2.5) and $\psi_{SS(D)} = 2\phi_F + V_{D(S)B}$) the terminal source (drain) has no more control over channel, i. e., this terminal goes into weak inversion regime. If $V_{D(S)B} = 0$ and neglecting the exponential term in Eq. (2.5), it is readily found the V_{GB} that also has no control over charge in the channel, as shown in Eq. (2.8). This special gate-bulk voltage is called threshold voltage (V_{T0}). In other words, it means the necessary gate-bulk voltage to leave the weak inversion but it does not say anything about to enter in strong inversion.

$$V_{TH}(V_{SB})|_{V_{SB}=0} = V_{T0} \simeq V_{FB} + \psi_{sa} + \gamma\sqrt{\psi_{sa}} \simeq V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \qquad (2.8)$$

However, these equations do not clearly show what is happening in the transistor and some approximations in MOS literature are done to simplify the final analysis. If the term $\sqrt{\psi_{SS(D)}}$ in Eq. (2.7) is expanded in Taylor's series around the specific potential surface (for example, ψ_{sa}) and considering first order term, we get

$$Q'_{IS(D)} = C'_{ox}(V_{GB} - V_{FB} - \psi_{sa} - \gamma\sqrt{\psi_{sa}} + n(\psi_{SS(D)} - \psi_{sa})) \qquad (2.9)$$

where

$$n = 1 + \frac{\gamma}{2\sqrt{\psi_{sa}}} \qquad (2.10)$$

n is defined as slope factor. From Eq. (2.9), one can readily conclude that

$$\frac{dQ'_{IS(D)}}{d\psi_{SS(D)}} = nC'_{ox} \qquad (2.11)$$

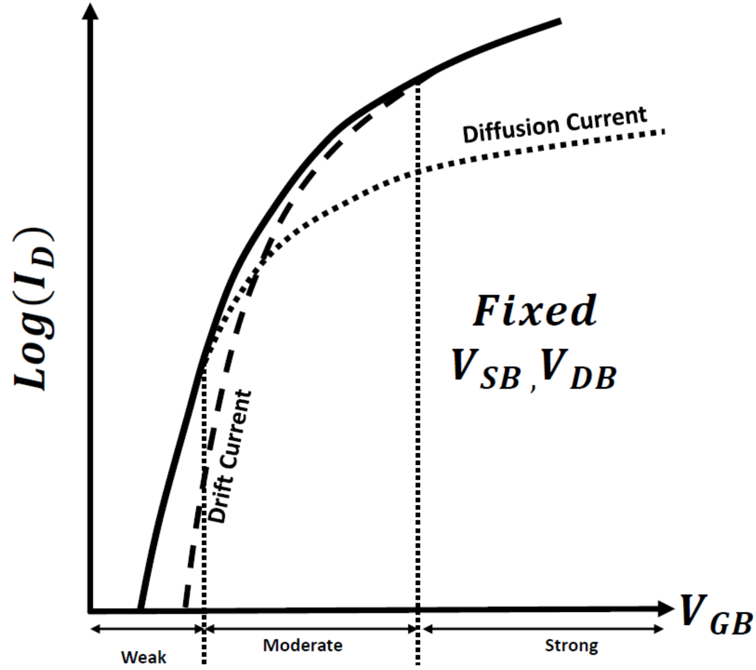


Figure 2.5: I_D Drift and diffusion current comprise ids.

Therefore, putting Eq. (2.11) in (2.4) and after some algebra efforts

$$I_{DS} = \underbrace{\frac{W}{L}\frac{\mu}{2nC'_{ox}}(Q'^2_{IS} - Q'^2_{ID})}_{\text{Drift Current}} + \underbrace{\frac{W}{L}\mu\phi_t(Q'_{ID} - Q'_{IS})}_{\text{Diffusion Current}} \tag{2.12}$$

Another well-known fact is that in strong inversion regime ($V_{GB} >> V_{T0}$) total drain current is mainly due to the presence of drift. On the other hand in weak inversion, of diffusion ($V_{GB} << V_{T0}$) [TSIVIDIS; MCANDREW (2010)]. However in moderate inversion both drift and diffusion are important as depicted in Fig. 2.5. This figure can be drawn readily figuring out Eq. (2.5) and (2.7) numerically and substituting in Eq. (2.12).

Of further interest is to note that Eq. 2.12 only depends on terminals inversion charge density. However, according to Eqs. (2.5) to (2.6) it is always needed to calculate $\psi_{SS(D)}$ and after $Q'_{I(D)S}$ in order to accomplish the final I_{DS} value. We can see in Fig. 2.3 that is missing a directly connection between external voltage and inversion charge density. The model that we are going to use in ZTC modeling uses an explicit approximation method, called Unified Charge-Control Model (UCCM). This approach that links the inversion charge density ($Q'_{I(D)S}$) with external bias voltage (V_{GB}, V_{DB}, V_{SB}).

UCCM is done using the concept of "Pinch-off Voltage" or V_P. For a fixed V_{GB}, the source or drain voltage that makes channel charge density corresponding to effective channel capacitance times thermal voltage is defined as pinch-off Voltage ($Q'_{IP} = nC'_{ox}\phi_t$) [SCHNEIDER; GALUP-MONTORO (2010)].

Other definitions for V_P employing some approximations are found in the literature as well. For instance, using again Eq. 2.5 but now fixing the $V_{S(D)B}$ Fig. 2.6 can be plotted. It deserves to note in the figure that as soon as $\psi_{SS(D)}$ leaves the ψ_{sa} or weak inversion regime it enters rapidly in strong inversion regime with a constant $\psi_{SS(D)}$ value of $\phi_0 + V_{S(D)B}$. Using this condition and Eq. 2.9, V_P is defined as the value of $V_{S(D)B}$ that makes inversion charge to be zero using strong inversion approximation in surface

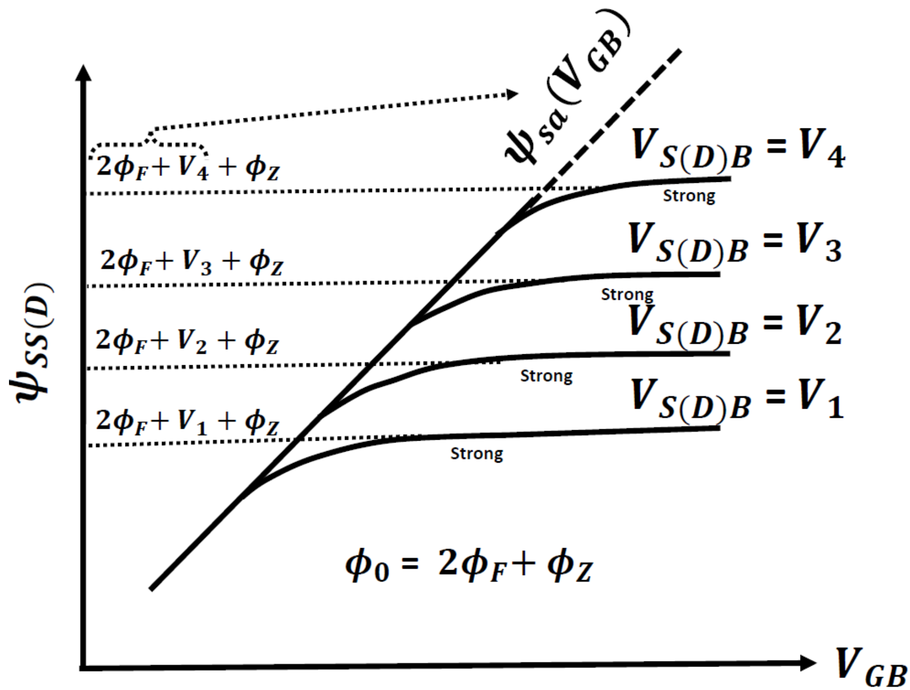


Figure 2.6: V_{GB} vs. $\psi_{SS(D)}$.

potential [TSIVIDIS; MCANDREW (2010)]. However, in a modeling without strong inversion approximation this inversion charge in V_P bias is not zero as shown in Fig 2.7. In V_P bias, inversion charge density is equals to $Q'_{IP} = nC'_{ox}\phi_t$. V_P is given by

$$V_P = \left(\sqrt{V_{GB} - V_{T0} + (\sqrt{\phi_0 + \gamma/2})^2} - \gamma/2\right)^2 - \phi_0 \tag{2.13}$$

or

$$V_P \approx \frac{V_{GB} - V_{T0}}{n} \tag{2.14}$$

In [SCHNEIDER; GALUP-MONTORO (2010)], UCCM links V_P with Q'_{IP} making it possible to bias the transistor in all-region of operation. This relationship is given by

$$V_P - V_{S(D)B} = \phi_t \left(\frac{Q'_{IP} - Q'_{I(D)S}}{Q'_{IP}} + ln(\frac{Q'_{I(D)S}}{Q'_{IP}})\right) \tag{2.15}$$

Another feature that deserve to highlight in adopted model is the definition of inversion level and normalization current [CUNHA; SCHNEIDER; GALUP-MONTORO (1998)]. These strategies are used to make transistor sizing procedure more user-friendly in a typical Analog Design Flow (ADF). This Unified Current Control Model (UICM) takes following definitions:

$$\frac{Q'_{I(D)S}}{Q'_{IP}} = \sqrt{1 + i_{f(r)}} - 1 \tag{2.16}$$

and

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SQ} \frac{W}{L} \tag{2.17}$$

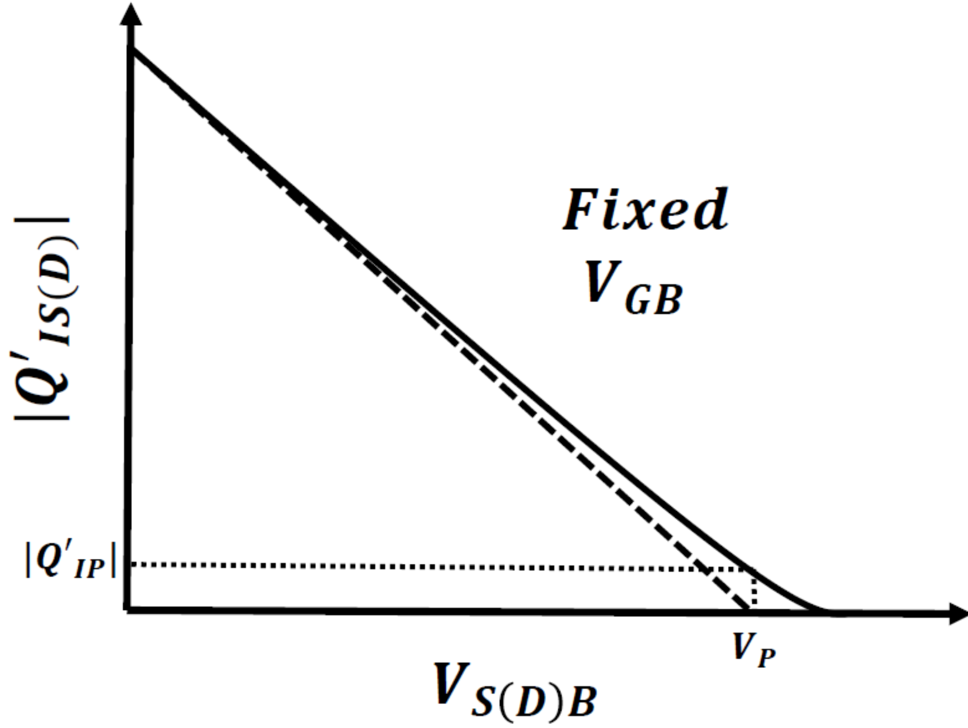


Figure 2.7: $Q'_{I(D)S}$ vs. $V_{S(D)B}$.

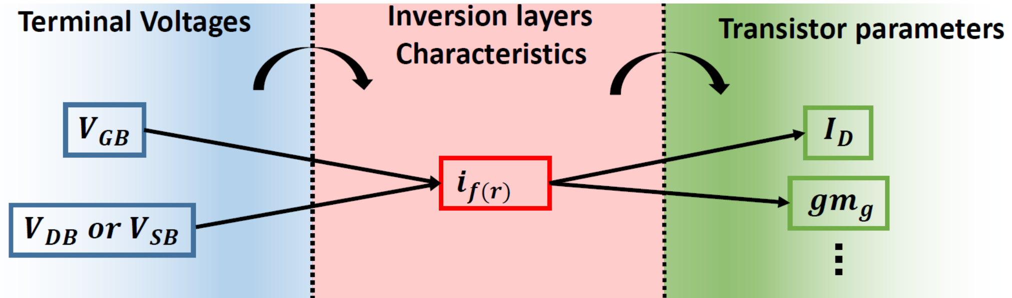


Figure 2.8: Connections among external voltages, interfaces characteristics, and drain current using UICM model.

where $i_{f(r)}$ is defined as the forward (reverse) inversion coefficient, and I_S is the normalization current. Also, Eq. (2.12) can be rearranged to the form of

$$I_{DS} = I_F - I_R \tag{2.18}$$

and

$$I_{F(R)} = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \left(\left(\frac{Q'_{I(D)S} - Q'_{IP}}{Q'_{IP}} \right)^2 - 2 \frac{Q'_{I(D)S}}{Q'_{IP}} \right) \tag{2.19}$$

where $I_{F(R)}$ is the forward (reverse) current. Substituting both Eq. (2.16) and (2.17) in (2.15) and (2.19), we get

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) \right] \tag{2.20}$$

and

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{2.21}$$

In summary, from this model Eqs. (2.20), (2.14) and (2.8) relates the source and drain inversion coefficients (forward and reverse), i_f and i_r, with the three external voltages applied to the transistor terminals, V_G, V_S and V_D, using the bulk terminal as reference. Eq. (2.21) links i_f and i_r with MOSFET drain current. All transistor parameters can be referred to $i_{f(r)}$ such as the transconductance, shown in Eq. (2.22) and (2.23). Fig. 2.8 shows the direct connections between external voltage passing through inversion level and ending up in I_{DS} and g_{mg}, for example. This UICM model is valid to operate in all-region of MOSFET operation (weak, moderate and strong inversion regime). This modeling does not address accumulation regime.

$$g_{mg} = \frac{g_{ms} + g_{md}}{n} \tag{2.22}$$

and

$$g_{ms(d)} = \frac{2I_S}{\phi_t}(\sqrt{1 + i_f(r)} - 1) \tag{2.23}$$

where g_{mg}, g_{md} and g_{ms} are gate, drain and source transconductance, respectively. There are more details about this UICM model in [SCHNEIDER; GALUP-MONTORO (2010)].

Also from this model, one can readily achieve the widespread g_{mg}/I_D expression that is widely used in analog designs, given by Eq. (2.24).

$$\frac{g_{ms(d)}}{I_{F(R)}} = \frac{2}{\phi_t(\sqrt{1 + i_f(r)} + 1)} \tag{2.24}$$

Finally, from Eq. (2.12) and with the aid of Fig. 2.5, we conclude that operation only in strong inversion or weak inversion is possible, taking either drift current or diffusion current, respectively. In this way, Eq. (2.25) and (2.26) are found for strong inversion regime in linear and saturation respectively, and Eq. (2.27), for weak inversion regime [SCHNEIDER; GALUP-MONTORO (2010)][TSIVIDIS; MCANDREW (2010)].

$$I_D = \frac{\mu C_{ox} n}{2}\left(\frac{W}{L}\right)[(V_P - V_{SB})^2 - (V_P - V_{DB})^2] \tag{2.25}$$

$$I_D = \frac{\mu C_{ox}}{2n}\left(\frac{W}{L}\right)(V_{GB} - V_{T0} - nV_{SB})^2 \tag{2.26}$$

$$I_D = I_0 e^{(V_P - V_S)/\phi_t}(1 - e^{V_{DS}/\phi_t}) \tag{2.27}$$

where

$$I_0 = \mu C_{ox} n \phi_t^2 e\left(\frac{W}{L}\right) \tag{2.28}$$

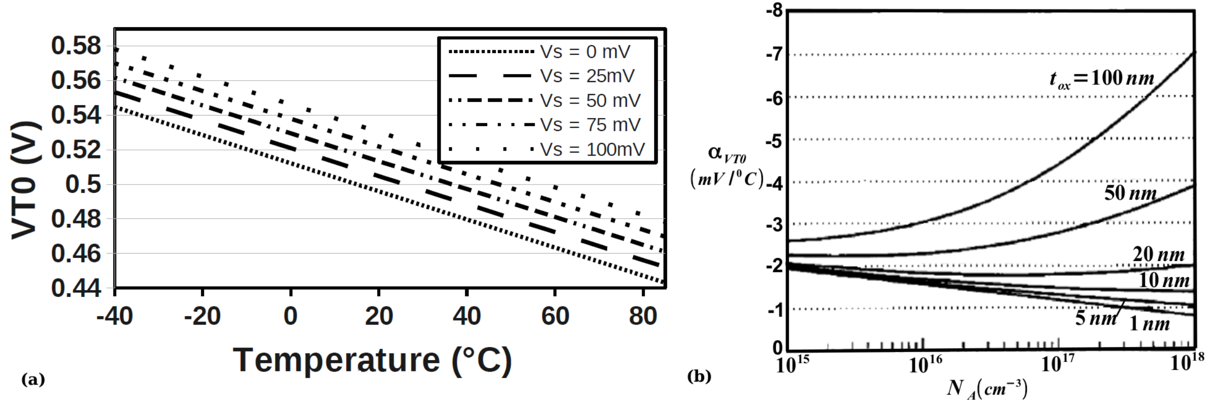


Figure 2.9: (a) V_{T0} versus temperature for different values of V_{SB} (0 to 100 mV) and $V_{GB} = 900mV$ in a 180nm CMOS process (b) $\alpha_{V_{T0}}$ vs. N_A for different t_{ox}.

2.2 MOSFET thermal dependence

Usually, it is reasonable to claim that there are three sources of temperature variations in MOSFET transistor: threshold voltage (V_{T0}), low-field mobility (μ) and slope factor (n). V_{T0} thermal dependence can be derived from Eq. (2.8) making a derivative with respect to temperature and assuming that $V_{FB} = constant - \phi_F$ [SCHNEIDER; GALUP-MONTORO (2010)]. It can be summarized by

$$V_{T0}(T) = V_{T0}(T_0) - |\alpha_{V_{T0}}|(T - T_0) \tag{2.29}$$

where

$$\left|\frac{\partial V_{T0}}{\partial T}\right|_{T=T0, V_{SB}=0} = |\alpha_{V_{T0}}| = \frac{1}{T_0}\left(1 + \frac{\gamma}{\sqrt{2\phi_F}}\right)\left(\frac{E_G}{2q} - \phi_F\right) \tag{2.30}$$

where E_G is the silicon band-gap energy and T_0 is the room temperature. Fig. 2.9 (a) shows V_{T0} versus temperature for different values of V_{SB} (0 to 100 mV) in an 180nm CMOS process. Fig. 2.9 (b) presents the expected values for $\alpha_{V_{T0}}$ for wide ranges of doping concentration (N_a) and oxide thickness (t_{ox}) [SZE (1981)]. The target technologies for this study are below having $\alpha_{V_{T0}}$ values between -3.5 and -0.5 $mV/^oC$ [SZE (1981)]; that is the range that the later analysis will use.

MOSFET low field mobility has very complex temperature dependence, defined by the interplay of following four scattering parameters: phonon scattering (μ_{ph}), surface roughness scattering (μ_{sr}), bulk charge Coulombic scattering (μ_{cb}), and interface charge Coulombic scattering (μ_{int}), as written in Eq. (2.31). It used, for example, in Berkeley Short-Channel IGFET Model (BSIM).

$$\left(\frac{1}{\mu_{eff}(T)}\right) \approx \left(\frac{1}{\mu_{ph}(T)}\right) + \left(\frac{1}{\mu_{sr}(T)}\right) + \left(\frac{1}{\mu_{cb}(T)}\right) + \left(\frac{1}{\mu_{int}(T)}\right) \tag{2.31}$$

Phonon scattering (μ_{ph}) refers to the potential for an electron to be scattered by a lattice vibration. As temperature increases, lattice vibrations increase and the probability of an electron being scattered by the lattice increases. In contrast, at low temperatures, electrons move more slowly, and lattice vibrations are small as well; thus, the ion impurity

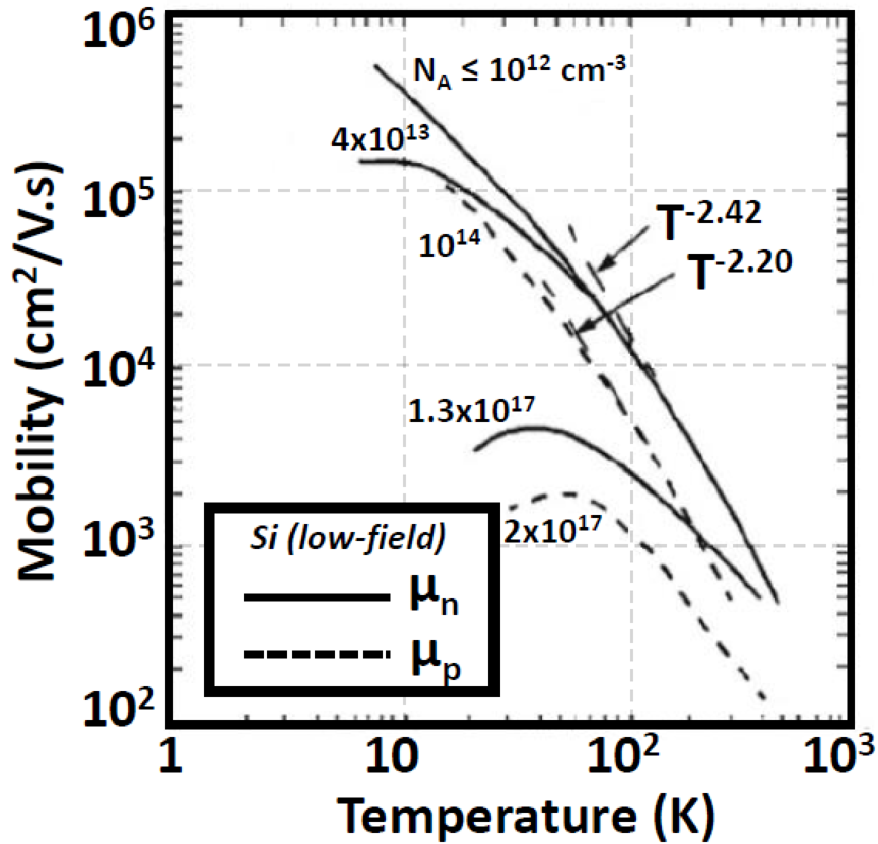


Figure 2.10: μ vs. temperature for different N_A.

forces become the dominant limitation of mobility. In this regime, decreasing temperature extends the amount of time electrons spend passing through an impurity ion, causing mobility to decrease as temperature decreases (μ_{cb}). This effect is emphasized in the high dopant concentration. Surface roughness and interface charge Coulombic scattering become dominant when high electric fields pull electrons closer to the Si/SiO2 surface (μ_{sr},μ_{int}). Fig. 2.10 shows μ versus temperature for different N_A [SZE (1981)].

A more simple expression is used to combine all these effects together. The temperature dependency of the mobility is given by

$$\mu(T) = \mu_{lf}(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{2.32}$$

where α_μ is the temperature dependence power coefficient for the mobility model. Values between -2.5 and -1.5 are typically found in the literature.

Finally, although slope factor (n) thermal dependence will be neglected in proposed ZTC modeling, it is discussed here. If one derives the first order Taylor's series approximation of Eq. (2.10) with respect to temperature, Eq. (2.33) are obtained.

$$n \approx n_0(1 + TC_n(T - T_0)) \tag{2.33}$$

where

$$TC_n = \frac{1}{n_0}\frac{\partial n}{\partial T}\bigg|_{T=T_0} = -\frac{1}{n_0}\frac{\gamma}{2(2\phi_F(T_0) + V_{SB})^{3/2}}\frac{1}{T_0}\left(\phi_F(T_0) - \left(\frac{E_{G0} + 3kT_0}{2q}\right)\right) \tag{2.34}$$

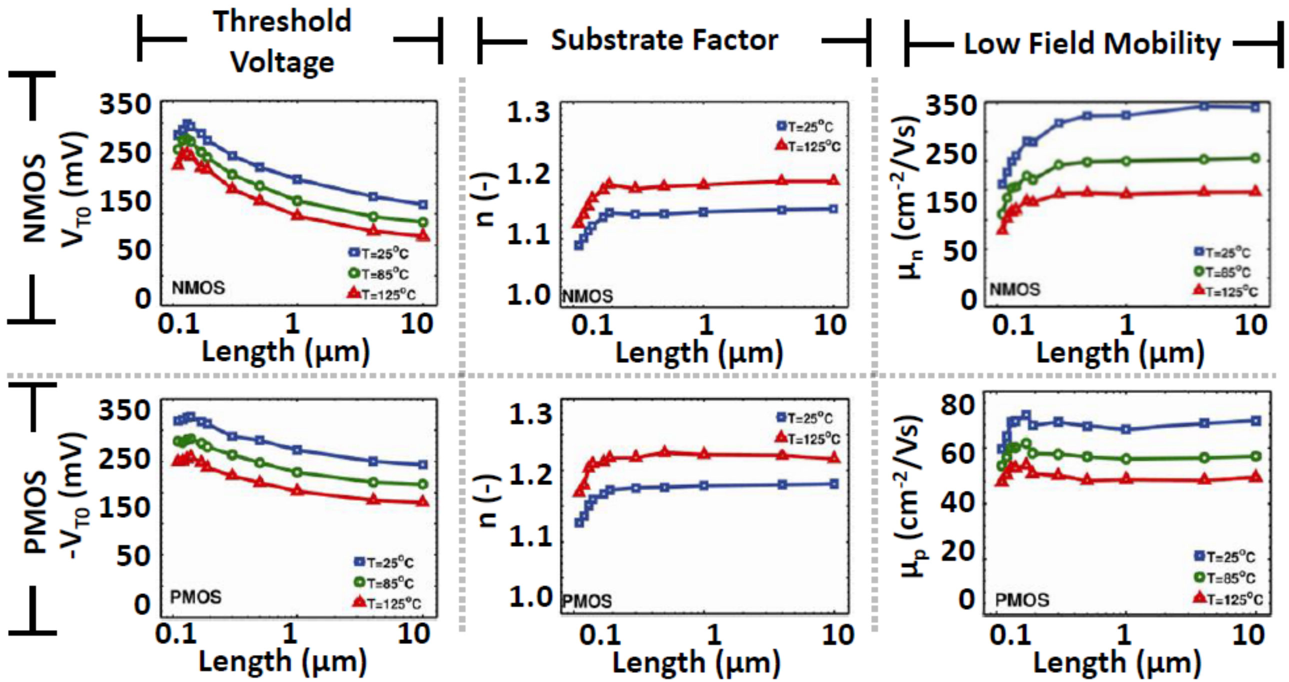


Figure 2.11: Threshold voltage (left), slope factor (center), and Mobility in saturation (right), as a function of channel length and temperature, NMOS (upper) and PMOS (lower) devices of a 110 nm CMOS technology.

Table 2.1: MOSFET Parameters extraction for 110 nm CMOS technology.

$TC_{eff}(X) = \frac{X_{REF_{max}} - X_{REF_{min}}}{(T_{max} - T_{min}) X_{REF(T_0)}}$	NMOS	PMOS
Mobility μ	-0.36 ... -0.46 $\%/^oC$	-0.2 ... -0.3 $\%/^oC$
Threshold Voltage V_{T0} (L=1 μm)	-0.275 $\%/^oC$	0.2 $\%/^oC$
Slope Factor n	0.038 $\%/^oC$	0.045 $\%/^oC$

n_0 is the slope factor at room temperature.

Recently, MOSFET parameters, such as weak inversion slope factor, threshold voltage, mobility, transconductance to current ratio, Drain-Induced Barrier Lowering (DIBL), and intrinsic gain, were examined with respect to bias conditions, geometry and temperature [MAKRIS; BUCHER (2012)]. All analyses were evaluated using measured data from NMOS and PMOS transistors of an 110 nm CMOS technology. Mobility was obtained in strong inversion with V_{DB} = 1V, and was extracted using the method proposed in [BUCHER; LALLEMENT; ENZ (1996)]. Threshold voltage V_{TO} was obtained from an adjusted constant current method [BAZIGOS et al. (2011)] in moderate inversion. The substrate slope factor was obtained noting that, combining Eq. (2.24) and Eq. (2.23) in weak inversion and saturation regime, Eq. (2.35) is derived and n can be extracted directly.

$$\frac{g_{mg}\phi_t}{I_F} = \frac{1}{n} \tag{2.35}$$

Fig. 2.11 shows mobility (μ), threshold voltage (V_{T0}) and slope factor (n) versus channel length and temperature for both channel type. Measurements also included scal-

ing effects. In summary, table 2.1 calculates effective temperature coefficient (TC_{eff}) for each parameters. In particular, it is desirable to point out that from this table 2.1 and Eqs. (2.21) and (2.17), mobility has more impact in drain current than slope factor regarding the temperature variations. This fact leads to neglect temperature dependence of n in our ZTC modeling to attain a more compact modeling.

2.3 ZTC Condition

In this text, the Zero Temperature Coefficient (ZTC) condition is addressed in a broad sense. It is defined as what are the requirements to provide a thermal independence of a particular device parameter or circuit performance. Or, ($\frac{1}{x}\frac{\partial x}{\partial T} = 0$, where x is the specific device parameter or circuit performance). For example, Fig. 2.1 (a) shows the drain current (on a log scale) as a function of the gate-bulk voltage (V_{GB}) of a saturated long-channel NMOSFET. Simulation temperature ranged from $-45^{o}C$ to $+85^{o}C$, for an 180 nm process. The Bias ZTC operation point can be seen around $V_{GB} \approx 760mV$ for a transistor with $V_T = 430mV$, resulting that the ZTC point occurs for an overdrive voltage around 330mV; the transistor operates, thus, in strong inversion.

This kind of behavior can be found in some circuit performance as well. For instance, in ring oscillator the oscillation frequency (f_{osc}) in function of the supply voltage (V_{DD}) at different temperature shows that there is a V_{DD} where the oscillation frequency is temperature independent, as shown in Fig. 2.12 (a). Fig. 2.12 (b) shows the thermal stability around this digital ZTC point ($V_{DD_{opt}}$)[BELLAOUAR et al. (1998)].

In Fig. 2.12 (a), it is convenient to note that, as long as V_{DD} is above the $V_{DD_{opt}}$, f_{osc} decreases with increasing temperature, and below of it an inverted behavior is experienced. In digital circuit design, this phenomenon is referred as Inverted Temperature Dependence (ITD) [DASDAN; HOM (2006)]. Due to ITD, it becomes very difficult to determine analytically the temperatures that maximize or minimize the delay of a cell or a path. As such, ITD has profound consequences for Static Timing Analysis (STA): (1) ITD essentially invalidates the approach of defining corners by independently varying voltage and temperature; (2) ITD makes it harder to find short paths, leading to difficulties in detecting hold time violations; and (3) the effect of ITD will worsen as supply voltages decrease and threshold voltage variations increase [DASDAN; HOM (2006)].

This Digital ZTC point was first modeled in [BELLAOUAR et al. (1998)]. It was found that the optimum supply voltage $V_{DD_{opt}}$ which results in temperature insensitive operation is proportional to the threshold voltage, given by Eq. (2.36). In this analysis, it was considered the simplified delay equation of a CMOS gate: $t_d = C_L V_{DD}/2I_{av}$, where C_L is the load capacitance and $I_{av} = \mu(T)(V_{DD} - V_{T0}(T))^{1.5}$ is the average current supplied by the gate to the load. There are many works on it [PARK et al. (1995)] [KUMAR; KURSUN (2006)].

$$V_{DD_{opt}} = V_{T0}(T_0) + 1.5\frac{|\alpha_{V_{T0}}|}{\alpha_{\mu}}T_0 \tag{2.36}$$

ZTC points can be also found in other devices such as MESFET [OJALA; KASKI (1993)], DTMOS[WANG; LIN; CHAO (2010)] and Zenner Diode [BURCEA (1977)]. For example, Zenner Diode, roughly speaking, is a diode which allows current to flow in the forward direction in the same manner as an ideal diode, but also permits it to flow in the reverse direction when the voltage is above a certain value known as the breakdown voltage, "Zener knee voltage", "Zener voltage", "avalanche point", or "peak inverse

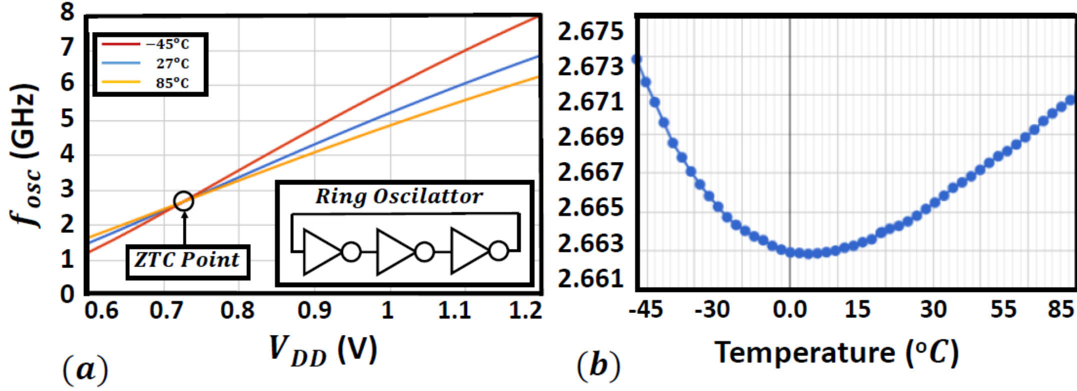


Figure 2.12: (a) Oscillation frequency (f_{osc}) vs. supply voltage (V_{DD}) for different temperature and (b) Oscillation frequency (f_{osc}) vs. temperature. These are simulated data of 130 nm CMOS technology using an inverter with L = 130nm, W_n = 130 nm and W_p = 520 nm. L is length, W_n and W_p are the widths of NMOS and PMOS transistor, respectively.

voltage".

Zener diode reverse breakdown is due to electron quantum tunneling (Zener effect) under high electric field strength or avalanche breakdown or both. Both effects are present in diodes of this type. Applying a reverse voltage across silicon Zener diodes up to about 5.6 voltage, the quantum tunneling is the predominant effect and shows a marked negative temperature coefficient. Above 5.6 voltage, the avalanche effect becomes predominant and exhibits a positive temperature coefficient. In about a 5.6 V, the two effects occur together, and their temperature coefficients nearly cancel each other out. Thus the 5.6 V diode is useful in temperature-critical applications, as shown in Fig. 2.13 (b). In the same picture, it is also shown ZTC point in MESFET Fig. 2.13 (a) and in DTMOS Fig 2.13 (c) and 2.13 (d).

Returning to MOSFET, Shoucair [SHOUCAIR (1989)] and Prijic and coworkers [PRIJIC; DIMITRIJEV; STOJADINOVIC (1992)] were the first to report the bias ZTC point for bulk CMOS in both the linear and the saturation regions. Temperature ranged between 27ºC and 200ºC.

In [SHOUCAIR (1989)], the bias ZTC analytical and experimental results were presented aiming to generate new design insights for VLSI CMOS circuits under temperature ranges between 25°C -250°C. Furthermore, the results suggested that state-of-the-art VLSI CMOS technologies at the time could be used to design on-chip voltage and current references. Therefore, a wide class of signal processing IC functions would be stable over wider temperature ranges. Shoucair also listed some of these environments that global temperature are the highest: automobile, the earth and space exploration (probes), the geothermal exploration, the aircraft engine and the nuclear reactor industries. Until that time, only experimental results were mentioned about ZTC condition in both linear and saturation regime of MOSFET transistor.

In summary, he found that there is V_{GB} at which if Eq. (2.37) holds, then the drain current would be independent of temperature ($\frac{\partial I_D}{\partial T} = 0$).

$$\frac{1}{I_D}\frac{\partial I_D}{\partial T} = 0 = \frac{1}{\mu(T)}\frac{\partial \mu(T)}{\partial T} - \left(\frac{m}{V_{GB} - V_{T0}(T)}\right)\frac{\partial V_{T0}(T)}{\partial T} \tag{2.37}$$

where $V_{T0}(T)$ and $\mu(T)$ are given by Eq. (2.29) and Eq. (2.32), respectively. In this modeling, square-law (strong inversion, Eq. (2.25) and (2.26)) for I_D was used. m

= 1 means operation in linear and m = 2 in saturation regime. Eq. (2.37) explains the reason for the name choice of 'Temperature-Coefficient' and where it is zero, the Zero Temperature Coefficient Condition is found.

A closed-form expression for $V_{GB}(ZTC)$ or V_{GZ} (necessary gate-bulk voltage to make current drain insensitive to temperature) was done minimising the least-squares deviations of the difference between left and right hand sides from Eq.(2.37) over a specified temperature range [T_1,T_2] where T_2>T_1. In addition, a more accuracy relationship regarding to $|\alpha_{V_{T0}}|$ was used, given by Eq. (2.40), and $\alpha_\mu = -1.5$ was used. Therefore, V_{GZ} found in [SHOUCAIR (1989)] is given by Eq. (2.38) and the drain current biased on V_{GZ}, by Eq. (2.39).

$$\begin{aligned} V_{GZ} = V_{T0}(T_0) - \alpha_{V_{T0}}T_0 - \frac{\alpha_{V_{T0}}}{6}(2m-3)(T_2-T_1) \\ +\gamma(\sqrt{V_{SB}+2\phi_F(T_{ave})} - \sqrt{2\phi_F(T_{ave})}) \\ -\frac{m\gamma}{1.5}\left(\frac{1}{\sqrt{V_{SB}+2\phi_F(T_{ave})}} - \frac{1}{\sqrt{2\phi_F(T_{ave})}}\right)\left(\phi_F(T_{ave}) - \frac{E_{G0}}{2q}\right) \end{aligned} \tag{2.38}$$

where $\phi_F(T_{ave}) = [\phi_F(T_2) - \phi_F(T_1)]/2$.

$$I_{DZ} = \frac{\mu_n(T_0)C_{ox}}{2}\left(\frac{W}{L}\right)\left(\frac{-mT_0\alpha_{V_{T0}}}{1.5}\right)^m \tag{2.39}$$

$$\alpha_{V_{T0}} = \left(2 + \frac{\gamma}{\sqrt{V_{SB}+2\phi_F(T)}}\right)\left(\frac{\phi_F(T)}{T} - \frac{k}{q}\left(\frac{3}{2} + \frac{E_{G0}}{2qT}\right)\right) \tag{2.40}$$

For a 2um CMOS Technology, he compared the analytical result with measured data and got an error about 5%. In his conclusion, he estimated, on basis of his experimental data, that voltage and current references exhibiting average $TC_{eff}s$ in the range of 100-600 ppm/^{o}C over 25-250°C should be achievable. It is worth emphasizing that slope factor n temperature dependence was not taken into account.

In Prijic [PRIJIC; DIMITRIJEV; STOJADINOVIC (1992)], the aim of this work was to improve the accuracy of ZTC point theory presented in [SHOUCAIR (1989)] by taking into account the influence of the slope factor n temperature dependence. It was calculated in the same manner as before, using least squares methodology, and obtaining similar equations.

Few years later, in [OSMAN et al. (1995)], Osman investigated the drain current ZTC point in Partially Depleted (PD) Silicon-on-Isolator (SOI) MOSFET. In addition, in his analysis it was included the thermal dependence of degradation of low-field mobility with respect to the applied transverse electric field, ($\theta(T)$). Eq. (2.41) represents this behavior.

$$\mu_{lf}(t) = \frac{\mu_{lf}(T_0)}{1+\theta(T)(V_{GS}-V_{T0}(T))} \tag{2.41}$$

To find V_{GZ}, he did same approach as in [SHOUCAIR (1989)][PRIJIC; DIMITRIJEV; STOJADINOVIC (1992)], minimising the least-squares deviations of the difference between left and right hand sides from Eq. (2.42). Eq. (2.42) is readily achieved making $\frac{\partial I_D}{\partial T} = 0$ in Eqs. (2.25),(2.26) and isolating the V_{GS} term.

$$V_{GS} - V_{T0}(T) = \frac{-B+\sqrt{B^2+4AC}}{2A} \tag{2.42}$$

where

$$
\begin{aligned}
A &= \frac{\alpha_\mu \theta(T)}{T} - \frac{\partial \theta(T)}{\partial T} \\
B &= \frac{\alpha_\mu}{T}\left(1 - \frac{V_{DS}\theta(T)}{2}n\right) + nV_{DS}\frac{\partial \theta(T)}{\partial T} \\
&+\theta(T)\alpha_{V_{T0}} + \theta(T)\left(\alpha_{V_{T0}} + \frac{1}{2}TC_n V_{DS}\right) \\
C &= \frac{\alpha_\mu}{T}V_{DS}n + V_{DS}\theta(T)n\alpha_{V_{T0}} - \left(\alpha_{V_{T0}} + \frac{1}{2}TC_n V_{DS}\right)
\end{aligned} \tag{2.43}
$$

for linear regime. Or

$$
\begin{aligned}
A &= \theta(T)\left(\frac{\alpha_\mu}{T} + TC_n\right) + \frac{\partial \theta(T)}{\partial T}n \\
B &= \frac{\alpha_\mu}{T} + TC_n + 2\alpha_{V_{T0}}\theta(T) - \theta(T)n\alpha_{V_{T0}} \\
C &= 2\alpha_{V_{T0}}
\end{aligned} \tag{2.44}
$$

for saturation regime.

Measured and calculated gate bias at the ZTC point (V_{GZ}) was plotted against the drain bias in both operating regions for NMOS and PMOS as shown in Fig. 2.14 [OSMAN et al. (1995)]. The found errors in ZTC point prediction for NMOS were about 4.8% in the linear region and about 0.2% in the saturation region with a maximum error of 4.8% over the entire range of drain bias. For PMOS, these errors were 4.1%, 3.2%, and 6.8%, respectively. These figures are much smaller than the error values computed by Shoucair [SHOUCAIR (1989)] (5-14%) and comparable to Prijic and coworkers [PRIJIC; DIMITRIJEV; STOJADINOVIC (1992)](3%) for the bulk MOSFET. This accuracy improvement was accomplished by considering the temperature dependence of all model parameters (V_{T0}, μ, θ and n). Shoucair, for example, examined the temperature dependence of only V_{T0}, and μ, while Prijic et. al. considered V_{T0}, μ and n.

All these ZTC modeling [SHOUCAIR (1989)][PRIJIC; DIMITRIJEV; STOJADINOVIC (1992)][OSMAN et al. (1995)] were aiming to provide an accuracy model against the CMOS or SOI-MOS technology of that time. Nevertheless, it visible that all these presented equations so far are not "user-friendly" for analog design purpose.

Then in 2001, Fylanovisky made this analysis more intuitive for MOSFET operating in strong inversion and saturation regime [FILANOVSKY; ALLAM (2001)]. Using a simplification of Eq. (2.26) with n=1 and taking only the thermal dependence of V_{T0} and μ, he achieved a simple expression for ZTC condition ($\frac{\partial I_D}{\partial T} = 0$),

$$
V_{GZ} = V_{T0}(T_0) - \alpha_{V_{T0}}T_0 = V_{T0}(T_0) + |\alpha_{V_{T0}}|T_0 \tag{2.45}
$$

where the assumption $\alpha_\mu = -2$ was adopted. Consequently, for drain ZTC current is

$$
I_{DZ} = \frac{\mu(T_0)T_0^2 C'_{ox}}{2}\left(\frac{W}{L}\right)\alpha_{V_{T0}}^2 \tag{2.46}
$$

It is clear that these Eq. (2.45) and (2.46) are more attractive to be used by designers to those previously reported.

Table 2.2: ZTC Operating Point with $\frac{W}{L} = \frac{10\mu m}{1\mu m}$

MOSFET	$V_{T0}(V)$	$V_{GZ}(V)$	I_{DZ} (μA)	i_{fz}
180 nm Regular	0.43	0.76	96.27	106
350 nm Regular	0.648	1.05	116.69	154
130 nm Regular	0.16	0.49	222.6	106
130 nm Low-Vt	0.1	0.44	274.8	112
130 nm Low-Power	0.6	0.87	128.1	74
130 nm Zero-Vt	0.063	0.23	97.7	32.5

Table 2.3: MOSFET ZTC Operating Point

Filanovsky concluded [FILANOVSKY; ALLAM (2001)] that there was a mutual compensation of mobility and threshold voltage temperature dependence at which may result in a zero temperature coefficient bias point of MOS transistor. Also, in the same paper [FILANOVSKY; ALLAM (2001)], he also proposed a voltage reference (as Shoucair mentioned [SHOUCAIR (1989)].) using this concept.

Recently in 2013, a new approach, called 'compact ZTC modeling,' which applies to any compact physical model, was proposed to describe the ZTC condition of a MOSFET [CHIAH; ZHOU; YUAN (2013)]. Beyond the usual drain-current ZTC operating point (V_{GZ},I_{DZ}), this model address some extra ZTC points, such as ones found in gate-bulk MOS capacitance. In Chiah [CHIAH; ZHOU; YUAN (2013)], ZTC voltages are calculated in the accumulation ($V_{ztc,sa}$) and depletion ($V_{ztc,ds}$) regions based on the unified regional modeling of surface potential for the gate capacitance at zero drain bias ($V_{DS} = 0$). Moreover, this analysis is also extended to the ZTC voltage ($V_{ztc,ds}$)) for gate capacitance in the depletion and saturation regions at any V_{DS}. Fig. 2.15 shows ZTC points found in [CHIAH; ZHOU; YUAN (2013)].

The main aim of Chiah work [CHIAH; ZHOU; YUAN (2013)] is to provide a process window with constant ZTC contours for different process parameters, such as body doping (N_A) and gate-oxide thickness (t_{ox}) at any drain biases. The process windows provide useful information in determining the optimum process parameters and operating voltages for circuit design in ruggedized electronics that operate at high-temperature conditions. Fig 2.16 shows process windows for V_{GZ} and $V_{ztc,ds}$ in (a) and V_{GZ} in function of V_{DS} in (b).

This ZTC modeling complies all-region operation of MOSFET, from accumulation to strong inversion regime. However, as it is a numerical approach (marks the cross-over ZTC points by Newton-Raphson solutions), it does not give a closed analytical result, which is essential for analog design purposes.

In summary, in the current literature, there is so far no closed-form ZTC modeling for drain current and transconductance which attends all-region operation of MOSFET transistor. As previously shown in Table 2.2, the bias ZTC condition can also occur in moderate inversion regime. The i_{fz} is defined here as ZTC forward inversion level and it will be seen in detail in the next section. Inversion level $i_f < 100$, means that the transistor is already operating in moderate inversion [SCHNEIDER; GALUP-MONTORO (2010)].

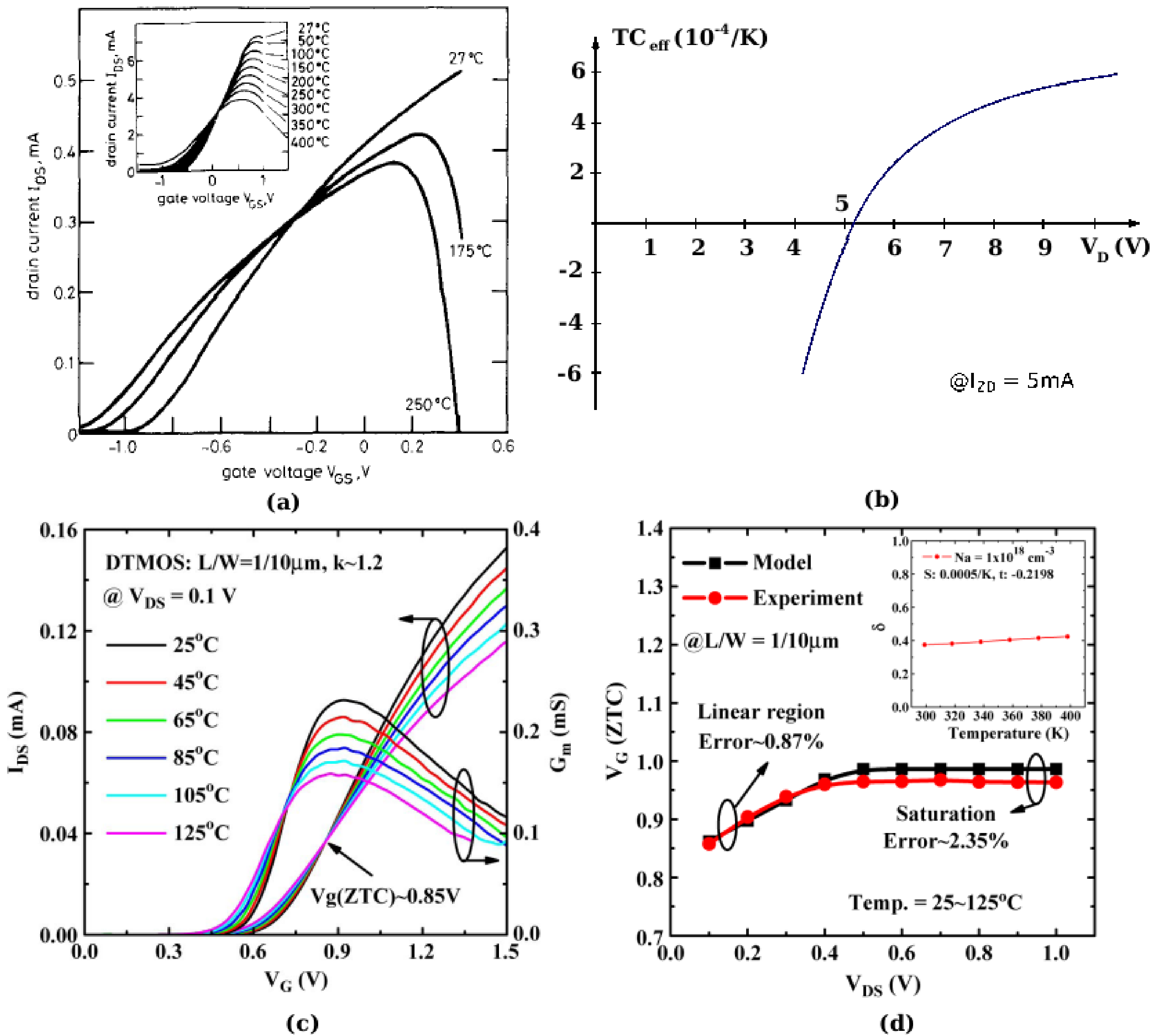


Figure 2.13: (a) Measured characteristics for DMESFET of form factor W/L = 50/2 in linear region and saturation region (b) TC_{eff} for Diode Zenner for different terminal voltage. (c) Experimental I_D vs. V_G and g_m characteristics of n-channel DTMOS in the linear region over a temperature range of 25^oC to 125^oC. Note that the ZTC point is 0.85 V when V_{DS} = 0.1 V in the linear region. (d) Theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor in both the linear and saturation regions.

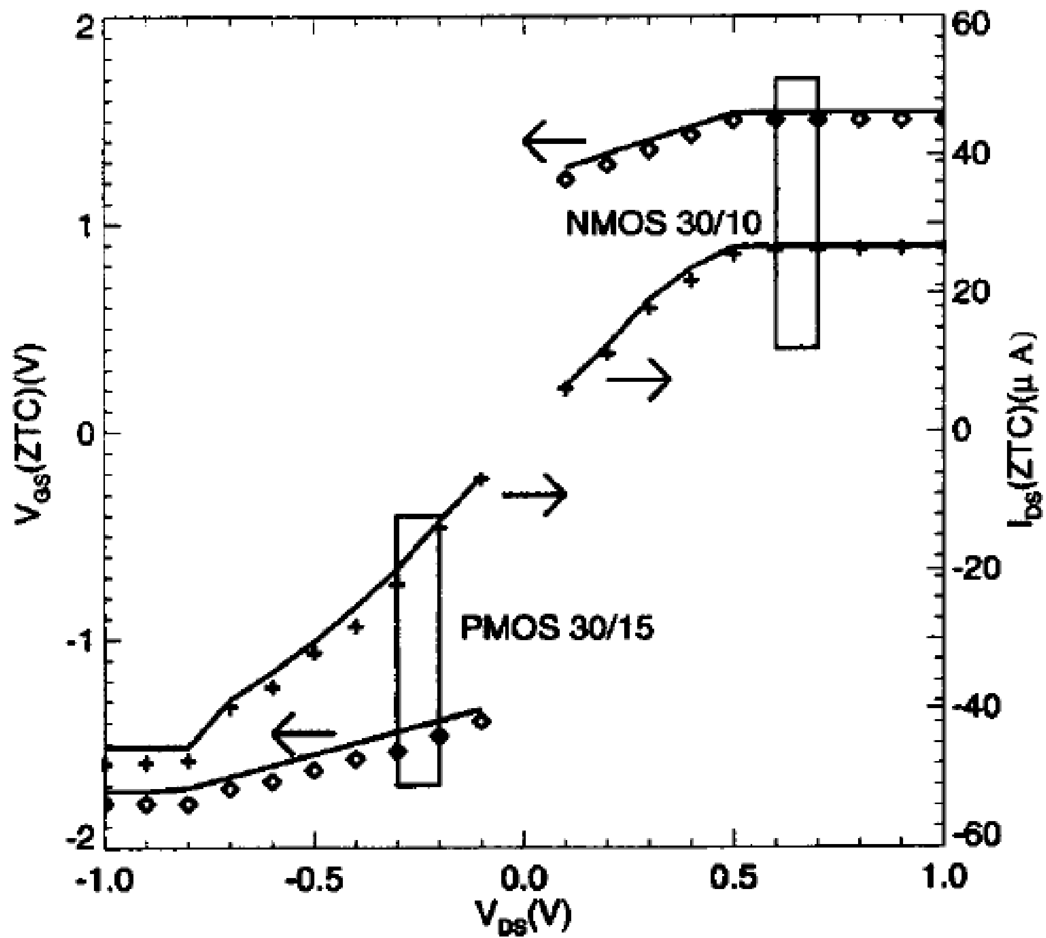


Figure 2.14: Measured and simulated gate bias (V_{GZ}) and drain current (I_{DZ}) at the ZTC point with drain bias (V_{DS}) in both linear and saturation regions for NMOS ($\frac{W}{L} = \frac{30\mu m}{10\mu m}$) and PMOS($\frac{W}{L} = \frac{30\mu m}{5\mu m}$).

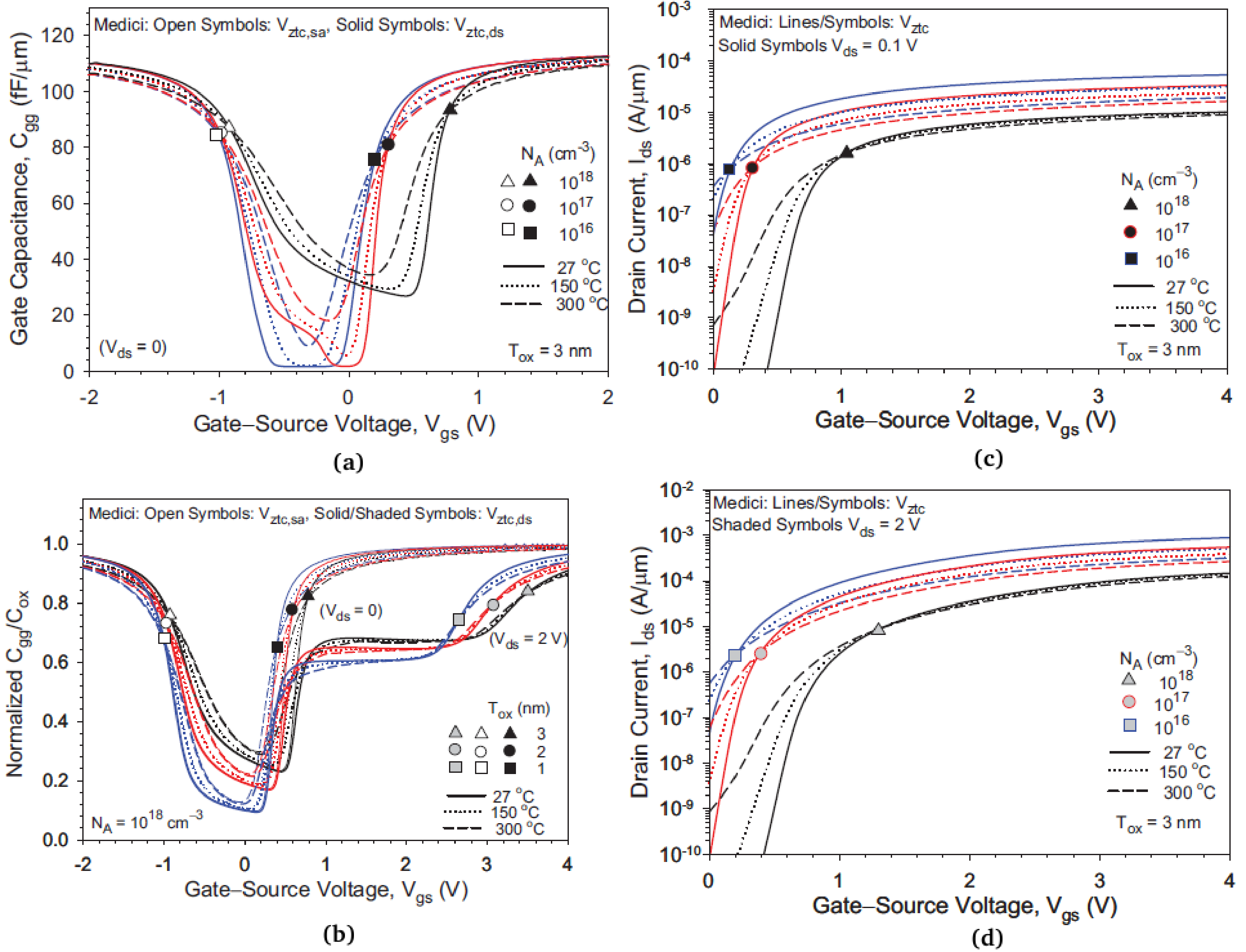


Figure 2.15: Gate capacitance versus gate voltage for (a) different body doping (at Vds = 0) and (b) different gate-oxide thickness (at Vds = 2 V), at 27 °C (solid line), 150 °C (dotted line), and 300 °C (dashed line) from an ideal MOS transistor, with the corresponding ZTC points extracted from the numerical data (symbols). Drain current versus gate voltage in (c) linear (Vds = 0.1 V) and (d) saturation (Vds = 2 V) modes for different body doping as indicated, at 27 °C (solid line), 150 °C (dotted line), and 300 °C (dashed line) from an ideal MOS transistor, with the corresponding ZTC points extracted from the numerical data (symbols).

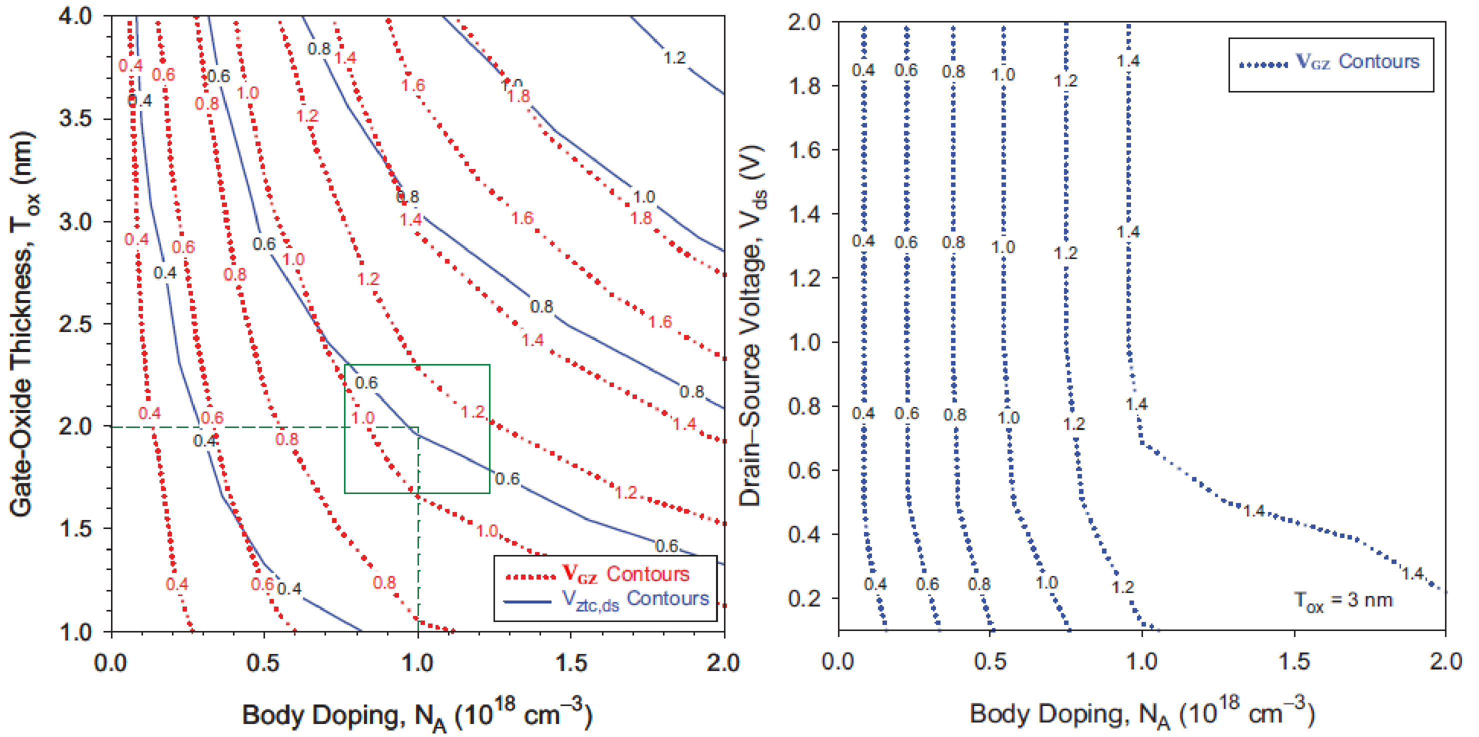


Figure 2.16: (a) Contour plots of constant $V_{ztc,ds}$ (solid line) and V_{GZ} (dotted line) extracted from the compact ZTC charge and current models, respectively, due to body doping and gate oxide thickness variations. The box illustrates a process window around the nominal values of $N_A = 10^{18}\ cm^{-3}$ and t_{ox} = 2 nm, which predicts a potential $V_{ztc,ds}$ variation from 0.5 V to 0.7 V and V_{GZ} variation from 0.85 to 1.3 V, respectively, if the variations in N_A and t_{ox} are given within the box. (b) Contour plot of constant V_{GZ} extracted from the compact ZTC drain current model at any V_{DS} due to body doping variations for devices operating in partial, dynamic, and full depletion modes.

2.4 MOSFET Bias ZTC Condition Analysis

All ZTC modelings [SHOUCAIR (1989); PRIJIC; DIMITRIJEV; STOJADINOVIC (1992); OSMAN et al. (1995); FILANOVSKY; ALLAM (2001)], the last section 2.3 presented, started from the premise that the transistor is operating in strong inversion. Perhaps influenced by experimental data of CMOS technologies of that time or based on previous references. However, in current technologies bias ZTC point can be found in moderate inversion as well, as shown in Table 2.2. This section analyzes the ZTC condition for drain-current bias using two different approaches. First, by classical analysis using strong inversion model (quadratic). Then, through a complete model, which allows the analysis of MOSFET behavior from weak inversion to strong, continuously.

2.4.1 ZTC Bias from Strong Inversion MOSFET Model

In this subsection, bias ZTC analysis in strong inversion is handled for both the saturation and linear regimes.

When long channel MOS is operating in saturation regime, its I-V behavior can be described by drain current equation Eq. (2.26) repeated below:

$$I_d = \frac{\mu_n C_{ox}}{2n}\left(\frac{W}{L}\right)(V_{GB} - V_{T0} - nV_{SB})^2 \tag{2.47}$$

If one differentiates the drain current expression with respect to temperature, a condition can be found where its dependence is negligible, i.e., $(dI_d)/(dT)|_{T=T} = 0$ [FILANOVSKY; ALLAM (2001)]. Isolating V_{GB} results in Eq. (2.48), that shows a bias condition where the drain current temperature dependence is negligible. We get

$$V_{GZ}(T) = V_{T0}(T) + nV_{SB} + 2\mu\left(\frac{(dV_{T0})/(dT)|_{T=T}}{(d\mu)/(dT)|_{T=T}}\right) \tag{2.48}$$

Substituting equations (2.29) and (2.32) in (2.48) , a V_{GB} bias voltage results for this condition is

$$V_{GZ}(T) = V_{T0}(T_0) + nV_{SB} - |\alpha_{V_{T0}}|T\left(1 + \frac{2}{\alpha_\mu}\right) + |\alpha_{V_{T0}}|T_0 \tag{2.49}$$

As mentioned in section 2.2, target-technologies for this study are below 350 nm which corresponds to $\alpha_{V_{T0}}$ values between -3.5 and -0.5 $mV/^oC$ [SZE (1981)]. For design purposes, $\alpha_\mu \approx -2$ is a reasonable consideration in modern technologies [FILANOVSKY; ALLAM (2001)]. Using this approximation, (2.49) becomes

$$V_{GZ} = V_{TH}(T_0) + nV_{SB} - \alpha_{V_{TH}}T_0 \tag{2.50}$$

Analyzing this expression, one can see that there is a gate voltage value, here called V_{GZ}, that satisfies the conditions stated before. The drain current is the same under this bias voltage, for any temperature. This operation point is called the ZTC bias point. Consequently, the drain current for this V_{GZ} is

$$I_{DZ} = \frac{\mu(T_0)T_0^2 C_{ox}}{2n}\left(\frac{W}{L}\right)|\alpha_{V_{T0}}|^2 \tag{2.51}$$

Where I_{DZ} is defined as the bias current where the transistor operates on ZTC point.

On the other hand, when MOSFET is operating in the linear regime, its I-V behavior can be described by drain current equation Eq. (2.25) along with (2.14), both repeated below:

$$I_D = \frac{\mu C_{ox} n}{2}\left(\frac{W}{L}\right)\left[(V_P - V_{SB})^2 - (V_P - V_{DB})^2\right] \tag{2.52}$$

where

$$V_P \approx \frac{V_{GB} - V_{T0}(T)}{n} \tag{2.53}$$

Putting Eq. (2.53) in (2.52), we get

$$I_D = \frac{\mu C_{ox}}{2n}\left(\frac{W}{L}\right)\left[(V_{GB} - V_{T0}(T) - nV_{SB})^2 - (V_{GB} - V_{T0}(T) - nV_{DB})^2\right] \tag{2.54}$$

If one differentiates with respect to temperature, we have

$$\frac{\partial I_D}{\partial T} = \frac{C_{ox}}{2n}\left(\frac{W}{L}\right)\Big(\frac{\partial \mu}{\partial T}((V_{GB} - V_{T0}(T) - nV_{SB})^2 - (V_{GB} - V_{T0}(T) - nV_{DB})^2) + \mu 2n|\alpha_{V_{T0}}|(V_D - V_S)\Big) \tag{2.55}$$

Applying ZTC condition in I_D, $\frac{\partial I_D}{\partial T} = 0$, knowing that $\frac{\partial \mu}{\partial T} = \frac{\mu \alpha_\mu}{T}$ (Appendix B.1), Eq (2.56) is obtained. Note that V_{GB} was already replaced by V_{GZ} which means the necessary gate-bulk voltage in order to achieve ZTC condition.

$$\frac{\partial I_D}{\partial T} = 0 = \Big(\frac{\alpha_\mu}{T}((V_{GZ} - V_{T0}(T) - nV_{SB})^2 - (V_{GZ} - V_{T0}(T) - nV_{DB})^2) + 2n|\alpha_{V_{T0}}|(V_D - V_S)\Big) \tag{2.56}$$

Isolating the term $V_{GZ} - V_{T0}(T)$, we get

$$V_{GZ} - V_{T0}(T) = -\left(\frac{n(V_{SB}^2 - V_{DB}^2)}{2(V_{DB} - V_{SB})} + \frac{T|\alpha_{V_{T0}}|}{\alpha_\mu}\right) \tag{2.57}$$

Moreover, finally substituting Eq. (2.29) in (2.57) for $V_{SB} = 0$ and $\alpha_\mu = -2$, Eq. (2.58) is obtained, where it shows what is the necessary gate-bulk voltage to achieve ZTC condition when MOS transistor is operating in strong inversion and linear regime.

$$V_{GZ} = V_{T0}(T_0) + |\alpha_{V_{T0}}|T_0 + \frac{nV_{DB}}{2} - \frac{|\alpha_{V_{T0}}|T}{2} \tag{2.58}$$

There is a large difference between Eq. (2.50) and Eq. (2.58), which represent ZTC bias point in saturation and linear regime, respectively. In Eq. (2.50), regardless of temperature, the ZTC bias point is the same. In contrast, in linear regime V_{GZ} changes proportionally to the temperature ($\frac{|\alpha_{V_{T0}}|T}{2}$), yielding different V_{GZ} for different temperature. It can be faced as there is a kind of V_{GZ} slipping throughout the entire temperature range. For example, if $|\alpha_{V_{T0}}| = 0.5$ mV/^{o}C, then a variation of around 32.5 mV under a temperature range between -45°C and 85°C will be found in measured V_{GZ}. Also, V_{GZ} in the linear regime is proportional to drain-bulk voltage (V_{DB}), as shown in Fig. 2.14.

2.4.2 ZTC Bias from UICM All-regime MOSFET Model

In a more general analysis, we must suppose that the bias ZTC condition in saturation regime can also appear in moderate inversion (Table 2.2). Thus, a complete MOSFET model must be used, such as one presented in section 2.1 and with more detail in [SCHNEIDER; GALUP-MONTORO (2010)], which describes continuously the transistor behavior in any inversion level. The Unified Current Control Model (UICM) is a design-oriented MOSFET model suitable for analog integrated-circuit design. From this model, the drain current of a long channel NMOSFET is given by Eqs. (2.21) and (2.17), repeated below for the sake of convenience in Eqs. (2.59) and (2.60).

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{2.59}$$

$$I_S = \mu_n C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{2.60}$$

Also, from this model Eqs. (2.20), (2.14) and (2.8) relates the source and drain inversion coefficients (forward and reverse), i_f and i_r, with the three external voltages applied to transistor terminals, V_G, V_S and V_D, using the bulk terminal as the reference. Again, equations are repeated bellow for sake of convenience.

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + ln\left(\sqrt{1 + i_{f(r)}} - 1\right)\right] \tag{2.61}$$

$$V_P = \frac{V_G - V_{T0}(T)}{n} \tag{2.62}$$

$$V_{T0}(T) = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{2.63}$$

If one derives drain current expression for temperature in the saturation region ($i_r << i_f$), the condition where its temperature dependence is negligible can be found, i.e., $(\partial I_D)/(\partial T)|_{T=T_1} = 0$. Using Eq. (3.47) and deriving it in function of temperature.

$$\left.\frac{\partial}{\partial T}(I_S i_f)\right|_{T=T_1} = I_S \left.\frac{\partial i_f}{\partial T}\right|_{T=T_1} + i_f \left.\frac{\partial I_S}{\partial T}\right|_{T=T_1} = 0 \tag{2.64}$$

The $\frac{\partial i_f}{\partial T}$ can be found deriving the expressions (2.61) and (2.62) with respect to temperature,

$$\frac{\partial}{\partial T}\left(\frac{V_G - V_{T0}}{n} - V_S\right) = \frac{\partial}{\partial T}(\phi_t[\sqrt{1+i_f} - 2 \\ + ln\left(\sqrt{1+i_f} - 1\right)]) \tag{2.65}$$

As V_G and V_S are temperature-independent $(\partial V_{G,S})/(\partial T)|_{T=T_1} = 0$,

$$\frac{\partial}{\partial T}\left(\frac{-V_{T0}}{n}\right) = \\ \frac{\partial \phi_t}{\partial T}\left[\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right] + \\ \phi_t \frac{\partial}{\partial T}\left(\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right) \tag{2.66}$$

Assuming that $\frac{\partial \phi_t}{\partial T} = \frac{\phi_t}{T}$ (Appendix B.2) and putting (2.29) in (2.66)

$$\frac{|\alpha_{V_{T0}}|}{n} = \frac{\phi_t}{T_1}\left[\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right] + \phi_t \frac{\partial}{\partial T}\left(\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right) \tag{2.67}$$

Noting that the second term of the right branch of the Eq. 2.67 is equal to

$$\frac{\partial}{\partial T}\left(\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right) = \left(\frac{1}{2(\sqrt{1+i_f}+1)}\right)\frac{\partial i_f}{\partial T} \tag{2.68}$$

And putting (2.68) in (2.67),

$$\frac{|\alpha_{V_{T0}}|}{n} = \frac{\phi_t}{T}\left[\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right] + \phi_t\left(\frac{1}{2(\sqrt{1+i_f}+1)}\right)\frac{\partial i_f}{\partial T} \tag{2.69}$$

Isolating the term $\frac{\partial i_f}{\partial T}$ from the Eq. (2.69), we get

$$\frac{\partial i_f}{\partial T} = (2(\sqrt{1+i_f}+1)) \left(\frac{|\alpha_{V_{T0}}|}{\phi_t n} - \frac{1}{T}\left(\sqrt{1+i_f} - 2 + ln(\sqrt{1+i_f} - 1)\right)\right) \tag{2.70}$$

The derivative of normalization current regarding the absolute temperature can be found from Eq. (2.60) and Eq. (2.32).

$$\frac{\partial I_S}{\partial T} = \frac{1}{2}C'_{ox}n\frac{W}{L}\frac{\partial}{\partial T}\left(\mu_n \phi_t^2\right) \tag{2.71}$$

where $(\partial n)/(\partial T)|_{T=T_1} = 0$, as explained in section 2.2. After some algebra,

$$\frac{\partial I_S}{\partial T} = \frac{1}{2}C'_{ox}n\frac{W}{L}\left(\frac{\partial \mu_n}{\partial T}\phi_t^2 + \frac{\partial \phi_t^2}{\partial T}\mu_n\right) \tag{2.72}$$

Therefore, we can use $\frac{\partial \mu_n}{\partial T} = \frac{\alpha_\mu \mu_n}{T}$ (Appendix B.1) and $\frac{\partial \phi_t^2}{\partial T} = \frac{2}{T}\phi_t^2$ (Appendix B.3)in (2.72), we obtain

$$\frac{\partial I_S}{\partial T} = I_S\left(\frac{\alpha_\mu + 2}{T}\right) \tag{2.73}$$

Finally, applying the equations (2.73) and (2.70) in (2.64) and after some algebra

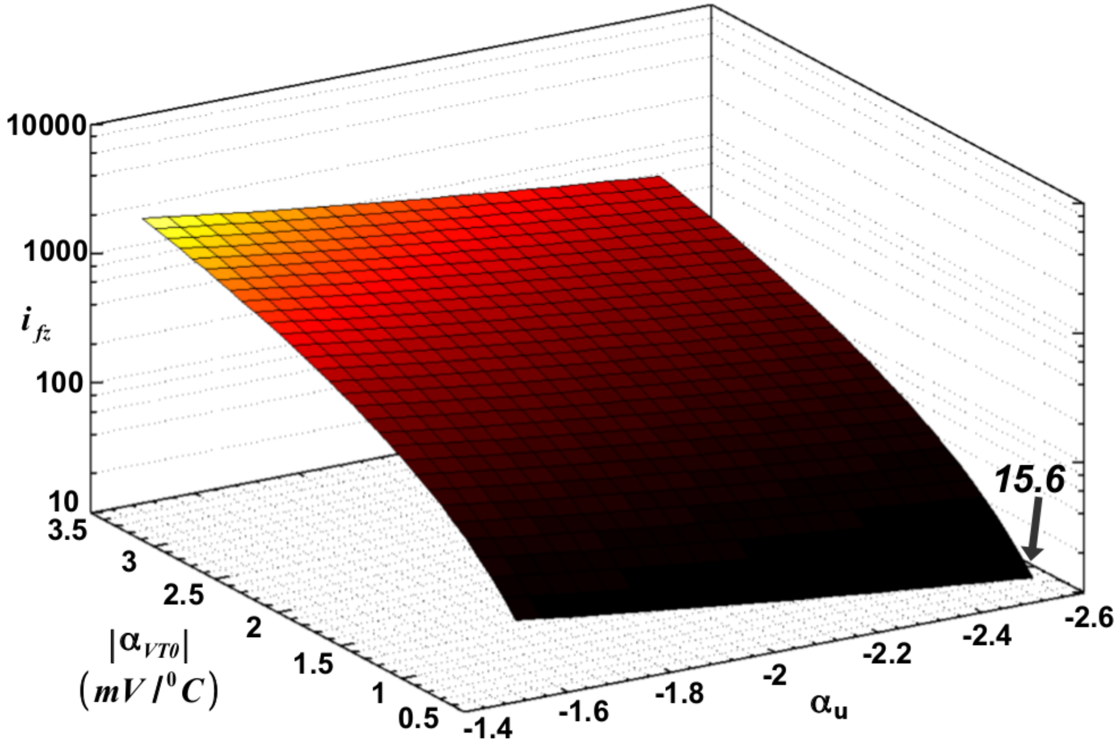


Figure 2.17: ZTC forward inversion level Surface (ZTCS). Graphic made with the script of appendix C.

$$\frac{|\alpha_{V_{T0}}|q}{nk} = \frac{|\alpha_{V_{T0}}|T}{n\phi_t} = \left(\frac{\alpha_\mu + 2}{2}\right)\left(\frac{-i_{fz}}{\sqrt{1+i_{fz}}+1}\right) + \left[\sqrt{1+i_{fz}} - 2 + ln\left(\sqrt{1+i_{fz}} - 1\right)\right] \tag{2.74}$$

For $\alpha_\mu \approx -2$,

$$\frac{|\alpha_{V_{T0}}|q}{nk} = \frac{|\alpha_{V_{T0}}|T}{n\phi_t} = \left[\sqrt{1+i_{fz}} - 2 + ln\left(\sqrt{1+i_{fz}} - 1\right)\right] \tag{2.75}$$

where k is the Boltzmann constant and i_{fz} is defined as the ZTC forward inversion level. Eq. (2.74) shows that if the transistor is biased in i_{fz}, the drain current is insensitive to temperature or, due to second order effects, presents low temperature sensitivity. Such effects will not be modeled in this thesis since the proposed modeling aim to generate a set of equations to support analog designers.

Fig. 2.17 shows the ZTC forward inversion level surface (ZTCS), i.e., all possible solutions of Eq. (2.74) for ZTC bias condition in function of α_μ and $\alpha_{V_{T0}}$. The range of possible values for each of such parameters, α_μ and $\alpha_{V_{T0}}$, has already been discussed in section 2.2. ZTCS shows that the minimum ZTC forward inversion level is around 15.6 for $\alpha_\mu = -2.5$ and $\alpha_{V_{T0}} = -0.5\ mV/^oC$. Since inversion coefficient $i_f = 3$ means the condition where $V_G = V_{T0}$ from Eqs. (2.61) and (2.62), one can conclude that ZTC bias condition always occurs for gate-bulk voltages larger than threshold voltage.

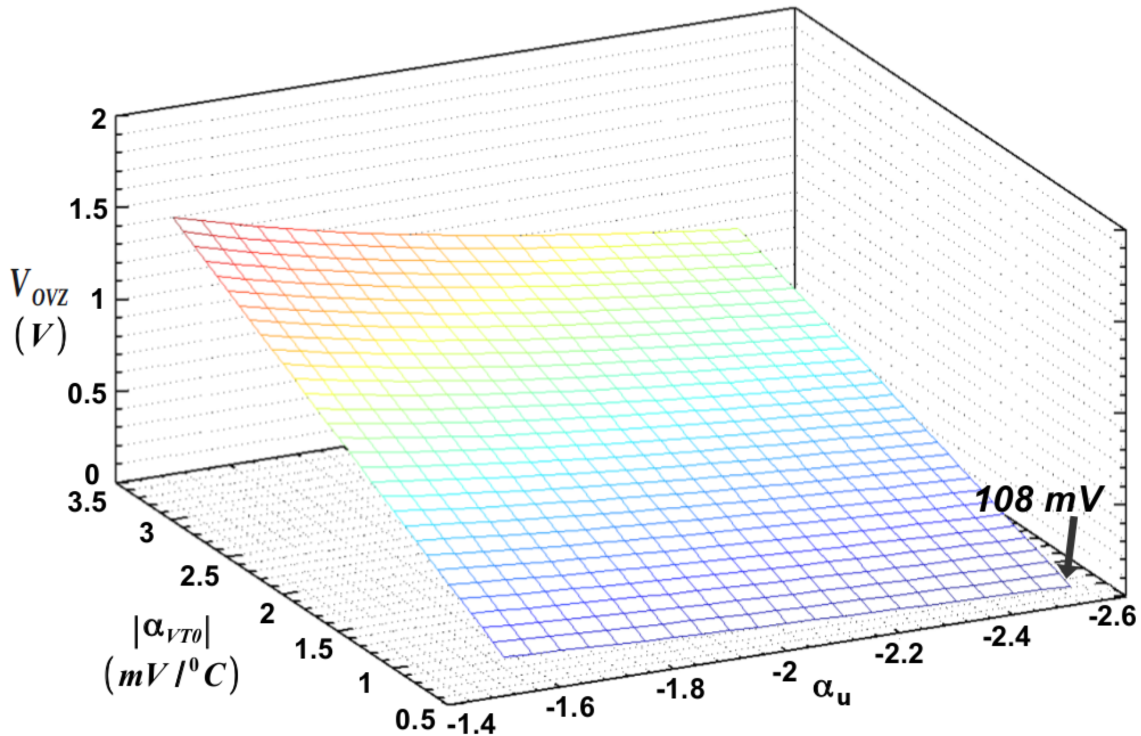


Figure 2.18: V_{OVZ} - the ZTC overdrive voltage. Graphic made with the script of appendix C.

Furthermore, it is visible that the ZTC inversion coefficient (i_{fz}) is only slightly dependent on α_μ, when compared to $\alpha_{V_{T0}}$ dependence. This observation justifies usual choice $\alpha_\mu \approx -2$ as a reasonable consideration for design purposes [FILANOVSKY; ALLAM (2001)].

To see how far ZTC bias point is from threshold voltage (the overdrive voltage for ZTC bias point), for $V_S = 0$, the i_{fz} can be straight applied in Eq. (2.61) and (2.62),

$$V_{GZ} - V_{T0} = V_{OVZ} = n\phi_t \left[\sqrt{1 + i_{fz}} - 2 + ln\left(\sqrt{1 + i_{fz}} - 1\right)\right] \tag{2.76}$$

where V_{OVZ} is defined as ZTC overdrive voltage. Fig. 2.18 shows all possible V_{OVZ} for any α_μ and $\alpha_{V_{T0}}$ combination in the same range that was used in Fig. 2.17. The minimum V_{OVZ} found is around $108mV$ meaning that ZTC bias point is always in the moderate inversion condition or above.

In analog and RF design, there is a well-known universal expression for MOS transistors, called transconductance-to-current ratio or colloquially "gm over id", which it is related to inversion level through Eq. (2.24), repeated in Eq. (2.77) for the sake of convenience. Several commercial tools provide, in their design environment, the transconductance to current ratio printing option of each transistor during design. It allows the designer evaluate and visualize how each transistor is behaving inside of the analog or RF block, regarding noise, mismatch, intrinsic gain, bandwidth, etc [BINKLEY (2007)]. Fig. 2.19 shows the transconductance-to-current ratio, or $(\frac{g_{mg}}{I_D})_Z$, related to calculated i_{fz} for each α_μ and $\alpha_{V_{T0}}$ combination in the same range that was used in Fig. 2.17 and 2.18.

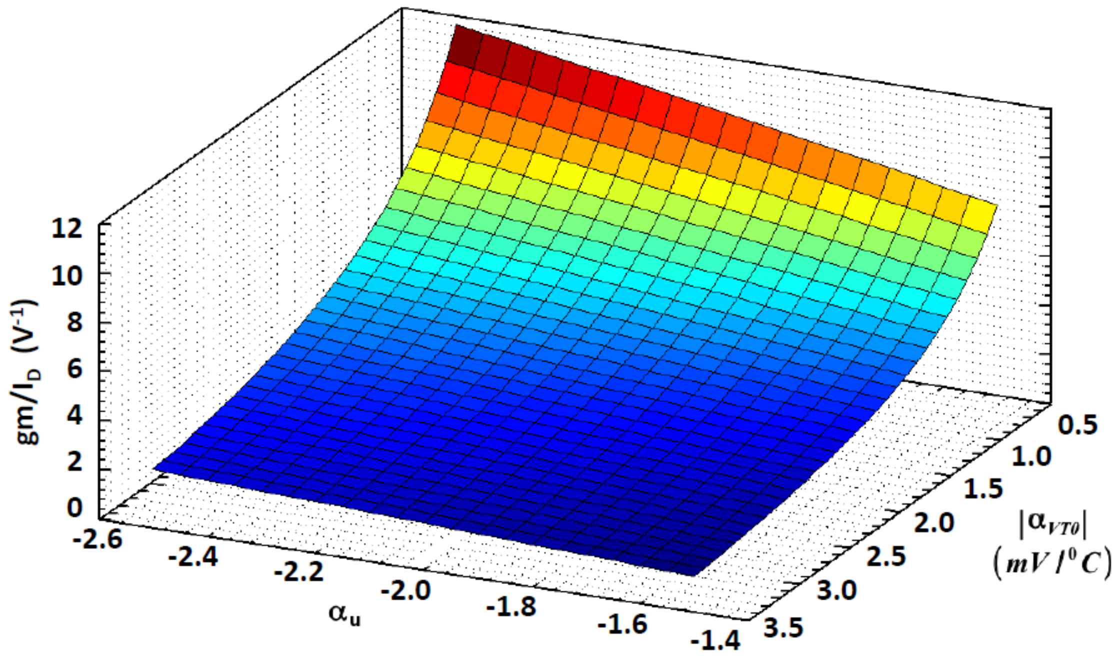


Figure 2.19: $(\frac{g_{mg}}{I_D})_Z$ or g_{mg} over I_D biased on i_{fz}. Graphic made with the script of appendix C.

Values of $(\frac{g_{mg}}{I_D})_Z$ between 1 and 12 were found.

$$\frac{g_{ms(d)}}{I_{F(R)}} = \frac{2}{\phi_t(\sqrt{1+i_f(r)}+1)} \tag{2.77}$$

Now using the assumption $\alpha_\mu \approx -2$ [Eq. (2.75)] together with Eq. (2.74) and (2.61) a simple expression for the ZTC gate-bulk voltage (V_{GZ} - related to i_{fz}) is found.

$$V_{GZ} = V_{T0}(T_0) + nV_S - \alpha_{V_{T0}} T_0 \tag{2.78}$$

Eq. (2.78) presents the same result already derived from the strong inversion model in Eq. (2.45) and (2.50). The ZTC drain-current, related to i_{fz}, can be found using Eq. (3.47)

$$I_{DZ} = I_{FZ} = I_S(T_0) i_{fz} \tag{2.79}$$

2.4.3 ZTC Bias Vicinity Condition from UICM Model

Beyond the understanding of bias ZTC point itself, it is interesting to study what happens if the transistor is biased in its vicinity. Filanovsky was the first to study and model it [FILANOVSKY; ALLAM (2001)]. As this section will show in details, the ZTC vicinity modeling is very relevant for Analog/RF design purpose. It gives the designer insights on the transistor thermal behavior with respect to temperature variations. Furthermore, it gives insights how to make the MOS transistor and, consequently, the circuit independent of temperature.

The ZTC vicinity condition can be analyzed using Eqs. (2.20) and (2.14), repeated

below in Eq. (2.80) and (2.81)

$$V_{GB}(i_f) = n\phi_t f(i_f) + V_{T0}(T) + nV_S \tag{2.80}$$

where

$$f(i_f) = \left[\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right] \tag{2.81}$$

Eq. (2.80) can be expanded in Taylor series around ZTC forward inversion level (i_{fz}). Therefore, first order approximation is given by

$$V_{GB}(i_f) \approx V_{GZ} + \left.\frac{\partial V_{GB}}{\partial i_f}\right|_{i_f=i_{fz}} (i_f - i_{fz}) \tag{2.82}$$

where

$$\frac{\partial V_{GB}}{\partial i_f} = \frac{n\phi_t}{2(\sqrt{1+i_f} - 1)} \tag{2.83}$$

Making $\alpha_\mu \approx -2$ [FILANOVSKY; ALLAM (2001)], the term $n\phi_t$ can be extracted from Eq. (2.74), we get

$$V_{GB}(T) \approx V_{GZ} - \frac{\alpha_{V_{T0}} \Delta i_f}{2f(i_{fz})(\sqrt{1+i_{fz}} - 1)} T = V_{GZ} - \beta_z \Delta i_f T \tag{2.84}$$

where $\Delta i_f = i_f - i_{fz}$ indicates how far the transistor is biased from ZTC operating point, and β_z is defined as ZTC slope. As the $if = I_d/I_S$ from the Eq. (3.47), the dependency of $V_{GB}(T)$ on the temperature can be found such that:

$$V_{GB}(T) \approx V_{GZ} - \frac{\beta_z \Delta I_d}{I_{SQ}\frac{W}{L}} T \tag{2.85}$$

where

$$\beta_z = \frac{\alpha_{V_{T0}}}{2f(i_{fz})(\sqrt{1+i_{fz}} - 1)} \tag{2.86}$$

Eq. (2.85) shows that V_{GB} approximately presents a linear temperature dependence in the vicinity of V_{GZ}, and that this dependence can be either positive or negative, depending on the ΔI_d chosen. Fig. 2.20 illustrates the temperature dependence of Eq. (2.85), showing that if one chooses $\Delta I_d > 0$ (bias current "after" the ZTC point), its derivative is positive or Proportional to Temperature Absolute Temperature (PTAT). If $\Delta I_d = 0$ is chosen (ZTC point), variation is zero. If $\Delta I_d < 0$ (bias current "before" the ZTC point), its derivative is negative or Complementary to Temperature Absolute Temperature (CTAT). One can conclude that a MOSFET operating in the vicinity of ZTC point presents a thermal behavior that can offer a positive or negative thermal dependence. The signal and magnitude of the dependence can be adjusted by choosing bias current. Note that the same analysis can be done for drain current, adjusting gate-bulk voltage at a certain distance from V_{GZ}.

ZTC slope (β_z) is entirely dependent on $\alpha_{V_{T0}}$, described by Eq. (2.86). Fig. 2.21 shows possible values for β_z under $\alpha_{V_{T0}}$ range between -3.5 and -0.5 mV/^{o}C and $\alpha_\mu \approx -2$.

In this ZTC vicinity analysis so far, it is supposed that applied bias current, or $I_D = I_{DZ} + \Delta I_d$, is temperature independent. However, a current with a temperature coefficient

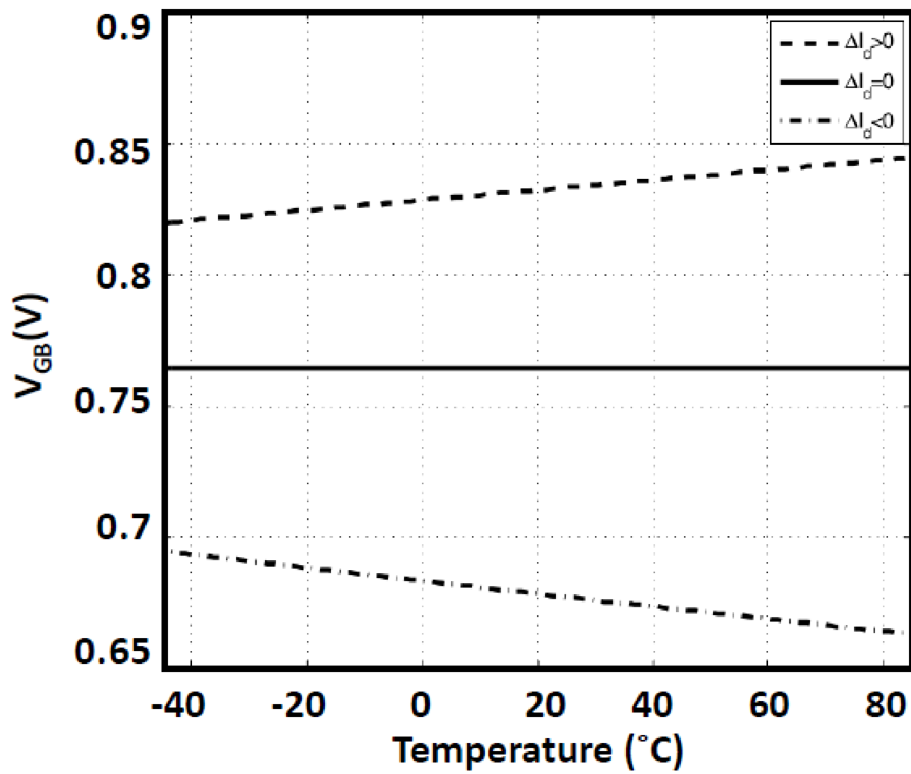


Figure 2.20: $V_{GB}(T)$ for $\Delta I_d > 0$, $\Delta I_d = 0$ and $\Delta I_d < 0$. Simulated data from 180 nm CMOS technology.

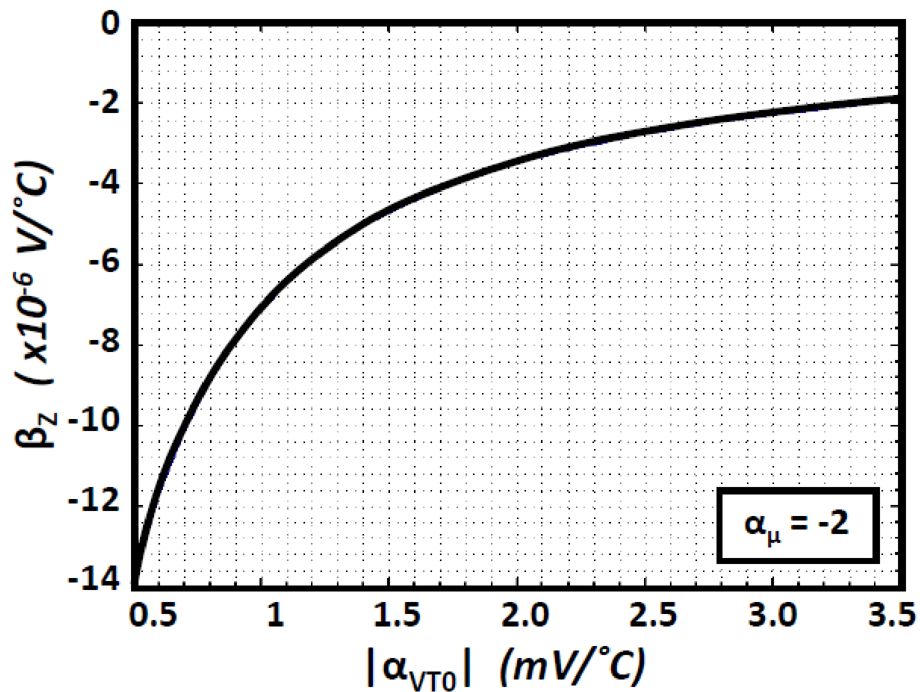


Figure 2.21: β_z in function of $|\alpha_{V_{T0}}|$. Note that, for adopted assumption $\alpha_\mu \approx -2$, β_z is always negative since it is only dependent of $\alpha_{V_{T0}}$. Graphic made with the script of appendix C.

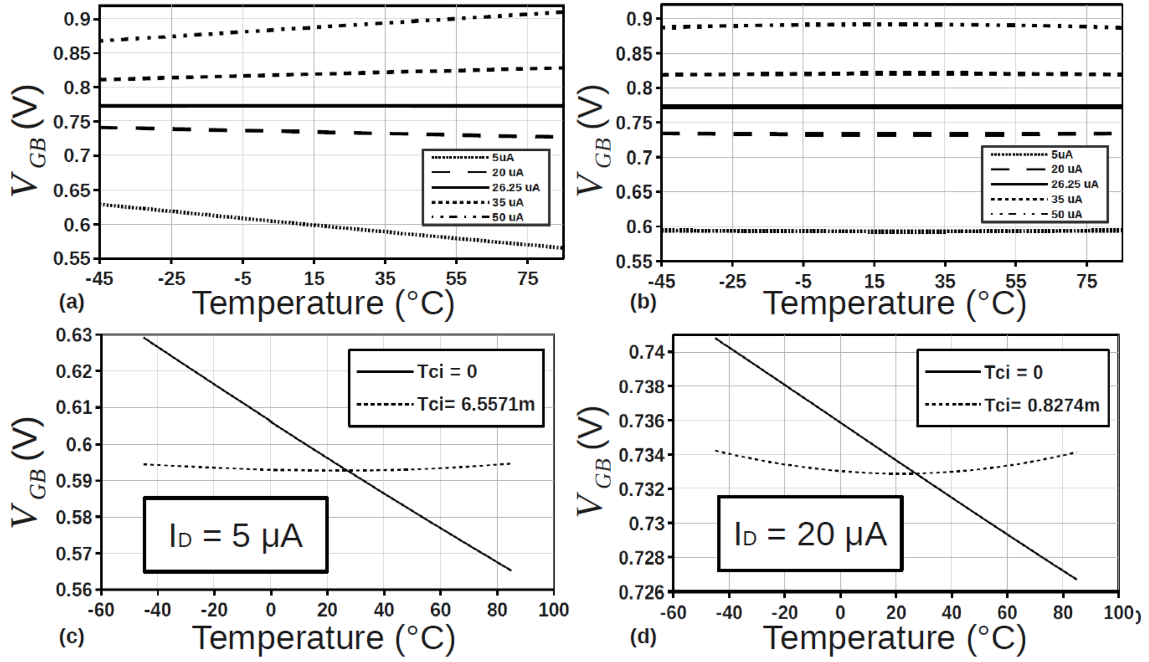


Figure 2.22: (a) simulations data for a diode-connected NMOS transistor (W/L = $2.5\mu m/1\mu m$) in 180 nm CMOS technology with five different bias current (5, 20, 26.25, 35, 50 μA), yielding distinct V_{GB} temperature dependence. (b) V_{GB} versus temperature enforcing right TC_I that cancels PTAT or CTAT behavior. (c) Zoom for $I_D = 5\mu A$. (d) Zoom for $I_D = 20\mu A$.

(TC_I) can be inserted in transistor drain in order to compensate the PTAT ($\Delta I_d > 0$) or CTAT ($\Delta I_d < 0$) $V_{GB}(T)$ behavior, given by Eq. (2.85) and illustrated in Fig 2.20 for 180 nm CMOS process.

Making the same procedure that has been done, but now applying a current with temperature dependence given by Eq. (2.87) in Eq. (2.59) for saturation regime and differentiating latter with respect to temperature, Eq. (2.88) is achieved.

$$I_D = (I_{DZ} + \Delta I_d)(1 + TC_I(T - T_0)) = I_{D0}(1 + TC_I(T - T_0)) \tag{2.87}$$

$$\frac{\partial}{\partial T}\left(I_S i_f\right)\Big|_{T=T_0} = I_S \frac{\partial i_f}{\partial T}\Big|_{T=T_0} + i_f \frac{\partial I_S}{\partial T}\Big|_{T=T_0} = I_{D0} TC_I \tag{2.88}$$

Now, using Eqs. (2.73) and (2.70) in (2.88) and after some algebra effort, we get

$$\frac{|\alpha_{V_{T0}}| q}{nk} = \frac{|\alpha_{V_{T0}}| T_0}{n\phi_{t_0}} = \left[\frac{TC_I T_0}{2} - \left(\frac{\alpha_\mu + 2}{2}\right)\right]\left(\frac{i_{f0}}{\sqrt{1+i_{f0}}+1}\right) + \left[\sqrt{1+i_{f0}} - 2 + ln\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{2.89}$$

where i_{f0} is inversion level related to I_{D0} under room temperature. Eq. (2.89) opens up scope for an interesting interpretation. For instance, TC_I = 0 leads to Eq. (2.89) to be the same as Eq. (2.74) such that i_{f0} becomes i_{fz}. Therefore, it is reasonable to claim that

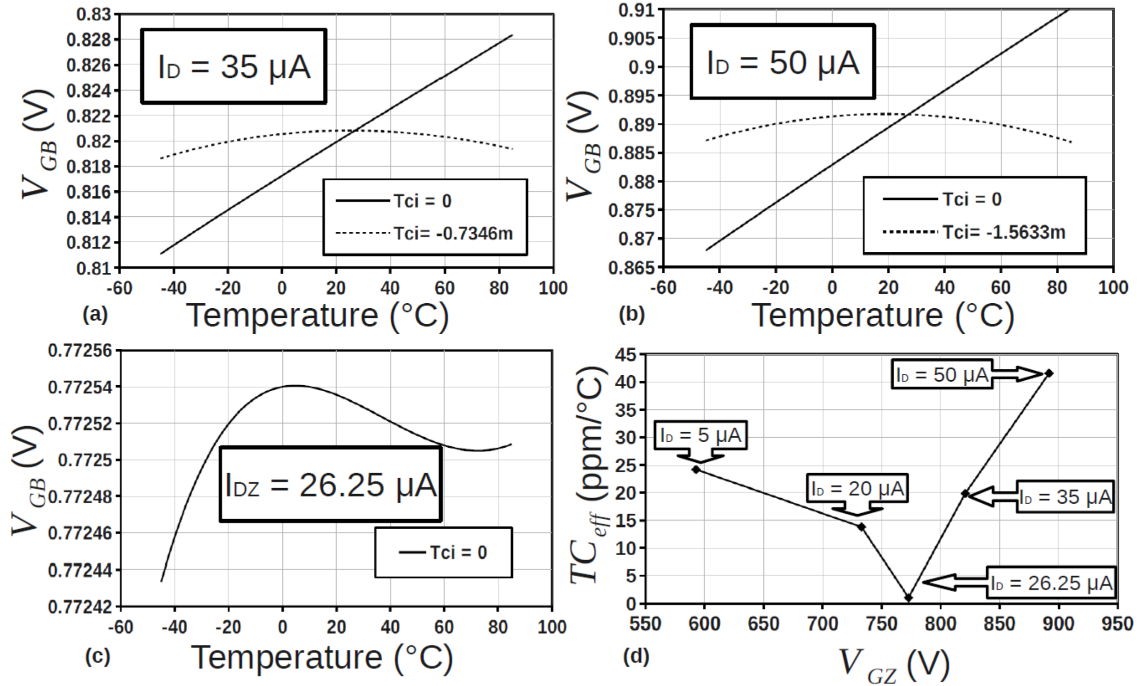


Figure 2.23: (a) Zoom for $I_D = 35\mu A$. (b) Zoom for $I_D = 50\mu A$. (c) Zoom for $I_D = 26.25\mu A$. (d) TC_{eff} for each vicinity condition.

applying a drain current with $TC_I \neq 0$ is equivalent to moving the ZTC forward inversion level to another value, i. e., i_{fz} to i_{f0}.

Fig 2.22 (a) shows simulations data for a diode-connected NMOS transistor with (W/L = $2.5\mu m/1\mu m$) in 180 nm CMOS technology. It is visible that five different bias current are applied: 5, 20, 26.25, 35, 50 μA, yielding distinct V_{GB} temperature dependence. These applied currents are temperature independent, i.e., TC_I = 0. In this picture, for I_{D0} = $26.25\mu A$ is equivalent to say that NMOS is working on bias ZTC point. For I_{D0} with $5\mu A$, $20\mu A$ and with $35\mu A$, $50\mu A$, the NMOS transistor is working on ZTC vicinity at CTAT and PTAT regime, respectively. This is in close agreement with Eq. (2.85).

On the other hand, if a current with a $TC_I \neq 0$ is applied, there is a specific value of inversion level, or i_{f0}, where it is maintained constant regarding the temperature variations, more specifically around T_0. Fig 2.22 (b), which shows V_{GB} versus temperature enforcing right TC_I that cancels PTAT or CTAT behavior, summarizes previous explained reasoning. In more details, Fig. 2.22 (c)(d) and Fig. 2.23 (a)(b) show V_{GB} temperature dependence being canceled for each applied I_{D0} with their suitable TC_I values. By contrast in Fig. 2.23, (c) this case does not needs a TC_I, or TC_I = 0, since it is on ZTC bias point.

Fig. 2.23 (d) shows the calculated Effective Temperature Coefficient (TC_{eff}) related to V_{GB} for each case, at which necessary TC_I to cancel temperature dependence was already applied. TC_{eff} is given by Eq. (2.90). According to Fig. 2.23 (d), even if a suitable value for TC_I is chosen, the V_{GB} thermal stability will be worse than if it was biased exactly over ZTC point. In addition to other secondary effects, this deterioration in thermal stability is easily explained by noting that Eq. (2.89) has a second derivative with respect to temperature. It does not occur in the case where the MOS transistor is biased exactly over the ZTC point [Eq. (2.74)].

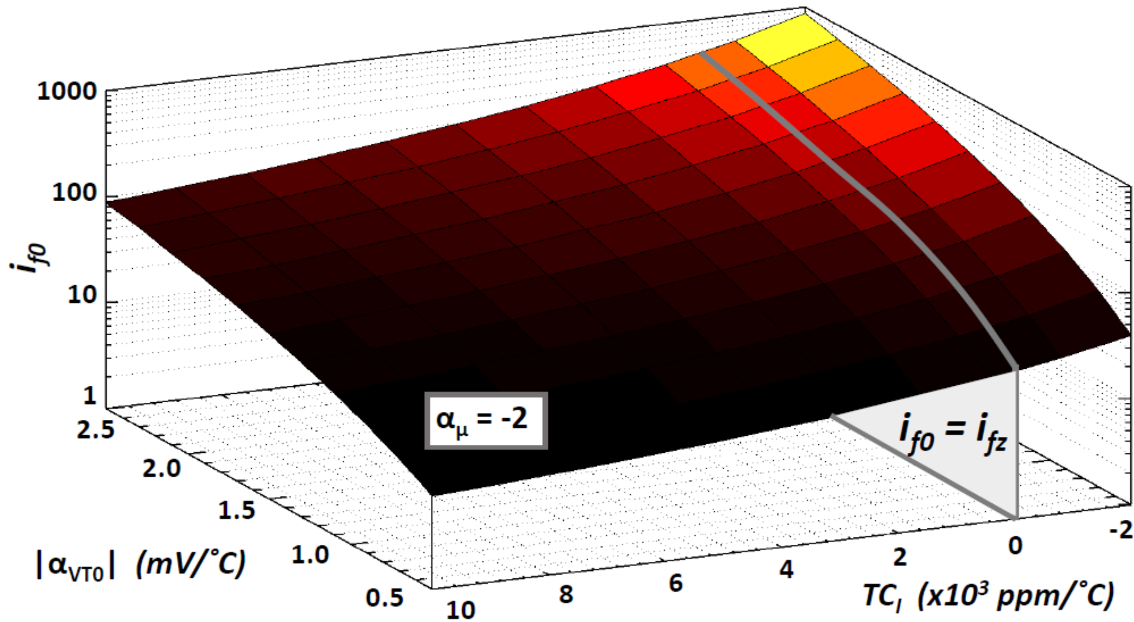


Figure 2.24: i_{f0} in function of TC_I and $\alpha_{V_{T0}}$. Graphic made with the script of appendix C.

$$TC_{eff}|_X = \frac{X_{max} - X_{min}}{(T_{max} - T_{min})X(T_0)} \tag{2.90}$$

where X is the desired parameter to be evaluated.

From Eq. (2.89) and making $\alpha_\mu \approx -2$, we get

$$\frac{|\alpha_{V_{T0}}|q}{nk} = \left(\frac{TC_I T_0}{2}\right)\left(\frac{i_{f0}}{\sqrt{1+i_{f0}}+1}\right) + \left[\sqrt{1+i_{f0}} - 2 + ln\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{2.91}$$

Fig. 2.24 demonstrates all possible solutions of Eq. (2.91) for i_{f0} in function of TC_I and $\alpha_{V_{T0}}$. It is worth noting that $TC_I = 0$ also means solutions of Eq. (2.75) that is explicit in Fig. 2.24.

In the same manner previously done, it is possible to bring out through Eqs. (2.61) and (2.62) the voltage overdrive related to each i_{f0}, as described by Eq. (2.92). Fig. 2.25 shows the overdrive voltage change around the ZTC point (TC_I = 0) for different values of the current temperature coefficients (TC_I). One may properly conclude that for technologies with higher values of $|\alpha_{V_{T0}}|$, it is possible to reach higher overdrive variations for the same range of TC_I.

$$V_{G0} - V_{T0} = V_{OV0} = n\phi_{t0}\left[\sqrt{1+i_{f0}} - 2 + ln\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{2.92}$$

where V_{G0} and V_{OV0} are gate-bulk and overdrive voltage for each i_{f0}, respectively.

In summary, analog designers can use all the presented ZTC modeling as a reference (including ZTC and its vicinity) to predict and avoid changes in the transistor behavior

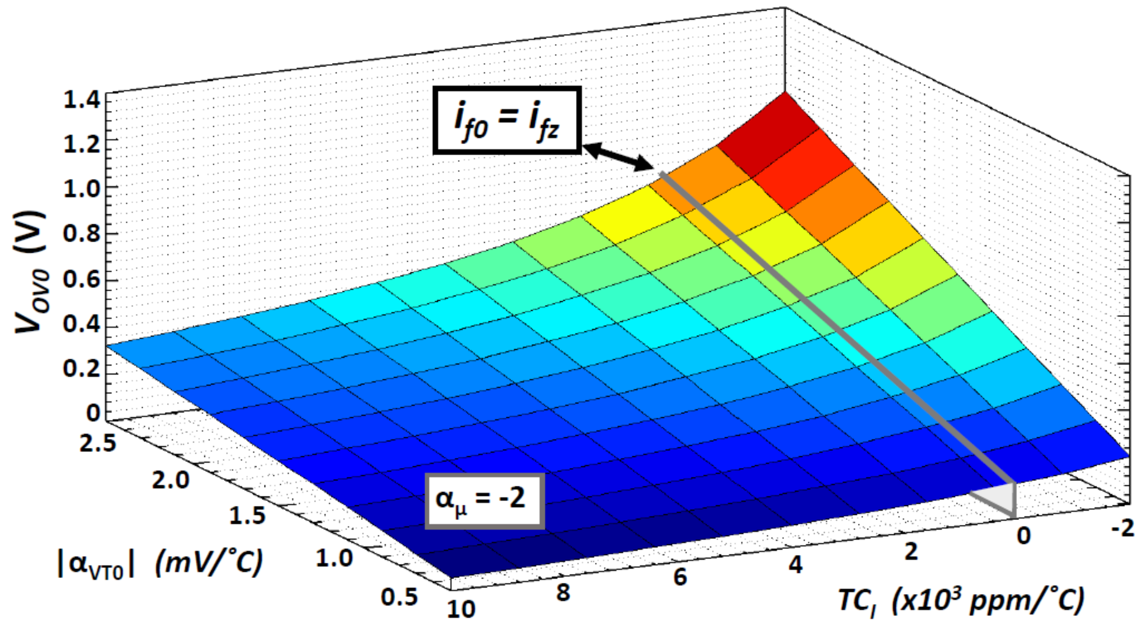
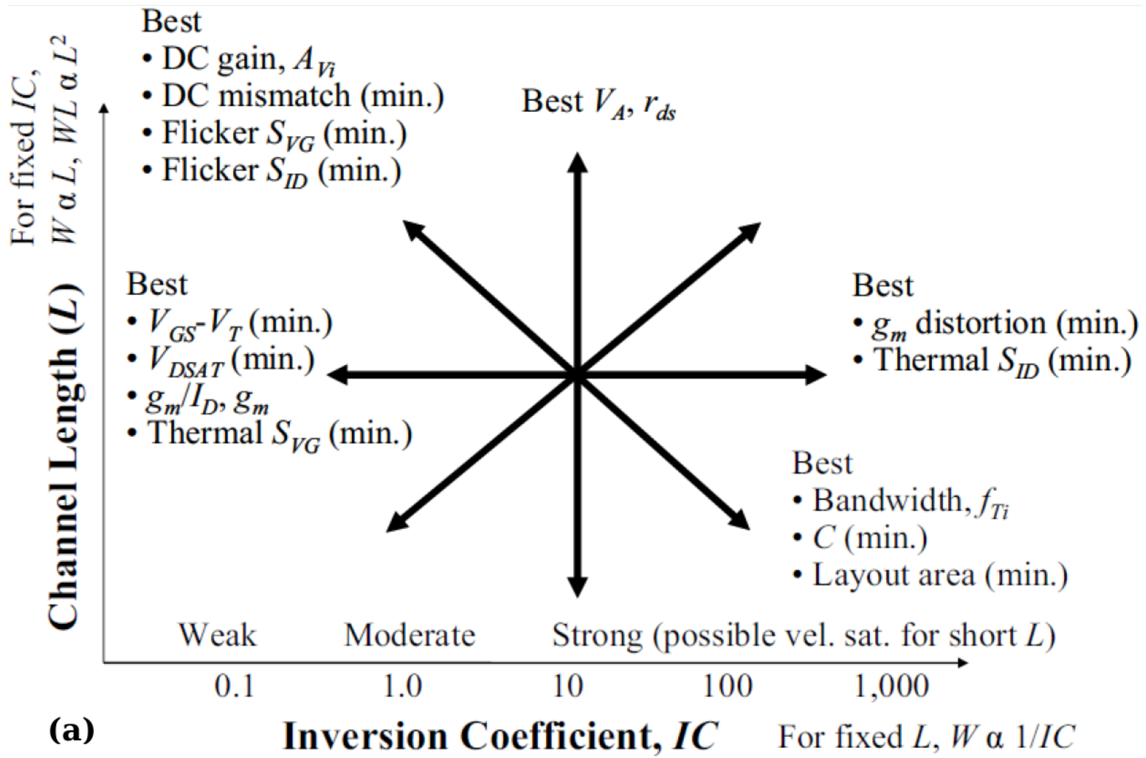


Figure 2.25: Overdrive voltage change around ZTC point (TC_I = 0) for different values of current temperature coefficients (TC_I). Graphic made with the script of Appendix C.

when there are temperature variations. A famous figure, Fig. 2.26 (a) [BINKLEY (2007)], which is used as guide by several designers, gives MOS device tradeoffs over its performance, embracing transconductance efficiency (g_m/I_d), Early voltage (V_A), intrinsic gain (g_m/g_{ds}), bandwidth (f_t), distortion, thermal noise (Thermal S_{VG} and S_{ID}), Flicker noise (Flicker S_{VG} and S_{ID}) and Mismatch. To explore all inversion levels of the MOS transistor, Fig. 2.26 (a) uses a similar concept of inversion level, introduced in [ENZ; KRUMMENACHER; VITTOZ (1995)]. However, this qualitative illustration does not give insight into temperature variation. In Fig. 2.26 (b), MOSFET operating plan is translated to the concept of inversion level defined in [SCHNEIDER; GALUP-MONTORO (2010)]. It is integrated inside of it how V_{GB} behaves in function of temperature and what is the needed TC_I (PTAT or CTAT) to keep the transistor inversion level immune to temperature variation. Also in proposed Fig. 2.26 (b), it is worth emphasizing that the center of the figure is over ZTC forward inversion level that is dependent of α_μ and α_{VT0}.



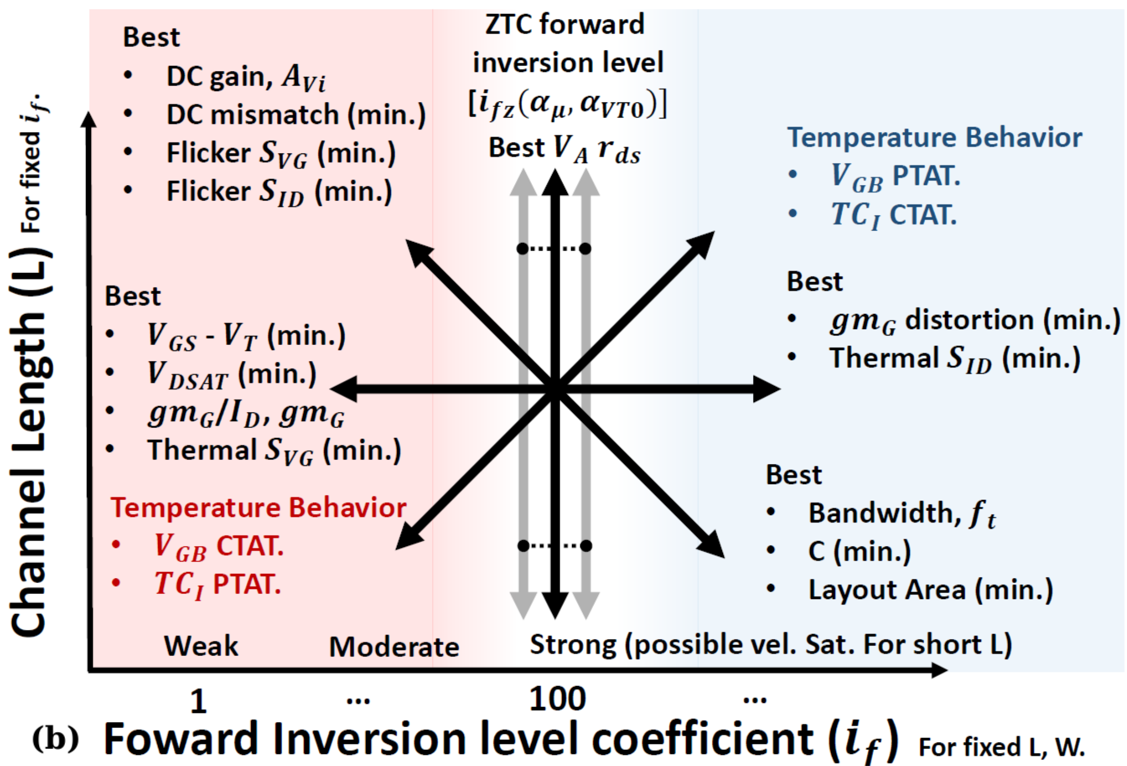


Figure 2.26: (a) The MOSFET operating plane illustrating tradeoffs in performance for the selected inversion coefficient and channel length. Copyright John Wiley and Sons Limited. (b) MOSFET operating plane translated to UCIM presented before including temperature behavior of MOSFET transistor.

2.5 MOSFET Transconductance ZTC Condition

As done in the last section for the bias operation point, a similar analysis can be developed for the MOSFET gate-transconductance (g_{mg}). to define a bias condition where g_{mg} does not change with temperature variation or presents a low dependence due to second orders effects. This condition is called Transconductance Zero Temperature Coefficient, or GZTC, and its definition is important since in any analog signal processing block the gain is fundamentally determined by the transistors transconductance, resulting that the gain is sensitive to temperature variations in most designs. If the design is developed with the GZTC point in mind, the gain results less sensitive to temperature.

Similarly to the last section, an inversion level (i_{fgz}) where the transconductance presents low temperature dependence can be found. From the combination of Eq. (2.22) and (2.23) in saturation regime, the small signal transconductance is related to forward inversion level as follows

$$g_{mg} = \frac{g_{ms}}{n} = \frac{2I_S}{n\phi_t}(\sqrt{1+i_f} - 1) \tag{2.93}$$

Applying the condition $(\partial g_{mg})/(\partial T)|_{T=T_1} = 0$, Eq. (2.94) is obtained (Appendix B.4).

$$0 = \alpha_\mu(\sqrt{1+i_{fgz}} - 1) - 2 + \frac{\sqrt{1+i_{fgz}}+1}{\sqrt{1+i_{fgz}}}\left(\frac{|\alpha_{V_{T0}}|q}{nk} + 2 - ln\left(\sqrt{1+i_{fgz}} - 1\right)\right) \tag{2.94}$$

One can note that, as in the case of bias current I_D, the condition GZTC is derived from the mutual cancellation of the mobility and threshold voltage dependencies on temperature, which happens for a particular bias condition, $V_{GB}(i_{fgz}) = V_{GGZ}$.

Fig. 2.27 (a) shows ZTC forward inversion level surface (ZTCS) from previous section and GZTC forward inversion level surface (GZTCS), i.e., all possible solutions of Eq. (2.74) and Eq. (2.94) as a function of α_μ and $\alpha_{V_{T0}}$. This solution shows that the minimum ZTC and GZTC forward inversion levels are different, resulting around 15.6 and 9.1 for the values $\alpha_\mu = -2.5$ and $\alpha_{V_{T0}} = -0.5\ mV/^oC$. Since the inversion level $i_f = 3$ defines the condition where $V_G = V_{T0}$ from Eqs. (2.61) and (2.62), one can readily conclude that both ZTC conditions always occur for gate-bulk voltages larger than the threshold voltage, in moderate or strong inversion.

In order to see how far each ZTC bias point is from threshold voltage (the overdrive voltage for ZTC and GZTC bias point), for $V_S = 0$, i_{fz} and i_{fgz} can be directly applied in Eq. (2.61) and (2.62),

$$V_{GZ(GZ)} - V_{T0} = V_{OVZ(GZ)} = n\phi_t f(i_{fz(gz)}) \tag{2.95}$$

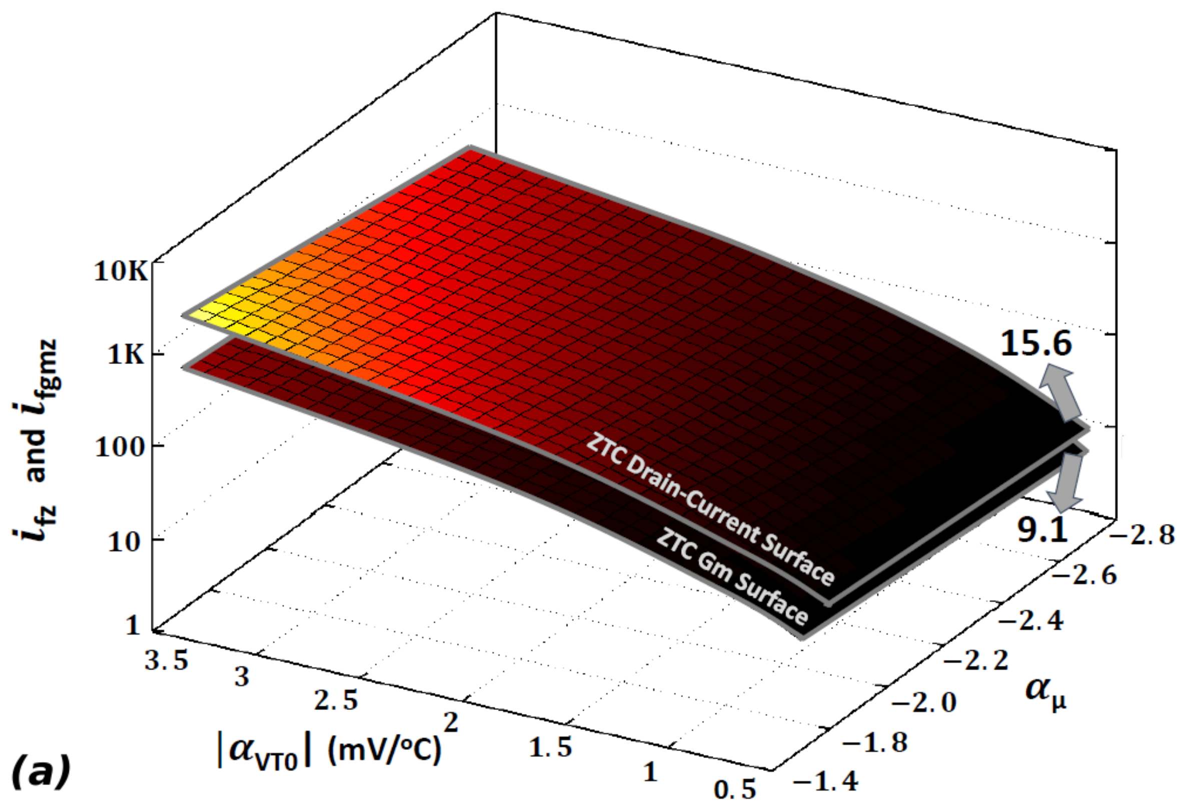
where

$$f(i_f) = \left[\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right] \tag{2.96}$$

V_{OVGZ} is defined as GZTC overdrive voltage. Fig. 2.27 (b) shows all possible overdrive voltages for any α_μ and $\alpha_{V_{T0}}$ combination in the same range that was used in Fig. 2.27 (a). The minimum V_{OVZ} and V_{OVGZ} found are around $108mV$ and $66mV$ respectively, meaning that both ZTC bias points are always in moderate or strong inversion

regime. Another conclusion is that ZTC will always be above the GZTC bias point, i.e., GZTC is working in ZTC vicinity with a CTAT behavior (Fig. 2.20), as can be also seen in Fig. 2.28 for a PMOS transistor in 130 nm CMOS technology (simulation data).

Finally, it is evaluated necessary TC_I in order to equalize i_{f0} = i_{gz}, i. e., to maintain i_{gz} stable over temperature variations in such manner that the transconductance (gm_g) becomes independent of temperature. Therefore, finding i_{gz} from Eq. (2.94) for each $|\alpha_{V_{T0}}|$ and α_μ and then putting in Eq. (2.89), the needed temperature coefficient, or TC_{IGZ}, to make the transconductance unvarying with temperature can be found, as shown Fig. 2.29. Unlike of previous results, α_μ has more impact than $|\alpha_{V_{T0}}|$ in TC_{IGZ}. Values between 3000 and 9500 ppm/^{o}C have been calculated, which comply with CMOS PTAT current reference found in literature, where TC_I between 1000 and 10000 are readily achieved [SERRA-GRAELLS; HUERTAS (2003)].



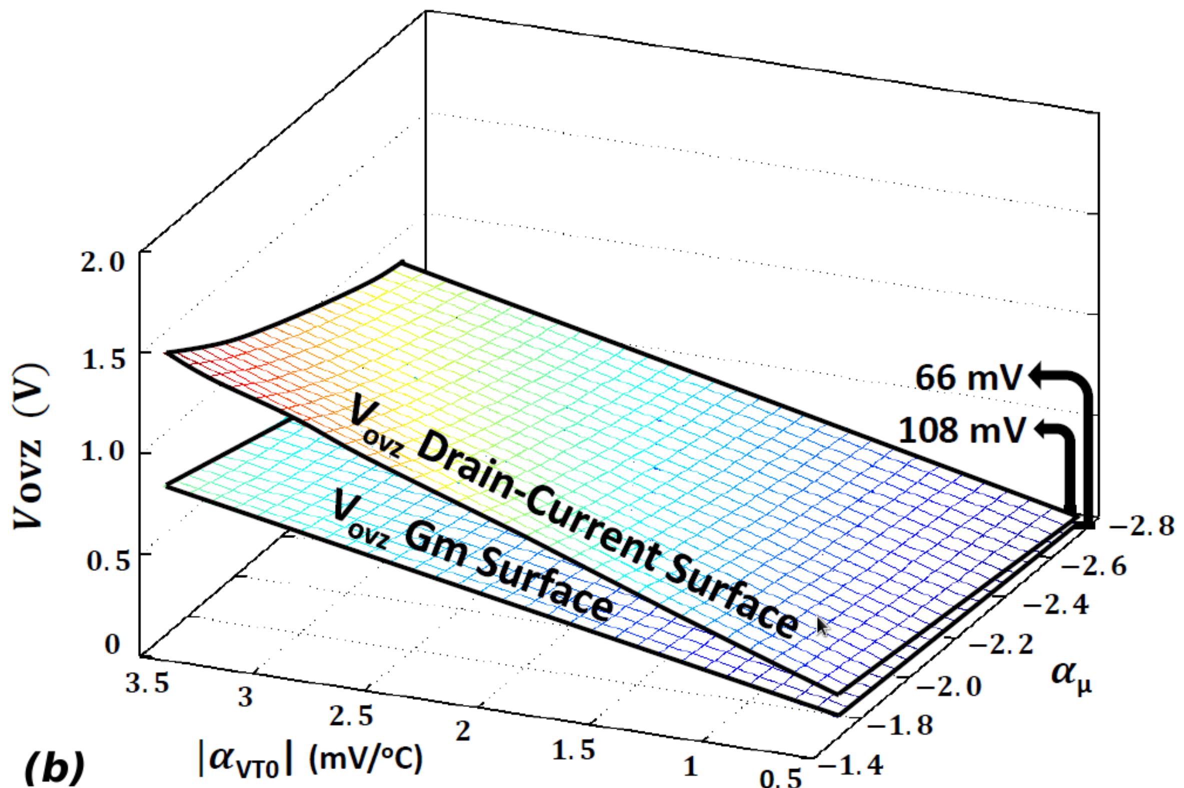


Figure 2.27: (a) ZTC forward inversion level surface (ZTCS) and GZTC forward inversion level surface (GZTCS) (b) overdrive voltage for the ZTC (V_{OVZ}) and GZTC bias point (V_{OVGZ}) as a function of the values for α_μ and $\alpha_{V_{T0}}$. Graphics made with the script of Appendix C.

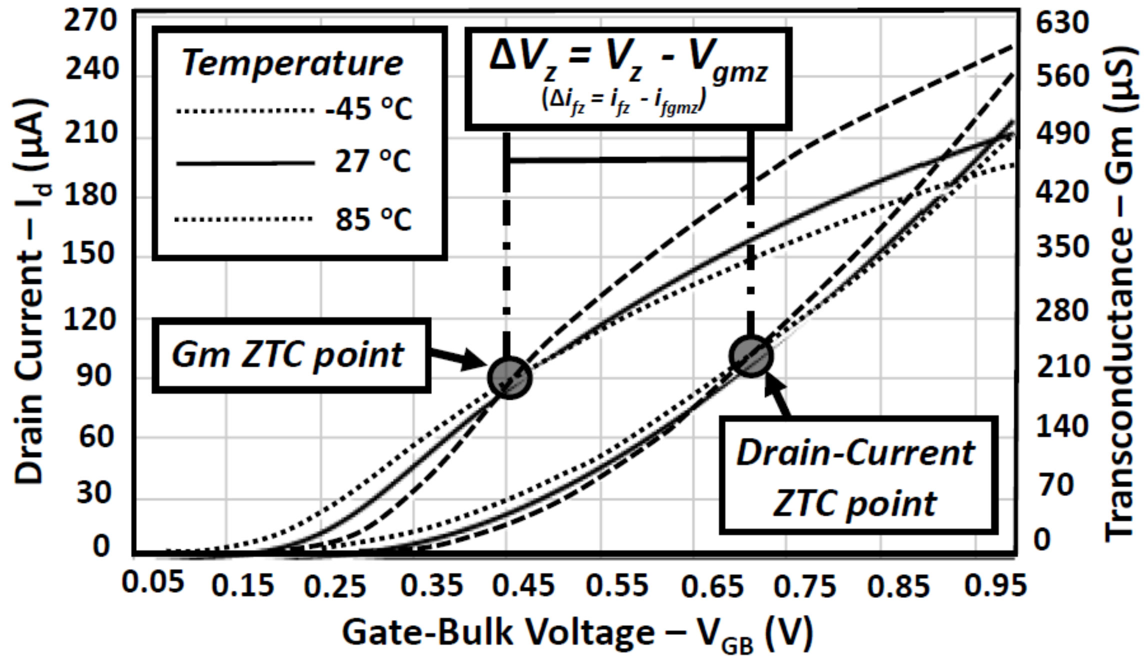


Figure 2.28: ZTC and GZTC condition for a PMOS transistor in a 130 nm process with $V_{T0} = 250$ mV. These curves have been plotted using V_{DS} = V_{GS}.

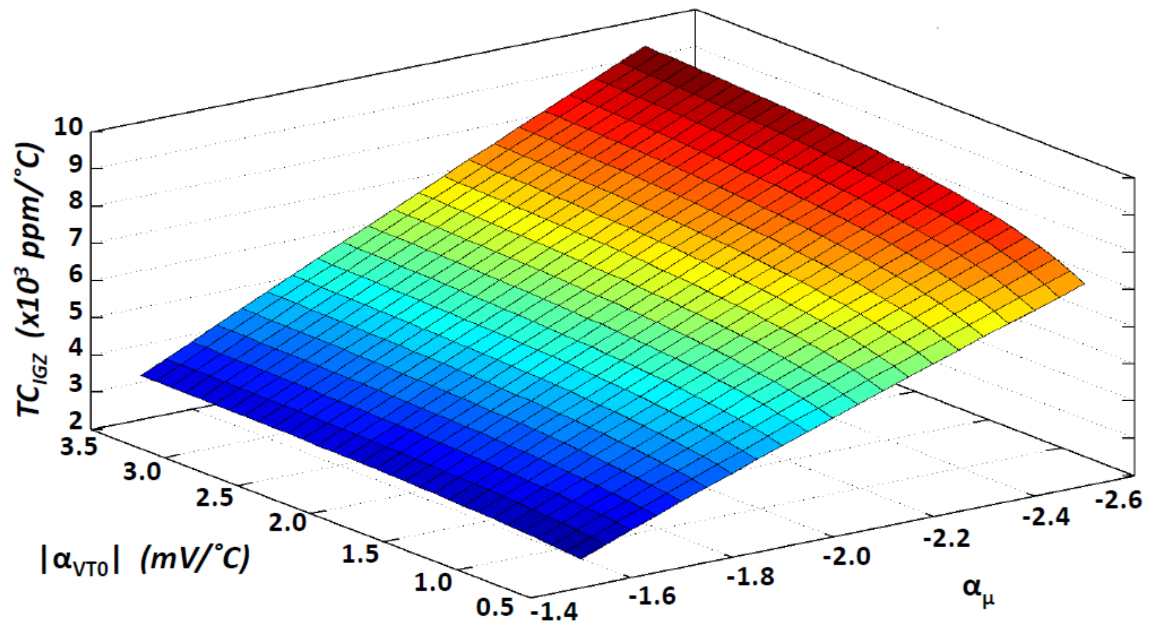


Figure 2.29: Necessary TC_I, or TC_{IGZ}, to keep the MOSFET transconductance temperature independent in function of $|\alpha_{V_{T0}}|$ and α_μ. Graphic made with the script of appendix C.

3 ANALOG APPLICATIONS USING ZTC CONDITION

In this chapter whole ZTC and GZTC analyses previously done are used to design temperature independent CMOS analog circuits. Firstly, two current references are proposed such that ZTC and ZTC vicinity concepts are handled to generate a current source with no temperature dependence. Then, two new voltage references are also proposed using a similar design methodology employed in previous current references. Finally, GZTC operating point is used to design the transconductor part of gm-C filters (Such filters are called here as GZTC Filters) with the aim of to make these circuits independent of temperature.

This chapter 3 is organized as follows: Sections 3.1 and 3.2 present two new current references. In Section 3.3 and 3.4, two new voltage references are proposed. Lastly, the concept of transconductor with low temperature dependence is embedded in Gm-C filters at Section 3.5.

3.1 Self-biased CMOS Current Reference based on ZTC Operation Condition - ZSBCR

Current references are essential building blocks for analog, mixed-signal and RF designs, often being used for biasing of analog subsystems inside the chip. The usual way to generate a current reference is through the implementation of a voltage reference [BANBA et al. (1999); MALCOVATI et al. (2001); KLIMACH et al. (2013)] and applying this voltage over a resistive device [BENDALI; AUDET (2007)]. Another approach is using a device where a physical property or condition naturally establishes an operating current to use as a reference [TALEBBEYDOKHTI et al. (2006); LIU; KUSSENER (2010); LUKASZEWICZ; BOREJKO; PLESKACZ (2011); YOO; PARK (2007); CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER (2005); FILANOVSKY; ALLAM (2001); FILANOVSKY; BAI; MOORE (2009); FIORI; CROVETTI (2005)].

Any kind of DC reference, either a voltage or a current one, must offer appreciable thermal stability and power supply rejection, as its main characteristics. In addition, adequate fabrication repeatability ensures that the biasing operation point of analog blocks is almost the same in any chip, and reveals how sensitive current generator is with respect to fabrication process variations. Here, proposed current references are designed to attend all requirements above described.

The main idea of this proposed current reference is to use the ZTC vicinity of NMOS transistor, instead of ZTC point itself. This approach compensates the thermal drift of a poly-silicon resistor, resulting in an equilibrium bias point with small temperature dependence [TOLEDO et al. (2014)]. Fig. 3.1 demonstrates the fundamental idea of circuit in

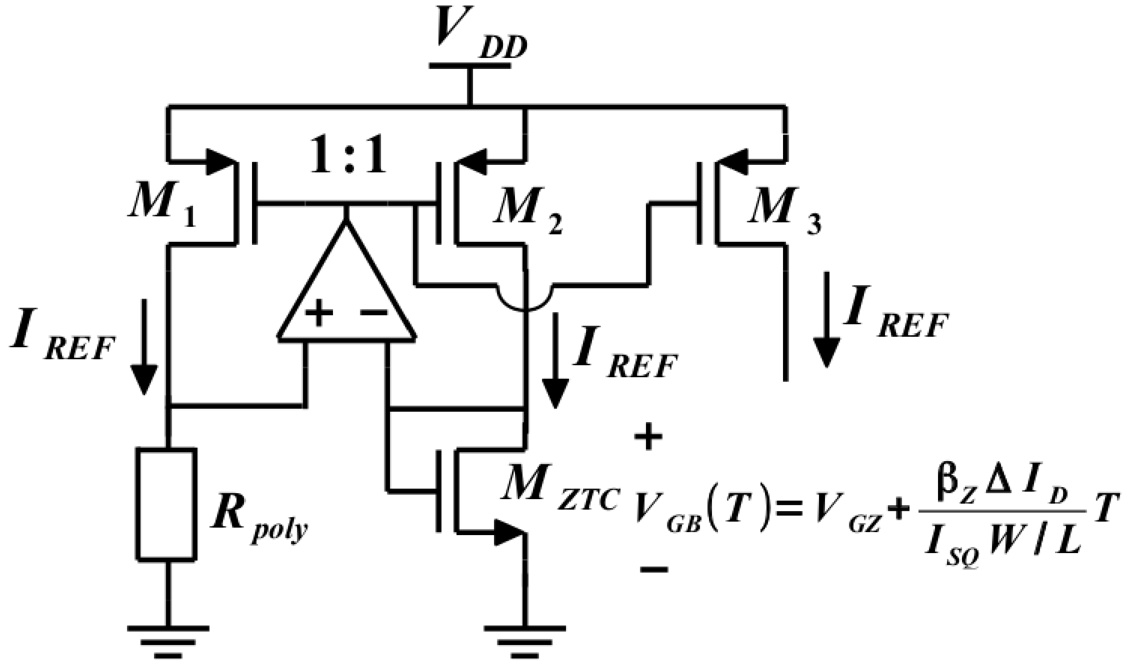


Figure 3.1: Idea of proposed Self-biased CMOS Current Reference based on ZTC Operation Condition.

a straightforward manner. If ΔI_D is chosen appropriately adjusting transistor size, then the temperature dependence of the poly resistor will be canceled, yielding a current reference with low thermal dependence. The Operational Transconductance Amplifier (OTA) performs the same function of previous current reference (Subsection 3.2): To mirror gate-bulk voltage (V_{GB}) of M_{ZTC} transistor across the poly-resistor (R_{poly}) as well as to maintain a high PSRR [CORDOVA; TOLEDO; FABRIS (2014)].

Fig. 3.2 shows the schematic of proposed self-biased current reference. It is composed of a ZTC NMOS transistor (M_{ZTC}) and a poly resistor (R_{poly}) inside a feedback loop implemented with an OTA (M7-M10). There is also a PMOS mirror formed by M1 - M3 for biasing, and a start-up circuit which is composed of M4 - M6.

3.1.1 Circuit Analysis

PMOS mirror formed by M1 - M4 is supposed to have a unitary gain in all branches for this analysis. The differential input of OTA and ZTC NMOS transistor Eq. (3.23) is derived applying Kirchhoff's voltage law (KVL) over the poly resistor.

$$R(T)(I_{DZ} + \Delta I_d) = R(T)I_{REF} = V_{OS} + V_{GB}(T) \tag{3.1}$$

where V_{OS} is OTA offset voltage. Poly resistor thermal dependence can be approximated as

$$R(T) \approx R(T_0)(1 + \alpha_1(T - T_0)) \tag{3.2}$$

where α_1 is poly-resistor thermal drift.

Using (2.85), (3.2) and (3.1), one can derive

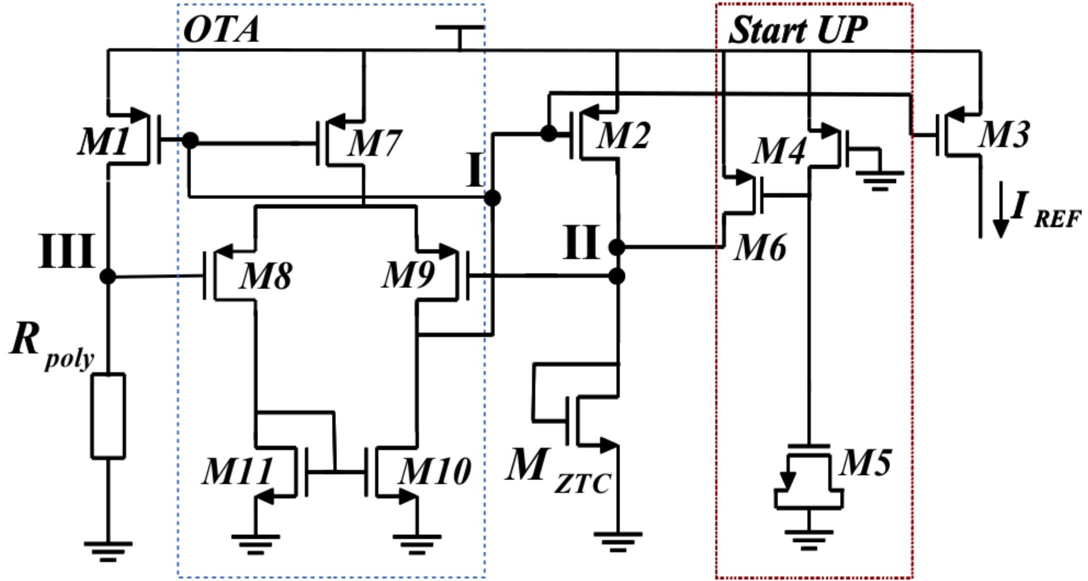


Figure 3.2: Self-biased CMOS Current Reference based on ZTC Operation Condition

$$
\begin{aligned}
&(1-\alpha_1 T_0)R(T_0)I_{REF} + (R(T_0)\alpha_1 I_{REF})T \\
&= V_{OS} + V_{GZ} - \left(\frac{\alpha_{VT0}(I_{REF}-I_{DZ})}{2I_{DZ}}\right)T
\end{aligned} \tag{3.3}
$$

Manipulating temperature dependent and independent parts Eq. (3.4) and (3.5) are derived, respectively.

$$
(1-\alpha_1 T_0)R(T_0)I_{REF} = V_{OS} + V_{GZ} \tag{3.4}
$$

and

$$
R(T_0)\alpha_1 I_{REF} = \left(\frac{\alpha_{VT0}(I_{REF}-I_{DZ})}{2I_{DZ}}\right) \tag{3.5}
$$

Now, terms $R(T_0)$ from (3.4) and I_{DZ} from (3.5) can be isolated

$$
R(T_0) = \frac{V_{OS}+V_{GZ}}{I_{REF}(1-\alpha_1 T_0)} \tag{3.6}
$$

$$
I_{DZ} = \frac{I_{REF}}{1-\frac{2}{\alpha_{V_{T0}}}R(T_0)\alpha_1 I_{REF}} \tag{3.7}
$$

Expressions (3.6) and (3.7) show dependence of the parameters of devices, $R(T_0)$ and I_{DZ}, and the current I_{REF}, i.e., for a different I_{REF}, a new sizing for R_{poly} and M_{ZTC} is required.

Regarding the stability of proposed circuit, Eq. (3.8) describes the gain loop transfer function.

$$
OL(s) = \frac{g_{m8,9}g_{m1,2}r_o(R(T_0)-r_{ztc})}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)\left(\frac{s}{p_3}+1\right)} \tag{3.8}
$$

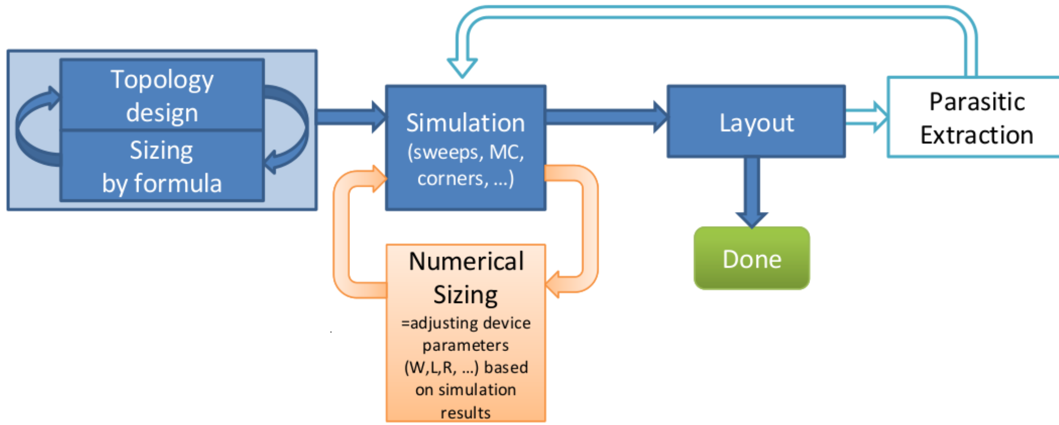


Figure 3.3: Numerical Sizing with Wicked^{TM}.

$$p_1 = \frac{1}{r_o C_I} \tag{3.9}$$

$$p_2 = \frac{1}{r_{ztc} C_{II}} \tag{3.10}$$

$$p_3 = \frac{1}{R(T_0) C_{III}} \tag{3.11}$$

where $g_{m8,9}$ is OTA transconductance, r_o is equivalent output resistance of OTA, r_{ztc} is equivalent resistance of ZTC transistor, $g_{m1,2}$ is transconductance of PMOS mirror and C_I, C_{II} and C_{III} are capacitance related to node I, II and III (Fig. 3.2), respectively.

3.1.2 Circuit Design

Circuit design was optimized through the use of MunEDA WiCkeD software [MUNEDA (2015)]. This solution is useful to improve yield, helping designers to spend less time in this activity, which is currently a market demand [SEMICONDUCTOR (2015)].

In this case, design process was done using the methodology presented in Fig (3.3) [WICKED (2013)]. An initial analytical sizing composes this approach, using design formulas previously described, followed by electrical simulation, numerical sizing, layout and parasitic extraction. Unlike traditional analog design method, where simulation is used only as a verification tool, the Wicked-MunEDA software modifies the device geometries iteratively based on simulation results, improving desired parameters. The main advantage of this process is to avoid intensive re-simulation time commonly present in traditional analog design flow [WICKED (2013)].

Analytical sizing was done using equations from subsection 3.1.1, with the assumption that the ZTC condition is strong inversion regime (Table 2.2), since this design also uses 180 nm CMOS process. Process documentation and simulations were used to evaluate device parameters, such as α_1 and $\alpha_{V_{T0}}$.

The first step is I_{REF} definition and correspondent resistor $R(T_0)$ from Eq. (3.6).

$$R(T_0) \approx \frac{V_{GZ}}{I_{REF}(1-\alpha_1 T_0)} = \frac{V_{T0}(T_0) - \alpha_{V_{T0}} T_0}{I_{REF}(1-\alpha_1 T_0)} \tag{3.12}$$

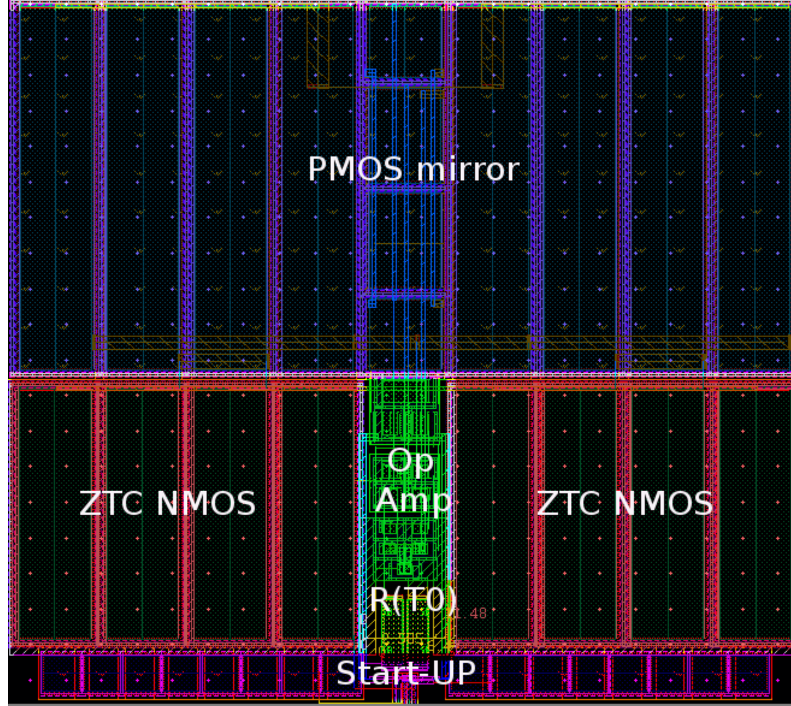


Figure 3.4: Layout - 100μm X 100μm

where V_{SB} = 0. Then, using (2.51) in (3.7), ZTC NMOS transistor can be sized.

$$\left(\frac{W}{L}\right)_{ZTC} = \frac{2n\left(\frac{-2}{\alpha_{V_{T0}}}R(T_0)\alpha_1 + \frac{1}{I_{REF}}\right)^{-1}}{\mu_n(T_0)T_0^2 C_{ox}\alpha_{V_{T0}}^2} \tag{3.13}$$

PMOS mirror M1-M2 can also be sized by Eq. (3.14), assuming that these transistors are working in strong inversion.

$$\left(\frac{W}{L}\right)_{1,2} = \frac{2nI_{REF}}{\mu_p(T_0)C_{ox}(V_{GB} + nV_{SB} - V_{T0})^2} \tag{3.14}$$

Stability issue can be analytically checked using Eq. (3.8) or can be simulated. Whatever the case, the proposed current reference does not have stability problems since OTA Gain-bandwidth product (GBW) does not need to be large.For example, the $p_1 << p_2$ and p_3, in contrast to previous ZSCCR current reference (Subsection 3.1.1) where insertion of ripple capacitors are required changing gain loop transfer function profile.

After initial sizing, numerical size adjustment is done to improve the circuit yield, using "Feasibility Optimization" (FEA) followed by "Deterministic Nominal Optimization" (DNO). FEA enables the circuit designer to check all electrical/geometrical constraints. DNO improves circuit sizing by changing the design parameters with unique gradient-based optimization algorithms, such as "least-square algorithm" and "parameter distance algorithm". Finally, a yield Optimization (YOP) analysis is done in our design method [WICKED (2013)]. Table 3.1 shows the final sizing achieved by this WiCkeD Flow.

3.1.3 Layout

The proposed self-biased CMOS current reference layout is relatively small, occupying only $0.01mm^2$, as shown in Fig. 3.4. Placement of devices was performed taking

Table 3.1: Device Sizing of proposed ZSBCR

Device	Width (μm)	Length (μm)
R_{poly} (7108.2 Ω)	2.62	17.65
M_{ZTC} (N=8)	35	10
M_1 (N=4)	50.6	10
M_2 (N=4)	50.6	10
M_3 (N=4)	50.6	10
M_4	2.75	0.18
M_5 (N=16)	5	5
M_6	2.75	0.18
M_7	2.75	2
M_8 (N=2)	1.5	2
M_9 (N=2)	1.5	2
M_{10}	1	2
M_{11}	1	2

N is multipler number

all precautions to minimize mismatch effects of global variations. Furthermore, PMOS mirror and ZTC NMOS were designed to occupy approximately 80% of the total layout area, because the sizes of both are dominant factors in determining local mismatch effects. Chapter 4 shows simulation results.

3.2 Resistorless Self-Biased ZTC Switched Capacitor Current Reference - ZSCCR

The fundamental idea of proposed Resistorless Self-Biased ZTC Switched Capacitor Current Reference (ZSCCR) can be understood with the aid of Fig. 3.5 [TOLEDO et al. (2015a)]. The main strategy is to use the low temperature dependence of Metal-Isolator-Metal (MIM) capacitor (C_R), available in this 180 nm CMOS process, along with ZTC operating point of MOS transistor, given by Eq. (2.78), to generate a current reference with neglected temperature dependence. To put it another way, $V_{GB} = V_{GZ}$ of M_{ZTC} is directly applied over pseudo-resistor (C_R, M_{S1} and M_{S2}) through an Operational Transconductance Amplifier (OTA), providing a current with no temperature dependence.

Fig. 3.6 (a) shows the schematic implementation of proposed ZSCCR [TOLEDO et al. (2015a)]. It is composed of a current-biased NMOS transistor operating in ZTC condition, which gate-bulk voltage is counterbalanced by a pseudo-resistor, which is formed by a switched capacitor (C_R). Equilibrium condition is accomplished using an OTA (M_1, M_2, M_3, M_4 and M_5) that controls the current mirror (M_8 and M_9) which is biasing both M_{ZTC} and pseudo-resistor. Pseudo-resistor is also comprised by two switches (Ms_1 and Ms_2) and a ripple reduction capacitor ($C_{1,2}$). M_Z and C_Z form the frequency compensation network, and M_{11}-$_{M13}$ form the start-up circuit. The addition of C_1 and C_2 is necessary to mitigate any ripple in output reference current, being both with the same value for easier frequency compensation.

This topology has a extra feature that are worth mentioning. Any deviation from ZTC bias point, for example resulting from device mismatch, can be easily trimmed by external clock frequency adjustment or changing the C_R value that could be settled by

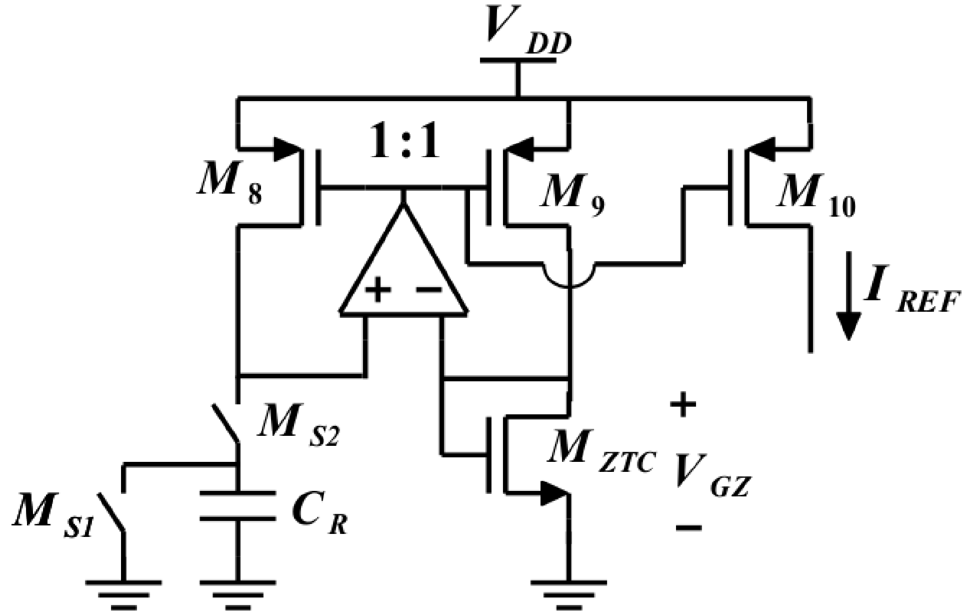


Figure 3.5: Idea of proposed Resistorless Self-Biased ZTC Switched Capacitor Current Reference.

a digital word. Remember that equivalent resistance of used switched capacitor is given by Eq (3.15) [BUTLER; JACOB BAKER (2005)]. However, this easy calibration feature was not addressed in the presented design.

$$R_e = \frac{1}{f_{ex}C_R} \tag{3.15}$$

where f_{ex} is the switching frequency.

Another interesting feature is that, due to feedback using OTA, a good Power Supply Rejection Ratio (PSRR) is achieved [CORDOVA; TOLEDO; FABRIS (2014)].

3.2.1 Circuit Analysis and Design

Two main subjects summarise Circuit Analysis and Design of this proposed topology: I_{REF} definition and stability analysis.

- *I_{REF} definition*

The PMOS current mirror formed by M_8 - M_{10} presents unitary gain in all branches. The OTA, which controls this mirror, keeps both M_{ztc} and R_{eq} under approximately the same voltage, resulting that

$$I_{REF} = V_{GZ} f_{ex} C_R = (V_{T0}(T_0) - \alpha_{V_{T0}} T_0) f_{ex} C_R \tag{3.16}$$

where V_S is zero. The OTA offset is considered negligible for this hand calculation. The expression used for V_{GZ} is the simple one derived for strong inversion regime since that chosen 180 nm CMOS technology for implementation of this current reference has ZTC point located 330 mV above threshold voltage, as Table 2.2 describes. From Eq. (3.16), one can readily conclude that design parameters that define the reference current are f_{ex} and C_R since V_{GZ} is fixed per technology, as explained in chapter 2. Knowing that

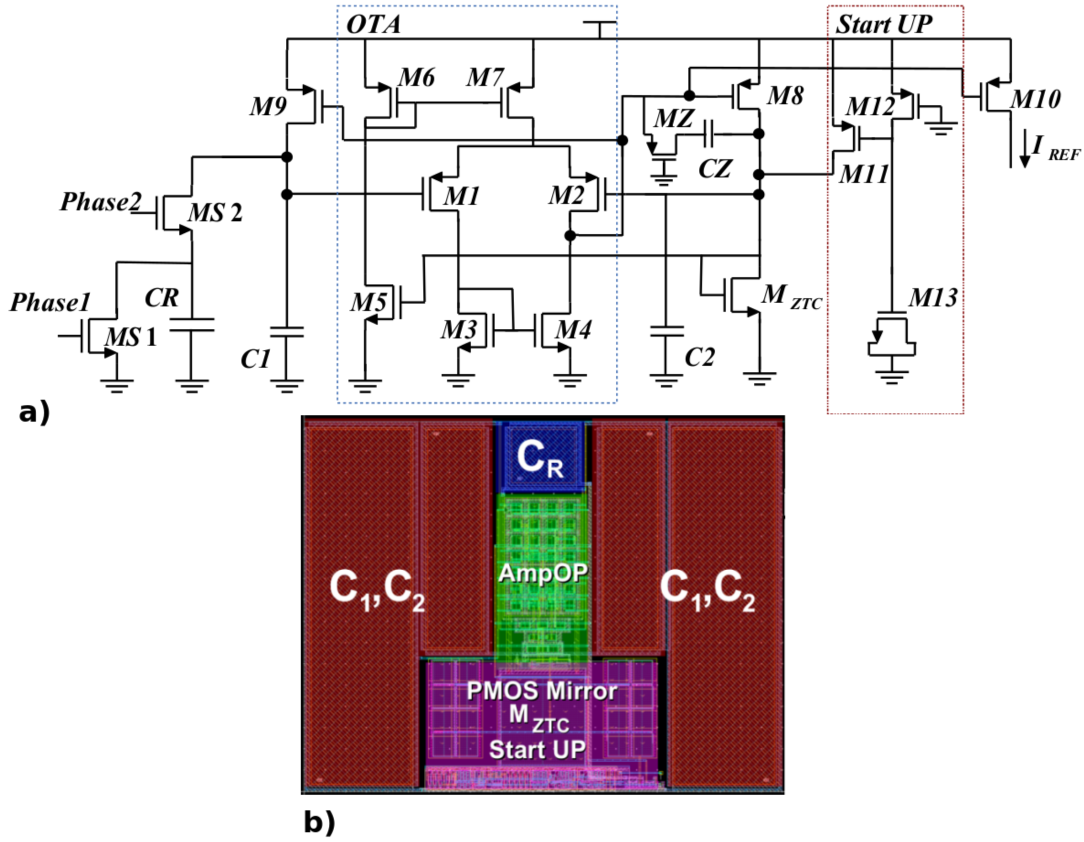


Figure 3.6: (a) The ZTC Switched Capacitor Current Reference (ZSCCR). (b) ZSCCR Layout - 100μm X 100μm in 180 nm CMOS process.

usually a typical CMOS chip solution has available a clock frequency for the digital part, it can be used together with C_R to define desired I_{REF} value.

After I_{REF} definition, according to application needs, and assuming that $C_{1,2} >> C_R$ for a fixed f_{ex}, Eq. (3.17) can be used to size M_{ztc} transistor. Eq. (3.17) is a simple combination of Eq. (3.16) and Eq. (2.51).

$$\left(\frac{W}{L}\right)_{ZTC} = \frac{(V_{T0}(T_0) - \alpha_{V_{T0}} T_0) f_{ex} C_R 2n}{\mu_n(T_0) T_0^2 C_{ox} \alpha_{V_T}^2} \tag{3.17}$$

• *Stability analysis*

Owing to insertion of ripple capacitor, C_1 and C_2, the gain loop transfer function must to be evaluated. Eq. (3.18) shows gain loop transfer function

$$OL(s) \approx \frac{gm_{1,2} gm_{8,9} r_{out} (1/C_R f_{ex} - 1/gm_{ZTC}) \left(\frac{1}{Z_1} + 1\right)}{\left(\frac{1}{P_1} + 1\right)\left(\frac{1}{P_1} + 1\right)\left(\frac{1}{P_3} + 1\right)} \tag{3.18}$$

where

$$P_1 \approx f_{ex} \frac{C_R}{C_1} \tag{3.19}$$

$$P_2 \approx \frac{1}{r_{out} C_{PMOS}} \quad (3.20)$$

$$P_3 \approx \frac{1}{R_Z C_Z + 1/gm_{ZTC}(C_Z + C_1)} \quad (3.21)$$

and

$$Z_1 \approx \frac{(1/gm_{ZTC} + 1/C_R f_{ex}) P_3 P_1}{P_1/C_R f_{ex} - P_3/gm_{ZTC}} \quad (3.22)$$

being gm_{ZTC} the transconductance of M_{ZTC}, $gm_{1,2}$ the transconductance of $M_{1,2}$, $gm_{8,9}$ the transconductance of $M_{8,9}$, r_{out} the OTA output resistance, C_{PMOS} the PMOS mirror capacitance and R_Z the triode resistance of M_Z. Note that in this analyzes C_1 = C_2 has been adopted.

Gain loop frequency operation must be analysed using Eq. (3.18) or simulated to achieve adequate phase margin (around 60°), defining M_Z and C_Z. Note that it is simple well-known miller compensation.

3.2.2 Layout

ZSCCR layout, shown in Fig. 3.6 (b) over a 100 μm x 100 μm area ($0.01mm^2$), was performed to minimize devices mismatch. Dummy devices for matching improvement and charge feed-through reduction devices are not shown in the schematic view, but they were included in the layout. MIM capacitors (C_1 and C_2) spend approximately 70% of the total area since their values are dominant factors in output current ripple. Table 3.2 shows final sizing achieved.

Table 3.2: Device Sizing of proposed ZSCCR

Device	Width (μm)	Length (μm)
C_R (0.57 pF)	15	12.6
M_{ZTC} (N=1)	1	2
C_1 (6 pF)	24	83.5
C_2 (6 pF)	24	83.5
M_1 (N=8)	2	2
M_2 (N=8)	2	2
M_3 (N=1)	1	2
M_4 (N=1)	1	2
M_5 (N=1)	1	2
M_6 (N=2)	2	2
M_7 (N=2)	2	2
M_8 (N=2)	2	2
M_9 (N=2)	2	2
M_{10} (N=2)	2	2
M_{11} (N=1)	2.75	0.18
M_{12} (N=1)	2.75	0.18
M_{13} (N=1)	5	5
M_{S1} (N=1)	0.88	0.18
M_{S2} (N=1)	0.88	0.18

N is multipler number

3.3 Electromagnetic Interference (EMI) Resisting MOSFET-Only Voltage Reference - EMIVR

The voltage reference is an analog building block that provides a constant voltage ideally insensitive to temperature, power supply voltage, process fabrication, packaging stresses and, load current variations. Usually, the last one is done in integrated CMOS technology using a circuit topology called regulator. A regulator drives current keeping a constant voltage for all or specific blocks of the chip using an error amplifier, PMOS pass transistor, and a voltage reference. Regardless of load current variations the regulator circuit ensures that the driven voltage is held constant [GEIGER; SANCHEZ-SINENCIO (1985)]. Therefore, in CMOS voltage reference design this issue is overlooked provided that if a reference voltage with immunity to current variation is required, then a regulator is implemented.

Another well-studied source of error in voltage reference is due to chip packaging stress. It can cause voltage offset in the desired voltage reference value (V_{REF}), generally defined as package shift. In other words, package shift is the offset in voltage of packaged voltage reference from its unpackaged value [ABESINGHA; RINCON-MORA; BRIGGS (2002)]. Effects such difference in thermal coefficient of expansion of package and silicon and/or presence of filler in plastic packages are the primary causes of package shift [ABESINGHA; RINCON-MORA; BRIGGS (2002)]. Techniques were proposed to at least reduce these source of error [FRUETT; MEIJER; BAKKER (2003)], however in this thesis they will be neglected.

In the current literature, the voltage reference is in generally classified by its can-

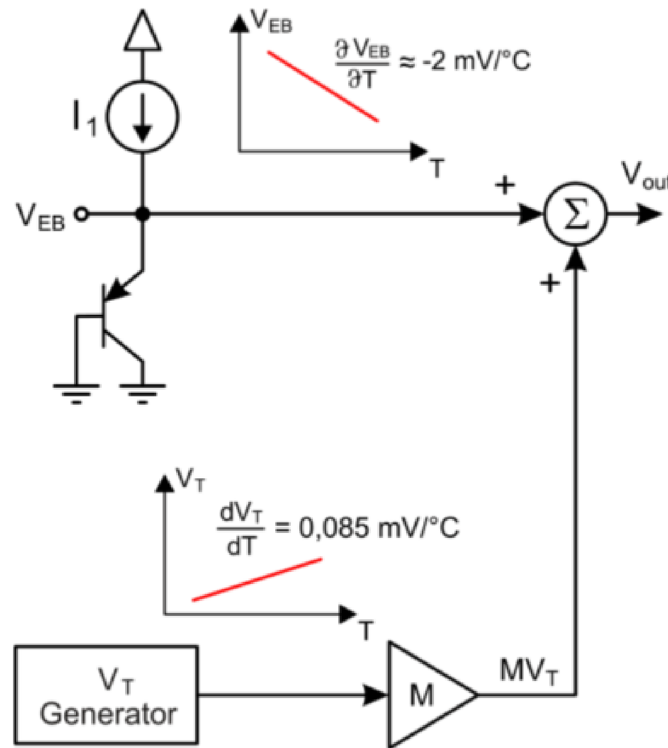


Figure 3.7: Basic concept of a bandgap voltage reference.

cellation strategy for temperature, i.e., bandgap or non-bandgap voltage reference. The bandgap solution is based on the compensation of a CTAT pn junction temperature dependence by a PTAT N-amplified thermal voltage [WIDLAR (1971)], as illustrated in Fig. 3.7. There are several implementations of bandgap structures such as, [MATTIA; KLIMACH; BAMPI (2015)][MATTIA; KLIMACH; BAMPI (2014a)][MATTIA; KLIMACH; BAMPI (2014b)] [MATTIA; KLIMACH; BAMPI (2014c)][KLIMACH et al. (2013)]. On the other hand, no pn junction is used in a non-bandgap structure. For example, in references based on Zener diodes or Zero Temperature Coefficient (ZTC) point of MOSFETs, which is the case of this thesis.

The next two proposed non-bandgap voltage reference are designed only taking into account temperature, power supply rejection and fabrication variations.

Steep growth of mass-market electronic communication systems is a natural source of numerous electromagnetic disturbances, making integrated circuits (ICs) more susceptible to this kind of interference. In the case of analog ICs, they are not solely disturbed at their output or input terminals. They are equally very susceptible to conducted EMI that is injected into the power supply that causes disturbances in their performance. These EMI amplitude variations may cause severe DC shift errors on sensitive nodes, driving the circuit out of its normal operation region [REDOUTE; STEYAERT (2005)].

As mentioned before, any voltage reference must offer adequate thermal stability and power supply rejection as well as a good fabrication repeatability as its principal characteristics. However, usually little or no consideration regarding EMI is taken into account during its design process. Even knowing that EMI can strongly interfere on its operation condition, as can be seen in [REDOUTE; STEYAERT (2010a)], where a modified Kuijk bandgap reference is analysed under the effect of a strong EMI injection. Moreover, in more recent technologies, for which the power supply voltage is being progressively re-

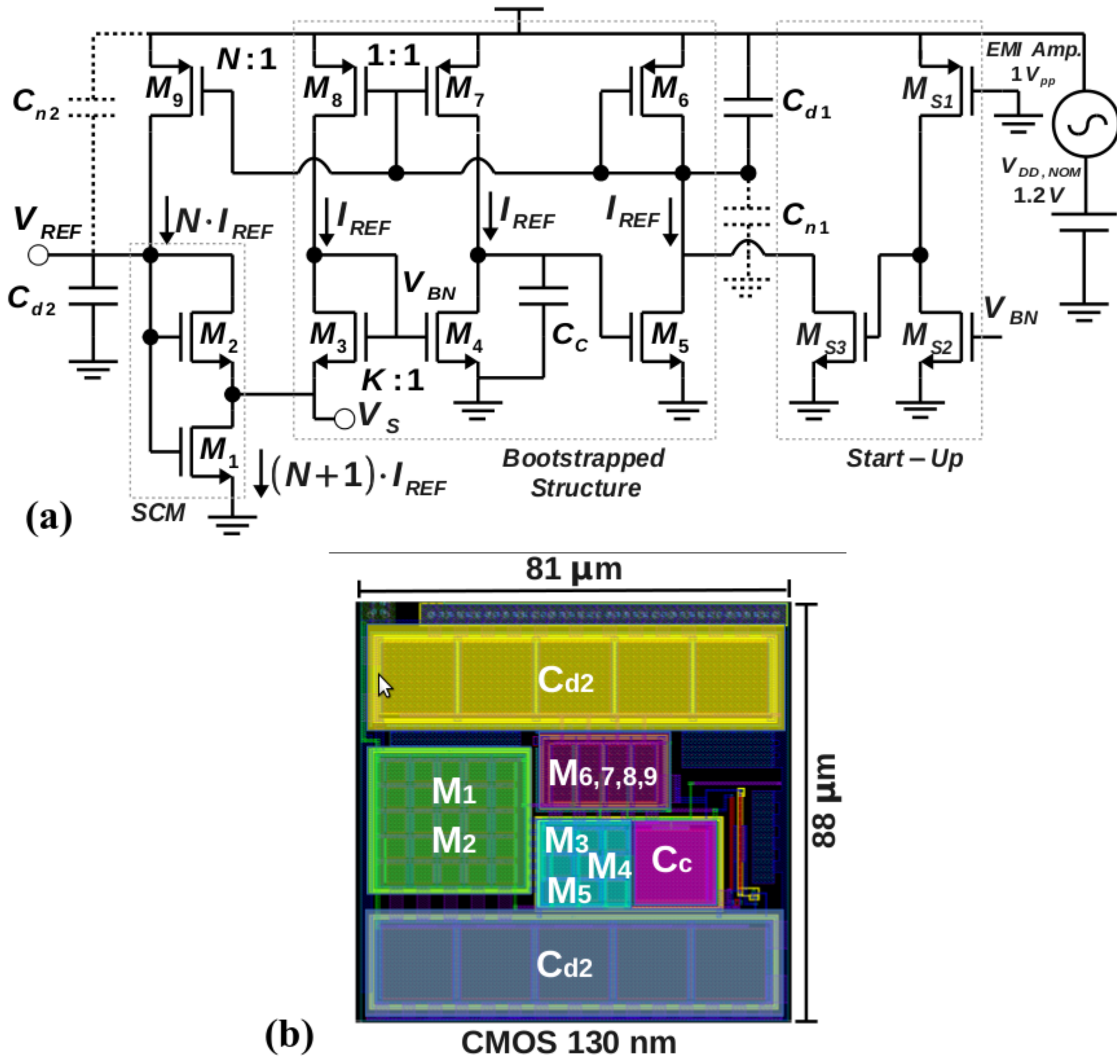


Figure 3.8: (a) Proposed EMI resisting CMOS voltage reference schematic circuit. (b) Layout Area: 81 μm X 88 μm

duced, the need for low-voltage high-precision references with high immunity to EMI is a major concern. Therefore, an EMI resisting non-bandgap MOSFET-Only voltage reference based on ZTC MOSFET operation condition is proposed and designed in a 130 nm CMOS technology.

The voltage reference schematic, depicted in Fig. 3.8 (a) and published in [CORDOVA et al. (2015)], is an all-MOS implementation of the self-biased current reference (SBCR) presented in [CORDOVA; TOLEDO; FABRIS (2014)]. The cores of the SBCR are the self-cascode MOSFET circuit (SCM - transistors M_1, M_2) and the bootstrapped structure (M_3, M_4, M_5, M_6, M_7, and M_8) [SILVA PIOVANI; SCHNEIDER (2011.)]. Transistor M_9 mirrors the bootstrapped current in order to bias the SCM. Since this reference is working with feedback, a compensation capacitor C_C is required for stability. Transistors (M_{S1} - M_{S3}) form the start-up circuit.

3.3.1 Circuit Analysis and Design

- *Temperature dependence cancellation*

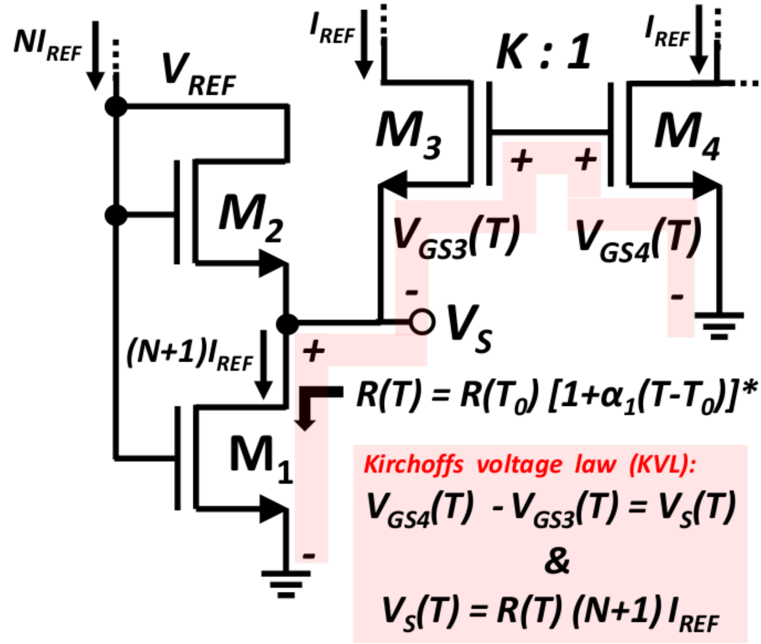


Figure 3.9: The thermal cancellation strategy used in proposed EMI Resisting MOSFET-Only Voltage Reference

The voltage and current reference are obtained directly from the gate-bulk voltage (V_{GS}=V_{REF}) and the drain current T(I_D=NI_{REF}) of M_1, respectively. The main idea of this topology is to compensate the thermal dependence of triode channel resistance of M_1 with a PTAT voltage (V_S) generated by the gate-bulk difference of transistors M_3 and M_4 ($V_{GS4} - V_{GS3}$), yielding a current reference with low thermal sensitivity. Afterwards, M_2 is designed to operate in the vicinity of the ZTC point to cancel the first order temperature dependence of the PTAT voltage (V_S). Fig. 3.9 illustrates the thermal cancellation strategy used in this proposed topology applying a zoom in the transistors of interest.

Applying the Kirchoff's voltage law (KVL) over the gate-bulk of M_4, M_3 and drain-source of M_1 terminals, Eq. (3.23) is derived.

$$R(T_0)(1 + \alpha_1(T - T_0))(N + 1)I_{REF} = V_{GS4}(T) - V_{GS3}(T) = V_S(T) \tag{3.23}$$

where

$$R(T_0) \approx \frac{n}{(W_1/L_1)\mu_n(T_0)C'_{ox}(V_{REF} - V_{T0}(T_0))} \tag{3.24}$$

and

$$\alpha_1 = -\frac{|\alpha_{V_{T0}}|}{(V_{REF} - V_{T0}(T_0))} - \frac{\alpha_\mu}{T_0} \tag{3.25}$$

Eq (3.24) and (3.25) are used based on the assumption that transistor M_1 is operating in strong inversion as well, since for standard transistor in 130 nm CMOS process the ZTC vicinity can be modeled using strong inversion aproximation as shown in Table 2.2. Then, $R(T_0)$ is the strong inversion triode resistance of M_1 at room temperature and α_1 is

its first order temperature dependence. After applying Eq. (2.85) in Eq. (3.23), one can handle separately the dependent and independent temperature terms,

$$(N+1)R(T_0)\alpha_1 = \frac{\beta_z}{I_{SQ}(n+1)}\left(\frac{\frac{W_4}{L_4}-\frac{W_3}{L_3}}{\frac{W_3}{L_3}\frac{W_4}{L_4}} + \frac{J_{DZ_4}-J_{DZ_3}}{I_{REF}}\right) \tag{3.26}$$

and

$$I_{REF} = \frac{nVs(T_0)}{(N+1)R(T_0)(1-\alpha_1 T_0)} \tag{3.27}$$

Eq. (3.26) ensures thermal first order cancellation with respect to I_{REF} and Eq. (3.27) defines its reference value. Regarding the voltage reference V_{REF}, transistor M_2 has to be sized at ZTC vicinity (In this case, below ZTC point providing a CTAT behavior at V_{GB}) in the sense that its first order temperature dependence can be canceled by $V_S(T)$ PTAT voltage. Therefore, applying Eq. (3.23) in Eq. (2.85) for M_2 transistor and once again manipulating separately the dependent and independent temperature terms,

$$\frac{\beta_z}{I_{SQ}n}\left(\frac{N}{\frac{W_2}{L_2}} - \frac{J_{DZ_2}}{I_{REF}}\right) - (N+1)R(T_0)\alpha_1 = 0 \tag{3.28}$$

and

$$V_{REF} = V_{T0}(T_0) - \alpha_{V_{T0}}T_0 + n(N+1)I_{REF}R(T_0)(1-\alpha_1 T_0) \tag{3.29}$$

In the same way, Eq. (3.28) ensures thermal first order cancellation regarding V_{REF} and Eq. (3.29) defines its reference value. In conclusion, presented set of equations, Eqs. (3.26) to (3.29), describe how to size transistors M_1 to M_4 in order to make both voltage and current low temperature dependents.

• *Reference EMI Analysis*

When EMI is injected into the positive power supply terminal, represented by top-right V_{emi} voltage source in Fig. 3.8 (a), V_{REF} can be polluted by undesirable EMI components [STANDARD (2004)]. Usually, there are two ways to evaluate these EMI power supply interferences: small signal analysis when EMI interference can be considered small enough and large signal analysis for high EMI power injection.

• • *Small-Signal Analysis:*

As long as EMI is sufficiently small, PSRR transfer function from EMI source to the reference voltage output node, or V_{REF}, can be calculated using a small-signal approach, Eq. (3.30). To reach this simple Eq. (3.30) some assumptions and definitions were made. R_L is equivalent self-cascode resistance, $C_{d1(2)}$ represent the MIM decoupling capacitor, $C_{n1(2)}$ is dominant parasitic capacitance and output resistances (r_0) and transconductances (g_m) of all MOS transistors are considered equals. Similar approach was also used in [GIUSTOLISI; PALUMBO (2003)].

$$H(s) = \frac{v_{ref}(s)}{v_{emi}(s)} \approx \frac{R_L}{r_o}\frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{\left(\frac{s}{\omega_{p1}}+1\right)\left(\frac{s}{\omega_{p2}}+1\right)} \tag{3.30}$$

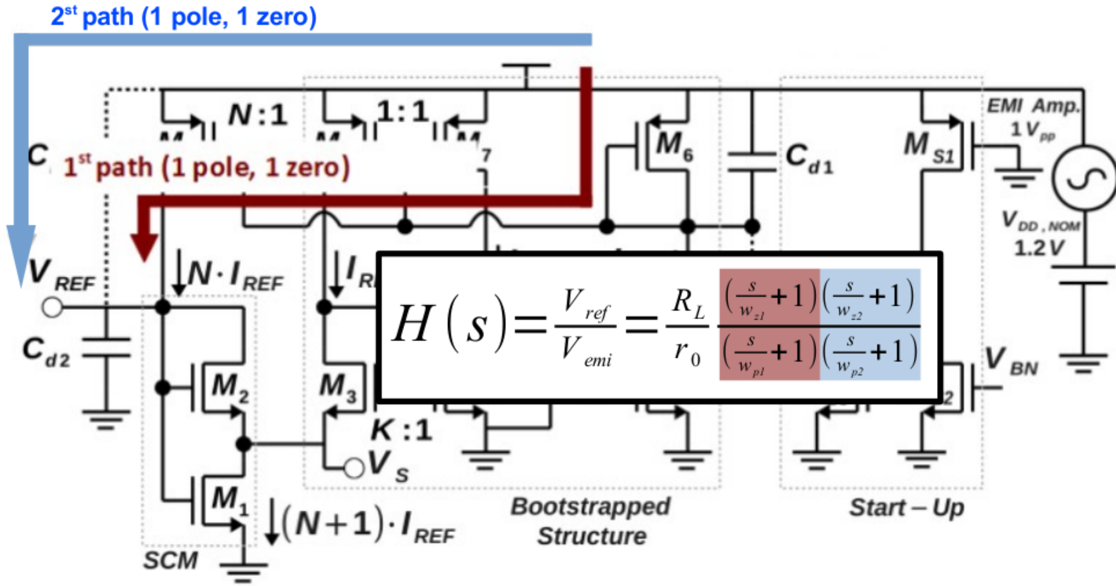


Figure 3.10: Poles and Zeros related to nodes and feedback capacitance in proposed EMI Voltage reference, respectively.

where

$$\omega_{z1}, \omega_{z2} = \frac{g_m}{C_{d1}}, \frac{1}{r_o C_{n2}} \tag{3.31}$$

and

$$\omega_{p1}, \omega_{p2} = \frac{2g_m}{C_{d1}}, \frac{1}{R_L C_{d2}} \tag{3.32}$$

Fig. 3.10 shows through two highlighted paths what are the nodes and capacitance feedback responsible for generating poles and zeros in simplified Eq. (3.30), respectively. Furthermore, one can readily conclude that there is a zero and pole close to each other due to the insertion of C_{d1} (ω_{z1} and ω_{p1}) which will improve EMI tolerance for middle to high frequencies. In proposed design, value of 10 pF was chosen for both C_{d1} and C_{d2}.

- • *Large-Signal Analysis:*

Ideally, the proposed voltage reference is free of DC shift, since the gate and source of M_9 are approximately shorted to each other with the aid of capacitor C_{d1}. However, for powerful high EMI frequencies, the gate of M_9 is not perfectly isolated from its source. This generates a voltage leakage on it mainly due to a capacitive division between C_{d1} and parasitic capacitance C_{n1}, the dotted capacitor in Fig. 3.8 (a). Therefore, for this EMI levels, total EMI interference that is coupled to the gate of M_9 appears across the drain of M_9 generating a DC shift in the average of V_{REF}.

All this qualitative analysis can be translated into two figures of merit: DC shift (DC_{shift}) and Ripple peak-to-peak voltage (V_{pp}). Both defined by Eq. (3.33) and Eq. (3.34) [REDOUTE; STEYAERT (2010b)], respectively. Note that these equations are used to evaluate how immune the reference is for larger signal EMI interference.

$$DC_{shift} = \frac{V_{REF} - V_{REF_{Average}}}{V_{REF}} 100\% \tag{3.33}$$

$$V_{pp} = V_{REF,max} - V_{REF,min} \tag{3.34}$$

3.3.2 Layout

The implemented voltage reference layout is small, occupying only 0.0075 mm^2, as shown in Fig. 3.8. The placement of devices was performed taking into account all precautions to minimize the mismatch effects. Table 3.3 shows final sizing used as input for layout design.

Table 3.3: Device Sizing of proposed EMIVR

Device	Width (μm)	Length (μm)
M_1	2.5	4
M_2	1.6	4
M_3	28	4
$M_{4,5}$	4	4
$M_{6,7,8,9}$	12	4
M_{S1}	0.28	20
M_{S2}	1	1
M_{S3}	0.28	20
C_{d1} (N=5)	15	15
C_{d2} (N=5)	15	15
C_C	15	15

N is multipler number

3.4 0.5 V Supply Schottky-diode based Voltage Reference - SBVR

As dimensions of thin-oxide transistors scale down, the supply voltage for these most aggressively scaled devices needs to be reduced below 1 V in order to limit electrical fields and guarantee sufficient device reliability. These effects of technology and power supply scaling still provide significant density and cost improvements for digital circuits.

The design of analog and RF CMOS circuits which can take advantage of highly scaled devices is an open area of research [KINGET (2007)]. That is the case of voltage references operating with ultra-low voltage supplies, which have been the subject of significant research in CMOS design in recent years [COLOMBO; WIRTH; BAMPI (2015)].

Many strategies have been explored to provide for the reduction of voltage references supply. One is the use of Schottky diodes instead of PN junction diodes [KINGET; CHATTERJEE; TSIVIDIS (2005); BUTLER; JACOB BAKER (2005)]. The former ones present lower forward bias voltage (0.2 to 0.4 V) than the last ones (0.5 to 0.6 V) for the same current density. Both diodes are compatible with current CMOS processes. In the meantime, mutual compensation of mobility and threshold voltage temperature dependencies, i.e. MOSFET ZTC has also been used to design voltage references [FILANOVSKY; ALLAM (2001),NAJAFIZADEH; FILANOVSKY (2004),LIU; HUANG (2005)].

Following such trends and knowing that Schottky diodes can be fabricated in almost any current CMOS mixed-signal fabrication process, a 0.5 V Schottky-diode voltage ref-

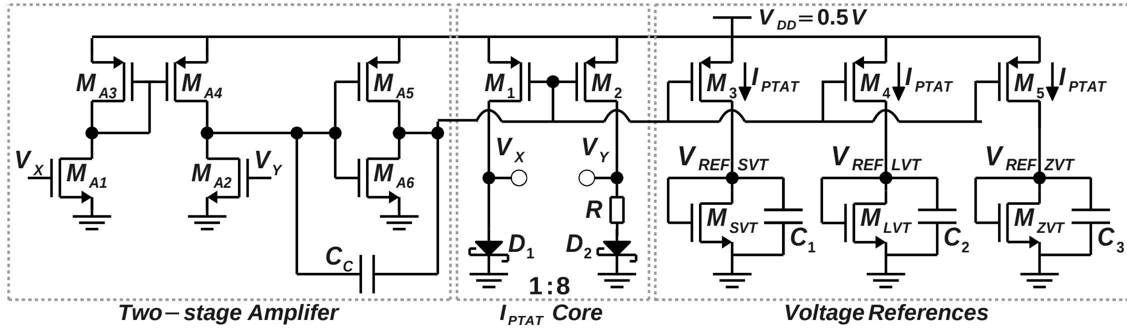


Figure 3.11: Proposed 0.5-V CMOS voltage reference schematic circuit.

erence based on MOSFET ZTC condition is proposed, as depicted in Fig. 3.11 [CORDOVA et al. (2015)].

The Proposed voltage reference is comprised by I_{PTAT} core generation (M_1, M_2, poly resistor R, Schottky diodes D_1 and D_2), two-stage Miller amplifier (Pseudo differential pair M_{A1} to M_{A4}, inverter as second stage M_{A5} to M_{A5} and C_c acting as miller capacitor), and three different diode-connected MOS transistors (Standard M_{SVT}, low threshold voltage M_{LVT} and zero threshold voltage M_{ZVT}). The main idea behind this implementation is that using a Schottky-based PTAT current reference to bias a diode-connected MOS transistor (M_{SVT}, M_{LVT} and M_{ZVT}) a temperature stable voltage can be generated. Such MOS transistors are biased below of ZTC point in such manner that their CTAT behaviors are compensated by applied Schottky-based PTAT current reference. It is worth to note that such idea was already well explained in section 2.4.3 of chapter 2, mainly in Figs. 2.22 and 2.23.

These types of transistors are available in the adopted 130 nm CMOS Process. Roughly speaking the differences among them are typically the bulk doping, or N_A, and deepness of shallow region at drain and source terminals [IBM (2011)]. Of course, the addition of such transistor features increases the manufacturing process cost.

As a matter of curiosity, in this CMOS process the Schottky diode is formed by the union of cobalt silicide region (anode) and lightly doped n-type region (cathode) near the surface. A deep n-type implant creates that. Cobalt silicide work function is such that the formed diode has a low forward voltage when compared to a silicon junction diode under the same junction current density. Schottky diode is, consequently, a fit replacement for their bipolar counterpart in the design of voltage references with ultra-low voltage supply.

3.4.1 Circuit Analysis and Design

All generated voltages reference are obtained directly from gate-bulk voltage (V_{GS}=V_{REF}) of transistors M_{SVT}, M_{LVT} and M_{ZVT}. From section 2.4.3 of chapter 2, Eq. (2.89), repeated below in Eq. (3.35) for sake of convenience, brings out necessary condition to stabilize gate-bulk voltage concerning to variations in temperature for a fixed drain current temperature coefficient, represented by variable TC_I. Consequently, applying found i_{f0} from Eq. (3.35) in Eq. (2.20), Eq. (3.36) gives the voltage reference value for each type of transistor.

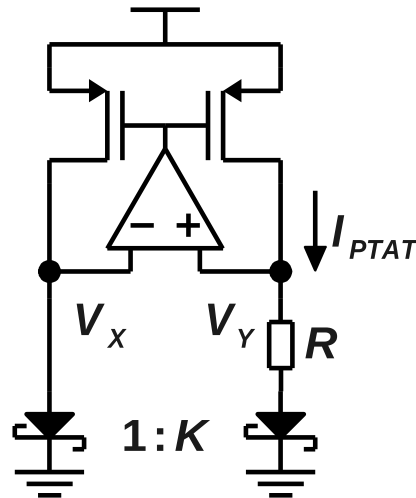


Figure 3.12: Low-voltage supply PTAT current reference.

$$\frac{|\alpha_{V_{T0}}|q}{nk} = \frac{|\alpha_{V_{T0}}|T_0}{n\phi_{t_0}} = \left[\frac{TC_I T_0}{2} - \left(\frac{\alpha_\mu + 2}{2}\right)\right]\left(\frac{i_{f0}}{\sqrt{1+i_{f0}}+1}\right) + \left[\sqrt{1+i_{f0}} - 2 + ln\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{3.35}$$

$$V_{REF} = V_{T0} + n\phi_{t0}\left[\sqrt{1+i_{f0}} - 2 + ln\left(\sqrt{1+i_{f0}} - 1\right)\right] \tag{3.36}$$

A suitable sizing of each diode-connected transistor of Fig. 3.11 can be easily made by combination of i_{f0} with Eqs. (2.59) and (2.60), yielding Eq. (3.37).

$$\left(\frac{W}{L}\right) = I_D(T_0)\left(\mu_n(T_0)C'_{ox}n\frac{\phi_{t0}^2}{2}i_{f0}\right)^{-1} \tag{3.37}$$

The only step remaining is an analysis of PTAT current reference. The low power PTAT current reference is generated using the difference of two Schottky diodes forward voltage operating with different junction current densities, obtained by identical current sources applied to each Schottky diodes with a different active area. Fig. 3.12 shows the schematic diagram of the PTAT current reference, implementing the operational amplifier with two stages for PSRR improvement. The PTAT current analysis was derived in [BAKER (2004)], and is shown below in Eqs. (3.38), (3.39) and (3.40).

$$I_{PTAT} = I_0(1 + TC_{PTAT}(T - T_0)) \tag{3.38}$$

where

$$I_0 = \frac{n\phi_{t0}\ln(K)}{R_0} \tag{3.39}$$

and

$$TC_{PTAT} = \frac{1}{T_0\left[1 + \alpha_1(T - T_0)\right]^2} \tag{3.40}$$

R_0 is poly resistance at room temperature and α_1 is its first order temperature dependence. Set of equations, Eq. (3.35) to (3.40), defines in a simple way the temperature cancelation strategy adopted in the proposed voltage reference topology.

3.4.2 Layout

The implemented voltage reference layout is small, occupying only 0.0075 mm^2, as shown in Fig. 3.13. The placement of devices was performed taking into account all precautions to minimize the mismatch effects. Table 3.4 shows final sizing used as input for layout design.

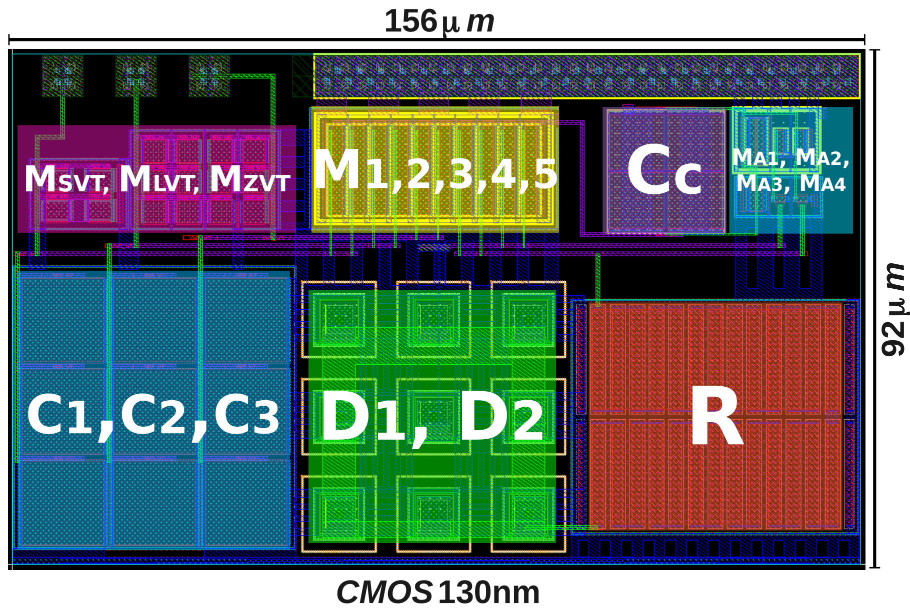


Figure 3.13: Proposed 0.5-V CMOS voltage reference layout.

Table 3.4: Device Sizing of proposed SBVR

Device	Width (μm)	Length (μm)
D_1	5	5
D_2 (N=8)	5	5
$M_{1,2,3,4,5}$ (N=8)	16	2
M_{STV}	3.2	2
M_{LVT}	2.65	2
M_{ZVT}	21.35	2
$C_{1,2,3}$ (MOS)(N=3)	15	15
$M_{A1,A2}$	1	2
$M_{A3,A4}$	4	1
M_{A5}	16	2
M_{A6}	4	1
C_c	10	10

N is multipler number

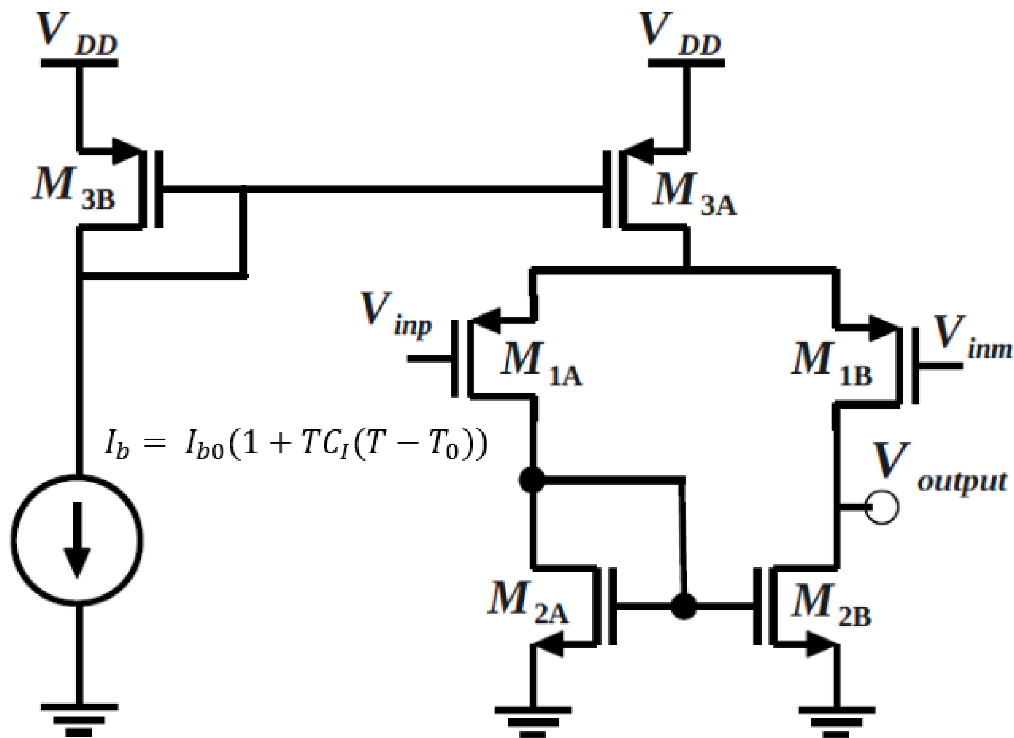


Figure 3.14: PMOS differential pair with active load.

3.5 GZTC Based Gm-C Filters

MOSFET Transconductors (Gm) are essential building blocks for analog, mixed-signal and RF designs. A large variety of analog/RF circuits uses them, such as filters, multipliers, oscillators, and amplifiers. In the middle of '80s, the use of transconductors in continuous time monolithic filters became very attractive for high-frequency applications. They distinguish from RC filters which are comprised by Operational Amplifiers (AmpOp) instead of Operational Transconductance Amplifiers (OTA) [GEIGER; SANCHEZ-SINENCIO (1985)]. Additionally, they play a fundamental role in the implementation of oscillators, sensing amplifiers and current-mode latch circuits (CML), where cross-coupled pair use them in an arrangement in order to generate a negative resistance.

Recently, power-management systems for microprocessors and portable devices have increased the demand for capacitor-less low drop-out (CL-LDO) voltage regulators. These regulators are circuits without off-chip capacitors, resulting in a reduced number of external components and smaller PCB area, thereby reducing total cost of the entire system. This type of implementation is usually comprised of three or more Gm stages, which directly affect the regulators performance (Phase Margin, Load and Line Transients, Load and Line Regulation and, Power Supply Rejection) [TORRES et al. (2014)]. In Radio Frequency (RF) domain, a significant research effort is being applied in the development of wideband receivers to replace multiple narrowband front-end solutions. A possible approach is the use of Low-Noise Transconductance Amplifiers (LNTA), instead of Low-Noise Amplifiers (LNA), which can deliver a satisfactory linearity performance presenting low noise and high bandwidth [GEDDADA et al. (2014)].

In Analog and RF CMOS literature, there are several proposed topologies for transconductors where the main concerns are noise [GEDDADA et al. (2014)], linearity [TSIVIDIS; CZARNUL; FANG (1986); KOZIEL; SZCZEPANSKI (2002)], and speed [LOPEZ-

MARTIN et al. (2005)]. Usually, temperature sensitivity is not considered in these designs and often is not even measured (in some works the temperature sensitivity is implicitly analyzed in corner PVT simulation).

Main idea of this section is to apply the necessary conditions in order to generate transconductor independent of temperature using the analysis of MOSFET GZTC bias point previously explored at subsection 2.5 [TOLEDO et al. (2015b)]. Or, in other words, try to make the CMOS transconductor more insensitivity as possible to temperature variations with GZTC aid. GZTC application into transconductor design flow opens new application area for thermal-aware Analog and RF CMOS Circuit Design, resulting some general design conditions that can be used in any CMOS process.

Herein, Gm-C filters at which the transconductor is biased at GZTC point are defined as GZTC-C Filters. As first approach, some classical and well-known Gm-C filters topologies were chosen in order to validate and evaluate the effectiveness of the GZTC bias point applied in each transconductor [TOLEDO et al. (2015b)]. Also, a PMOS differential pair with active load as transconductor was chosen for this proof-of-concept. However, the principles here described can be adopted and generalized to other transconductor circuits.

Fig. 3.14 shows transconductor schematic that was used in Gm topologies. This classical topology is composed by a biasing current mirror $M_{3A(B)}$, a transconductance differential stage $M_{1A(B)}$ and, an active mirror load $M_{2A(B)}$ [BAKER (2004)].

Fig. 3.15 shows all adopted topologies: a single-ended resistor emulator, an impedance converter (gyrator), a first order filter and a second order filter. The main parameters of these four topologies are strongly dependent on transistor's transconductance. Eqs. (3.41) and (3.42) give the input impedance of single-ended resistor emulator and impedance converter, respectively.

$$Z_{in} = \frac{1}{g_{m1}} \tag{3.41}$$

$$Z_{in}(s) = \frac{sC_L}{g_{m1}g_{m2}} \tag{3.42}$$

Also, the low-frequency gain and dominant pole frequency of first order filter are defined by transconductance parameters as indicated in Eq. (3.43).

$$\frac{V_{output}(s)}{V_{input}(s)} = \frac{g_{m1}}{g_{m2} + sC_1} \tag{3.43}$$

Finally the low pass (V_A), band pass (V_B) and high pass terms (V_C) of second order filter comply with Eq. (3.44) to (3.46), where the transconductance of the three blocks directly affects their performance.

$$\frac{V_{output}(s)}{V_{input}(s)} = \frac{(C_1C_2)s^2V_C + (g_{m3}C_1)sV_B + g_{m2}g_{m1}V_A}{(C_1C_2)s^2 + (g_{m3}C_1)s + g_{m2}g_{m1}} \tag{3.44}$$

$$\omega_0 = \sqrt{\frac{g_{m2}g_{m1}}{C_1C_2}} \tag{3.45}$$

$$Q = \frac{1}{g_{m3}}\sqrt{\frac{g_{m2}g_{m1}C_2}{C_1}} \tag{3.46}$$

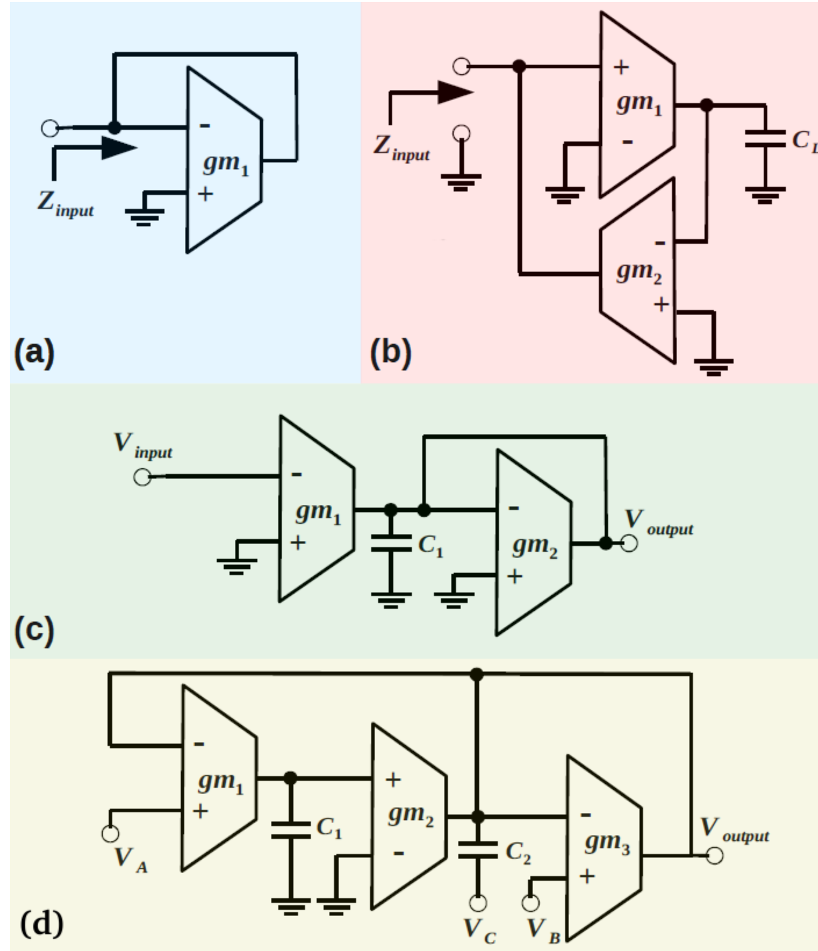


Figure 3.15: (a) single-ended resistor emulator (b) impedance inverter (c) first order filter (d) second order filter.

3.5.1 Circuit Analysis and Design

Considering a fixed bias current (I_{DGZ}), the $M_{1A(B)}$ aspect ratio (W/L) must be defined so that its inversion level is i_{fgz} and then it is necessary to ensure that the GZTC bias condition remains stable over temperature. Using Eq. (2.21), the $M_{1A(B)}$ aspect ratio (W/L) is given by

$$\left(\frac{W}{L}\right) = \frac{I_{DGZ}}{i_{fgz}\mu C'_{ox} n \frac{\phi_t^2}{2}} \tag{3.47}$$

where i_{fz} is found by

$$0 = \alpha_\mu(\sqrt{1+i_{fgz}} - 1) - 2 + \\ \frac{\sqrt{1+i_{fgz}}+1}{\sqrt{1+i_{fgz}}}\left(\frac{|\alpha_{V_{T0}}|q}{nk} + 2 - ln\left(\sqrt{1+i_{fgz}} - 1\right)\right) \tag{3.48}$$

As this condition is located in ZTC bias vicinity (below the bias ZTC point), it is necessary to cancel its CTAT bias behavior (Fig. 2.28 (b)) by applying a small amount of

PTAT bias current, as shown in Fig. 3.14 and described by Eq. (3.49).

$$I_B = I_{DGZ}(1 + TC_I(T - T_0)) \tag{3.49}$$

The requested Current Bias Temperature Coefficient (TC_I) can be found simply using Eq. (2.89), repeated below as a matter of convenience, with i_{fz} that was already found in Eq. (3.48).

$$\frac{|\alpha_{V_{T0}}|q}{nk} = \frac{|\alpha_{V_{T0}}|T_0}{n\phi_{t_0}} = \left[\frac{TC_I T_0}{2} - \left(\frac{\alpha_\mu + 2}{2}\right)\right]\left(\frac{i_{fgz}}{\sqrt{1+i_{fgz}}+1}\right) + \left[\sqrt{1+i_{fgz}} - 2 + ln\left(\sqrt{1+i_{fgz}} - 1\right)\right] \tag{3.50}$$

Combination of Eq. (3.47) with Eq. (3.50) means that if $M_{1A(B)}$ are biased in GZTC condition along with right amount of PTAT current defined by TC_I coefficient, the transconductance of differential pair will present very low temperature sensitivity.

4 SIMULATIONS AND MEASUREMENTS RESULTS

All circuits have been implemented in two different CMOS processes: XFAB 180nm and IBM 130nm, being the ZTC current references designed in the first one and the ZTC voltage references and GZTC filters in the last one. Except for the filters, all simulations results were achieved with the extracted view of laid out circuits.

Proposed ZTC currents references were included in a Multi Layer Mask (MLM) run two years ago called MLM2013. However, owing to funding issues together with no accomplished deadlines, the chip tape-out was unfortunately not realized. Fig. 4.1 (a) shows where the ZTC current references were inserted into the MLM2013 reticle.

Regarding the ZTC voltage references, we have received 40 samples from an IBM 130 nm fabrication run by MOSIS services, where the dies are divided into ten unpackaged and 30 packaged on a QFN80. The fabricated chip contains the works of 7 M.Sc. and 2 Ph.D. students. Fig. 4.1 (b) shows the micrograph of overall fabricated chip with an area of 2.5 x 2.5 mm^2. At this time, five among the ten unpackaged have been measured and are presented here. Another samples have been made available for other purposes. Until this delivery time of the dissertation, the PCB to measure packaged samples are being fabricated.

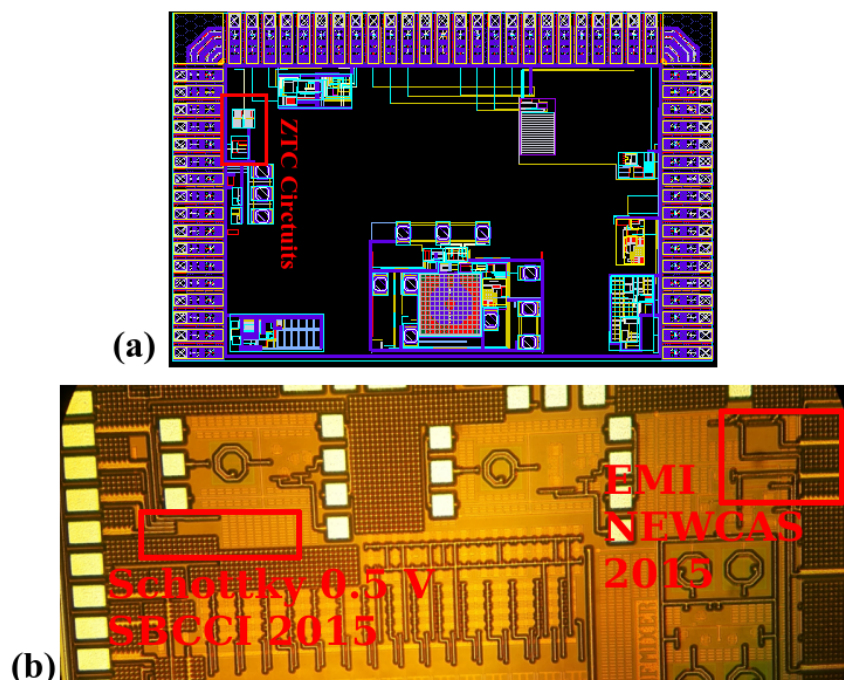


Figure 4.1: (a) Test die inside of MLM2013 reticle (b) Micrograph of IBM 130 nm die.

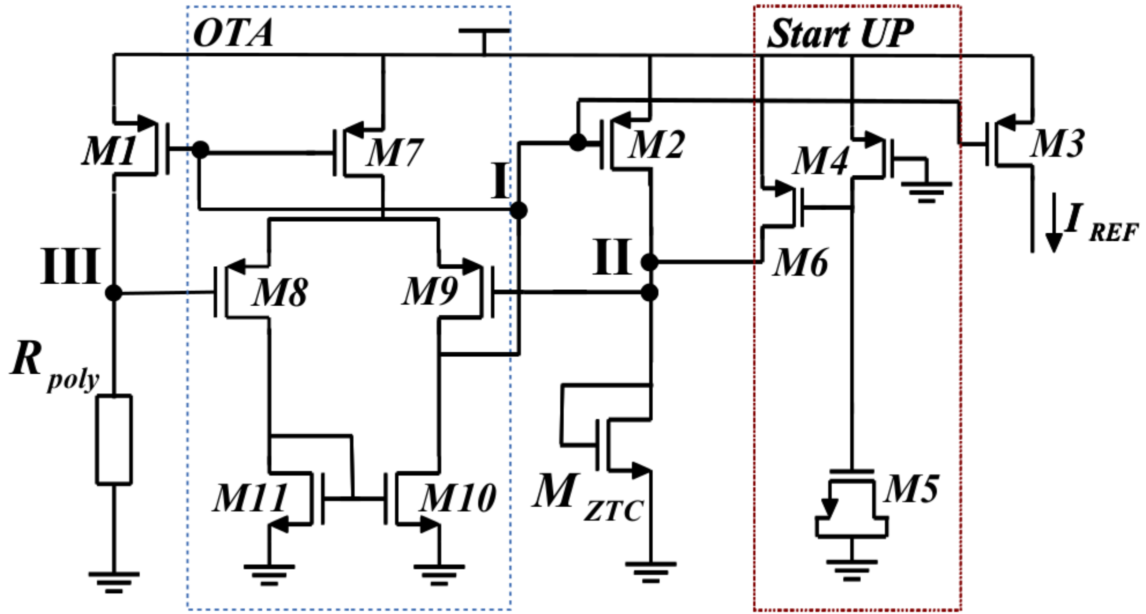


Figure 4.2: Self-biased CMOS Current Reference based on ZTC Operation Condition

4.1 Self-biased CMOS Current Reference based on ZTC Operation Condition - ZSBCR

Schematic of Self-biased CMOS Current Reference is repeated here again for convenience of the reader in Fig 4.2. The circuit was designed to generate 5 μA, as shown in Fig. 4.3. The good thermal stability of reference is evident from -40^oC to $+85^oC$ in this Figure. The effective temperature coefficient, as given by Eq. (4.3), is 15 ppm/^{o}C, under V_{DD} = 1.8 V. The power supply sensitivity resulted around $1\%V$ for a V_{DD} range of 1.4 to 1.8 V, as shown in Fig. 4.4.

Since the impact of fabrication process is critical for performance repeatability of circuit, Monte Carlo (MC) simulation was done separately only for local mismatch effects and for average process variations including mismatch, with 1000 runs each. For average process MC, all similar devices are changed in the same way for each run. For local mismatch MC, the parameters of each transistor are changed individually for each run. Fig. 4.5 (a) shows the spread of reference current, with a $\sigma/\mu = 4.5\%$ for mean process variation + mismatch, while only local mismatch is shown in Fig. 4.5 (b), and yields $\sigma/\mu = 0.65\%$. From these simulations, one can conclude that average process variations (batch-to-batch) are the leading cause of yield reduction.

Fig. 4.5 (c) presents the spread of TC_{eff} for average process variations and mismatch, where 98 % of the parts yields a TC_{eff} below 100 ppm/^{o}C. Fig. 4.5 (d) presents the same spread but only for local mismatch, where all parts have TC_{eff} < 60 ppm/^{o}C. Clearly the factors which are major contributors to the spread are average process variations (batch-to-batch).

Table 4.1 presents a comparison of recently published current references, clearly showing that the main advantage of our new topology is the low temperature coefficient.

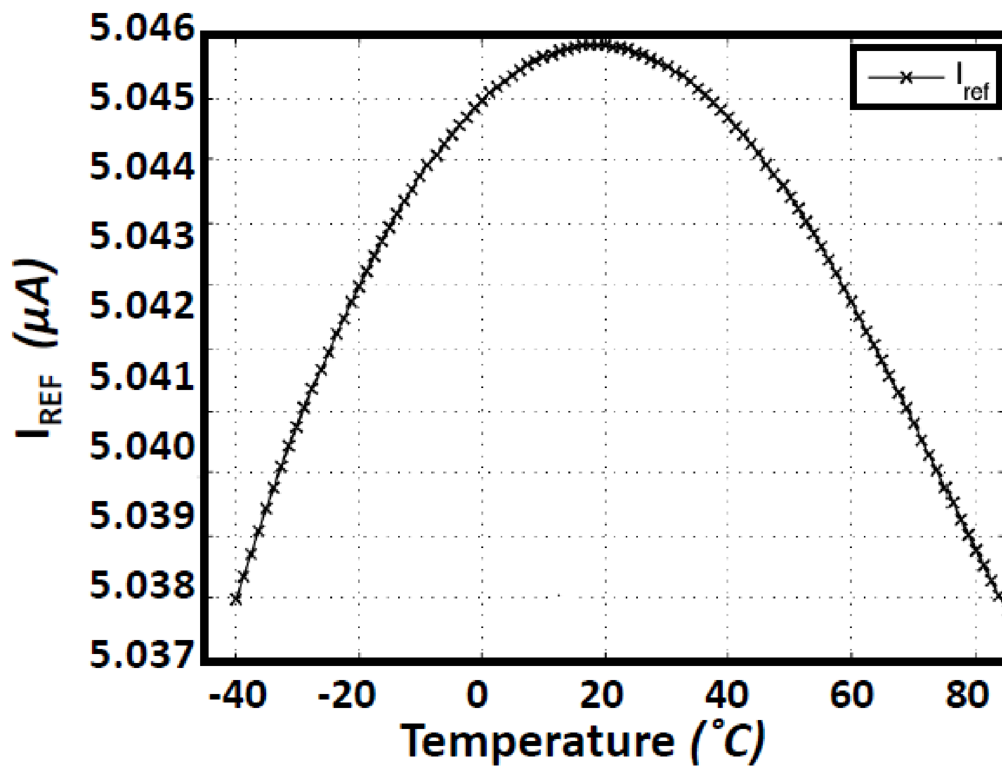


Figure 4.3: Current Reference vs. temperature

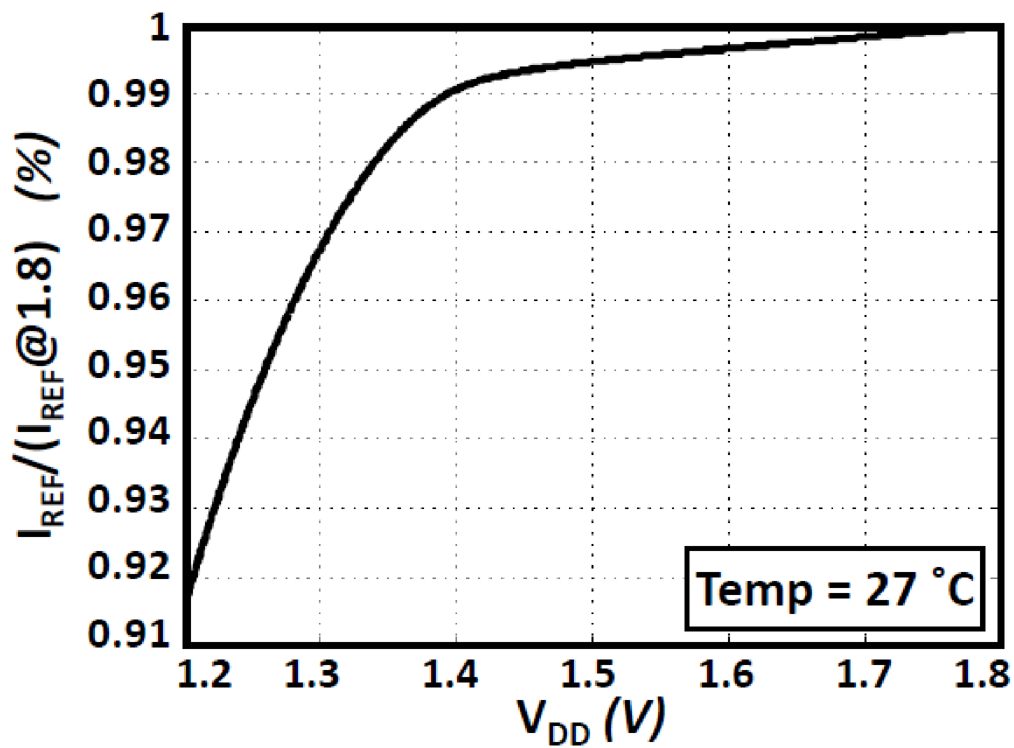


Figure 4.4: Normalized Power Supply Sensitivity

Table 4.1: Comparison of CMOS Current References

Specification	**This Work***	[1]* - I	[1]* - II	[2]*	[3]**	[4]*	[5]*	[6]**	Unit
Technology	**0.18**	0.35	0.35	0.18	0.18	0.18	0.065	1.5	μm
Temperature	**-40 to 85**	-30 to 100	-30 to 100	20 to 80	0 to 100	-20 to 120	-40 to 125	-20 to 70	^{o}C
Power Supply	**1.4-1.8**	N/A	N/A	1.5	1	2	3.3	1.2	V
I_{REF}	**5**	15.1	13.65	N/A	144	263.5	6.45	0.0004	μA
Temperature Coefficient	**15**	130	28	383	185	170	55	2500	ppm/^{o}C
Power	**342**	N/A	N/A	850	227	80	155	0.002	μW
Area	**10000**	4200	4200	N/A	315000	N/A	N/A	45,000	μm^2

* Simulation Results ** Experimental Results

[1] FIORI; CROVETTI (2005) [2] TALEBBEYDOKHTI et al. (2006) [3] BENDALI; AUDET (2007)

[4] LIU; KUSSENER (2010) [5] LUKASZEWICZ; BOREJKO; PLESKACZ (2011) [6] CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER (2005)

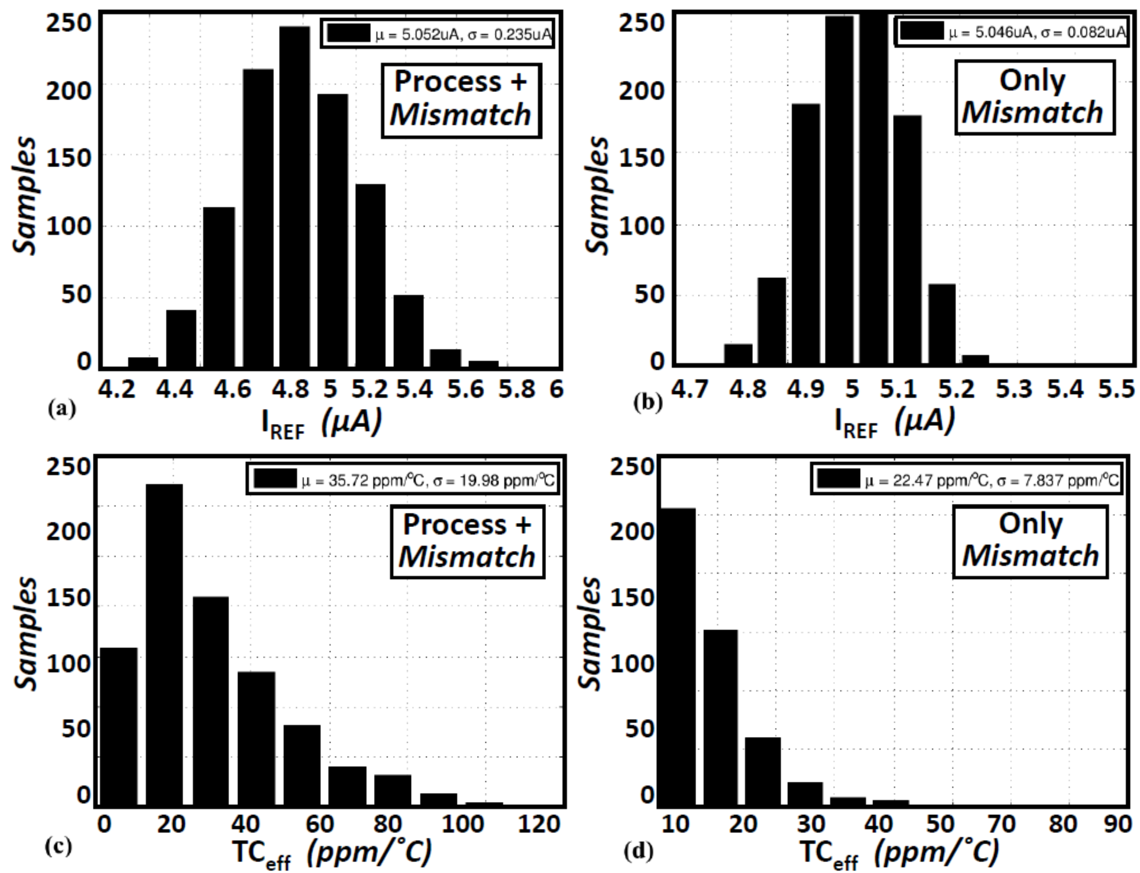


Figure 4.5: (a) I_{REF} Monte Carlo simulation including process and mismatch. (b) I_{REF} Monte Carlo simulation only for mismatch. (c) TC_{eff} Monte Carlo simulation including process and mismatch. (d) TC_{eff} Monte Carlo simulation only for mismatch.

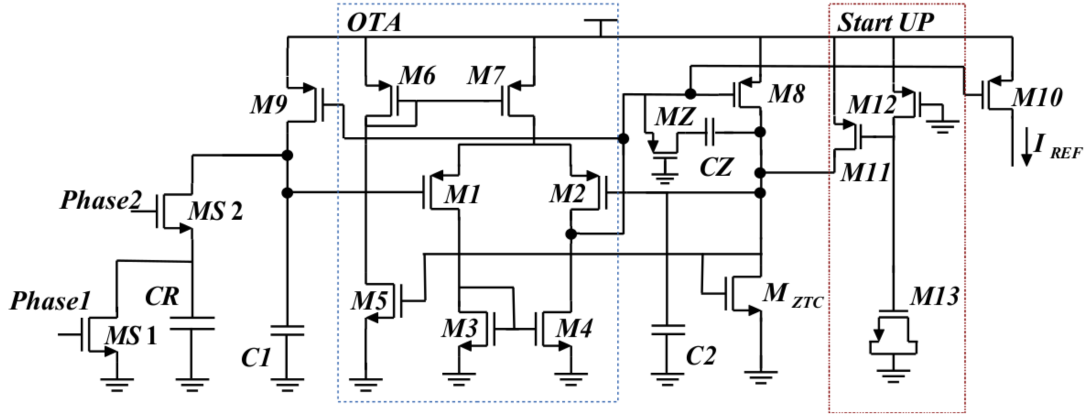


Figure 4.6: ZTC Switched Capacitor Current Reference (ZSCCR).

4.2 Resistorless Self-Biased ZTC Switched Capacitor Current Reference - ZSCCR

The schematic of the circuit is repeated here again for the convenience of the reader, in Fig 4.6. Fig. 4.7 shows post-layout simulation results of the output current in the time domain and Fig. 4.8 shows its temperature dependence, where $I_{REF_{MAX}}$, $I_{REF_{MIN}}$ and $I_{REF_{MED}}$ are maximum, minimum and medium value of output current, respectively. An average output current of 5.88 μA resulted from typical parameters using a switching frequency of 12.5 MHz, presenting an effective temperature coefficient (TC_{eff}) of 60 ppm/^{o}C for the -45 ^{o}C to 85 ^{o}C temperature range, under 1.8V supply. TC_{eff} is defined as Eq. (4.3).

$$TC_{eff} = \frac{I_{REF_{max}} - I_{REF_{min}}}{(T_{max} - T_{min})I_{REF(T_0)}} \tag{4.1}$$

To analyse the robustness of network stability, a Periodic Steady-State (PSS) analysis along with a Periodic Stability (PSTB) analysis were done [KUNDERT (1999)], indicating a Phase-Margin of 63° for the gain loop transfer function (Eq. (3.18)). Fig. 4.9 shows the gain loop magnitude and phase.

Monte-Carlo simulation over 100 runs, including average process and mismatch effects, indicates a standard deviation of the output current of 324 nA, and an average TC_{eff} of 116 ppm/^{o}C. 88$\%$ of the samples had a TC_{eff} lower than 200 ppm/^{o}C.

Table 4.2 presents a comparison of recently published current references. Clearly the main advantages of our new topology are competitive area and low temperature coefficient.

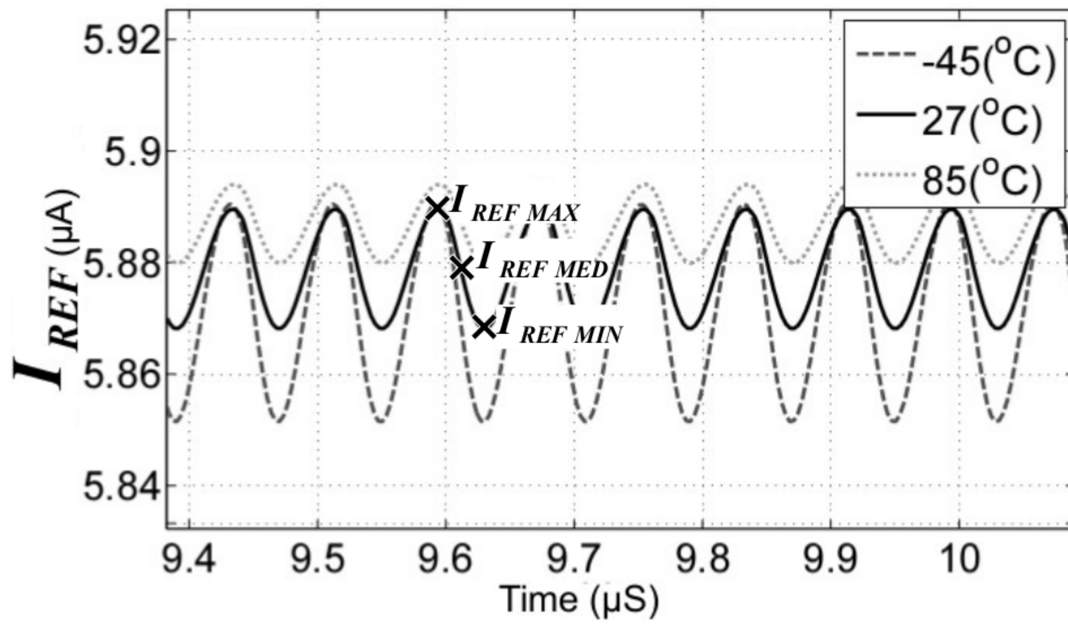


Figure 4.7: I_{REF} in time domain

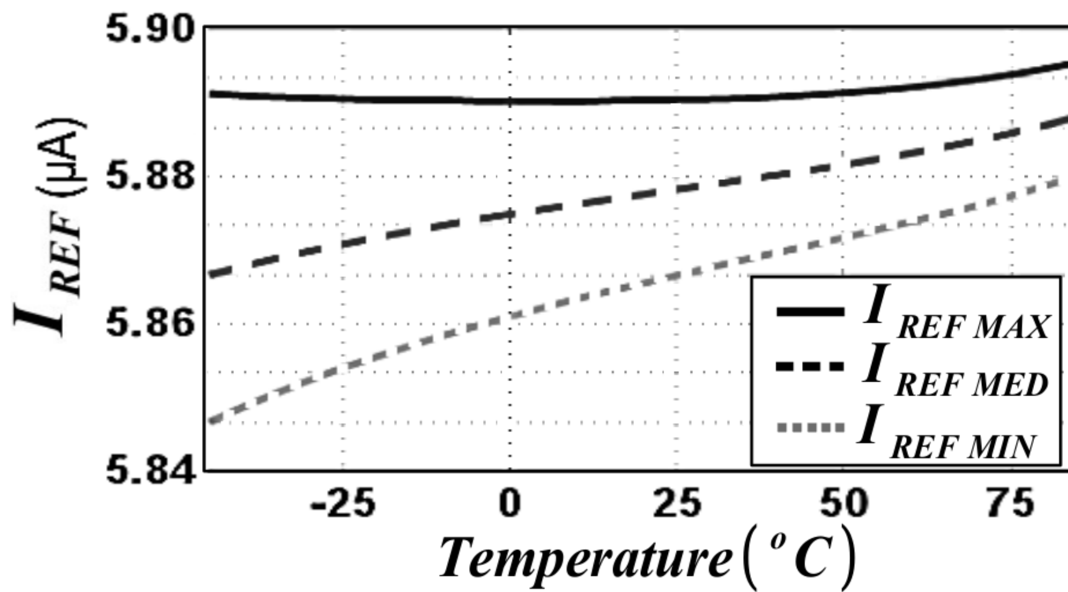


Figure 4.8: I_{REF} vs. Temperature

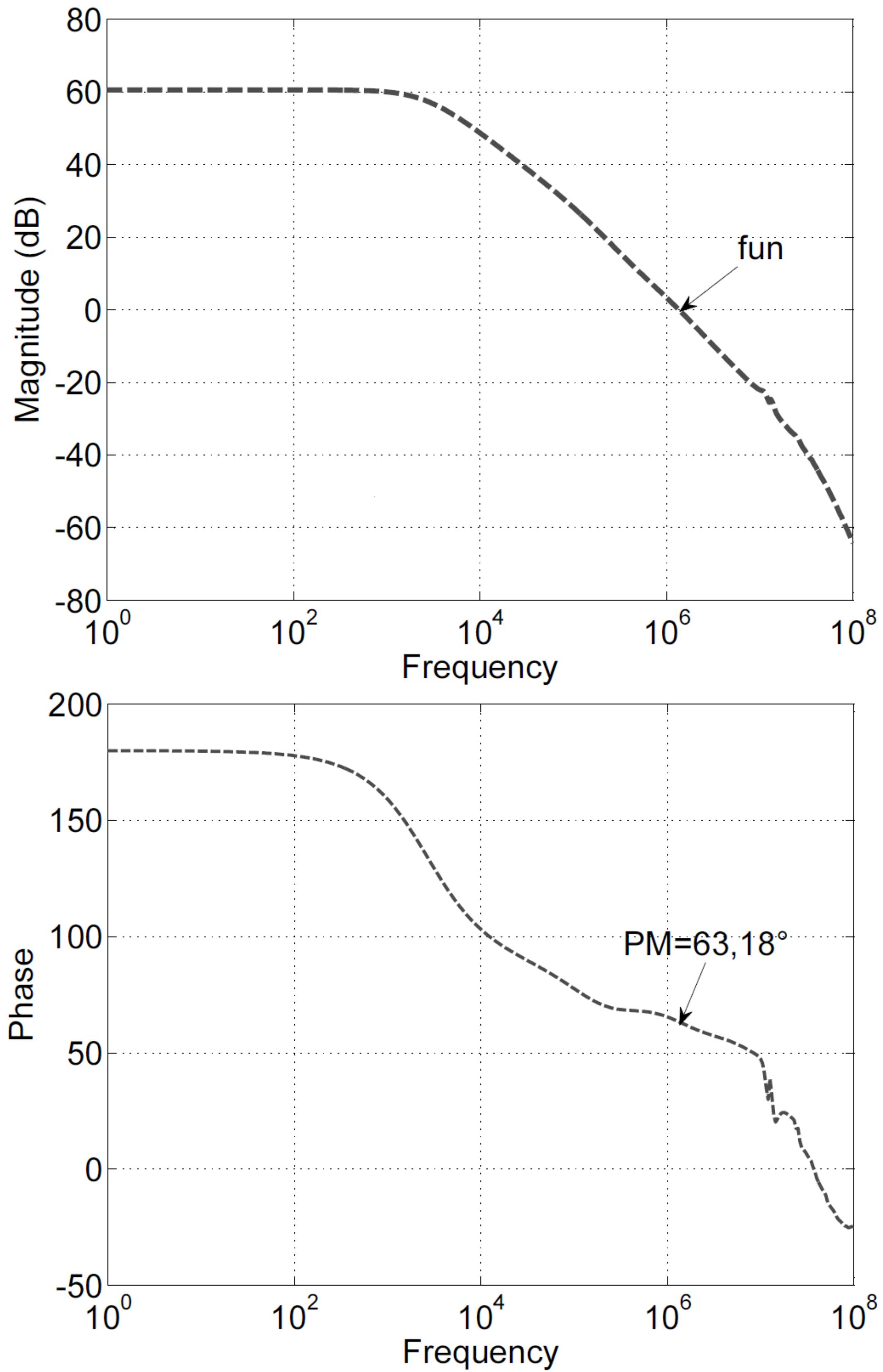


Figure 4.9: Gain loop transfer function. (a) Magnitude (b) Phase. PSS+PSTB analyzes were performed for this result.

Table 4.2: Comparison of CMOS Current References

Specification	[1]*	[2]**	[3]**	**This Work***	Unit
Technology	0.18	1.5	0.18	**0.18**	μm
Temperature	-40 to 85	-20 to 70	0 to 100	**-40 to 85**	^{o}C
Power Supply	1.4-1.8	1.2	1	**1.8**	V
I_{REF}	5	0.0004	144	**5.88**	μA
TC_{eff}	15	2500	185	**60**	ppm/^{o}C
Power	342	0.002	227	**63**	μW
Area	10,000	45,000	315,000	**10,000**	μm^2

*Simulation **Experimental

[1] TOLEDO et al. (2014) [2] CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER (2005) [3] BENDALI; AUDET (2007)

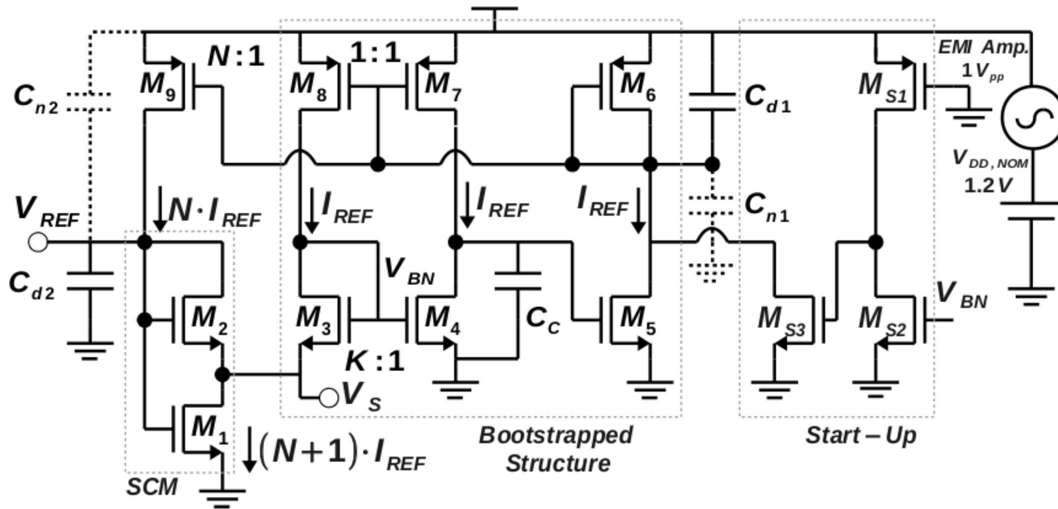


Figure 4.10: Proposed EMI resisting CMOS voltage reference schematic circuit.

4.3 Electromagnetic Interference (EMI) Resisting MOSFET-Only Voltage Reference - EMIVR

Fig 4.10 shows the schematic of the circuit for the convenience of the reader. The proposed voltage reference circuit has been validated with Cadence™post-layout simulations. Fig. 4.11 shows simulated reference voltage as a function of the temperature in the range from -55 to 125 ^{o}C with 1.2 V of supply voltage, resulting a reference voltage around 395 mV at room temperature, with a Effective Temperature Coefficient (TC_{eff}) of 146 ppm/^{o}C. TC_{eff} is given by Eq. (4.2).

$$TC_{eff} = \frac{V_{REF_{max}} - V_{REF_{min}}}{(T_{max} - T_{min})V_{REF(T_0)}} \tag{4.2}$$

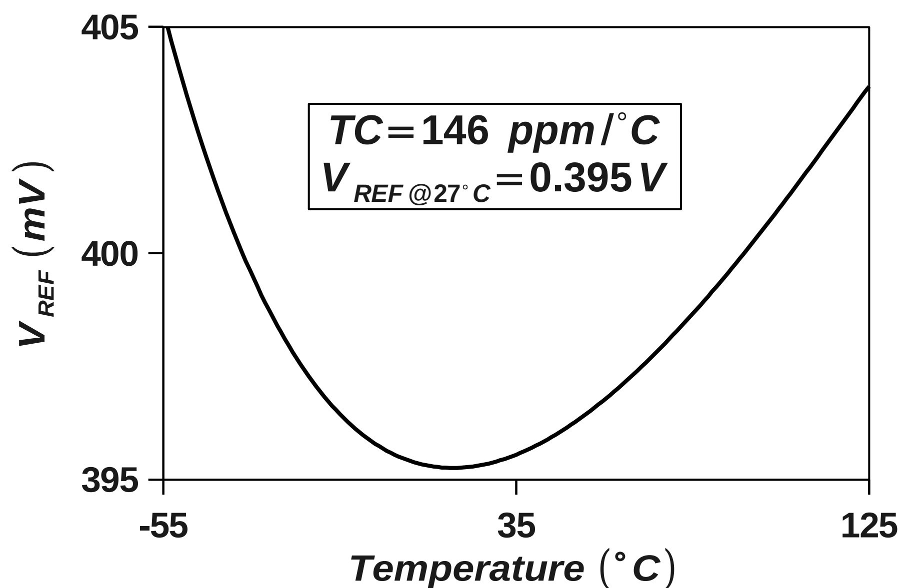


Figure 4.11: V_{REF} vs Temperature. (b) Power Supply Rejection Ratio of V_{REF}

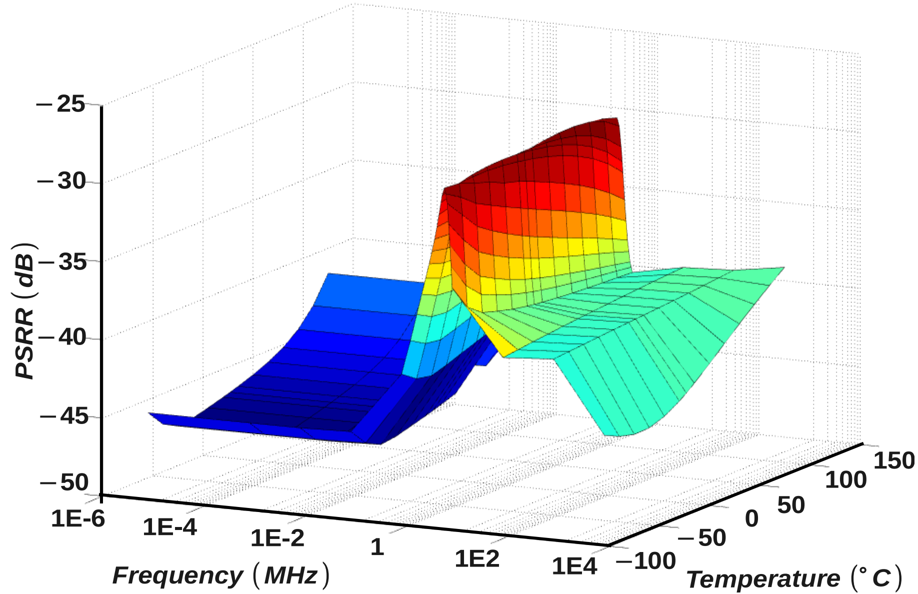


Figure 4.12: V_{REF} Power Supply Rejection Ratio

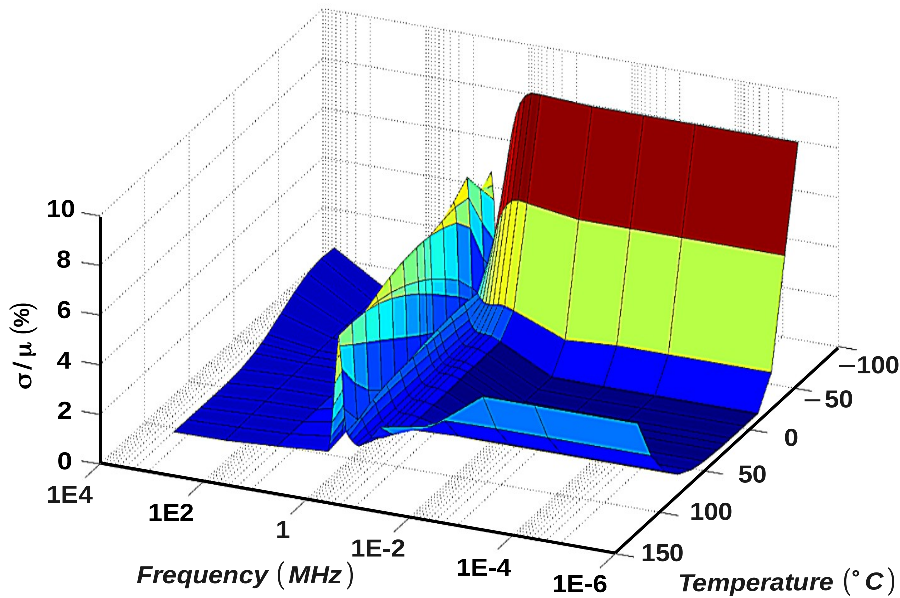


Figure 4.13: V_{REF} Power Supply Rejection Ratio

Fig. 4.12 presents the Power Supply Rejection Ratio (PSRR) in function of frequency ($10KHz$ to $1GHz$) and temperature (-55 to $+125^o$C). Each graph point is average (μ) value of a Monte Carlo (MC) simulation for 100 samples. MC simulation have been done taking into account local mismatch effects and average process variations. It is worth to note that rejection improvement has been achieved especially due to the C_{d1} insertion. More specifically for frequencies around 1 MHz. In addition, Fig. 4.13 shows the PSRR process sensitivity (σ/μ) for the same range of Fig. 4.12, where σ is the standard deviation for each 100 MC run. From this figure, one can see that for frequencies lower than $10KHz$ and temperatures lower than -40^oC the PSRR process variation sensitivity increases very much. In summary, All relevant performance figures, such as line regulation, PSRR, TC_{eff} and sensitivities are listed in Table 4.3.

Table 4.3: Simulated Performance of the voltage reference.

Process CMOS	**0.13μm**	**Unit**
$V_{DD,NOM}$, $V_{DD,MIN}$	1.2, 0.6	V
V_{REF}	395	mV
I_{REF}	2.05	uA
LR (V_{REF})	6.67	mV/V
LR (I_{REF})	134.4	nA/V
Process sensitivity (V_{REF}) (σ/μ)†	3.7	%
Process sensitivity (I_{REF}) (σ/μ)†	10	%
TCeff (Vref) (-55 to 125°C)†	μ =146 ; σ =9.7	ppm/^{o}C
TCeff (Iref) (-55 to 125°C)†	μ =300 ; σ =149	ppm/^{o}C
PSRR@100 kHz (V_{REF},I_{REF})	(-41.5, -138.9)	dB
PSRR@1 MHz (V_{REF},I_{REF})	(-39, -123.4)	dB
Power@ $V_{DD,NOM}$	10.27	μW
Area	0.0075	mm^2

* Simulation Results †Process and Mismatch (1000 runs)

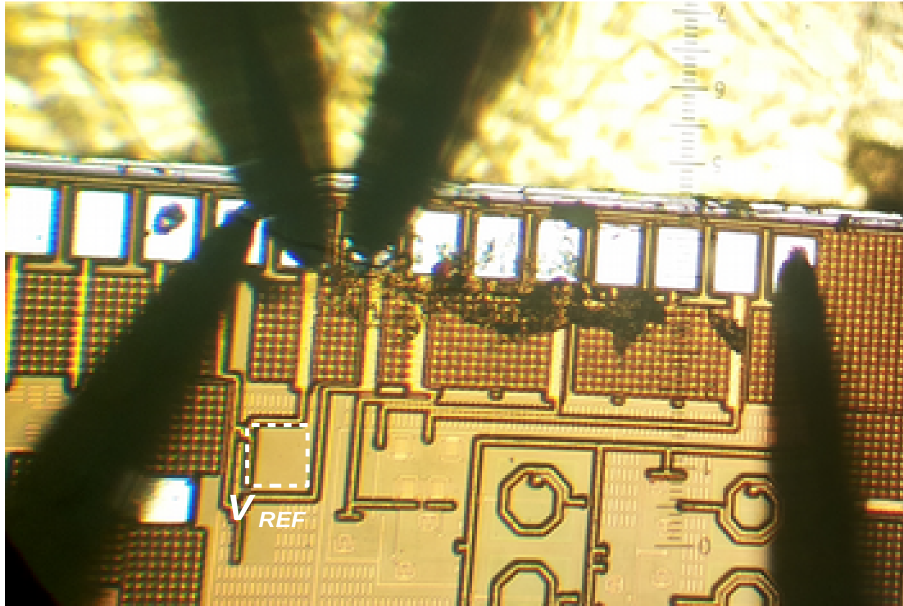


Figure 4.14: Micrograph of a small area of the chip, fabricated in IBM 130nm, where the proposed V_{REF} is highlighted.

The reference was fabricated in IBM 130nm process as shown in Fig 4.14. The supply voltage sensitivity of five bare-die samples were measured as shown in Fig. 4.15, were 'extracted' means the simulated behavior for comparison purposes.

Regarding EMI disturbances, the voltage reference has been simulated using an EMI source injected in the power supply according the DPI standard [STANDARD (2004)]: the EMI frequency ranges between 150 kHz and 1 GHz. A maximum EMI level of 4 dBm (1 V_{pp} amplitude) under $V_{DD,NOM}$ (supply swings between 0.7 to 1.7 V) has been chosen in order to not affect the proper functioning of the voltage reference. The EMI coupling from the power supply to reference node V_{REF} has been characterized using a DC shift and peak-to-peak ripple in the SCM, Eq. (3.33) and (3.34) [REDOUTE; STEYAERT (2010b)]. The DC shifts and EMI peak-to-peak are shown in Figs. 4.16 (a) and (b),

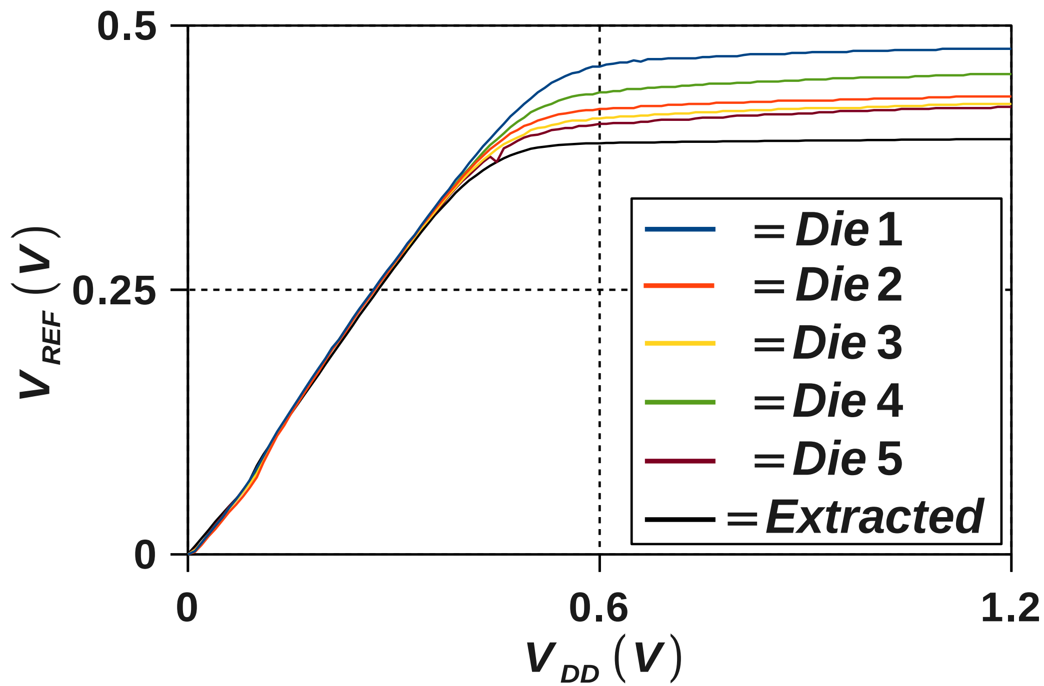
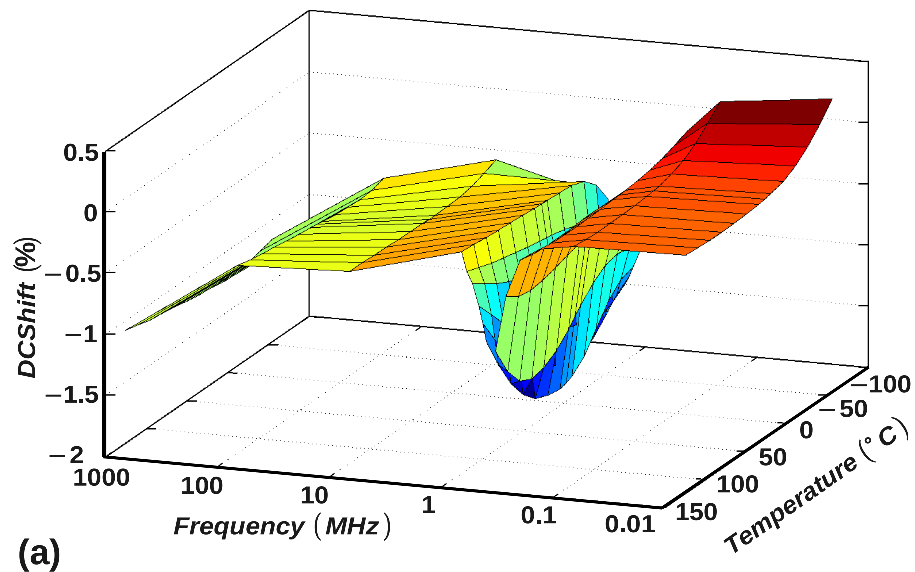


Figure 4.15: V_{REF} vs. V_{DD}, dies # 1-5

respectively. The same range used in Fig. 4.12 and 4.13 has been adopted in Figs. 4.16 (a) and (b) as well. Process DC shift and peak-to-peak sensitivity are pictured in Fig. 4.17 (a) and (b), respectively.

Table 4.6 shows the comparison between our proposed voltage reference and the reference of [REDOUTE; STEYAERT (2010a)]. Our VR attains a better peak-to-peak ripple of 35.81 mV and a worst DC shift of 1.7 $\%$ for the same EMI source (4 dBm), while consuming less power and area.



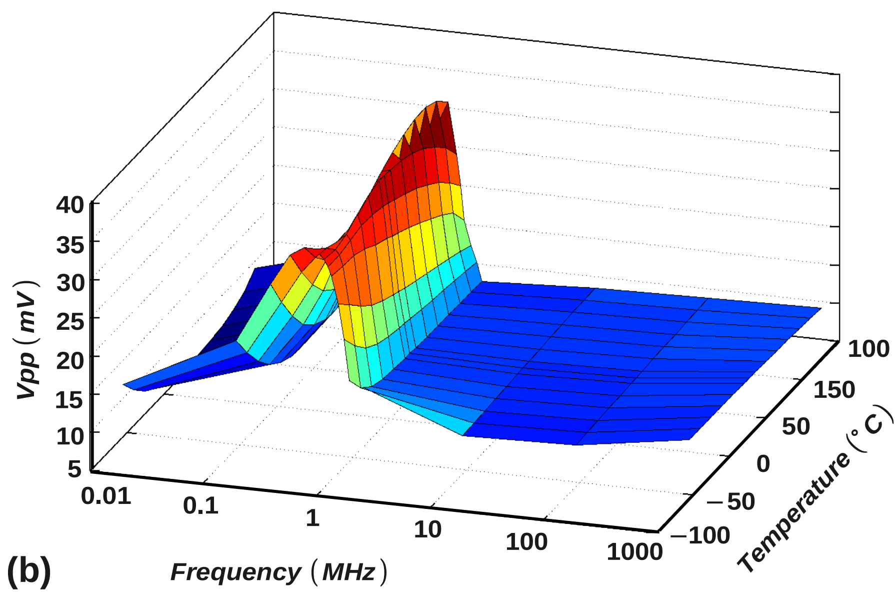


Figure 4.16: (a) DC shift as a function of the EMI frequency and temperature. (b) Peak-to-peak ripple on V_{REF} as a function of the EMI frequency and temperature. EMI level = 4 dBm

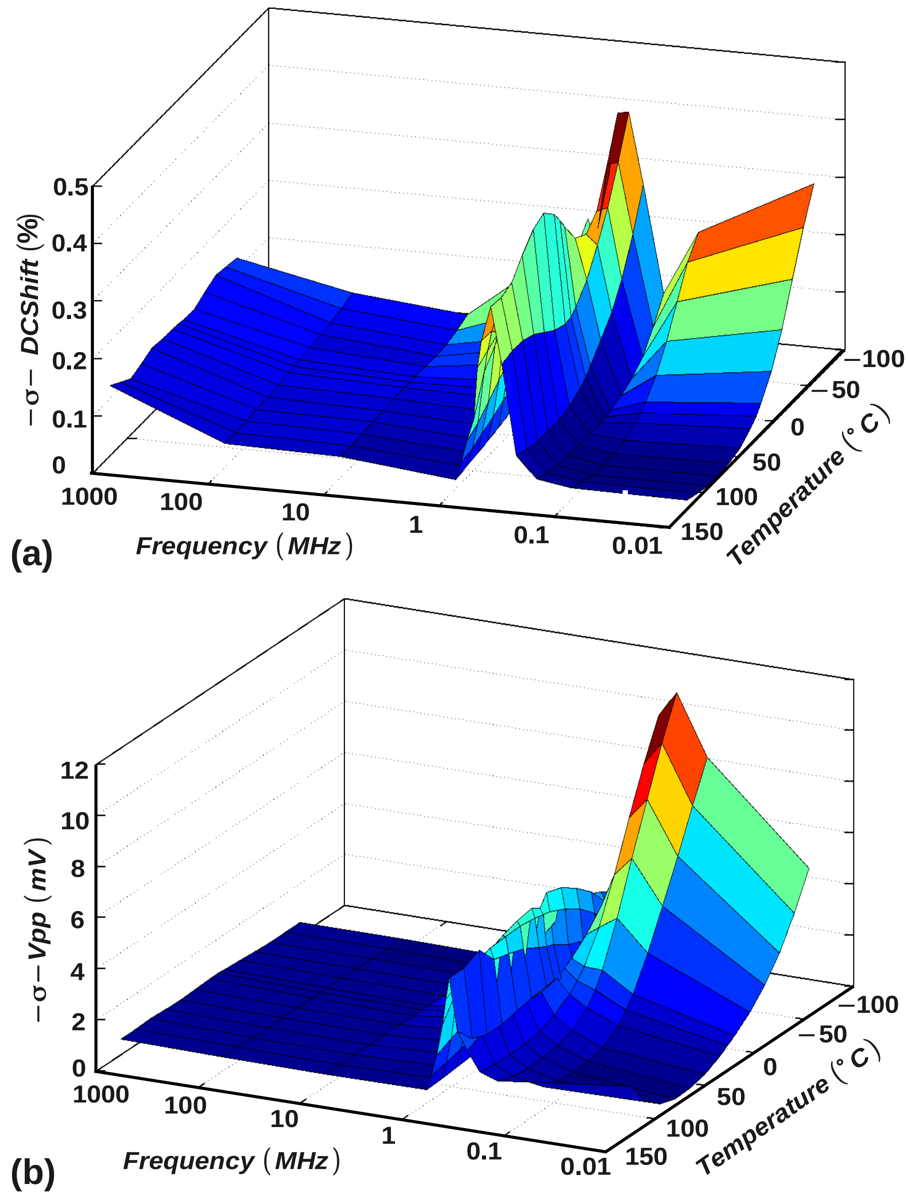


Figure 4.17: (a) DC shift process sensitivity as a function of the EMI frequency and temperature. (b) Peak-to-peak ripple process sensitivity on V_{REF} as a function of the EMI frequency and temperature. EMI level = 4 dBm

Table 4.4: Comparison with other works.

Case	**Conducted EMI** $@V_{DD}$		
Standard	IEC 62132-4. DPI Method[STANDARD (2004)]		
	This Work	$[1][2]^{\theta}$	
Process CMOS	0.13-μm	0.35-μm	
Topology	ZTC-based	PPDAL-Kuijk	Unit
$V_{DD,NOM}$	1.2	3.3	V
$\overline{V_{REF}}$	$0.395^{\star}$	1.2	V
MIN	$0.423^{\oplus}$	-	V
AVG	$0.4416^{\oplus}$	-	V
MAX	$0.472^{\oplus}$	-	V
EMI Level	$4 \leftrightarrow 1$ V_{pp}		dBm
DC Shift$_{MIN-MAX}$	$-1.7 \leftrightarrow 0.5$ $^{\bullet\star}$	$-0.5 \leftrightarrow 2$	%
PP ripple$_{MIN-MAX}$	$5.4 \leftrightarrow 35.8$ $^{\bullet\star}$	$25 \leftrightarrow 75$	mV
Power	10.27 *	283.8	uW
MIN	$11.5^{\oplus}$	-	
AVG	$13.3^{\oplus}$	-	
MAX	$14.7^{\oplus}$	-	
Area	0.0075	0.1	mm^2

*@(27C,$V_{DD,NOM})^{\theta}$; Third-Topology; $^{\bullet}$ for V_{REF})
$^{\oplus}$ Measurement $^{\circ}$ Area = 0.3mm^2 $\rightarrow$ 3 Circuits

[1] REDOUTE; STEYAERT (2010a) [2] REDOUTE; STEYAERT (2010b)

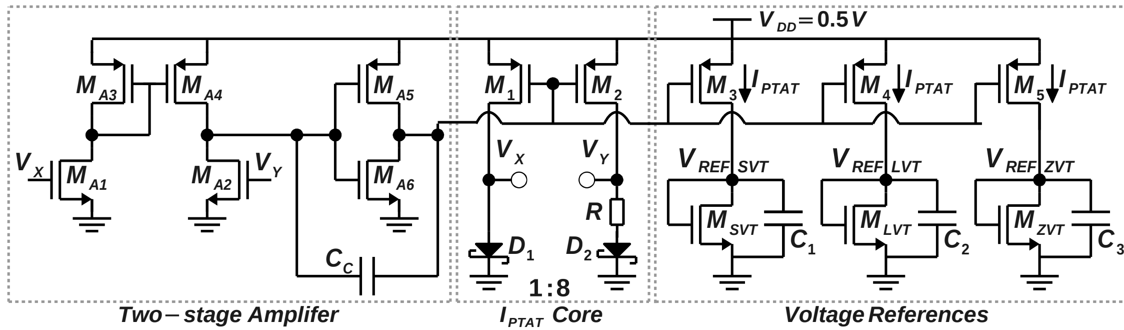


Figure 4.18: Proposed 0.5-V CMOS voltage reference schematic circuit.

4.4 0.5 V Supply Schottky-diode based Voltage Reference - SBVR

Using a nominal supply voltage of 0.5 V, the proposed voltage reference shown again in Fig. 4.18 was validated using BSIM4 models [ALL (2013)] provided by the foundry and within the temperature range of -55 to 125°C. DC and AC simulations were run to estimate the following performance parameters: PTAT current (I_{PTAT}) and reference voltages (V_{REF}), TC_{eff}, line regulation (LR), power supply rejection ratio ($PSRR$) and power consumption.

Fig. 4.19 shows the temperature dependence of PTAT current reference, that was designed for a nominal value of 1 μA under 27°C and a temperature coefficient TC of 4000 ppm/°C. The PTAT TC is not constant, and decreases at high temperatures, above 90°C, as can be noted from Fig. 4.19.

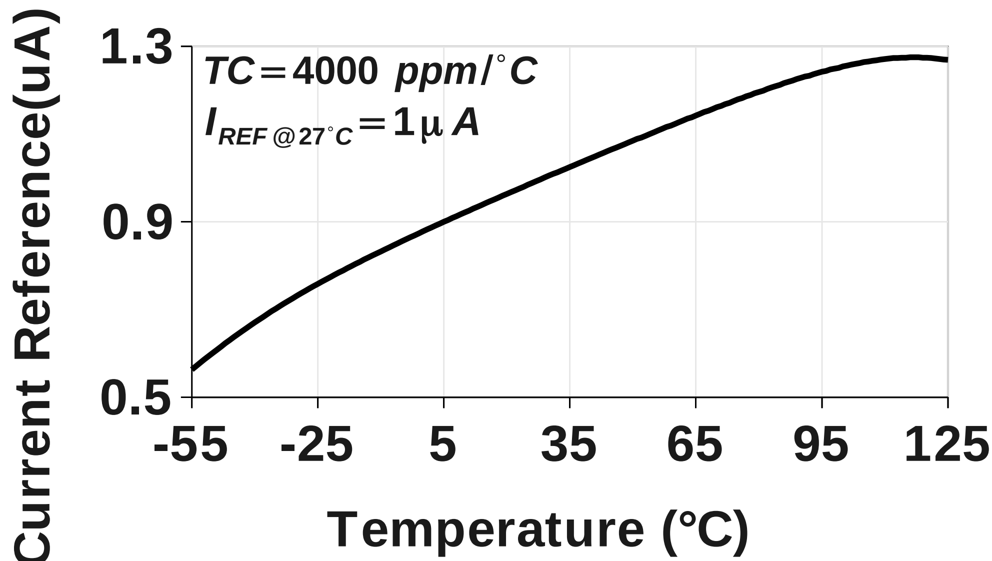


Figure 4.19: PTAT current reference variation over temperature.

Temperature sensitivity of voltage reference is shown in Figs. 4.20, 4.21 and 4.22 for the three threshold MOSFETs, 'standard-V_T' (SVT), 'low-V_T' (LVT) and 'zero-V_T' (ZVT). The obtained simulated nominal reference voltages were of 312 mV, 237 mV and 51 mV with TCs of 214 ppm/°C, 372 ppm/°C and 953 ppm/°C, respectively.

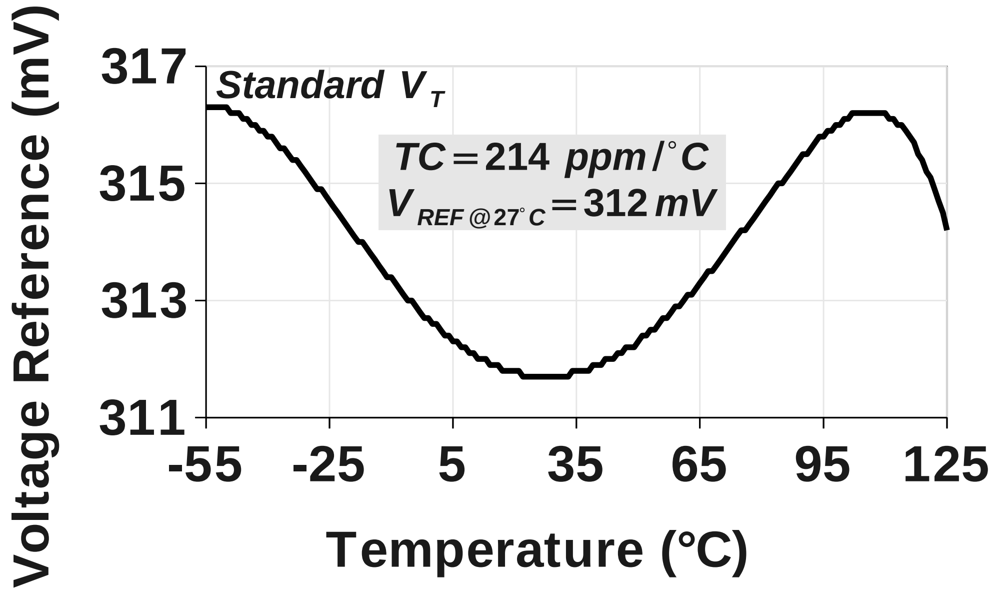


Figure 4.20: Voltage reference (standard-V_T) variation over temperature.

Fig. 4.23 exhibits simulated power supply rejection (PSRR) of each output reference voltage at room temperature.

The impact of fabrication process variations on reference performance was estimated using Monte Carlo analysis. Table 4.5 summarizes each performance variations (mean and standard deviation) for I_{PTAT}, V_{REF}, TC, LR, and $PSRR$, as shown in the second, third, and fourth columns in Table 4.5 for the herein considered SVT, LVT, and ZVT transistor cases, respectively.

During the revision of this thesis, after M.Sc. defense, some preliminary measurements have been done. Fig. 4.24 shows the micrograph of our proposed 0.5 V Voltage Reference. All measurements have been made using thermal chuck and a semiconductor parameter analyzer under 4-wire measurement (also known as force/sense mode), which can accurately measure currents under 1 pA.

Fig. 4.25 (a) and (b) display the measurements results for supply voltage versus $V_{REF,SVT}$, $V_{REF,LVT}$ and $V_{REF,ZVT}$ and values of each sample at 0.5 V and room temperature respectively, showing that the proposed circuit is working within the predicted MC simulations. For example, from table 4.5 the $V_{REF,ZVT}$ average value is 51 mV with a standard deviation of 11.7 mV. Our VR post-fabrication generated reference voltages of 68.4, 65.8, 62.24, 57.84, 60.68 mV, meaning that for this batch they are below 2-sigma. This statement is also valid for $V_{REF,SVT}$ and $V_{REF,LVT}$.

Derived from Fig. 4.25 (a) at $V_{DD} = 0.5$, the left side of Fig. 4.25 (c) list all Line Regulation (LR) measurements for each output. For $V_{REF,SVT}$, $V_{REF,LVT}$ in general the LR results have been twice larger as compared with simulation results. In the case of zero-V_T transistor, there have been 2 samples which were 30% larger than expected value and 3 samples following the same pattern as standard-V_T and low-V_T transistor. The total power consumption for each chip is placed in the right side of Fig. 4.25 (c). The maximum power found was 6.1 μW for the chip 2.

The curves V_{REF} versus temperature are shown in Figs. 4.25 (d), (e) and (f) for the five measured samples. Unfortunately, all PADs related to $V_{REF,SVT}$ and two PADS related

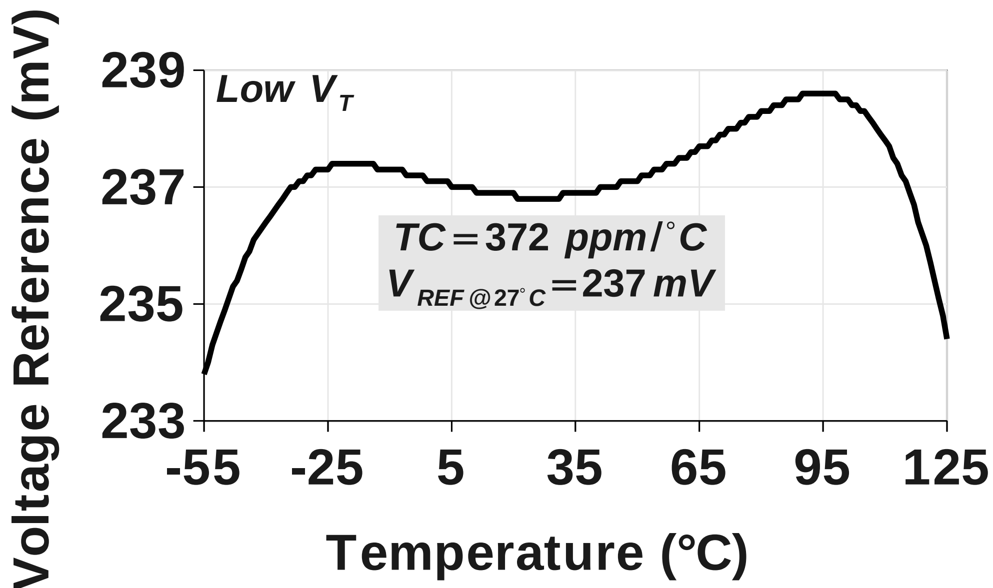


Figure 4.21: Voltage reference (low-V_T) variation over temperature.

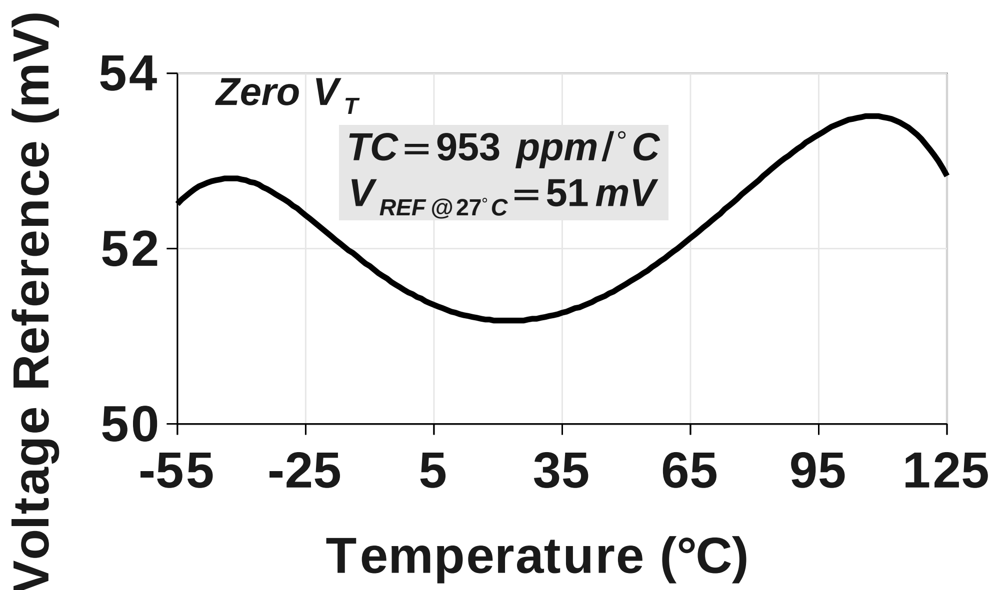


Figure 4.22: Voltage reference (zero-V_T) variation over temperature.

to $V_{REF,LVT}$ have been damaged during temperature sweeping measurements. Given that TC_{eff} is calculated by Eq. 4.3, all measured TC_{eff}s can be seen on the figures. For the $V_{REF,LVT}$ the best TC_{eff} was 66.7 $ppm/^oC$ and for the $V_{REF,ZVT}$, 376 $ppm/^oC$. According to table 4.5, all presented measurements results are in agreement with the simulation.

$$TC_{eff} = \frac{V_{REF_{max}} - V_{REF_{min}}}{(T_{max} - T_{min})V_{REF(T_0)}} \tag{4.3}$$

Table 4.6 shows a comparison between other Schottky-diode-based voltage references

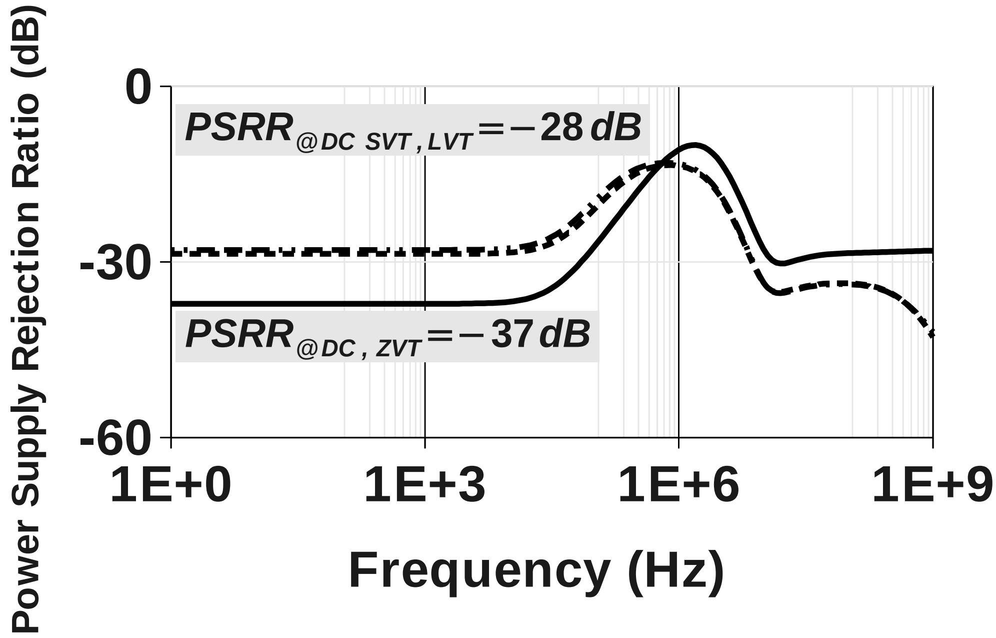


Figure 4.23: Power supply rejection ratio of the proposed voltage reference.

Table 4.5: Simulated Performance of the SUB-1V V_{DD} Schottky based reference.

Process CMOS	0.13-mm⋆			Unit
Temp. Rage	-55 ↔ 125			^{o} C
$V_{DD,NOM}$	0.5			V
V_{DD} Range	0.45 ↔ 1.2			V
$\overline{V_{REF}}$ ⊕	312	238	52	mV
$\overline{I_{PTAT}}$ ⊕	1			uA
LR (V_{REF})	35.5	39	13.5	mV/V
LR (I_{PTAT})	466			nA/V
$\overline{V_{REF}}$ †	μ = 312 ; σ = 17.8	μ= 237 ; σ= 23.2	μ = 51 ; σ= 11.7	mV
$\overline{V_{REF}}$ μ/σ	5.7	9.7	22.5	%
TC (V_{REF}) † 98% Samples	μ = 214; σ= 133 < 440	μ = 372; σ = 268 < 810	μ = 953; σ = 676 < 2300	ppm/°C
PSRR@ DC † 100% Samples	μ = -28; σ = 1.3 < -26	μ = -27.5; σ = 1.45 < -24	μ = -36.8; σ = 1.8 < -33	dB
PSRR@100 kHz † 100% Samples	μ = -20; σ = 2 < -18	μ = -19; σ = 2 < -15	μ = -27; σ = 2.3 < -20	dB
PSRR@1 MHz † 100% Samples	μ = -14;σ = 1.2 < -10	μ = -13.3; σ = 1.2 < -11	μ = -11; σ = 1.7 < -8	dB
Power⊕	5.9			uW
Area	0.014			mm^2

⊕ 27 ^{o}C $V_{DD,NOM}$); ⋆ Simulation results; † Process and Mismatch (1000 runs)

reported. Our proposed topology was designed to optimize power consumption in a wider temperature range, while maintaining a comparable TC to the other implementations. Our design used at least 10 times lower current than the previous works in Table 4.6.

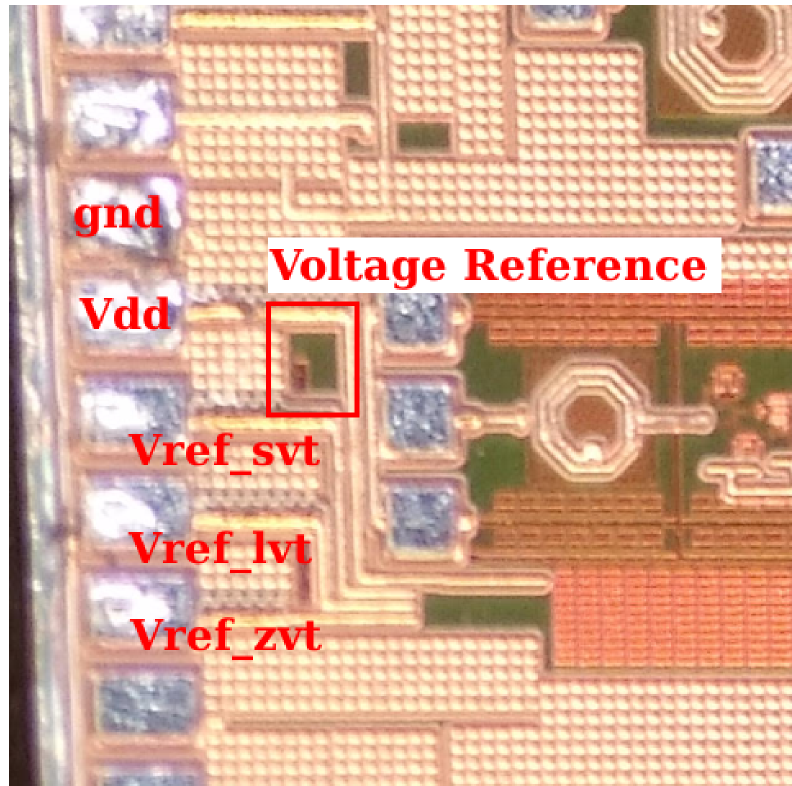


Figure 4.24: Micrograph of our proposed 0.5 V Voltage Reference in IBM 130 nm die

Table 4.6: Performance comparison for SUB-1V V_{DD} Schottky based reference

	This Work*	KINGET et al. (2008)	BUTLER; JACOB BAKER (2005)	
CMOS Process	0.13 μm*	90 nm	0.5 μm	Unit
Temp. Rage	-20 $\leftrightarrow$ 120	5 $\leftrightarrow$ 100	5 $\leftrightarrow$ 70	°C
$V_{DD,NOM}$	0.5	0.6	2.5	V
$V_{DD,MIM}$	0.45	0.5	1.2	V
V_{REF} $^{\oplus}$	262.2	251	400	mV
$\Delta V_{REF}/\Delta V_{DD}$	8	3	1.4	mV/100mV
TC_{eff} (V_{REF})	66.7	263	107	ppm/°C
Power$^{\oplus}$	5.5	450	59.4	uW
Area	0.014	0.02	N/A	mm^2

$^{\oplus}$@(°27C, $V_{DD,NOM}$); * Measuments Results for Chip 1 and M_{LVT};

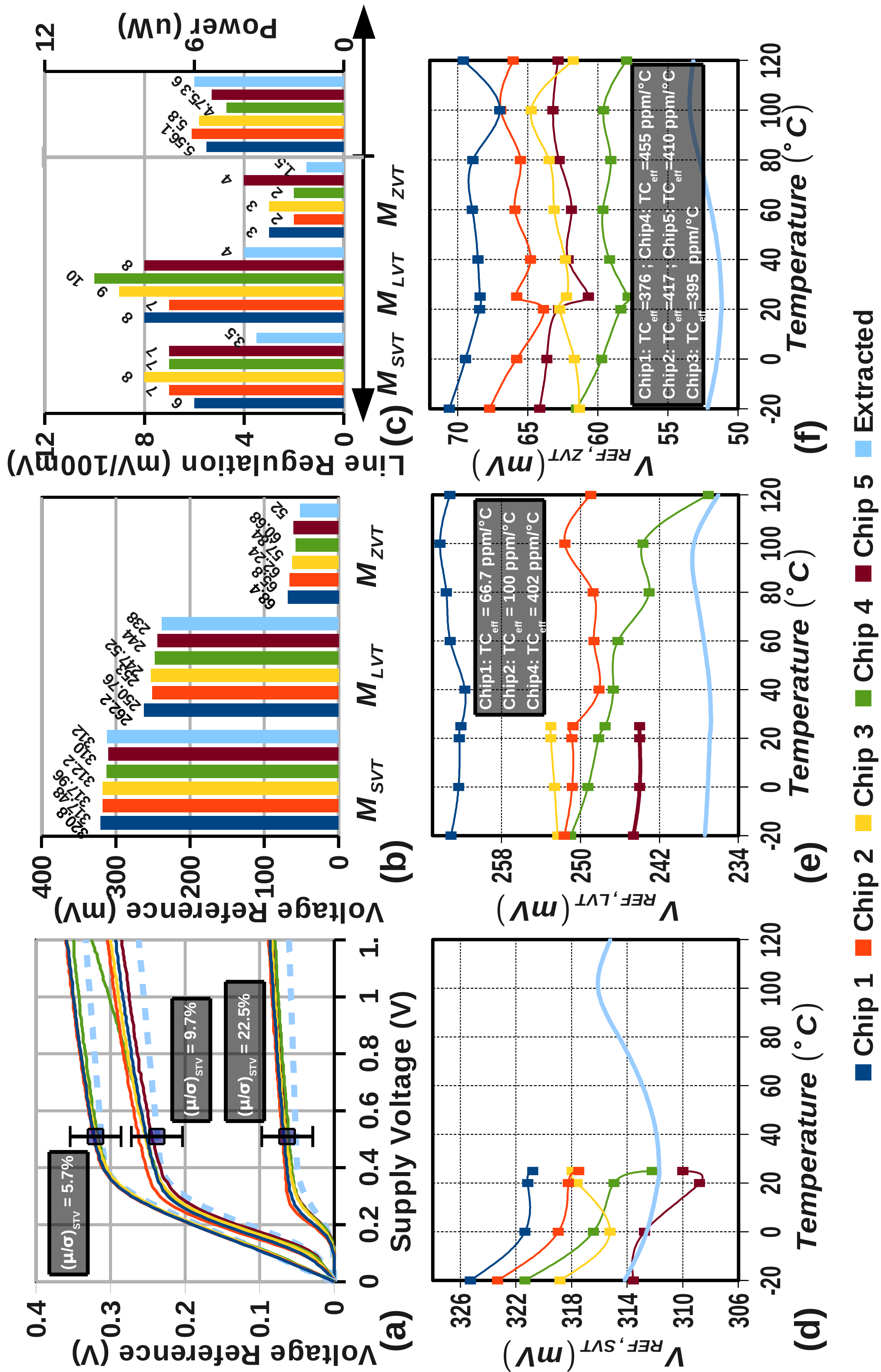


Figure 4.25: (a) Measurements line sensitivity for 5 samples (b) V_{REF} for each sample (c) All Line Regulation (LR) measurements for each output (d,e,f) V_{REF} versus temperature for $V_{REF,SVT}$, $V_{REF,LVT}$ and $V_{REF,ZVT}$ reference voltages, respectively.

4.5 GZTC Based Gm-C Filters

The application circuits presented here were designed and simulated in IBM 130 nm CMOS commercial process in schematic level only since parasitics would mainly degrade frequency response. Schematics of each circuit are repeated here for the convenience of the reader in Fig. 4.26 .The calculated bias current is 4 μA for each transcondutor, with a TC_I around 3000 ppm/^{o}C. A current reference with TC_I between 1000 and 10000 ppm/^{o}C is easily achievable in CMOS technology [SERRA-GRAELLS; HUERTAS (2003)]. For instance, the PTAT current used in one of work presented in this thesis was 4000 ppm/^{o}C, as demonstrated at subsection 4.4. The capacitors C_L = C_1 = 10 pF were used in the impedance converter and the first order filter. The capacitors C_1 = C_2 = 15 pF were employed in the second order filter.

Fig. 4.27 (a) presents the frequency response of input impedance of the single-ended resistor emulator. When the curves are zoomed one can note that the equivalent resistance presents low temperature sensitivity. Fig. 4.27 (b) shows equivalent resistance $(1/g_m)$ versus temperature, confirming a low sensitivity to temperature variations (continuous line), i.e., the equivalent resistance temperature coefficient is TC_{eff} = 34 ppm/^{o}C under a supply voltage V_{DD} = 1.2 V. The resulting coefficient is comparable to TCs obtained in some CMOS voltage and current reference circuits found in the literature [GOPAL; BAGHINI (2014)][TOLEDO et al. (2014)]. On the other hand, if it is not applied the right amount of PTAT current the equivalent resistance will be more susceptible to temperature variations, as also shown (dashed line) in Fig. 4.27 (b) resulting a TC'_{eff} = 1568 ppm/^{o}C. The apostrophe on TC_{eff} means that this estimation was not done putting required TC_I in the transconductor in order to make it independent of temperature.

The impedance converter also presented a good thermal immunity, resulting a TC_{eff} = 52.5 ppm/^{o}C (TC'_{eff} = 3300 ppm/^{o}C), as can be seen in Fig. 4.28 (a). Regarding the filters, a TC_{eff} of 44.5 ppm/^{o}C (TC'_{eff} = 1495 ppm/^{o}C) for the dominant pole (Fig. 4.28 (b)) and a TC_{eff} of 27 ppm/^{o}C (TC'_{eff} = 970 ppm/^{o}C) for the quality factor (Fig. 4.29) were obtained from the simulations of first order and second order filters, respectively.

To predict vulnerability to manufacturing process variations (average process variations + mismatch), 1000 simulations samples under a temperature range of -45 to 85^oC (-45,-15, 27, 55 and 85 ^oC) were performed for the first order filter. Both cases were accomplished: TC_I = 0 and TC_I = 3000 ppm/^oC. Fig. 4.30 shows that biasing the trasnconductor at GZTC point along with suitable current temperature coefficient (TC_I) the average process variation (μ) of dominant pole holds constant regarding the temperature. Note that standard deviation (σ) around μ has negligible changes over entire temperature range since it is only dependent of manufacturing process variations [GALUP-MONTORO et al. (2005)].

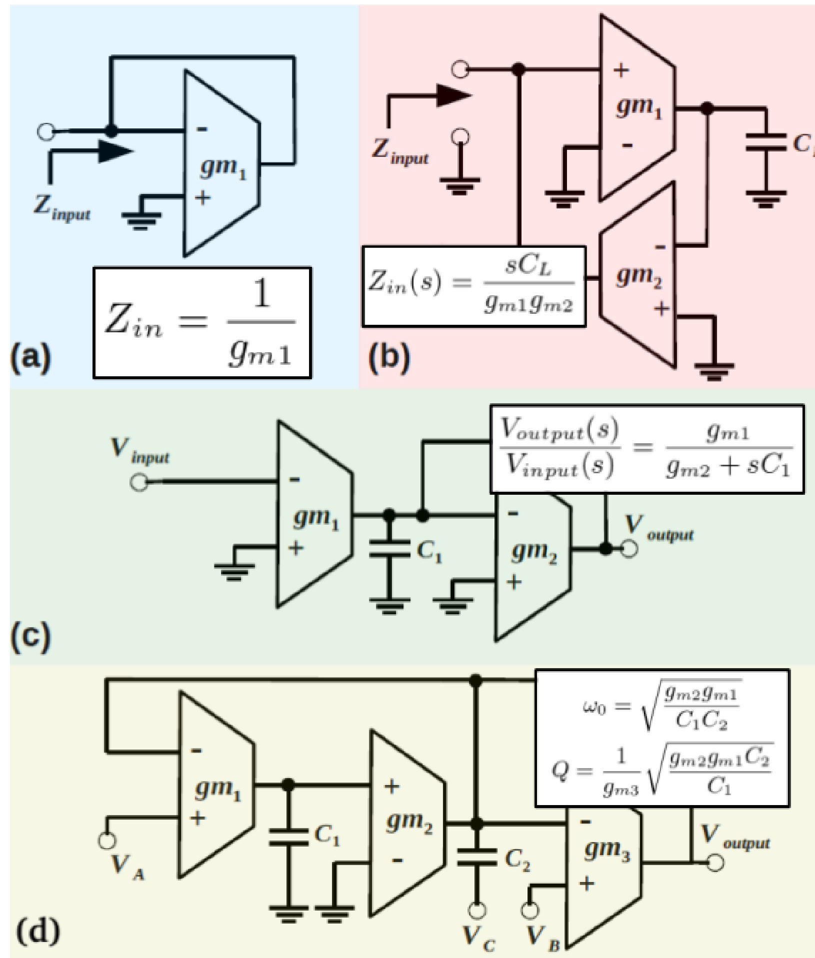


Figure 4.26: (a) single-ended resistor emulator (b) impedance inverter (c) first order filter (d) second order filter.

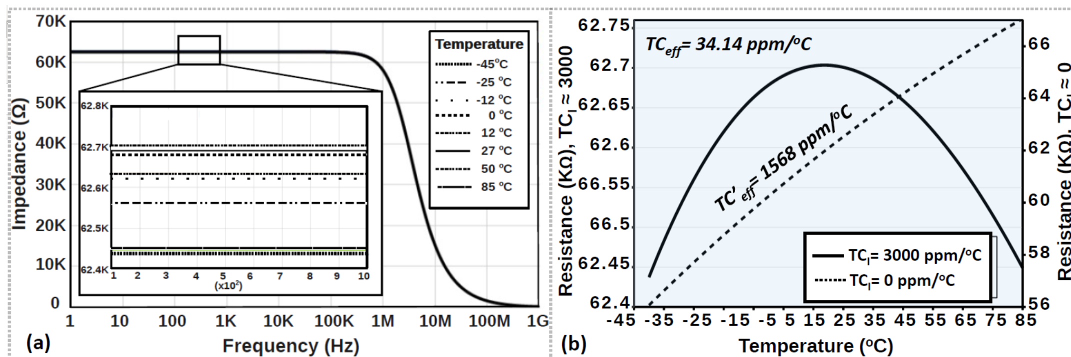


Figure 4.27: (a) Input impedance of single-ended resistor emulator (b) Equivalent Resistance vs. Temperature. Effective Temperature Coefficient is given by $TC_{eff} = \frac{I_{REF_{max}} - I_{REF_{min}}}{(T_{max}-T_{min})I_{REF(T_0)}}$.

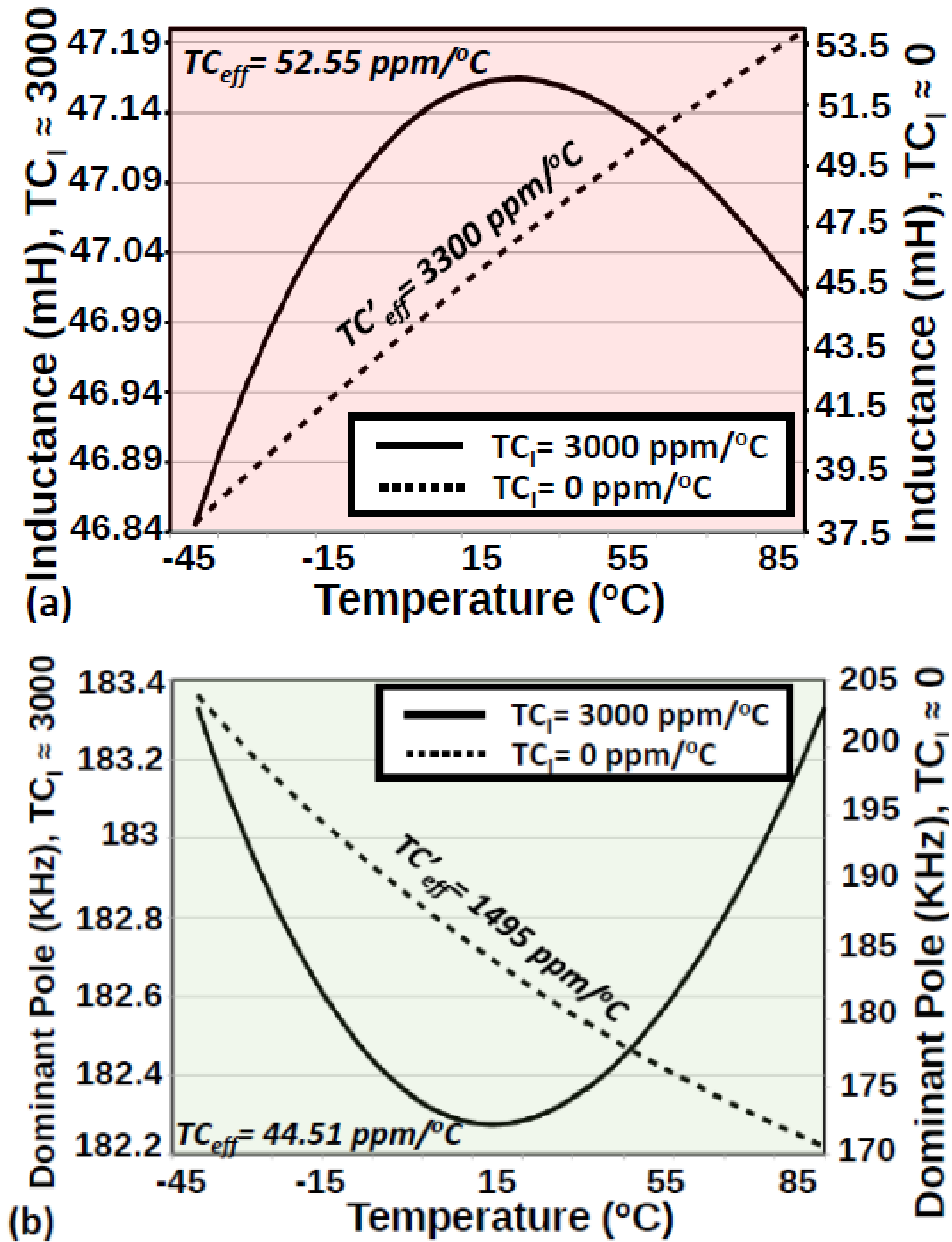


Figure 4.28: (a) Equivalent Inductance vs. Temperature (b) Dominant Pole vs. Temperature.

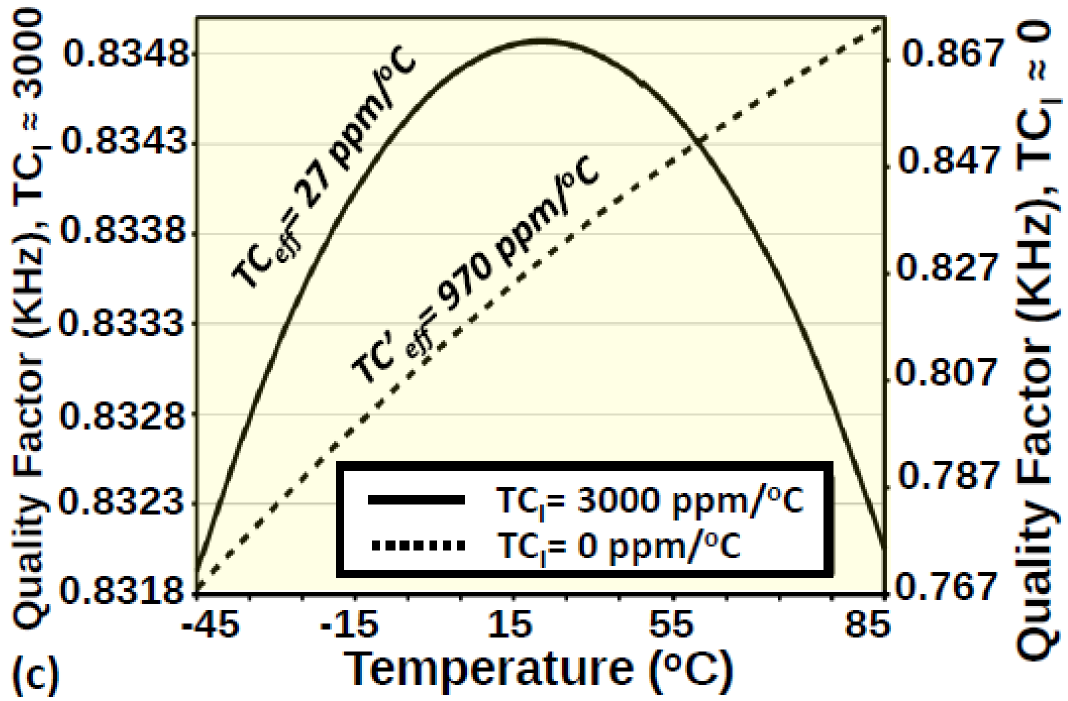


Figure 4.29: Quality Factor vs. Temperature.

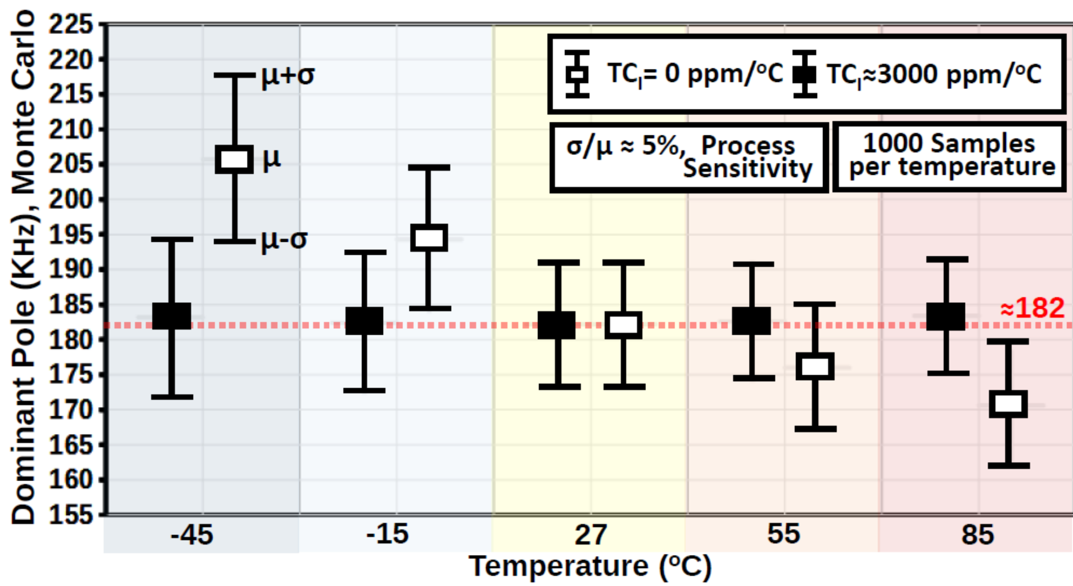


Figure 4.30: Dominant pole Monte Carlo simulations for a temperature range of -45 to 85^oC. For each temperature (-45,-15, 27, 55 and 85 ^oC), 1000 samples were performed.

5 CONCLUSION

This thesis presented a new approach for CMOS analog design with low temperature sensitivity, specifically those that will operate in high-performance SoC solution where changes in temperature inside the chip have a huge swing range. MOSFET ZTC and GZTC conditions were investigated, modeled and used as references to develop a group of application circuits to support the approach. The circuits were: two ZTC-based current references, two ZTC-based voltage reference, and four classical Gm-C filters biased at GZTC bias point.

Both operation conditions, ZTC, and GZTC were analyzed using a MOSFET model that is continuous from weak to strong inversion. In current literature, such modelings can be found only for strong inversion regime. In proposed ZTC and GZTC modeling, their process dependence was detailed, demonstrating that these conditions always occur from moderate to strong inversion operation in any CMOS fabrication process. It is worth mentioning that in modern CMOS technologies, like CMOS 22 nm, both biasing points are still available [WOLPERT; AMPADU (2012)], allowing the analog designer to employ them as a design strategy.

Two current references were devised taking advantage of the ZTC modeling: a self-biased current reference and a resistorless switched-capacitor current reference. The former was designed for an average current of 5 μA at room temperature under a power supply higher than 1.4 V. Post-layout simulation for typical device parameters resulted in effective temperature coefficient of 15 ppm/^{o}C from -40 to $+85^o$C. A maximum of 100 ppm/^{o}C for the same temperature range is achieved considering process and mismatch variability effects. The latter was designed for a reference current of 5.88 μA under a supply voltage of 1.8 V, occupying a silicon area around $0.010mm^2$. Results from post-layout circuit simulation show an effective temperature coefficient (TC_{eff}) of 60 ppm/^{o}C from -45 to +85 ^{o}C and a power consumption of 63 μW. Monte-Carlo simulation over 100 runs, including average process and mismatch effects, indicates a standard deviation of the output current about 324 nA, and an average TC_{eff} of 116 ppm/^{o}C. 88% of the samples had a TC_{eff} lower than 200 ppm/^{o}C.

Also, more two new voltage references were proposed, exploring the ZTC bias condition as a design option. The EMI resisting MOSFET-Only voltage reference achieved a high immunity to conducted EMI (A maximum DC shift and peak-to-peak ripple of -1.7 $\%$ and 35.8m V_{pp} for a 4 dBm EMI injection, respectively). The Temperature Coefficient was 146 ± 9.7 ppm/^{o}C. For the 0.5 V power supply Schottky-diode-based, voltage reference, instead of bipolar junction diodes, Schottky diodes were proved to help reduce the supply voltage reduction of a PTAT current source. The current is used to bias a diode-connected MOS transistor in the vicinity of the ZTC point. This second proposed voltage reference circuit was designed for the three threshold voltage MOSFETs available in the

IBM 130 nm CMOS process ('standard-V_T', 'low-V_T' and 'zero-V_T'). resulting nominal reference voltages of 312 mV, 237 mV and 51 mV with TCs of 214 ppm/°C, 372 ppm/°C, and 953 ppm/°C, respectively. Temperature ranged from -55 to +125°C. The total power consumption of design is just 5.9 μW, at least ten times lower when compared to the other Schottky-diode implementations found in the literature. Therefore, the proposed topology shows that Schottky-diode-based voltage references in CMOS offer a promising alternative for the design of ultra-low voltage references. Both voltage references were fabricated and measurements will be done as soon as possible.

Finally, the interrelationship between the ZTC and GZTC conditions proved to be promising to make low temperature sensitivity MOSFET transconductance. Recalling that it is inserted into a large variety of analog/RF circuits, the GZTC technique is very effective to make temperature independent Analog/RF circuits. Such as filters, multipliers, oscillators, and amplifiers. As a proof-of-concept, some example circuits were presented and designed using the GZTC technique. These were a single-ended resistor emulator, an impedance converter, a first order, and a second order filter in a 130 nm CMOS commercial process. They presented improved stability with varying temperature in their key performance parameters, from 27 ppm/^{o}C to 53 ppm/^{o}C.

Comparisons with state of the art circuits are sometimes difficult because of the scarcity of data, especially regarding variability results. The best was done to provide a fair comparison for each proposed reference. Whereas for the GZTC-Filters, just an initial investigation was performed. It is fair to say that the presented modeling has the potential to improve the analog design methodology significantly when taking into account variations of temperature in the design flow. These claims are backed by thorough simulation results presented in this thesis.

5.1 Future Work

There is certainly much work to do in both areas: ZTC modeling and circuit design using the ZTC bias condition. Chiefly for the GZTC bias point since there is a broad range of circuits that have high dependence of the transconductance in its main performances. The author list below some possible improvements to address in futures works.

ZTC modeling focused on analog design:

- The author used both presented modelings as the design guide for initial hand calculation which served as input to the EDA environment. However, no comparison between the proposed modeling and experimental data was conducted to analyze how reliable the modeling is. This result would be appreciable for design purpose.
- Investigation of second-order effects exactly on ZTC and GZTC point. This subject remains poorly explained in the current literature. Fig. 5.1 shows the zoomed on ZTC point, and deviation dependent on temperature is visible.

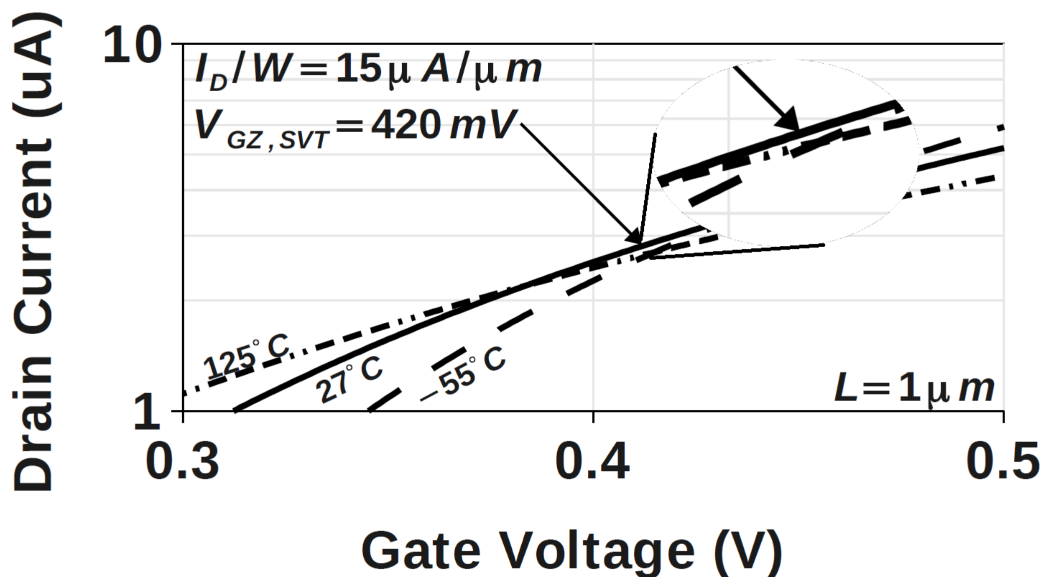


Figure 5.1: Second order effects on ZTC bias point

- Fig. 5.2shows the ZTC bias point as a function of channel length. Owing to the continuous scaling of CMOS devices, short channel effects are present in the MOS transistor and, consequently, also evident in the ZTC point. No ZTC modeling taking into account short channel effects was found in the literature.

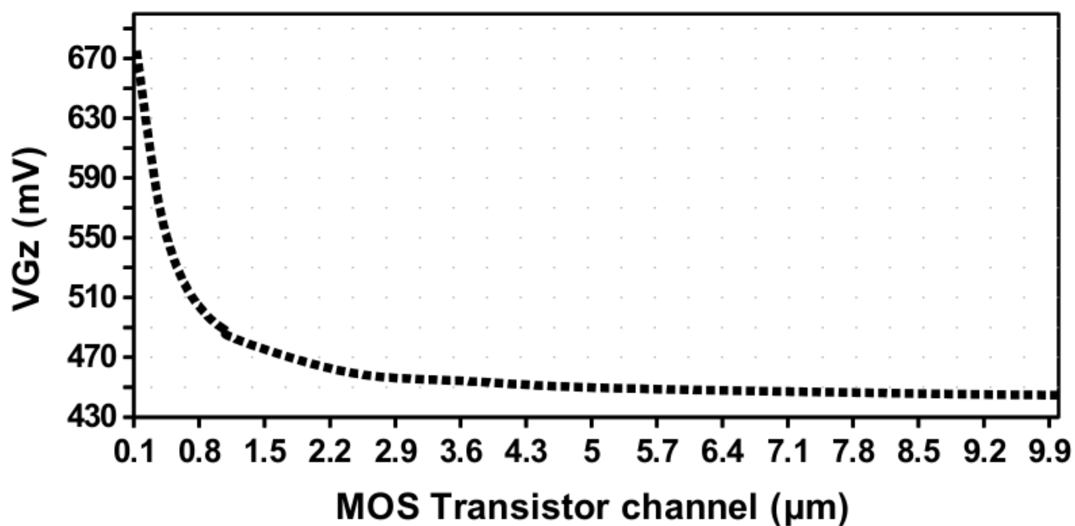


Figure 5.2: Short channel effects on ZTC bias point

- There is no relationship found in the literature between ZTC point and Digital ZTC; both exploited in section 2.3. Knowing the ZTC points of PMOS and NMOS transistor, would it be possible to predict the required V_{DD} in order to make the inverter delay independent of temperature?
- Another interesting modeling regards the ZTC found in MOS Capacitance. In section 2.3, it also was shown that there are two ZTC points at MOS capacitor. One in accumulation regime and another in depletion regime. A particular design could benefit from a capacitor with low temperature dependence applying the two points.

- This thesis did not cover, but there is also a ZTC point in the triode resistance of MOS transistor. As in the case of the MOS capacitor, this behavior could also be explored in a design application. Therefore, modeling of ZTC triode resistance becomes worthwhile.

Circuit design using ZTC modelings:

- New topologies for voltage and current reference circuits can be investigated and developed.
- GZTC bias point remains unexplored in CMOS Analog/RF design. This bias point can be an application to a large variety of circuits where MOSTFET transconductance plays a fundamental role in their performances. Notable examples are Capacitor-Less Low Drop Out (CL-LDO) [TORRES et al. (2014)] and Low Noise Transcoductance Amplifier (LNTA) [GEDDADA et al. (2014)].
- It would be very interesting to analyze how would be the impact of radiation effects on ZTC references proposed here. This may informs how immune the ZTC point is in respect to radiation interference.

REFERENCES

ABESINGHA, B.; RINCON-MORA, G.; BRIGGS, D. Voltage shift in plastic-packaged bandgap references. **Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on**, [S.l.], v.49, n.10, p.681–685, Oct 2002.

ALL, N. P. et. **BSIM4 v4.8.0 MOSFET Model, User's Manual**. 2013.

ALLEN, P. **"CMOS Analog Circuit Design"**. [S.l.]: The Oxford Series in Electrical and Computer Engineering, 2011.

BAKER, R. J. **CMOS Circuit Design, Layout, and Simulation, Second Edition**. [S.l.]: Wiley-IEEE Press, 2004.

BANBA, H. et al. "A CMOS Bandgap Reference Circuit with Sub-1-V Operation". **IEEE J. Solid-State Circuits**, [S.l.], v.SC-6, n.1, p.2–7, Feb 1999.

BAZIGOS, A. et al. An Adjusted Constant-Current Method to Determine Saturated and Linear Mode Threshold Voltage of MOSFETs. **Electron Devices, IEEE Transactions on**, [S.l.], v.58, n.11, p.3751–3758, Nov 2011.

BELLAOUAR, A. et al. Supply voltage scaling for temperature insensitive CMOS circuit operation. **Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on**, [S.l.], v.45, n.3, p.415–417, Mar 1998.

BENDALI, A.; AUDET, Y. "A 1-V CMOS current reference with temperature and process compensation". **IEEE Trans. Circuits Syst.**, [S.l.], v.54, n.2, p.1424–1429, 2007.

BINKLEY, D. Tradeoffs and Optimization in Analog CMOS Design. In: MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, 2007. MIXDES '07. 14TH INTERNATIONAL CONFERENCE ON, 2007. **Anais...** [S.l.: s.n.], 2007. p.47–60.

BUCHER, M.; LALLEMENT, C.; ENZ, C. C. "An Efficient Parameter Extraction Methodology for the EKV MOST Model". **Conference on Microelectronic Test Structures.**, [S.l.], v.9, n.1, p.145–150, March 1996.

BURCEA, T. Mathematic Relations And Procedure For Designing A Zenner Voltage Stabilizer. **Industrial Electronics and Control Instrumentation, IEEE Transactions on**, [S.l.], v.IECI-24, n.3, p.258–268, Aug 1977.

BUTLER, D.; JACOB BAKER, R. Low-voltage bandgap reference design utilizing Schottky diodes. In: CIRCUITS AND SYSTEMS, 2005. 48TH MIDWEST SYMPOSIUM ON, 2005. **Anais...** [S.l.: s.n.], 2005. p.1794–1797 Vol. 2.

CAMACHO-GALEANO, E.; GALUP-MONTORO, C.; SCHNEIDER, C. "A 2-nW 1.1-V self-biased current reference in CMOS technology". **IEEE Trans. Circuits Syst. II**, [S.l.], v.52, n.2, p.61–65, 2005.

CHIAH, S. B.; ZHOU, X.; YUAN, L. Compact Zero-Temperature Coefficient Modeling Approach for MOSFETs Based on Unified Regional Modeling of Surface Potential. **Electron Devices, IEEE Transactions on**, [S.l.], v.60, n.7, p.2164–2170, July 2013.

COLOMBO, D. M.; WIRTH, G.; BAMPI, S. Sub-1 V band-gap based and MOS threshold-voltage based voltage references in 0.13 μm CMOS. **Analog Integrated Circuits and Signal Processing**, [S.l.], v.82, n.1, p.25–37, 2015.

CORDOVA, D. et al. EMI Resisting MOSFET-Only Voltage Reference Based on the ZTC Condition. In: NEW CIRCUITS AND SYSTEMS CONFERENCE (NEWCAS), 2015 IEEE 11TH INTERNATIONAL, 2015. **Anais...** [S.l.: s.n.], 2015. p.1–4.

CORDOVA, D. et al. 0.5 V Supply Voltage Reference Based on the MOSFET ZTC Condition. In: SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN, 28., 2015, New York, NY, USA. **Proceedings...** ACM, 2015. p.9:1–9:7. (SBCCI '15).

CORDOVA, D.; TOLEDO, P.; FABRIS, E. A low-voltage current reference with high immunity to EMI. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2014 27TH SYMPOSIUM ON, 2014. **Anais...** [S.l.: s.n.], 2014. p.1–6.

CUNHA, A.; SCHNEIDER, M.; GALUP-MONTORO, C. An MOS transistor model for analog circuit design. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.33, n.10, p.1510–1519, Oct 1998.

DASDAN, A.; HOM, I. Handling Inverted Temperature Dependence in Static Timing Analysis. **ACM Trans. Des. Autom. Electron. Syst.**, New York, NY, USA, v.11, n.2, p.306–324, Apr. 2006.

DEFENSE, U. D. of. **Integrated circuits manufacturing, general specification, std MILPRF38535H.** [S.l.: s.n.], 2012.

ENZ, C.; KRUMMENACHER, F.; VITTOZ, E. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. **Analog Integrated Circuits and Signal Processing**, [S.l.], v.8, n.1, p.83–114, 1995.

FARADAY, M. **"Experimental researches in electricity."**. 1st.ed. [S.l.]: Bernard Quaritch, London, 1839.

FILANOVSKY, I.; ALLAM, A. Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits. **Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on**, [S.l.], v.48, n.7, p.876–884, Jul 2001.

FILANOVSKY, I.; BAI, B.; MOORE, B. A CMOS voltage reference using compensation of mobility and threshold voltage temperature effects. In: CIRCUITS AND SYSTEMS, 2009. MWSCAS '09. 52ND IEEE INTERNATIONAL MIDWEST SYMPOSIUM ON, 2009. **Anais...** [S.l.: s.n.], 2009. p.29–32.

FIORI, F.; CROVETTI, P. "A new compact temperature-compensated CMOS current reference". **IEEE Trans. Circuits Syst. II**, [S.l.], v.52, n.11, p.724–728, 2005.

FRUETT, F.; MEIJER, G.; BAKKER, A. Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.38, n.7, p.1288–1291, July 2003.

GALUP-MONTORO, C. et al. A compact model of MOSFET mismatch for circuit design. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.40, n.8, p.1649–1657, Aug 2005.

GEDDADA, H. et al. Wide-Band Inductorless Low-Noise Transconductance Amplifiers With High Large-Signal Linearity. **Microwave Theory and Techniques, IEEE Transactions on**, [S.l.], v.62, n.7, p.1495–1505, July 2014.

GEIGER, R.; SANCHEZ-SINENCIO, E. Active filter design using operational transconductance amplifiers: a tutorial. **Circuits and Devices Magazine, IEEE**, [S.l.], v.1, n.2, p.20–32, March 1985.

GILBERT, W. **"De magnete"**. [S.l.]: Peter Short, London, 1600.

GIUSTOLISI, G.; PALUMBO, G. A detailed analysis of power-supply noise attenuation in bandgap voltage references. **Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on**, [S.l.], v.50, n.2, p.185–197, Feb 2003.

GOPAL, H.; BAGHINI, M. Trimless, PVT Insensitive Voltage Reference Using Compensation of Beta and Thermal Voltage. In: VLSI DESIGN AND 2014 13TH INTERNATIONAL CONFERENCE ON EMBEDDED SYSTEMS, 2014 27TH INTERNATIONAL CONFERENCE ON, 2014. **Anais...** [S.l.: s.n.], 2014. p.528–533.

GOULD, C. et al. "A comprehensive reviewer of thermoelectric technology, microelectrical and power generation properties". **26th Int Conf in Microelectronics.**, [S.l.], p.329–332, 2008.

IBM. **RF/CMOS Design Kit**. 2011.

KINGET, P. Designing analog and RF circuits for ultra-low supply voltages. In: SOLID STATE CIRCUITS CONFERENCE, 2007. ESSCIRC 2007. 33RD EUROPEAN, 2007. **Anais...** [S.l.: s.n.], 2007. p.58–67.

KINGET, P.; CHATTERJEE, S.; TSIVIDIS, Y. Ultra-Low Voltage Analog Design Techniques for Nanoscale CMOS Technologies. In: ELECTRON DEVICES AND SOLID-STATE CIRCUITS, 2005 IEEE CONFERENCE ON, 2005. **Anais...** [S.l.: s.n.], 2005. p.9–14.

KINGET, P. et al. Voltage references for ultra-low supply voltages. In: CUSTOM INTEGRATED CIRCUITS CONFERENCE, 2008. CICC 2008. IEEE, 2008. **Anais...** [S.l.: s.n.], 2008. p.715–720.

KLIMACH, H. et al. "Resistorless switched-capacitor bandgap voltage reference with low sensitivity to process variations". **Electronics Letters**, [S.l.], v.49, p.1448–1449, 2013.

KLIMACH, H. et al. A resistorless switched bandgap voltage reference with offset cancellation. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2013 26TH SYMPOSIUM ON, 2013. **Anais...** [S.l.: s.n.], 2013. p.1–5.

KOZIEL, S.; SZCZEPANSKI, S. Design of highly linear tunable CMOS OTA for continuous-time filters. **Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on**, [S.l.], v.49, n.2, p.110–122, Feb 2002.

KUMAR, R.; KURSUN, V. Reversed Temperature-Dependent Propagation Delay Characteristics in Nanometer CMOS Circuits. **Circuits and Systems II: Express Briefs, IEEE Transactions on**, [S.l.], v.53, n.10, p.1078–1082, Oct 2006.

KUNDERT, K. Introduction to RF simulation and its application. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.34, n.9, p.1298–1319, Sep 1999.

LIU, C.-P.; HUANG, H.-P. A CMOS Voltage Reference with Temperature Sensor using Self-PTAT Current Compensation. In: SOC CONFERENCE, 2005. PROCEEDINGS. IEEE INTERNATIONAL, 2005. **Anais...** [S.l.: s.n.], 2005. p.37–42.

LIU, W.; KUSSENER, E. "A resistor-Free Temperature-Compensated CMOS Current Reference". **Proceedings IEEE International Symposium on Circuits and Systems**, [S.l.], p.845–848, 2010.

LOPEZ-MARTIN, A. et al. Low-Voltage Super class AB CMOS OTA cells with very high slew rate and power efficiency. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.40, n.5, p.1068–1077, May 2005.

LUKASZEWICZ, M.; BOREJKO, T.; PLESKACZ, W. "A Resistorless Current Reference Source for 65 nm CMOS Technology with Low Sensitivity to Process, Supply Voltage and Temperature Variations". **Proceedings IEE International Symposium on Design and Diagnostics of Eletronic Circuit and System**, [S.l.], p.75–79, April 2011.

MAKRIS, N.; BUCHER, M. Temperature scaling of CMOS analog design parameters. In: ELECTROTECHNICAL CONFERENCE (MELECON), 2012 16TH IEEE MEDITERRANEAN, 2012. **Anais...** [S.l.: s.n.], 2012. p.187–190.

MALCOVATI, P. et al. "Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage". **IEEE J. Solid-State Circuits**, [S.l.], v.36, p.1076–1081, July 2001.

MATTIA, O. E.; KLIMACH, H.; BAMPI, S. 2.3 Ppm/oC 40 nW MOSFET-only Voltage Reference. In: INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN, 2014., 2014, New York, NY, USA. **Proceedings...** ACM, 2014. p.215–220. (ISLPED '14).

MATTIA, O.; KLIMACH, H.; BAMPI, S. 0.7 V supply, 8 nW, 8 ppm/oC resistorless sub-bandgap voltage reference. In: CIRCUITS AND SYSTEMS (MWSCAS), 2014 IEEE 57TH INTERNATIONAL MIDWEST SYMPOSIUM ON, 2014. **Anais...** [S.l.: s.n.], 2014. p.479–482.

MATTIA, O.; KLIMACH, H.; BAMPI, S. 0.9 V, 5 nW, 9 ppm/oC resistorless sub-bandgap voltage reference in 0.18 um CMOS. In: CIRCUITS AND SYSTEMS (LASCAS), 2014 IEEE 5TH LATIN AMERICAN SYMPOSIUM ON, 2014. **Anais...** [S.l.: s.n.], 2014. p.1–4.

MATTIA, O.; KLIMACH, H.; BAMPI, S. Sub-1 V supply 5 nW 11 ppm/°C resistorless sub-bandgap voltage reference. **Analog Integrated Circuits and Signal Processing**, [S.l.], p.1–9, 2015.

MUNEDA. **www.muneda.com**. 2015.

NAJAFIZADEH, L.; FILANOVSKY, I. A simple voltage reference using transistor with ZTC point and PTAT current source. In: CIRCUITS AND SYSTEMS, 2004. ISCAS '04. PROCEEDINGS OF THE 2004 INTERNATIONAL SYMPOSIUM ON, 2004. **Anais...** [S.l.: s.n.], 2004. v.1, p.I–909–11 Vol.1.

NARENDRA, S.; FUJINO, L.; SMITH, K. Through the Looking Glass - The 2015 Edition: trends in solid-state circuits from isscc. **Solid-State Circuits Magazine, IEEE**, [S.l.], v.7, n.1, p.14–24, winter 2015.

OJALA, P.; KASKI, K. Analytically extracted ZTC point for GaAs MESFET. **Circuits, Devices and Systems, IEE Proceedings G**, [S.l.], v.140, n.6, p.424–430, Dec 1993.

OSMAN, A. et al. Zero-temperature-coefficient biasing point of partially depleted SOI MOSFET's. **Electron Devices, IEEE Transactions on**, [S.l.], v.42, n.9, p.1709–1711, Sep 1995.

PARK, C. et al. Reversal of temperature dependence of integrated circuits operating at very low voltages. In: ELECTRON DEVICES MEETING, 1995. IEDM '95., INTERNATIONAL, 1995. **Anais...** [S.l.: s.n.], 1995. p.71–74.

PELTIER, J. **"Investigation of the heat developed by electric currents in homogeneous materials and at the junction of two different conductors."**. [S.l.: s.n.], 1834.

PRIJIC, Z.; DIMITRIJEV, S. S.; STOJADINOVIC, N. "The determination of zero temperature coefficient point in CMOS transistor". **Microelectron. Reliab.**, [S.l.], v.32, n.6, p.769–773, 1992.

REDOUTE, J.-M.; STEYAERT, M. Current mirror structure insensitive to conducted EMI. **Electronics Letters**, [S.l.], v.41, n.21, p.1145–1146, Oct 2005.

REDOUTE, J.; STEYAERT, M. Kuijk Bandgap Voltage Reference With High Immunity to EMI. **Circuits and Systems II: Express Briefs, IEEE Transactions on**, [S.l.], v.57, n.2, p.75–79, Feb 2010.

REDOUTE, J.; STEYAERT, M. **EMC of Analog Integrated Circuits**. [S.l.]: Springer, 2010.

SATO, T. et al. On-chip thermal gradient analysis and temperature flattening for SoC design. In: DESIGN AUTOMATION CONFERENCE, 2005. PROCEEDINGS OF THE ASP-DAC 2005. ASIA AND SOUTH PACIFIC, 2005. **Anais...** [S.l.: s.n.], 2005. v.2, p.1074–1077 Vol. 2.

SCHNEIDER, C.; GALUP-MONTORO, C. **CMOS Analog Design Using All-Region MOSFET Modeling**. 1st.ed. [S.l.]: Cambridge University Press, 2010.

SEEBECK, T. **"Magnetische polarization der metalle und erze durch temperature-differenzen."**. [S.l.]: Akad Berlin, 1840.

SEMICONDUCTOR, I. H. **http**://www.investopedia.com/features/industryhandbook/semiconductor.asp. 2015.

SERRA-GRAELLS, F.; HUERTAS, J. Sub-1-V CMOS proportional-to-absolute temperature references. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.38, n.1, p.84–88, Jan 2003.

SHOUCAIR, F. Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors. **Electronics Letters**, [S.l.], v.25, n.17, p.1196–1198, Aug 1989.

SILVA PIOVANI, D. E.; SCHNEIDER, M. Design of a Temperature-Compensated Voltage Reference based on the MOSFET Threshold Voltage. In: SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEM DESIGN (SBCCI 11), BRAZIL, 24., 2011. **Anais. . .** [S.l.: s.n.], 2011. p.39–43.

SMITH, E.; CO. **"The collected works of Sir Humphry Davy"**. [S.l.]: Peter Short, London, 1840.

STANDARD, I. . [S.l.]: Measurement of E/M Immunity 150kHz to 1GHz – Part 4: Direct Power Injection Method, 2004. IEC62132-4. (Ed.1:ICs).

SZE, M. **Physics of Semiconductor Device**. [S.l.]: Wiley, 1981.

TALEBBEYDOKHTI, N. et al. "Constant Transconductance Bias Circuit with an On-Chip Resistor". **Proceedings IEEE International Symposium on Circuits and Systems**, [S.l.], p.2857–2860, May 2006.

TOLEDO, P. et al. Self-biased CMOS current reference based on the ZTC operation condition. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2014 27TH SYMPOSIUM ON, 2014. **Anais. . .** [S.l.: s.n.], 2014. p.1–7.

TOLEDO, P. et al. Resistorless Self-Biased ZTC Switched Capacitor Current Reference. In: LASCAS 2015 - IEEE LATIN AMERICAN SYMPOSIUM ON CIRCUITS AND SYSTEM, 2015. **Anais. . .** [S.l.: s.n.], 2015. p.1–4.

TOLEDO, P. et al. CMOS Transconductor Analysis for Low Temperature Sensitivity Based on ZTC MOSFET Condition. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2015 28TH SYMPOSIUM ON, 2015. **Anais. . .** [S.l.: s.n.], 2015. p.1–7.

TORRES, J. et al. Low Drop-Out Voltage Regulators: capacitor-less architecture comparison. **Circuits and Systems Magazine, IEEE**, [S.l.], v.14, n.2, p.6–26, Secondquarter 2014.

TSCHANZ, J. et al. Adaptive Frequency and Biasing Techniques for Tolerance to Dynamic Temperature-Voltage Variations and Aging. In: SOLID-STATE CIRCUITS CONFERENCE, 2007. ISSCC 2007. DIGEST OF TECHNICAL PAPERS. IEEE INTERNATIONAL, 2007. **Anais. . .** [S.l.: s.n.], 2007. p.292–604.

TSIVIDIS, Y.; CZARNUL, Z.; FANG, S. MOS transconductors and integrators with high linearity. **Electronics Letters**, [S.l.], v.22, n.5, p.245–246, February 1986.

TSIVIDIS, Y.; MCANDREW, C. **Operation and Modeling of the MOS Transistor**. 3rd.ed. [S.l.]: Oxford, 2010.

WANG, K.-T.; LIN, W.-C.; CHAO, T.-S. The Zero-Temperature-Coefficient Point Modeling of DTMOS in CMOS Integration. **Electron Device Letters, IEEE**, [S.l.], v.31, n.10, p.1071–1073, Oct 2010.

WICKED, M. **Wicked Design Flow**. 2013.

WIDLAR, R. "New developments in IC voltage regulators". **IEEE J. Solid-State Circuits.**, [S.l.], v.6, n.1, p.2–7, Feb 1971.

WOLPERT, D.; AMPADU, P. **"Managing Temperature Effects in Nanoscale Adaptive Systems"**. [S.l.]: Springer, 2012.

YOO, C.; PARK, J. "CMOS current reference with supply and temperature compensation". **Electronics Letters**, [S.l.], v.43, n.25, December 2007.

LIST OF PUBLICATIONS

Publications regarding the thesis subject:

1. **TOLEDO, P.** ; KLIMACH, H. ; CORDOVA, D. ; BAMPI, S. ; FABRIS, E. "Low Temperature Sensitivity CMOS Transconductor Based on GZTC MOSFET Condition" **JICS - Journal of Integrated Circuits and Systems** (Ed. Português) , 2016. (under review)
2. CORDOVA, D. ; **TOLEDO, P.** ; KLIMACH, H. ; BAMPI, S. ; FABRIS, E. "A More Complete ZTC Condition Analysis for a 0.5 V Schottky-based Voltage Reference" **JICS - Journal of Integrated Circuits and Systems** (Ed. Português) , 2016. (under review)
3. CORDOVA, D. ; **TOLEDO, P.** ; KLIMACH, H. ; BAMPI, S. ; FABRIS, E. "EMI Resisting MOSFET-Only Voltage Reference Based on the ZTC Condition. [Extended Version]" **AICSP - Analog Integrated Circuits and Signal Processing**, 2016. (under review)
4. **TOLEDO, P.** ; KLIMACH, H. ; CORDOVA, D. ; BAMPI, S. ; FABRIS, E. "MOSFET ZTC Condition Analysis for a Self-biased Current Reference Design" **JICS - Journal of Integrated Circuits and Systems** (Ed. Português) , 2015.
5. **TOLEDO, P.** ; KLIMACH, H. ; CORDOVA, D. ; BAMPI, S. ; FABRIS, E. "CMOS Transconductor Analysis for Low Temperature Sensitivity Based on ZTC MOSFET Condition" In: the 28th Symposium, 2015, Salvador. **Proceedings of the 28th Symposium on Integrated Circuits and Systems Design - SBCCI '15**.
6. CORDOVA, D. ; **TOLEDO, P.** ; KLIMACH, H. ; BAMPI, S. ; FABRIS, E. "0.5 V Supply Voltage Reference Based on the MOSFET ZTC Condition" In: the 28th Symposium, 2015, Salvador. **Proceedings of the 28th Symposium on Integrated Circuits and Systems Design - SBCCI '15**.
7. **TOLEDO, P.** ; KLIMACH, H. ; CORDOVA, D. ; BAMPI, S. ; FABRIS, E. . "Resistorless Switched-Capacitor Current Reference Based on the MOSFET ZTC Condition." In: **6th IEEE Latin American Symposium on Circuits and Systems**, 2015, Montevideo, Uruguay. 6th IEEE Latin American Symposium on Circuits and Systems, 2015.
8. CORDOVA, D. ; **TOLEDO, P.** ; KLIMACH, H. ; BAMPI, S. ; FABRIS, E. "EMI Resisting MOSFET-Only Voltage Reference Based on the ZTC Condition." In: **Proceedings of the 13th IEEE International NEW Circuits And Systems (NEWCAS) conference**, 2015, Grenoble. 13th IEEE International NEW Circuits And Systems (NEWCAS) conference, 2015.
9. **TOLEDO, P.** ; KLIMACH, H. ; CORDOVA, D. ; BAMPI, S. ; FABRIS, E. "Self-biased CMOS Current Reference based on the ZTC Operation Condition". In: the

27th Symposium, 2014, Aracaju. **Proceedings of the 27th Symposium on Integrated Circuits and Systems Design - SBCCI '14**. p. 1.

10. CORDOVA, D. ; **TOLEDO, P.** ; FABRIS, E. "A Low-Voltage Current Reference with High Immunity to EMI". In: the 27th Symposium, 2014, Aracaju. **Proceedings of the 27th Symposium on Integrated Circuits and Systems Design - SBCCI '14**. p. 1.

Publications about other topics but published during Master's Degree period:

1. NEGREIROS M., CORDOVA D., RECKZIEGEL E., PARIS L;, GUEX J., **TOLEDO P.** and FABRIS E. "System-Level Analysis for a New SBCD Transponder SoC". In: **5th Workshop on Circuits and System Design**, 2015, Salvador. 5th Workshop on Circuits and System Design, 2015. (accepted for publication)
2. NEGREIROS, M. ; **TOLEDO, P.** ; FABRIS, E. ; CORDOVA, D. ; PARIS, L. ; GUEX, J.; RECKZIEGEL, E. . "A New DSP-Based Satellite Transponder SoC for the Brazilian System of Data". In: **52nd Design Automation Conference**, 2015, San Francisco. IP Design Track, 2015.
3. FABRIS, E. ; PARIS, L.; **TOLEDO, P.** ; GUEX, P. ; NEGREIROS, M. ; RECKZIEGEL, E. . "DSP-Based Satellite Transponder SOC." In: **CDNLive EMEA 2015 - Cadence User Conference**, 2015, Munich. CDNLive EMEA 2015 - Cadence User Conference, 2015.
4. PARIS, L. ; **TOLEDO, P.** ; GUEX, P. ; FELLINI, H. ; COSTA, M.; FELIPE, A. ; RECKZIEGEL, E.; OLIVEIRA, T.; FABRIS, E. . "Digital IC Design Flow at IC-Brazil Training Program TC1". In: **XXI Iberchip Workshop on Circuits and Systems**, 2015, Montevideo, Uruguay. XXI Iberchip Workshop on Circuits and Systems, 2015.
5. **TOLEDO, P.**; CAICEDO, J. ; DORNELLAS, H. ; SCHMIDT, A. ; CORDOVA, D. ; SANTANA, D. ; FABRIS, E. " Analog and RF IC Design Training at IC Brazil Program TC 1". In: **4th Workshop on Circuits and System Design**, 2014, Aracaju. 4th Workshop on Circuits and System Design, 2014.
6. FIERRO, G. ; **TOLEDO, P.** ; FERREIRA, S. ; FABRIS, E. . "A 0.18 μm Variable Gain Transimpedance Amplifier for 2.4 GHz IEEE 802.15.4 Direct Conversion Receiver". In: **3th Workshop on Circuits and System Design**, 2013, Curitiba. 3th Workshop on Circuits and System Design, 2013.

APPENDIX A   IMPACT OF TEMPERATURE VARIATIONS ON TWO-STAGE MILLER AMPLIFIER

To exemplify the temperature variations impact on analog circuits, a classical 130 nm CMOS two-stage miller amplifier has been designed and its performances have been investigated under temperature variations. Fig. A.1 shows the used topology. The adopted design methodology was a classical one found in [ALLEN (2011)]. The verification testbenchs can also be found in the same reference [ALLEN (2011)]. As a matter of completeness, table A.1 shows all expected specifications to be fulfilled in this example design.

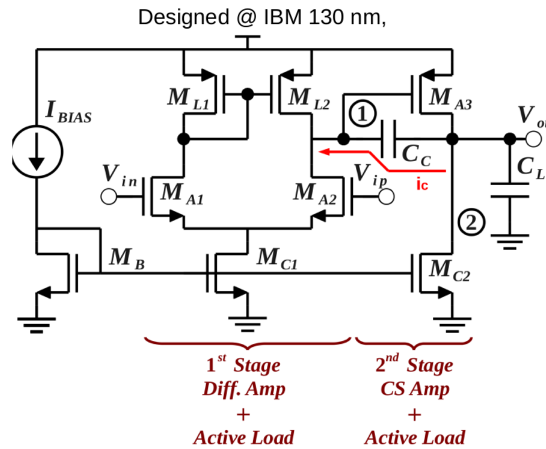


Figure A.1: Classical two-stage Miller amplifier.

Fig. A.2 shows the simulations results for both design approaches: (in black) without worrying about temperature variations and (in red) the ZTC-based design where the ZTC vicinity behavior has been annulled applying a right amount of temperature dependence (TC) in the current bias (I_{BIAS}). The ZTC-based design is well explained in section 2.4.3. In Fig. A.2 (a) and (c), it is visible that using the approach presented in this thesis the GBW and PM thermal sensibilities have been relevantly attenuated. However, two special cases deserve to be commented. The first one is about the total integrated noise, as shown in Fig. A.2 (b). Even demonstrating a lower thermal sensitivity, there is a extra added noise for temperatures below to 27 ^{o}C when compared with previous implementation. The second one and most critical, it is the slew rate lost at temperatures below to 27 ^{o}C. This drawback can be mitigated increasing the power budget.

Table A.1: Miller amplifier specifications

Specifications	Expected Results
Power Supply	VDD = 1.2V; VSS = 0V
Output voltage swing	$Vout_{max}$ = VDD – 0.2V ; Vout_min = 0.2V ;
DC Current Consumption	$<$ 700uA
Unit gain bandwidth (GBW)	$>$ 10 MHz
Slew-rate	$>$ 10 V/μs
Phase Margin (PM)	$>$ 60° for unit gain feedback (-Vin = Vout)
DC or low frequency differential gain	$>$ 50 dB
Common Mode Ratio Rejection (CMRR)	$<$-50 dB
DC input offset	$<$ 150 μV
Integrated Output Noise 100 Hz to 100 KHz	$<$ 100 μV_{RMS}
DC Power Supply Rejection (PSR)	$<$ -55 dB

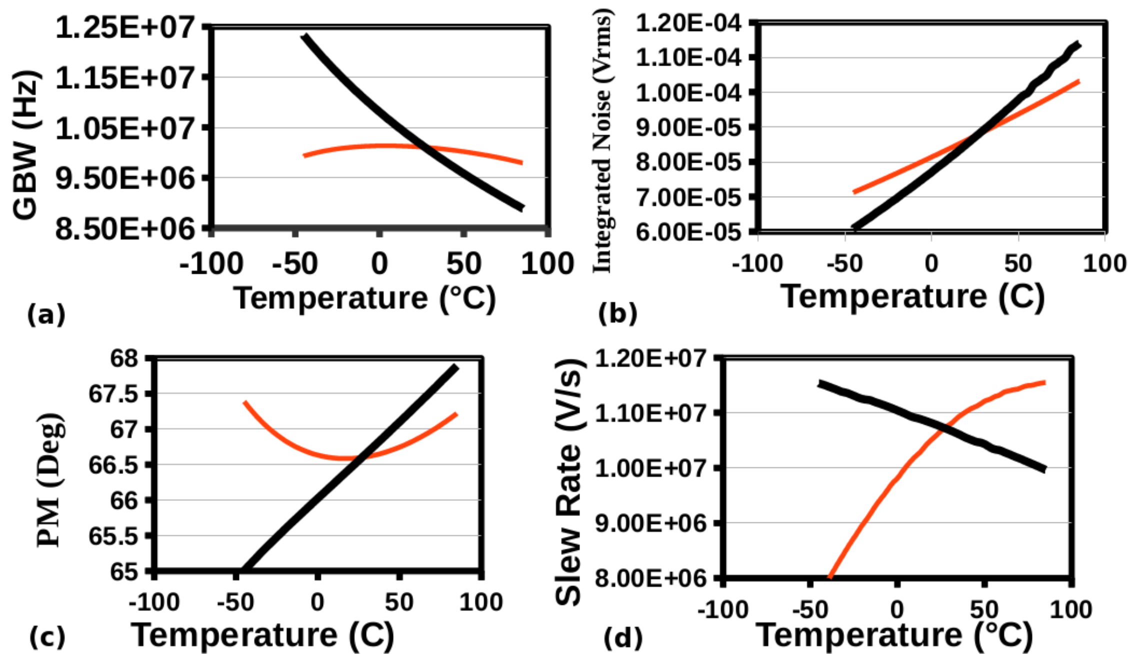


Figure A.2: Miller Amplifier: (a) GBW (b) Integrated Noise (c) PM (d) Slew Rate.

APPENDIX B EXPRESSIONS

Some expressions which were used during the thesis development are derived here.

B.1 $\frac{\partial\mu}{\partial T} = \frac{\mu\alpha_\mu}{T}$

From Eq. (2.32) and repeated below, the low-field mobility dependence on temperature is given by

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{B.1}$$

if one differentiates with respect to temperature, we get

$$\frac{\partial\mu}{\partial T} = \frac{\partial}{\partial T}\left(\mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu}\right) = \frac{\mu(T_0)}{(T_0)^{\alpha_\mu}}\frac{\partial}{\partial T}(T)^{\alpha_\mu} \tag{B.2}$$

As $\frac{\partial}{\partial x}(x^a) = ax^{a-1}$, we get

$$\frac{\partial\mu}{\partial T} = \frac{\alpha_\mu\mu(T_0)}{(T_0)^{\alpha_\mu}}(T)^{\alpha_\mu-1} \tag{B.3}$$

Multiplying both numerator and denominator by temperature (T),

$$\frac{\partial\mu}{\partial T} = \frac{\alpha_\mu\mu(T_0)}{(T_0)^{\alpha_\mu}}(T)^{\alpha_\mu-1}\frac{T}{T} = \frac{\alpha_\mu}{T}\underbrace{\mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu}}_{\mu(T)} \tag{B.4}$$

Then,

$$\frac{\partial\mu}{\partial T} = \frac{\mu\alpha_\mu}{T} \tag{B.5}$$

B.2 $\frac{\partial\phi_t}{\partial T} = \frac{\phi_t}{T}$

Knowing that $\phi_t = \frac{kT}{q}$ [SZE (1981)], its derivative with respect to T is then

$$\frac{\partial\phi_t}{\partial T} = \frac{k}{q} \tag{B.6}$$

Multiplying both numerator and denominator by temperature (T),

$$\frac{\partial\phi_t}{\partial T} = \frac{k}{q}\left(\frac{T}{T}\right) = \frac{\phi_t}{T} \tag{B.7}$$

B.3 $\frac{\partial \phi_t^2}{\partial T} = \frac{2}{T}\phi_t^2$

Knowing that $\phi_t^2 = \left(\frac{kT}{q}\right)^2$ [SZE (1981)], then its derivative with respect to T is

$$\frac{\partial \phi_t^2}{\partial T} = \left(\frac{k}{q}\right)^2 2T \tag{B.8}$$

Multiplying both numerator and denominator by temperature (T),

$$\frac{\partial \phi_t^2}{\partial T} = \left(\frac{k}{q}\right)^2 2T\left(\frac{T}{T}\right) = \left(\frac{2}{T}\right)\underbrace{\left(\frac{kT}{q}\right)^2}_{\phi_t^2} \tag{B.9}$$

Then,

$$\frac{\partial \phi_t^2}{\partial T} = \frac{2}{T}\phi_t^2 \tag{B.10}$$

B.4 GZTC Condition - $(\partial g_{mg})/(\partial T)|_{T=T_1} = 0$

Gate-bulk transconductance is given by Eq. (2.93) and repeated in Eq. (B.11) as a matter of convenience,

$$g_{mg} = \frac{g_{ms}}{n} = \frac{2I_S}{n\phi_t}(\sqrt{1+i_f}-1) \tag{B.11}$$

Applying the condition $(\partial g_{mg})/(\partial T)|_{T=T_1} = 0$ in Eq. (B.11),

$$\frac{\partial g_{mg}}{\partial T} = \left(\frac{2}{n}\right)\frac{\partial}{\partial T}\left(\frac{I_S}{\phi_t}(\sqrt{1+i_f}-1)\right) = 0 \tag{B.12}$$

Replacing I_S, or Eq. (2.17), in Eq (B.12)

$$\frac{\partial g_{mg}}{\partial T} = C'_{ox}\left(\frac{W}{L}\right)\frac{\partial}{\partial T}\left(\mu(T)\phi_t(T)(\sqrt{1+i_f}-1)\right) = 0 \tag{B.13}$$

Or,

$$\frac{\partial g_{mg}}{\partial T} = C'_{ox}\left(\frac{W}{L}\right)\left[\frac{\partial}{\partial T}\left(\mu(T)\phi_t(T)\right)(\sqrt{1+i_f}-1) + \mu(T)\phi_t(T)\frac{\partial}{\partial T}(\sqrt{1+i_f}-1)\right] = 0 \tag{B.14}$$

The term $\frac{\partial}{\partial T}\left(\mu(T)\phi_t(T)\right)$ can be found using Appendix B.1 and B.2,

$$\frac{\partial}{\partial T}\left(\mu(T)\phi_t(T)\right) = \frac{\partial \mu(T)}{\partial T}\phi_t(T) + \frac{\partial \phi_t(T)}{\partial T}\mu(T) = \frac{\mu\alpha_\mu}{T}\phi_t(T) + \frac{\phi_t(T)}{T}\mu(T) \tag{B.15}$$

On the other hand, the term $\frac{\partial}{\partial T}(\sqrt{1+i_f}-1)$ is given by

$$\frac{\partial}{\partial T}(\sqrt{1+i_f}-1) = \left(\frac{1}{2\sqrt{1+i_f}}\right)\frac{\partial i_f}{\partial T} \tag{B.16}$$

where $\frac{\partial i_f}{\partial T}$ is given by Eq. (2.70).

$$\frac{\partial i_f}{\partial T} = (2(\sqrt{1+i_f}+1))$$
$$\left(\frac{|\alpha_{V_{T0}}|}{\phi_t n} - \frac{1}{T}\left(\sqrt{1+i_f} - 2 + ln(\sqrt{1+i_f}-1)\right)\right) \tag{B.17}$$

Substituting Eqs. (B.15) to (B.17) in (B.14) and after some algebra, we get

$$0 = \alpha_\mu(\sqrt{1+i_{fgz}}-1) - 2 +$$
$$\frac{\sqrt{1+i_{fgz}}+1}{\sqrt{1+i_{fgz}}}\left(\frac{|\alpha_{V_{T0}}|q}{nk} + 2 - ln\left(\sqrt{1+i_{fgz}}-1\right)\right) \tag{B.18}$$

which defines the GZTC condition. The i_{fgz} is defined as GZTC forward inversion level.

APPENDIX C OCTAVE SCRIPTS

All scripts used in GNU Octave software for ZTC and GZTC analysis are listed here. More details about each script can be found in comments described at each line of script. Fig. C.1 shows how the script structure is and explains how each part of script connects to another part.

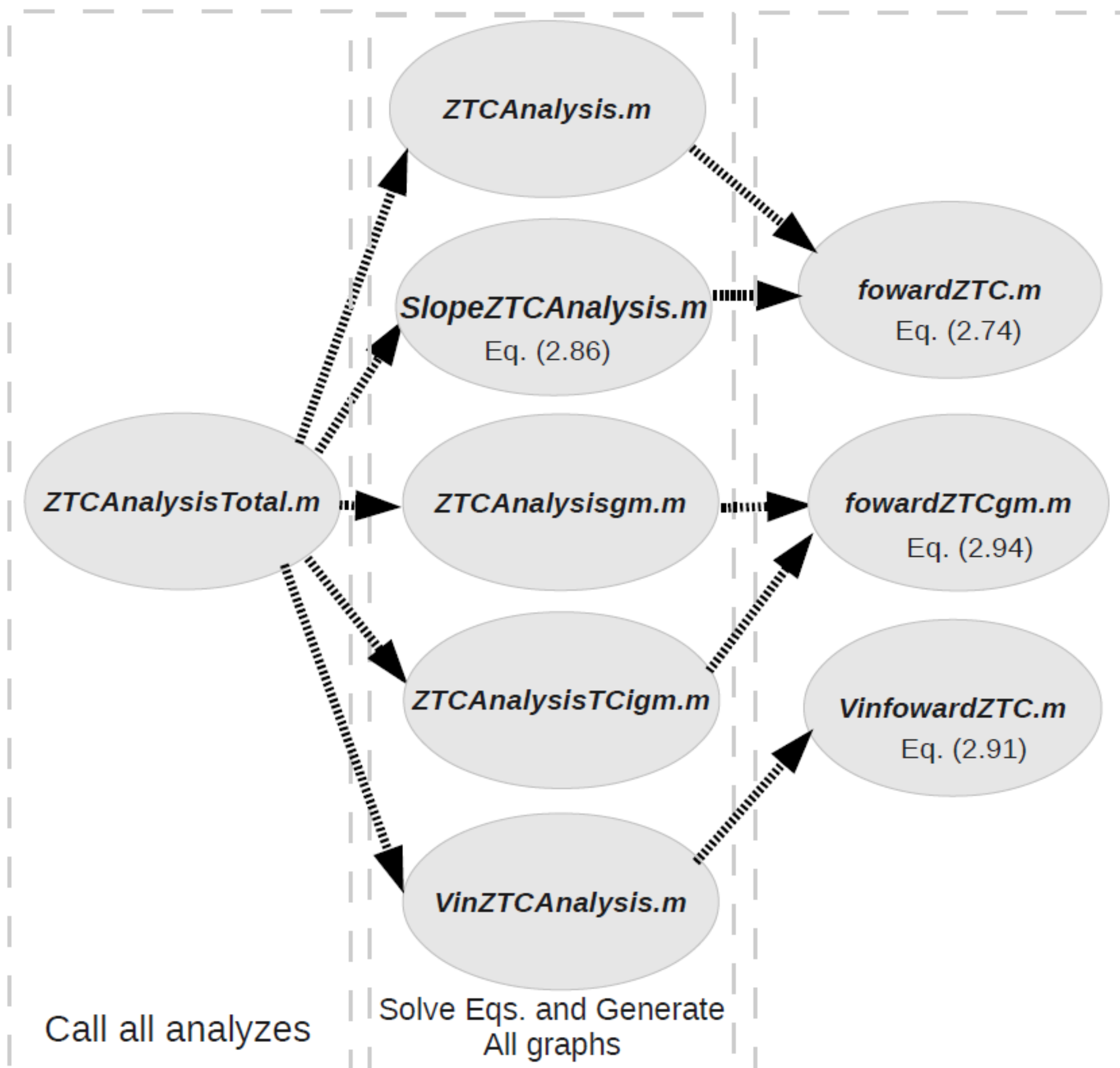


Figure C.1: Script Structure

C.1 ZTCAnalysisTotal.m

Script responsible to call all analyzes together.

```
function ZTCAnalysisTotal

ZTCAnalysis
SlopeZTCAnalysis
ZTCAnalysisgm
ZTCAnalysisTCigm
VinZTCAnalysis

endfunction
```

C.2 ZTCAnalysis.m

Script for ZTC inversion level calculation:

```
function ZTCAnalysis
n = 1.3; % Slope factor used in this estimation.
phi = 26e-3; % Thermal voltage.
avt = [0.5e-3:0.1e-3:3.5e-3]; % temperature dependence of VT
tcu = [-1.5:-0.05:-2.5]; % temperature dependence power coefficient mobility.
tcu2 = tcu; % tcu copy
    % inverting tcu
    for t = 1:length(tcu)
        tcu(t) = tcu2(length(tcu) + 1-t);
    endfor
    % Calculating each solution for Eq. (2.74), or ZTC inversion level.
    for j = 1:length(avt)
        for i = 1:length(tcu)
          i_fztc_vs_tcu(i,j) = fzero(@(ni) fowardZTC(ni,avt(j),tcu(i)),
          15 + i + 5*j);
        endfor
    endfor
%Plotting ZTC forward inversion level vs. avt vs. tcu
grid on
figure(1)
surf(avt,tcu,i_fztc_vs_tcu); colormap([hot]);
grid minor;
set(gca, 'zscale', 'log');
set (gca, "fontsize", 20);
title('Ifztc x avt x tcu');
xlabel('avt');
ylabel('tcu');
zlabel('ifztc');
%Calculating the ZTC overdrive for each ZTC forward inversion level
for j = 1:length(avt)
    for i = 1:length(tcu)
         ZTC_overdrive(i,j) = n*phi*(sqrt(i_fztc_vs_tcu(i,j) +1)
```

```
         - 2 + log(sqrt(i_fztc_vs_tcu(i,j) +1) - 1));
    endfor
endfor
%Plotting ZTC overdrive vs. avt vs. tcu
figure(2)
mesh(avt,tcu,ZTC_overdrive)
grid minor;
set (gca, "fontsize", 20);
title('ZTC Overdrive x avt x tcu');
xlabel('avt');
ylabel('tcu');
zlabel('ZTC Overdrive');
%Calculating ZTC gm/id for each ZTC forward inversion level
for j = 1:length(avt)
    for i = 1:length(tcu)
         ZTC_gm_over_id1(i,j) = 2/(n*phi*(sqrt(i_fztc_vs_tcu(i,j)+1)+1));
    endfor
endfor
%Plotting ZTC gm/id
figure(3)
surf(avt,tcu,ZTC_gm_over_id1)
grid minor;
set (gca, "fontsize", 20);
title('ZTC gm_over_id1 x avt x tcu');
xlabel('avt');
ylabel('tcu');
zlabel('ZTC_gm_over_id1');
ZTC_gm_over_id1(1,1)
endfunction
```

C.3 SlopeZTCAnalysis.m

Script for ZTC slope factor (β_z) calculation:

```
function SlopeZTCAnalysis
n = 1.3; % Slope factor used in this estimation.
phi = 26e-3; % Thermal voltage.
avt = [0.5e-3:0.1e-3:3.5e-3]; % temperature dependence of VT
tcu = [-1.5:-0.05:-2.5]; % temperature dependence power coefficient mobility.
tcu2 = tcu; % tcu copy
    % inverting tcu
    for t = 1:length(tcu)
        tcu(t) = tcu2(length(tcu) + 1-t);
    endfor
    % Calculating the ZTC slope factor
    for j = 1:length(avt)
        i_fztc(j) = fzero(@(ni) fowardZTC(ni,avt(j),-2), 5*j);
        f_i(j) = sqrt(1+i_fztc(j)) - 2 + log(sqrt(1+i_fztc(j)) - 1);
```

```
        b_z(j) = (-1)*((avt(j))/(2*f_i(j)*(sqrt(1+i_fztc(j)) - 1)));
    endfor
%Plotting the ZTC slope factor vs. temperature dependence of VT
grid on
figure(1)
plot(avt,b_z); colormap([hot]);
grid minor;
set (gca, "fontsize", 20);
title('Beta z x avt');
xlabel('avt');
ylabel('Beta z');
endfunction
```

C.4 ZTCAnalysisgm.m

Script for GZTC inversion level calculation:

```
function ZTCAnalysisgm
n = 1.3; % Slope factor used in this estimation.
phi = 26e-3; % Thermal voltage.
avt = [0.5e-3:0.1e-3:3.5e-3]; % temperature dependence of VT
tcu = [-1.5:-0.05:-2.5]; % temperature dependence power coefficient mobility.
tcu2 = tcu; % tcu copy
    % inverting tcu
    for t = 1:length(tcu)
        tcu(t) = tcu2(length(tcu) + 1-t);
    endfor
     % Calculating each solution for Eq. (2.94), or GZTC inversion level.
    for j = 1:length(avt)
        for i = 1:length(tcu)
          i_fztc_vs_tcu(i,j) = fzero(@(ni) fowardZTCgm(ni,avt(j),tcu(i)),
          1 + i + 5*j);
        endfor
    endfor
%Plotting GZTC forward inversion level vs. avt vs. tcu
grid on
figure(1)
surf(avt,tcu,i_fztc_vs_tcu); colormap([hot]);
set(gca, 'zscale', 'log');
set (gca, "fontsize", 20);
title('Ifztc x avt x tcu');
xlabel('avt');
ylabel('tcu');
zlabel('ifztc');
hold on;
%Calculating the GZTC overdrive for each GZTC forward inversion level
    for j = 1:length(avt)
        for i = 1:length(tcu)
```

```
            ZTC_overdrive(i,j) = n*phi*(sqrt(i_fztc_vs_tcu(i,j) +1)
            - 2 + log(sqrt(i_fztc_vs_tcu(i,j) +1) - 1));
        endfor
    endfor
%Plotting GZTC overdrive vs. avt vs. tcu
figure(2)
mesh(avt,tcu,ZTC_overdrive)
set (gca, "fontsize", 20);
title('ZTC Overdrive x avt x tcu');
xlabel('avt');
ylabel('tcu');
zlabel('ZTC Overdrive');
ZTC_overdrive(1,1)
hold on;
endfunction
```

C.5 ZTCAnalysisTCigm.m

Script for calculation of required TC_I for each GZTC inversion level in order to stabilize the bias point regarding temperature variation:

```
function ZTCAnalysisTCigm
n = 1.3; % Slope factor used in this estimation.
phi = 26e-3; % Thermal voltage.
avt = [0.5e-3:0.1e-3:3.5e-3]; % temperature dependence of VT
tcu = [-1.5:-0.05:-2.5]; % temperature dependence power coefficient mobility.
tcu2 = tcu; % tcu copy
    % inverting tcu
    for t = 1:length(tcu)
        tcu(t) = tcu2(length(tcu) + 1-t);
    endfor
%Calculating required TCi in order to stabilize the gmz bias point
    for j = 1:length(avt)
        for i = 1:length(tcu)
            i_fgz(i,j) = fzero(@(ni) fowardZTCgm(ni,avt(j),tcu(i)),
            1 + i + 5*j);
             TCi_gmz(i,j) = (2*((avt(j)*q)/(kb*n) - sqrt(i_fgz(i,j) +1)
             + 2 - log(sqrt(i_fgz(i,j) +1) - 1))*(sqrt(1+i_fgz(i,j))+1)
             + (tcu(i) + 2.0))/(i_fgz(i,j)*T0);
        endfor
    endfor
%Plotting GZTC forward inversion level vs. avt vs. tcu
figure(1)
surf(avt,tcu,i_fgz); colormap([hot]);
set(gca, 'zscale', 'log');
set (gca, "fontsize", 20);
grid on
title('i_fgz x avt x tcu');
```

```
xlabel('avt');
ylabel('tcu');
zlabel('i_fgz');
hold on;
%Plotting TCi required for each GZTC forward inversion level vs. avt vs. tcu
figure(2)
surf(avt,tcu,TCi_gmz);
set (gca, "fontsize", 20);
grid on;
title('TCi_gmz x avt x tcu');
xlabel('avt');
ylabel('tcu');
zlabel('TCi_gmz');
hold on;
endfunction
```

C.6 VinZTCAnalysis.m

Script for calculation of required TC_I in function of i_{f0} and $\alpha_{V_{T0}}$:

```
n = 1.3; % Slope factor used in this estimation
phi = 26e-3; % Thermal voltage.
avt = [0.5e-3:2e-4:2.5e-3]; % temperature dependence of VT
tci = [-2000e-6:1.2e-3:10000e-6]; % Effective Temperature Coefficient
% Calculating each if0 in function of temperature dependence of VT and TCi
for j = 1:length(avt)
    if((j==1))
        for i = 1:length(tci)
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 10);
        endfor
    endif
    if((j==2))
        for i = 1:length(tci)
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 10);
        endfor
    endif
    if((j==3))
        for i = 1:length(tci)
              if(i<3)
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
              100);
              else
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 10);
              endif
        endfor
    endif
    if((j==4))
        for i = 1:length(tci)
```

```
            if(i<3)
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
            100);
            else
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 10);
            endif
        endfor
    endif
    if((j==5))
        for i = 1:length(tci)
            if(i<4)
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
            200);
            else
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 10);
            endif
        endfor
    endif
    if((j==6))
        for i = 1:length(tci)
            if(i<5)
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
            200);
            else
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 10);
            endif
        endfor
    endif
    if((j==7))
        for i = 1:length(tci)
            if(i<4)
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
            200);
            else
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 80);
            endif
        endfor
    endif
    if((j==8))
        for i = 1:length(tci)
            if(i<4)
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
            200);
            else
            i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 80);
            endif
        endfor
    endif
```

```
    if((j==9))
        for i = 1:length(tci)
              if(i<4)
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 200);
              else
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 80);
              endif
        endfor
    endif
    if((j==10))
        for i = 1:length(tci)
              if(i<4)
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
              200);
              else
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 80);
              endif
        endfor
    endif
    if((j==11))
        for i = 1:length(tci)
              if(i<4)
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)),
              200);
              else
              i_f0(i,j) = fzero(@(ni) VinFowardZTC(ni,avt(j),tci(i)), 80);
              endif

        endfor
    endif
endfor
%Plotting if0 vs. TCi  vs. avt0
grid on
figure(1)
surf(avt,tci,i_f0); colormap([hot]);
grid minor;
set(gca, 'zscale', 'log');
set (gca, "fontsize", 20);
title('If0');
xlabel('avt');
ylabel('tci');
zlabel('if0');
%Calculating if0 voltage overdrive
    for j = 1:length(avt)
        for i = 1:length(tci)
             ZTC_overdrive(i,j) = n*phi*(sqrt(i_f0(i,j) +1)
             - 2 + log(sqrt(i_f0(i,j) +1) - 1));
        endfor
```

```
    endfor
%Plotting if0 voltage overdrive vs. TCi  vs. avt0
figure(2)
surf(avt,tci,ZTC_overdrive)
grid minor;
set (gca, "fontsize", 20);
title('Vin ZTC Overdrive x avt x tci');
xlabel('avt');
ylabel('tci');
zlabel('Vin ZTC Overdrive');
endfunction
```

C.7 fowardZTC.m

Implementation of Eq. (2.74).

```
function y = fowardZTC(ni,avt,tcu)
q =  1.602176565e-19; % magnitude of electron charge
kb = 1.3806488e-23; % Boltzmann constant
y = -1*(avt*q)/(n*kb)+((tcu+2)/(2))*((-ni)/(sqrt(1+ni)+1))
+ sqrt(1+ni) -2 + log(sqrt(1+ni)-1);
endfunction
```

C.8 fowardZTCgm.m

Implementation of Eq. (2.94).

```
function y = fowardZTCgm(ni,avt,tcu)
q =  1.602176565e-19;% magnitude of electron charge
kb = 1.3806488e-23;% Boltzmann constant
y = tcu*(sqrt(1+ni)-1) - 2 +
((sqrt(1+ni)+1)/(sqrt(1+ni)))*((avt*q)/(kb*n)+2-log(sqrt(1+ni)-1));
endfunction
```

C.9 VinFowardZTC.m

Implementation of Eq. (2.91).

```
function y = VinFowardZTC(ni,avt,tci)
q =  1.602176565e-19;% magnitude of electron charge
kb = 1.3806488e-23;% Boltzmann constant
T0 = 300;% Room Temperature
y = -1*(avt*q)/(n*kb)+((tci*T0)/(2))*((ni)/(sqrt(1+ni)+1))
+ sqrt(1+ni) -2 + log(sqrt(1+ni)-1);
endfunction
```

APPENDIX D SUMMARY IN PORTUGUESE

MODELAMENTO E ANÁLISE DO COEFICIENTE NULO DE TEMPERATURA (ZTC) DO MOSFET PARA APLICAÇÕES ANALÓGICAS DE BAIXA SENSIBILIDADE TÉRMICA

D.1 INTRODUÇÃO - CAPÍTULO 1

Este capítulo contextualiza cronologicamente a íntima relação entre a temperatura e a eletrônica. Onde o foco principal são as aplicações atuais utilizando tecnologia CMOS. É explicado e exemplificado que a contínua miniaturização das tecnologias CMOS (principal motivo da variação local da temperatura) junto com a temperatura ambiente (variação global de temperatura e que é dependente da aplicação) tendem a modificar os desempenhos dos circuitos eletrônicos. O capítulo conclui com a importância do desenvolvimento de um procedimento de projeto para atenuar o efeito da temperatura nas aplicações analógicas, onde é escolhido como o ponto de partida o modelamento e a análise do coeficiente nulo de temperatura (ZTC) do MOSFET. Os principais objetivos da dissertação são então descritos, assim como a estrutura do trabalho.

A lista de contribuições referente a essa dissertação é:

- O modelamento do coeficiente nulo de temperatura (ZTC) do MOSFET levando em conta todos os níveis de inversão do dispositivo [SCHNEIDER; GALUP-MONTORO (2010)]. Principal resultado usando essa abordagem é que o ponto de polarização pode ocorrer entre região moderada e forte. Vale destacar que até o momento este efeito só tinha sido modelado no regime forte de operação.
- Como consequência, o mesmo modelo de transistor foi também usado para modelar o efeito ZTC na transcondutância do transistor MOS.
- A vizinhança do ponto ZTC também é abordada e modelada. Este conceito é então descrito como essencial para o projetista analógico já que o comportamento em temperatura do transistor poderia ser ajustado de acordo com a necessidade.
- Ambos conceitos, ZTC e sua vizinhança, foram usados para gerar e modelar duas novas referências de corrente e duas novas referências de tensão.
- Por último, a condição ZTC na transcondutância do MOS é então aplicada em transcondutores que compõem alguns filtros Gm-C, fornecendo circuitos com baixa sensibilidade térmica nas suas principais performances.

D.2 MODELAMENTO ZTC E SUAS APLICAÇÕES - CAPÍTULO 2, 3 E 4

D.2.1 MODELAMENTO ZTC - CAPÍTULO 2

Este capítulo estuda cronologicamente a condição ZTC no MOSFET e algumas de suas estratégias de modelamento. A condição ZTC no MOSFET se deriva *praticamente* do cancelamento mútuo da dependência térmica da mobilidade e da tensão de limiar [FILANOVSKY; ALLAM (2001)], para uma particular polarização de porta. Em resumo, esta condição define um ponto de trabalho no transistor MOS (V_{GZ}, I_{DZ}) onde a corrente de dreno apresenta baixa sensibilidade térmica. Fig. 2.1 ilustra tal comportamento térmico.

O ponto de polarização ZTC é atualmente encontrado em qualquer tecnologia CMOS planar, para ambos transistores N e PMOS, e sua definição é dependente do processo de fabricação. Neste caso, o ponto ZTC na corrente de dreno está subordinado à dependência térmica da mobilidade e da tensão de limiar. Uma maneira fácil de visualizá-lo é observando o impacto da variação de temperatura na corrente de dreno utilizando o modelo I-V clássico do transistor, Eq. 2.26. Notando que a corrente de dreno é diretamente proporcional a mobilidade e ao mesmo tempo ela aumenta quando a tensão de limiar diminui,

e que ambos, mobilidade e tensão de limiar, diminuem com o aumento da temperatura, pode-se calcular então que um efeito cancela o outro em um certo ponto de polarização de porta-bulk.

Na literatura, as Eqs. (2.50) e (2.51) são frequentemente adotadas para modelar o efeito ZTC. A primeira define a tensão de porta necessária para o transistor entrar na condição ZTC e a segunda a corrente. Ambas partem da premissa que o ZTC esteja no regime forte de operação. Entretanto, utilizando uma breve extração por simulação da condição ZTC em algumas tecnologias CMOS comerciais, resumida na tabela 2.2, foi concluído que o efeito ZTC pode ocorrer também em regime moderado de operação. Dessa maneira, esse capítulo explora, como objetivo principal, o modelamento da condição ZTC levando em conta todos os níveis de inversão do transistor MOS e é enfatizado que a mesma sempre deve ocorrer acima da tensão de limiar. Isto é, em um regime de operação moderado para forte. O modelo do transistor usado foi o modelo unificado controlado por corrente UICM (ou antigamente referenciado como ACM) [SCHNEIDER; GALUP-MONTORO (2010)]. Eq. (2.74) junto com a Eq. (2.79) descrevem o ZTC utilizando o modelo UICM. Alguns gráficos, tais como Figs. 2.17, 2.18 e 2.19, são construídos a partir desta análise mais completa mostrando como ZTC se comporta em função da dependência térmica da mobilidade e da tensão de limiar.

Por seguinte, a vizinhança da condição ZTC é também modelada. Filanovsky foi o primeiro estudá-la e modelá-la em [FILANOVSKY; ALLAM (2001)]. A mesma abordagem foi aqui adotada porém o modelo UICM foi usado. As Eqs. (2.85) e (2.86) são aqui definidas as quais explicam de uma forma simples como ajustar o comportamento térmico do transistor MOS, como mostado na Fig. 2.20. Além disso, é também proposto uma maneira de cancelar a dependência térmica da vizinhança do ZTC: aplicando uma corrente de polarização com uma derivada térmica de primeira ordem. Eq. (2.89) é então ineditamente derivada mostrando que a condição ZTC pode ser deslocada para outros valores de tensão de porta. Um conjunto de gráficos extraidos por simulações, Figs. 2.22 e 2.23, ilustra a validade desta interpretação.

Por último, uma análise similar é feita para a condição ZTC na transcondutância do transistor MOS (GZTC), como ilustrado na Fig. 2.28. A expressão Eq. (2.94) é assim derivada onde indica que, se o transistor é polarizado em i_{fgz} (nível de inversão GZTC) juntamente com uma certa dependência térmica na corrente de polarização (TC_{IGZ}), a sua transcondutância terá uma baixa sensibilidade térmica. Figs. 2.27 e 2.29 mostram os possíveis valores para i_{fgz} e TC_{IGZ} em função da dependência térmica da mobilidade e da tensão de limiar, respectivamente.

D.2.2 APLICAÇÕES BASEADAS EM ZTC - CAPÍTULO 3 E 4

Nos capítulos 3 e 4, oito circuitos são projetados utilizando as análises feitas no capítulo 2. Os circuitos foram implementados em dois diferentes processos: XFAB 180 nm e IBM 130 nm. As duas fontes de corrente ZTC foram projetadas em XFAB enquanto as duas de tensão em IBM. Os quatros filtros gm-C baseados em GZTC também foram projetados em IBM. Tirando os filtros, todos os resultados de simulação foram extraídos levando em conta os parasitas pós-layout. Também são incluídas algumas medidas experimentais.

A primeira fonte de corrente, publicada em [TOLEDO et al. (2014)] e chamada de Corrente de Referência CMOS Auto-Polarizada (ZSBCR), é realizada utilizando o MOSFET na vizinhança da condição ZTC. O conceito está concentrado em igualar a dependência térmica do transistor MOS com a dependência térmica de um resistor integrado do tipo

polisilício. A Fig. 3.1 mostra o conceito empregado na topologia proposta e a Fig. 3.2 a implementação em CMOS 180 nm. Gerando uma referência de 5 μA (Fig. 4.3), o circuito opera com uma tensão de alimentação de 1.4 à 1.8 V (Fig. 4.4), ocupando uma área em torno de $0.010mm^2$ (Fig. 3.4). Segundo as simulações, o circuito apresenta um coeficiente de temperatura efetivo (TC_{eff}) de 15 ppm/^{o}C para -45 à +85 ^{o}C (Fig. 4.3) e uma sensibilidade à variação de processo de $\sigma/\mu = 4.5\%$ incluindo efeitos de variabilidade dos tipos processo e descasamento local (Fig. 4.5). A sensibilidade de linha encontrada nas simulações é de aproximadamente $1\%/V$ (Fig. 4.4).

A segunda fonte de corrente, publicada em [TOLEDO et al. (2015a)] e chamada de Corrente de Referência Sem Resistor Auto-Polarizada com Capacitor Chaveado (ZSCCR), é implementada aproveitando as baixas sensibilidades térmicas da condição ZTC e dos capacitores Metal-Isolator-Metal (MIM). A Fig. 3.5 mostra o conceito empregado na topologia proposta e a Fig. 3.6 (a) a implementação também feita em CMOS 180 nm. Resultando em uma corrente de referência de 5.88 μA (Fig. 4.7), para uma tensão de alimentação de 1.8 V, o circuito ocupa uma área de $0.010mm^2$, como mostrado na Fig. 3.6 (b). Resultados de simulações mostram um TC_{eff} de 60 ppm/^{o}C para um intervalo de temperatura de -45 à +85 ^{o}C (Fig. 4.8) e um consumo de potência de 63 μW.

A primeira referência de tensão proposta, publicada em [CORDOVA et al. (2015)], é uma Referência de Tensão resistente à pertubações eletromagnéticas contendo apenas MOSFETs (EMIVR). A ideia principal envolvida na dessensibilização térmica da tensão de referência é o uso da vizinhança do ZTC no dimensionamento de um self-cascode MOSFET (SCM), como mostrado na Fig. 3.9. Gerando um valor de referência de 395 mV (Fig. 4.11), o circuito é projetado no processo CMOS 130 nm (Fig. 3.8), ocupando em torno de 0.0075 mm^2 de área de silício (Fig. 3.8), e consumindo apenas 10.3 μW. Simulações pós-leiaute apresentam um TC_{eff} de 146 ppm/^{o}C, para um intervalo de temperatura de -55 à $+125^o$C (Fig. 4.11). Uma fonte EMI de 4 dBm (1 V_{pp} de amplitude) aplicada na alimentação do circuito, de acordo com o padrão Direct Power Injection (DPI), resulta em um máximo de desvio DC e ondulação Pico-à-Pico de -1.7 $\%$ e 35.8m V_{pp}, respectivamente (Fig. 4.11).

A segunda referência de tensão, publicada em [CORDOVA et al. (2015)], é uma Tensão de Referência baseada em diodo Schottky com 0.5V de alimentação (SBVR). Ela gera três saídas, cada uma utilizando MOSFETs com diferentes tensões de limiar (standard-V_T, low-V_T, e zero-V_T). Todos disponíveis no processo adotado CMOS 130 nm. As tensões de referência são geradas através da aplicação de uma corrente de polarização com uma certa dependência térmica (Fig. 4.19) em cima dos transistores configurados no modo diodo (Fig. 3.11). Este projeto resultou em três diferentes voltages de referências: 312, 237, e 51 mV, apresentando um TC_{eff} de 214, 372, e 953 ppm/^{o}C no intervalo de temperatura de -55 à 125°C, respectivamente (Fig. 4.20, 4.21 and 4.22). O circuito ocupa em torno de 0.014 mm^2 (Fig. 3.13), consumindo um total de 5.9 μW.

Por fim, os circuitos gm-C são projetados usando o conceito GZTC: um emulador de resistor, um inversor de impedância, um filtro de primeira ordem e um filtro de segunda ordem (Fig. 3.15). Os circuitos também são simulados no processo CMOS 130 nm, resultando em uma melhora na estabilidade térmica dos seus principais parâmetros, indo de 27 à 53 ppm/^{o}C (Fig. 4.27, 4.28, 4.28 and 4.29).

D.3 CONCLUSÃO - CAPÍTULO 5

Esta dissertação apresentou uma nova abordagem para projetos CMOS analógicos com baixa sensibilidade térmica, especialmente para aqueles inseridos em sistemas em CHIP de alto desempenho onde as mudanças na temperatura tem um enorme intervalo de variação. Como ponto de partida, investigou-se e modelou-se as condições ZTC e GZTC usando ambas como referência para desenvolver um grupo de aplicações. Os circuitos implementados foram: duas correntes de referência baseadas em ZTC, duas tensões de referência baseadas em ZTC e quatro gm-c filtros polarizados em GZTC. A metodologia apresentada se mostrou bastante promissora dando ao projetista analógico uma visão de como o seu circuito pode variar com temperatura (Fig. 2.26).

Os circuitos também foram confrontados com algumas implementações encontradas na literatura. Essas comparações as vezes são difíceis de serem realizadas devido à falta de dados, especialmente em relação a variabilidade. Considerando que para os gm-c filtros apenas uma investigação inicial foi feita, é justo afirmar que todo o modelamento aqui apresentado junto com as suas interpretações tem um potencial relevante para melhorar a metodologia de projeto analógico, principalmente quando as variações de temperatura são de grande amplitudes. Estas afirmações são aqui apoiadas por resultados de simulações apresentados nesta dissertação.

D.3.1 TRABALHOS FUTUROS

Há certamente muito mais trabalhos à serem desenvolvidos em ambas as áreas: modelamento ZTC e projetos analógicos/RF usando (G)ZTC. Principalmente para condição GZTC, uma vez que existe uma enorme gama de circuitos os quais tem uma alta dependência do parâmetro transcondutância nos seus desempenhos. Abaixo há uma lista de possíveis aperfeiçoamentos que podem guiar futuros trabalhos.

- Os modelos apresentados foram usados apenas como um guia inicial de projeto nos cálculos à mão, os quais serviram como entrada para o ambiente de EDA. Entretanto, nenhuma comparação entre o modelo proposto e os dados experimentais foi conduzida. Tal procedimento seria bastante relevante para fins de design medindo assim o quão o modelo é fidedigno.
- A investigação dos efeitos de segunda ordem exatamente nas condições ZTC e GZTC. Este assunto permanece mal explicado na literatura (Fig. 5.1).
- A Fig. 5.2 mostra o ponto ZTC em função do canal do transistor. Nenhum modelamento ZTC foi encontrado levando em conta efeitos de canal curto.
- O autor não encontrou na literatura nenhuma relação entre a condição ZTC Digital e as condições ZTC modeladas aqui. Sabendo os pontos ZTC do transistor PMOS e NMOS seria possível estimar o V_{DD} requerido para fazer o atraso do inversor independente da temperatura ?
- Outro modelamento interessante e relevante seria para as condições ZTC localizadas na Capacitância MOS (Secção 2.3). Provavelmente algum particular design poderia se beneficiar desta capacitância de baixa dependência térmica.
- Esta dissertação não abordou, porém existe também um ponto ZTC na resistência de triodo do transistor MOS. Igualmente ao caso da capacitância MOS, a mesma observação pode ser feita para a resistência triodo ZTC.
- Novas topologias para fontes de corrente e de tensão podem ser investigadas e desenvolvidas.

- A condição GZTC permanece inexplorada principalmente quando trata-se de projetos analógicos/RF CMOS. Esta condição pode ser usada em aplicações onde a transcondutância do MOSFET desempenha um papel fundamental em suas performances. Exemplos notáveis são Reguladores sem capacitor externo (CL-LDO) [TORRES et al. (2014)] e transcondutores de baixo ruido (LNTA) [GEDDADA et al. (2014)].
- Seria bastante interessante analisar qual seria o impacto do efeito de radiação nas referências ZTC aqui propostas.