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Electrical characteristics and interface structure of HfAlO/SiON/Si(001) stacks

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The electrical characteristics of RuO_2/HfAlO/SiON/Si(001) capacitors prepared by thermal nitridation of the Si substrate previously to HfAlO ultrathin film deposition were determined. A dielectric constant of 19 and a gate current density of 67 mA/cm^2 for an equivalent oxide thickness of 1.1 nm have been determined, whereas non-nitrided capacitors gave substantially lower dielectric constant and higher gate current density. The structure and integrity of the stacks after thermal annealing were accessed by means of spectroscopic ellipsometry and x-ray reflectometry, indicating that thermal N incorporation into the gate dielectric stacks forms an effective diffusion barrier, leading to a smoother, SiO_2-like interface. The HfAlO films grown on nitrided substrates were seen also to have lower porosity, percentage of voids, and density of oxygen vacancies. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2715112]

The use of insulating materials bearing dielectric permittivity much larger (high k) than that of silicon oxide or oxynitrides in advanced, Si-based complementary metal oxide semiconductor field effect transistor (MOSFET) devices is compulsory for all forthcoming technology nodes requiring gate dielectric with capacitance equivalent to SiO_2 thickness (EOT) smaller than 1 nm.[1] One of the very few surviving candidate material is hafnium aluminate (HfAlO),[2–4] since it has appreciably high dielectric constant (15–25) and crystallization temperature, even if the properties of transistors made up with HfAlO as gate dielectric are drastically degraded by several thermodynamical instabilities[3–6] appearing during fabrication processing, such as (i) interdiffusion with the Si substrate, (ii) oxygen diffusion and the consequent uncontrollable lower-k interlayer growth, (iii) boron penetration, (iv) film stoichiometry change owing to Al and Hf losses, and others. Despite these drawbacks, HfAlO remains attractive because of symmetric threshold voltage (V_{th}) or, in other words, the fact that p-type FETs suitable for low standard power device application can be obtained without counterimplantation.[3] Thus, there is currently a worldwide challenge to engineer HfAlO ultrathin films on Si which can survive all thermal steps of fabrication technology following gate dielectric deposition, keeping EOT, gate current density, charge carrier mobility, and other electrical characteristics within device design specifications. The most promising approach consisted of finding routes for N incorporation into HfAlO films,[2,7] rendering it resistant even to the critical thermal processing step of dopant activation usually performed by rapid thermal annealing (RTA) around 1000 °C. These included N incorporation into HfAlO films on Si through different routes: (i) during film deposition,[5] (ii) by postdeposition annealing (PDA),[2,3,6] and (iii) by thermal nitridation of the Si substrate prior to HfAlO film deposition. It is noteworthy, however, that any valid route must control and moderate the N concentration near the dielectric/Si interface in order to avoid degradation of the density of interface electronic states (D_{it}) and the charge carrier mobility of the transistor.[8] We report here on the investigation of *CV* and *IV* characteristics of RuO_2/HfAlO/Si capacitors, in which the Si substrate surfaces underwent very mild thermal nitridation before HfAlO film deposition. The structure, composition, and integrity of these thin film stacks were also accessed and correlated with the observed electrical characteristics.

The Si(001) substrates were wet chemically cleaned, HF last, and promptly nitrided in 10 mbars of NH_3 at 700 °C for 30 s. Nuclear reaction analysis and narrow resonant nuclear reaction profiling[9] (results not shown here) revealed that this thermal nitridation led to the formation of a silicon oxynitride film, approximately 0.4 nm thick, containing 5×10^{13} N/cm^2 homogeneously distributed therein. The same nuclear reaction analysis revealed that this oxynitride layer resists well, unless for partial N loss, to simulation of the dopant activation thermal processing step, namely, RTA at 1000 °C for 10 s, both in oxygen and in vacuum. HfAlO films were deposited on these SiON/Si(001) substrates by magnetron sputtering from a $(HfO_2)_{0.7}(Al_2O_3)_{0.3}$ target in Ar plasma. RuO_2 electrodes were also deposited by reactive magnetron sputtering from a Ru target in Ar/O_2 plasma. The

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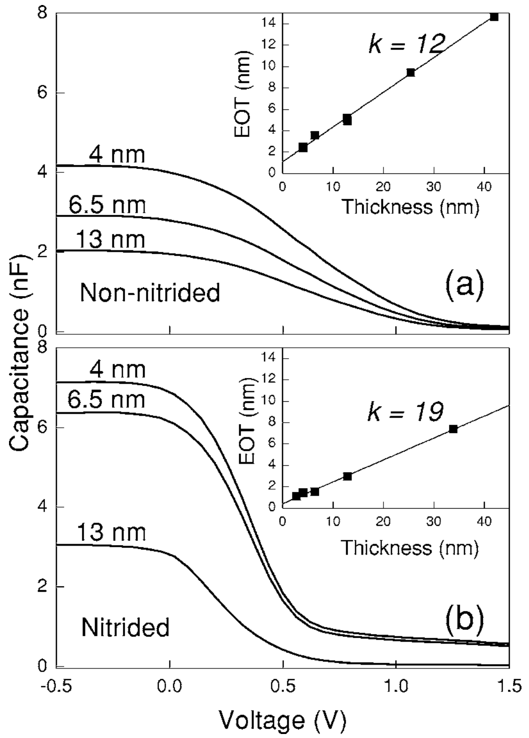

FIG. 1. *CV* characteristics at 1 MHz for (a) RuO_2/HfAlO/Si and (b) RuO_2/HfAlO/SiON/Si capacitors. The corresponding EOT vs HfAlO film thicknesses for RuO_2/HfAlO/Si and RuO_2/HfAlO/SiON/Si MOS structures are given in the insets.

samples were analyzed, before and after thermal annealing in 1000 mbars of O_2 at 600 °C for 30 min, by spectroscopic ellipsometry[10] (SE) and by x-ray reflectometry (XRR).[11] *CV* and *IV* characteristics of RuO_2/HfAlO/SiON/Si stacks were determined in 3×10^5 μm^2 capacitors.

The *CV* characteristics at 1 MHz for non-nitrided and nitrided substrates are given in Figs. 1(a) and 1(b), respectively. The corresponding EOT × HfAlO film thicknesses as determined from the *CV* characteristics are given in the insets. The characteristics of the RuO_2/HfAlO/SiON/Si capacitors are clearly superior. In particular, the determined dielectric permittivity of 19 is close to the bulk figure for HfAlO. In Fig. 2 the gate current densities at a gate voltage of 1 V are given as a function of EOT, both for non-nitrided and nitrided substrates. Nitridation has a striking beneficial effect on the electrical performance,[12] as leakage currents remain approximately constant in the lower EOT range, whereas for the non-nitrided substrate the leakage current increases exponentially with the decrease of EOT. The obtained figure of 67 mA/cm^2 at 1 V gate voltage for a 1.1 nm EOT is comparable to the best results found in the literature.

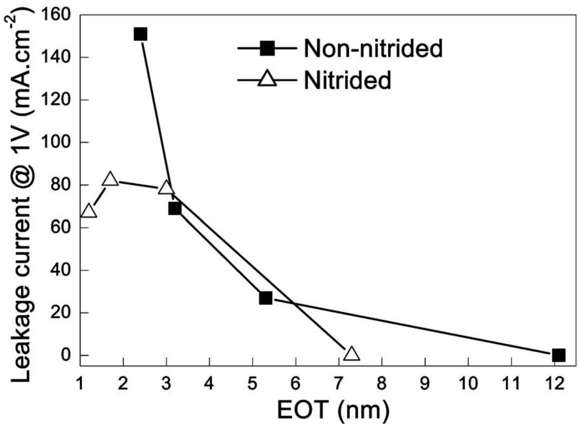

FIG. 2. Gate current density vs EOT for RuO_2/HfAlO/Si and RuO_2/HfAlO/SiON/Si MOS structures, measured at a gate voltage of 1 V.

In order to interpret SE results, a three-layer model is adopted here as sketched in Fig. 3. In the case of HfAlO/Si, the best fitting of the SE curves with the Tauc-Lorentz equations[13] was obtained assuming an interface composition of the kind Hf–Al–O–Si, or in other words a mixture of HfAlO and amorphous-Si (*a*-Si) inclusions originated in the native SiO_2 layer. On the other hand, in the HfAlO/SiON/Si structures the best fit was obtained assuming a SiON-like interface, which did not change significantly after PDA. The interfacial layer is thicker (see Table I) in HfAlO/Si than in HfAlO/SiON/Si, consistently with the *CV* data of Fig. 1. Thus, the superior electrical properties of the RuO_2/HfAlO/SiON/Si capacitors as compared to non-nitrided structures are apparently due to a chemically inert, subnanometric SiO_2-like interface promoted by the incorporation of N previously to high-*k* film deposition.[14] One notices also from Table I that the thickness of the surface layer as well as the percentage of voids (i.e., porosity) are larger for the HfAlO/Si than for the HfAlO/SiON/Si structures. Furthermore, SE also points out to a more stable structure than those obtained for HfAlO deposited by atomic layer deposition on SiN/Si,[15] where a dissociation of the SiN interlayer was observed. Finally, the density of oxygen vacancies seems to be lower in the present films than in previous cases discussed in the literature.

The XRR results for HfAlO/Si and HfAlO/SiON/Si structures are shown in Fig. 4, where the solid lines represent the numerical simulations of the curves on the basis of a three-layer model similar to that used to simulate the SE results. Special care has been taken for the simulation of the fringe minima, since the shapes of these minima are extremely sensitive to the thicknesses of the model ultrathin component layers. The interpretation of XRR results takes into account the roughness of each interface, according to

TABLE I. Characteristic parameters extracted from simulation of the SE and XRR data on the basis of the three-layer models depicted in Fig. 3. *t* stands for thickness and σ for roughness, both in nm±0.1.

	Surface				Bulk			Interface			
	t (SE)	*t* (XRR)	%voids (SE)	σ (XRR)	*t* (SE)	*t* (XRR)	σ (XRR)	*t* (SE)	*t* (XRR)	%*a*-Si (SE)	σ (XRR)
HfAlO/Si	1.7	0.5	56.3	0.4	7.2	6.7	0.4	0.7	0.4	54.9	0.4
HfAlO/SiON/Si	1.0	0.4	51.0	0.4	7.4	6.9	0.5	0.5	0.1	⋯	0.0

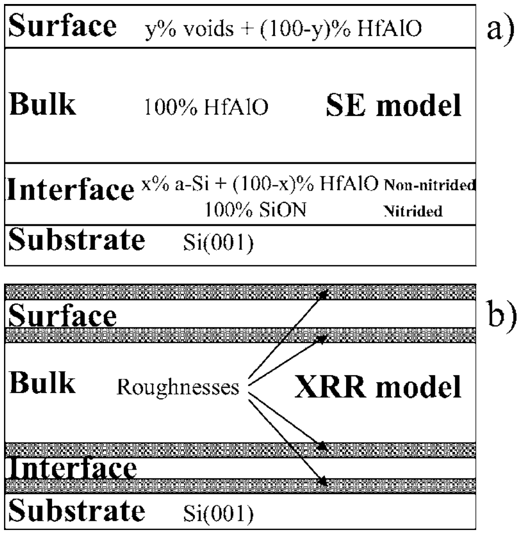

FIG. 3. Sketch of the three-layer models used in the simulation of (a) SE and (b) XRR data.

Table I. It is noteworthy that the dielectric/semiconductor interface of the HfAlO/SiON/Si structure has a significantly smaller roughness than HfAlO/Si. Furthermore, the dielectric/semiconductor interfacial layer of the HfAlO/SiON/Si structure is smaller than those previously obtained by XRR in the literature.[16] These characteristics are also not very severely modified by annealing. A smoother interface seems to be another effect of N incorporation leading to superior electrical quality of the HfAlO/SiON/Si stacks.

In summary, we investigated HfAlO/SiON/Si stacks concerning their potential use as gate dielectrics. The dielectric permittivity of 19, close to the bulk figure, and the gate current density of 67 $\mathrm{mA/cm^2}$ at 1 V for EOT of 1.1 nm set HfAlO/SiON/Si as a very attractive replacement for SiO_2. SE and XRR characterizations made clear the relevance of N incorporation in gate dielectric stacks, as it promotes HfAlO films with lower porosity, percentage of voids, and density of oxygen vacancies, as well as a smoother, free of *a*-Si precipitates interface. The action of the subnanometric SiON interlayer as a barrier for Hf or Al diffusion contributes significantly to the improved electrical properties of the nitrided structures.

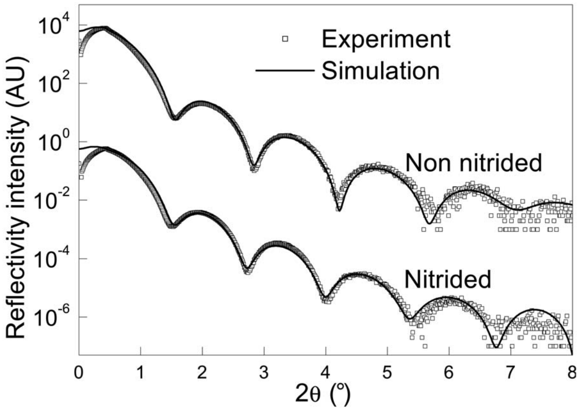

FIG. 4. XRR results for HfAlO/Si and HfAlO/SiON/Si stacks with experimental data (symbols) and simulated (lines) data.

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