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MCML Gate Design Methodology and the Tradeoffs between MCML and CMOS Applications

Thesis presented in partial fulfillment of the requirements for the degree of Master of Microelectronics

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ABSTRACT

This work proposes a simulation-based methodology to design MOS Current-Mode Logic (MCML) gates and addresses the tradeoffs of the MCML versus static CMOS circuits. MCML is a design style developed focusing in a high-speed logic circuit. This logic style works with the principle of steering a constant bias current through a fully differential network of input transistors. The proposed methodology uses the quadratic transistor model to find the first design solution, through SPICE simulations, make decisions and resizes the gate to obtain the required solution. The method considers a uniform sizing of the pull-down network transistors. The target solution is the best propagation delay for a predefined gate noise margin. We design MCML gates for three different process technologies (XFAB XC06, IBM130 and PTM45), considering gates up to three inputs. We compare the solutions of the proposed methodology against commercial optimization software, Wicked™, that considers different sizing for PDN differential pairs. The solutions of the software results in a 20% of improvement, when compared to the proposed methodology, in the worst case input delay for the XFAB XC06 technology, and 3% in IBM130. We demonstrate through ring oscillators simulations that MCML gates are better for high speed and small logic path circuits when compared to the CMOS static gates. Moreover, by using MCML frequency dividers we obtained a maximum working frequency that almost doubles the frequency achieved by CMOS frequency dividers, dissipating less power than static CMOS circuits. We demonstrate through a reliability analysis that the analog behavior of MCML gates makes them susceptible to PVT variations. The global variations are compensated by the bias control circuits and with the increase of the PDN transistor width. This procedure compensates the gain loss of these transistors in a worst case variation. In other hand, this increasing degrades the propagation delay of the gates. The MCML gates reliability is heavily affected by the mismatching effects. The difference of the mirrored bias current and the mismatching of the differential pairs and the PUN degrade the design yield. The results of the layout extracted simulations demonstrate that MCML gates performs a better propagation delay performance over gates that depend on complexes pull-up networks in standard CMOS implementation, as well as multi-stages static CMOS gates. Considering the gate layout implementation we demonstrate that the standard structures of pull-up and bias current mirror present in the gate are prejudicial for the MCML gate area

Keywords: MOS Current-Mode Logic, MCML, MCML gate design, MCML Application.

Metodologia de Projeto de Portas Lógicas MCML e a Comparação entre Portas Lógicas CMOS e MCML

RESUMO

Este trabalho propõe uma metodologia de projeto para células digitais MOS *Current-Mode Logic* (MCML) e faz um estudo da utilização destes circuitos, frente à utilização de células CMOS tradicionais. MCML é um estilo lógico desenvolvido para ser utilizado em circuitos de alta frequência e tem como princípio de funcionamento o direcionamento de uma corrente de polarização através de uma rede diferencial. Na metodologia proposta o dimensionamento inicial da célula lógica é obtido a partir do modelo quadrático de transistores e através de simulações SPICE analisa-se o comportamento da célula e se redimensiona a mesma para obter as especificações desejadas. Esta metodologia considera que todos os pares diferencias da rede de *pull-down* possuem o mesmo dimensionamento. O objetivo através desta metodologia é encontrar a melhor frequência de operação para uma dada robustez da célula digital. Dimensionamos células lógicas MCML de até três entradas para três tecnologias (XFAB XC06, IBM130 e PTM45). Comparamos os resultados da metodologia proposta com o software comercial de otimização de circuitos, Wicked™, o qual obteve uma resposta de atraso 20% melhor no caso da tecnologia XFAB XC06 e 3% no caso do processo IBM130. Através de simulações de osciladores em anel, demonstramos que a topologia MCML apresenta vantagens sobre as células digitais CMOS estáticas, em relação à dissipação de potência quando utilizada em circuitos de alta frequência e caminhos de baixa profundidade lógica. Também demonstramos, através de divisores de frequência, que estes circuitos quando feitos na topologia MCML podem atingir frequências de operação que em geral são o dobro das apresentadas em circuitos CMOS, além do mais atingem este desempenho com uma dissipação de potência menor que circuitos CMOS. A natureza analógica das células MCML as torna susceptíveis às variações de processo. Variações globais são compensadas pelo aumento dos transistores da PDN, já casos de descasamentos, por não terem um método de compensação, acabam por degradar a confiabilidade do circuito. Na avaliação da área ocupada por célula, a topologia MCML mostrou consumir mais área do que a topologia CMOS.

Palavras-Chave: MOS Current-Mode Logic, MCML ,design de portas lógicas MCML, Aplicações MCML.

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LIST OF ACRONYMS AND ABBREVIATIONS

BDD	Binary Decision Diagram
CAD	Computer-Aided Design
CML	Current-Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
DCVSL	Differential Cascode Voltage Switch Logic
EDA	Electronic Design Automation
FA	Full Adder
HDL	Hardware Description Language
IC	Integrated Circuit
MCML	MOS Current-Mode Logic
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PDN	Pull-Down Network
PNR	Place and Route
PVT	Process Voltage Temperature
PUN	Pull-Up Network
ROBDD	Reduced Ordered Binary Decision Diagram
VLSI	Very Large Scale Integration
SoC	Systems on Chip

CONTENTS

1. INTRODUCTION

The advance of electronic components is only possible through the advance of the semiconductor industry. For five decades this integration has followed the Moore's Law (MOORE, 1965). Moore's Law predicts that the number of available transistors packed into a single IC grows exponentially, doubling approximately every two years.

The transistor scaling makes possible the development of very large-scale integrated (VLSI) circuits and this integration increases the circuit design complexity. This complexity demands the optimization of different cost-functions that sometimes are divergent among themselves. The main cost functions of a VLSI design are the die area, operation frequency, power dissipation, testability, reliability and time-to-market. The goal of obtaining a design solution that satisfies these constraints make the designer explores different circuit topologies and design methodologies. Several possible circuit families implement a logic circuit. Some examples of logic styles are the static CMOS, Pseudo-NMOS (KRAMBECK, LEE e LAW, 1982), Dynamic Circuits (KRAMBECK, LEE e LAW, 1982), Differential Cascode Voltage Switch Logic (HELLER, GRIFFIN, *et al.*, 1984). Figure 1.1 depicts the implementation of the NAND2 circuit with these circuit styles.

Among existing logic families the static CMOS, shown in Figure 1.1(a), is the most used. This logic style is popular due to its robustness and nearly zero static power dissipation. The static CMOS logic gate is a combination of two networks. The pull-up network (PUN) provides the connection between the output and the supply voltage while the pull-down network (PDN) is responsible to connect the output to the ground node. These networks are complementary between each other. Hence, only one of them is conducting in a steady state. The network characteristic of static CMOS family requires 2N transistors to implement an N-input logic gate.

Alternatively to static CMOS, the pseudo-NMOS family, depicted in Figure 1.1(b), has as main goal achieve a lower propagation delay. This logic style uses only one weak pull-up device and stronger pull-down devices. The simplification on the pull-up network reduces the overall load capacitance and thus increases the speed. The main drawback is the existence of static current when the output is at a low output level, leading to high static power dissipation. Furthermore, the pseudo-NMOS logic family is a ratioed logic, meaning that the correct behavior of the gate depends on defining an

adequate ratio between the current capabilities of pull-up and pull-down devices. Notice that the low output is not the ground supply voltage. The voltage divisor between the pull-up and pull-down networks determines the low output voltage.

Dynamic circuits, Figure 1.1(c), overcome the pseudo-NMOS problems by connecting the PMOS transistor to a clock signal and adding a footer NMOS transistor. This logic divides the logic operation into two modes: the precharge mode and evaluation mode. During the precharge phase, the PMOS transistor is ON and the footer NMOS is OFF. Therefore, the output is charged to the high voltage value. In the evaluations phase, the PMOS is OFF and the footer is ON. Hence, the output can be discharge depending on the input values. On the other hand, the design of dynamic circuits require a careful clocking design, consumes significant dynamic power and are sensitive to noise during evaluation.

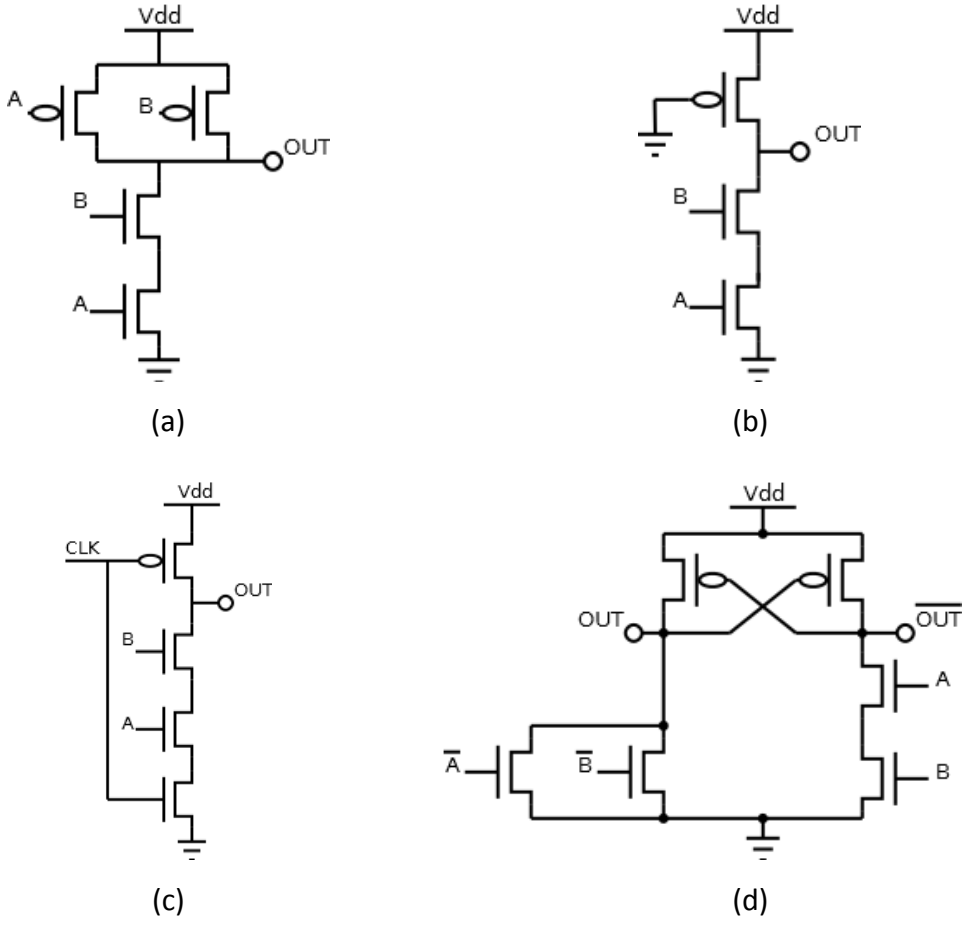


Figure 1.1: NAND2 circuit implemented with (a) static CMOS (b) pseudo-NMOS (c) dynamic circuit (d) DCVSL

The DCVSL style, Figure 1.1(d), also aims to overcome the problem of static power consumption of pseudo-NMOS family. This style works with a differential signal and computes the true and complementary outputs using a pair of NMOS pull-down networks. For any given input pattern, one of the pull-down networks will be ON and the other OFF. The cross couple PMOS transistors work in opposite phase according to the value of the outputs that control it gates. Therefore, no current path between the supply and ground voltage is created. The differential characteristic of DCVSL topology requires 2N NMOS and the cross-coupled PMOS transistors to implement an N input logic gates. Moreover, DCVSL requires dual rail wiring.

Except to the pseudo-NMOS logic family, all logic styles presented until now are rail-to-rail logic families, i.e., the output voltage levels of the gates are close to one of the power supplies. Since the voltage swing is proportional to the charge amount necessary to change the output logic state, for a determined current capability and a definied load, rail-to-rail logic is often slower than the types of logic that use a lower output swing. Furthermore, even though some styles present almost zero static power dissipation, such styles still present dynamic power dissipation that occurs whenever the voltage value of a node changes. In the static CMOS logic family, the dynamic power dissipation can be divided into two components: the output charge current and the short circuit current. Therefore, in high speed switching circuits, these circuits can increase significantly the total dissipated power (ROGER e PLETT , 2006).

There are different integrated circuits design strategies. The chosen design methodology influences in the final design solution. The full custom design methodology specifies the characteristics of each individual transistor. Hence, this strategy potentially maximizes the circuit performances. In another hand, the full custom design is becoming much complex and timing consuming. Nowadays, the circuits' complexity makes this methodology unfeasible for digital circuit applications. However, analog circuits still use this methodology to find a design solution that fit the design specifications.

To overcome the complexity of integrated circuit design the semi-custom design methodology use some automated steps and can compose a complex circuit reusing pre-designed circuit blocks. The most advanced digital circuit design methodology is the standard cell design flow. This strategy has as input the RTL description of the required circuit and a digital standard cell library. A digital standard cell is a transistor network

that provides a Boolean logic function (AND, OR, XOR or inverter, e.g.) or a storage function (flip-flop or latch). Besides of these digital cells, the standard cell library should provide some special cells (Filler cells, Antenna Cells, e.g.) that are used in the design flow to satisfy the layout design rules and make possible the automate circuit generation. These cells are pre-designed and pre-characterized being compatible with the automated design flow requirements. The standard cell design flow have two main design steps: the logic synthesis and the physical synthesis. The logic synthesis defines the logic used to implement the RTL circuit description. Each logic function used in the logic synthesis is characterized in the standard cell library. The physical synthesis uses the logic cells layout definitions present in the standard cell library to place and route the logic blocks. Therefore, the physical synthesis generates a GDSII layout data which corresponds to the file sent to the foundry to the IC manufacturing.

1.1 Motivation

As cited before, the designer must explore different circuit topologies to find the best relation between the cost functions of a specific circuit. Focusing in high-speed circuits an alternative design style is the MOS current-mode logic family (MCML), Figure 1.2. MCML works with the principle of steering a constant bias current through a fully differential network of input transistors (YAMASHINA e YAMADA, 1992) (MIZUNO, YAMASHINA, *et al.*, 1996). The output logic values come from a reduced swing voltage, resultant of a drop voltage on a pair of complementary load devices. Notice that there are two main factors that make the MCML circuits advantageous for the high-speed applications. The reduced logic swing decreases the charge amount necessary to generate a logic transition in a certain load amount. The second feature is the constant bias current that gives an independent behavior among the power consumption and frequency operation. Therefore, MCML already used in many high-speed applications such as ring oscillators, frequency synthesizers, serial transceivers, etc (LIN, HSU, *et al.*, 2013) (LUO, ZHANG, *et al.*, 2015) (AUDZEVICH, WATTS, *et al.*, 2014).

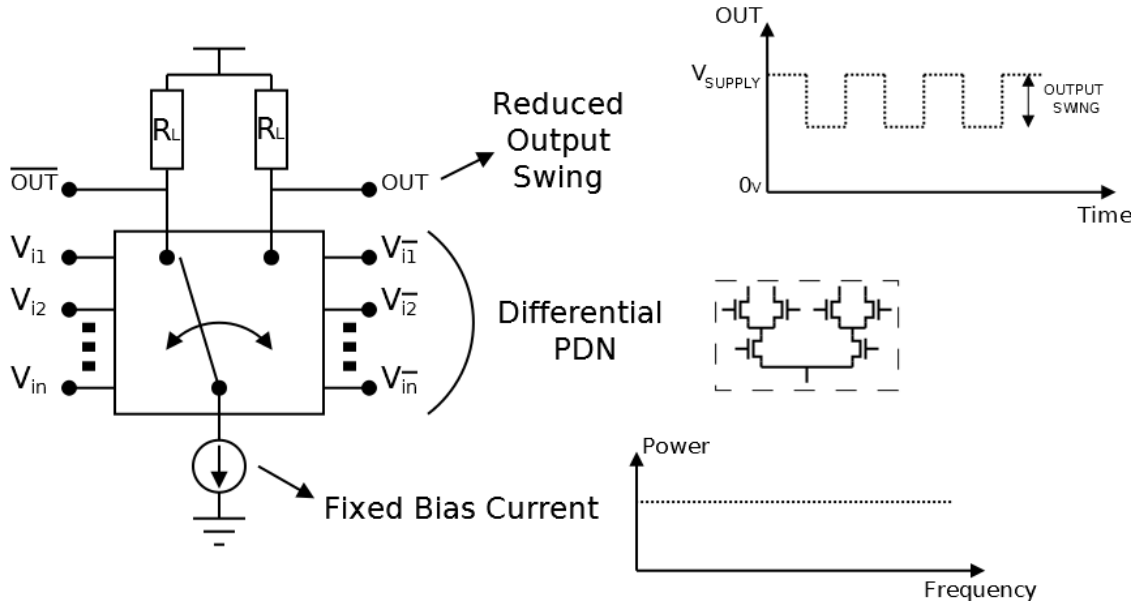


Figure 1.2: MCML characteristics.

Nowadays, several tools are available to accelerate and automate the process of constructing digital circuits using the static CMOS logic family. Even though, if a logic style presents advantages over static CMOS, the time-to-market cost can be crucial for the logic styles choice. Therefore, in order to reduce this cost, and be successfully adopted in the digital design flow, is interesting that a logic style be suitable to the conventional top-down design flow supported by the available EDA environments. Hence, the building blocks should bear the form of standard cell. The introduction of standard cell libraries characteristics in these blocks makes its use more suitable in the digital design flow.

Note that the standard cell digital design flow produces the solutions that are dependent on the standard cell library quality. A good standard cell library, among other specifications, must present a large set of cells and an efficient relation between power consumption, frequency response and robustness. The design of MCML standard cell represents a complex task since the gate has an analog topology, where robustness is hard to be achieved and requires imposing constraints to guarantee the gate functionalities. Furthermore, MCML digital gate design presents several design parameters correlated with each other. Hence, a design methodology to optimize such gates is required. In that way (MUSICER, 2000) design the MCML standard gates using an exhaustive method. Other works focus on obtaining a noise margin and propagation delay analytical models for MCML inverter gate (ALIOTO e PALUMBO, 2003b)

(CARUSO e MACCHIARELLA, 2007) . The same authors also expand this analysis for two-input gates (ALIOTO e PALUMBO, 2003a) (CARUSO e MACCHIARELLA, 2008). More complex analytical formulations to optimize gates up to two-inputs are addressed by (HASSAN, ANIS e ELSMASRY, 2005) and (OSMAN e MAITHAM, 2010). However, the accuracy of these methodologies depends on correctly defining several fitting parameters.

Each logic family presents different electrical characteristics. The evaluation of these characteristics through different applications determines the tradeoffs of logic style use. Besides the different circuit applications, the logic families can change its electrical characteristics as the MOS technology is scaled down. The MOS technology scaling does not optimize all circuits in the same rate. The process advance mainly focus on the digital circuit optimization. It means that the MOSFETs devices become more attractive for the static CMOS applications (LEWYN, YTTERDAL, *et al.*, 2009). Therefore, the tradeoffs of logic family's applications against the static CMOS logic style cannot be the same through different technology nodes.

1.2 Objective

The objective of this work is to propose a design methodology for MCML gates and analyze the tradeoffs of electrical performances and physical characteristics between CMOS and MCML gates. The proposed methodology focuses in designing a set of cells that can be used in a MCML digital standard cell library. The design procedure should be able to size several relations of bias current and output voltage swing given to the designer options of drive strength and a view of the output voltage swing effects to show the influence of the parameters standardization among different gates. Moreover, the goal is design gates up to three inputs and develops a methodology that has an easy CMOS technology node migration.

Once designed the MCML gates, the tradeoffs of MCML family use also should be addressed against the static CMOS style. The work must extend this evaluation to different MOS technology nodes in order to analyze the effects of technology scaling on the MCML topology circuits.

1.3 Master's Thesis Organization

The next sections are organized as follows:

Chapter 2: MCML design basics – Provides the reader the basic operation of an MCML digital gate, as well as a discussion on how the different design parameters impact the electrical characteristics of the gate. The MCML gates design metrics are also presented.

Chapter 3: Design Methodology – Describes the proposed methodology for MCML digital gate design and presents the analysis and results of a set of gates design for three different CMOS technologies.

Chapter 4: Performance and Constraints of MCML and CMOS – Presents some design challenges of standard cell digital library comparing them between CMOS and MCML. This chapter also describes the effects of MOS technology nodes scaling on the both logic styles and presents results and discussions of some circuits performances implemented on both logic families.

Chapter 5: Silicon Implementation – Reports the physical implementation of MCML structures, as well the gates requirements to insert the designed gates into a physical synthesis tool. The analysis of analog extracted simulations results also is presented.

Chapter 6: Conclusions - Presents some conclusions and summarizes the contributions of this work.

2 MCML DESIGN BASICS

2.1 Basic Operation

In general, MCML gate consists of three parts: the pull-up resistance, the pull-down logic network and the bias current source, as illustrated in Figure 2.1.

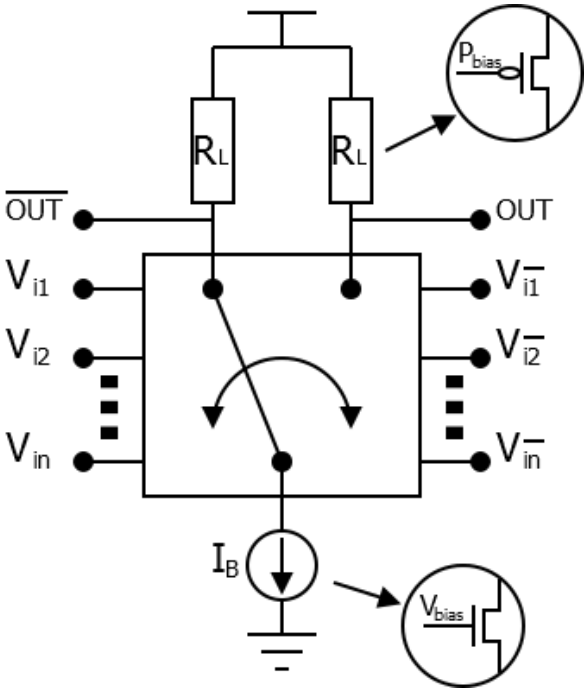


Figure 2.1: MCML gate structure.

Integrated polysilicon resistors or PMOS transistors operating in the triode region are used to implement the pull-up sub-circuits. The polysilicon resistor has better tolerance to PVT (process, voltage and temperature) variation. However, for standard cell library design, PMOS transistor is the most suitable alternative due to the less area overhead. To overcome the problem of PVT variations, a bias control circuit sets the gate voltage of PMOS transistor.

A transistor operating in saturation region implements a current mirror of a current source and generates the bias current I_B of the logic gate. This current is steered to right or left pull-up resistors by the pull-down network (PDN) according to the differential signal values on inputs ($V_{i1}, V_{\imath 1}, V_{i2}, V_{\imath 2} \ldots, V_{in}, V_{\imath n}$). The output voltage

corresponding to the branch where the current is steered, is a function of the voltage drop across the pull up equivalent resistor, given by:

$$V_{out} = V_{DD} - I_B \, x \, R_L \qquad (2.1)$$

At the complementary output, the voltage drop does not appear since no current is flowing through the load. Hence, the output node voltage is pulled up to supply voltage.

2.2 MCML Inverter/Buffer

The PDN implements the logic function of MCML gates. The simplest MCML logic gate implementation is the inverter/buffer gate. Figure 2.2 depicts the inverter gate schematic, where M3 and M4 are PMOS transistors that implement the resistive loads, M1 and M2 compose the differential pair that defines the cell's logic function. Because of the MCML differential characteristic, the buffer cell presents the same topology, being only necessary change the complementary output nodes to change its function.

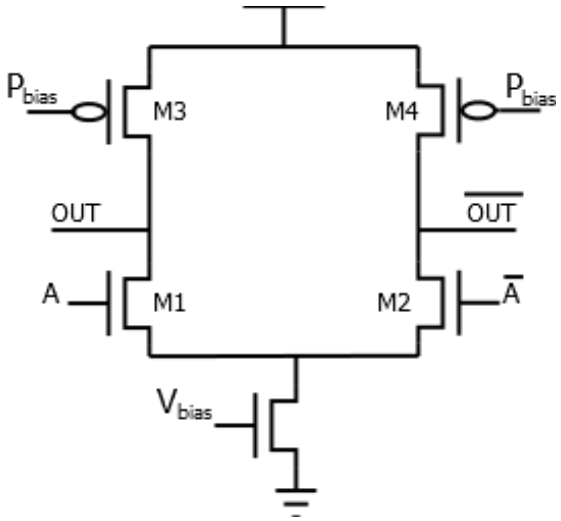


Figure 2.2: MCML inverter gate

The design of MCML inverter should take into account different design parameters that are correlated each other. The output voltage swing, bias current and the transistor differential pair sizing are design parameters that must be studied to find the required performance of the circuit. The following sections present the design parameters and address the correlation between then and the gate performances.

2.2.1 Voltage Swing

In MCML logic gates, the output voltage swing represents the voltage difference between the logic '1' and logic '0' at the output. The voltage swing, ΔV is function of the bias current I_B and the pull-resistance R_L, as follows (2009 EPFL):

$$\Delta V = R_L I_B \tag{2.2}$$

One of the main advantages of MCML gates is the possibility of reducing the signal swing. Compared to the conventional CMOS gates, that present the signal swing equals to the supply voltage, the MCML smaller signal swing reduces the charge amount necessary to change the logic value of a certain load.

The lower bound of voltage swing is the switching capability of the gate. The voltage swing must be high enough to make sure that the tail bias current will be switched to one of the two output branches. It is equivalent to say that the gain of each MCML gate should be high enough to achieve a required noise margin.

A large signal analysis of a differential pair quantifies the lower bound voltage swing for an inverter gate. Assuming that the transistor M1 of Figure 2.3 is in the cutoff region, the inequality (2.3) must be satisfied. Note that, in this inequality, V_T corresponds to the transistor threshold voltage. Now look to the other branch, the transistor M2 is the transistor that flow all the bias current I_B, so the gate-source voltage of transistor M2, V_{gs2}, is represented by equation (2.4). Combining (2.3) with (2.4) and rearranging, the resultant equation is (2.5). Therefore, the minimum voltage swing of an inverter MCML gate is the overdrive voltage, V_{OV}, of the differential pair transistors. Remembering that the overdrive voltage is function of transistor sizing, the lower bound of voltage swing is hardly affect by them. More detail equations for the differential pair equations can be found in (RAZAVI, 2001).

$$V_{DD} - \Delta V - Vx < V_T \tag{2.3}$$

$$V_{gs2} = V_{DD} - Vx \tag{2.4}$$

$$\Delta V > V_{gs2} - V_T = V_{OV2} \tag{2.5}$$

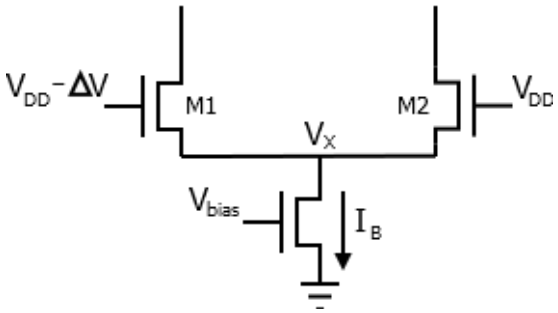


Figure 2.3: Differential Pair.

On the other hand, the voltage swing has as upper bound the nonlinearity of PMOS loads. Large voltage swings correspond to a high drain-source voltage, V_{DS}, on the pull-up transistors. It requires that the PMOS transistors work closer to its saturation voltage, V_{DSat}, increasing the nonlinearities.

The drain voltage of the current mirror determines another bound for high voltage swing values. Large voltage swing pulls down that voltage and forces the current source to operate out of saturation (MUSICER, 2000).

2.2.2 Robustness

The switching threshold of a logic gate is defined as the point where $V_{in} = V_{out}$. In MCML logic gates, this point corresponds to the time when the current flowing through the both pull-up resistances are equal. Therefore, on this point the differential input $(v_i = V_A - V_A)$ and output $(v_o = V_{OUT} - V_{OUT})$ must be equals to zero. It correspond to the output voltages of $V_{out} = V_{DD} - \Delta V/2$.

The noise margin represents the robustness of a logic gate against external or internal perturbations. In MCML circuits, the noise margin usually is set by process variations and external noise such as crosstalk (BRUMA, 2003). This work takes as reference the method of -1 slope point of the DC transfer gates curve. Figure 2.4 depicts this DC transfer gate curve, in which the axes represent the differential input and output voltages. The used method defines the noise margin as $V_{OHmin} - V_{IHmin}$, where V_{ILmax} and V_{IHmin} are the input voltages that $\partial_{vo}/\partial_{vi} = -1$, then V_{OHmin} and V_{OLmax} are the corresponding output values.

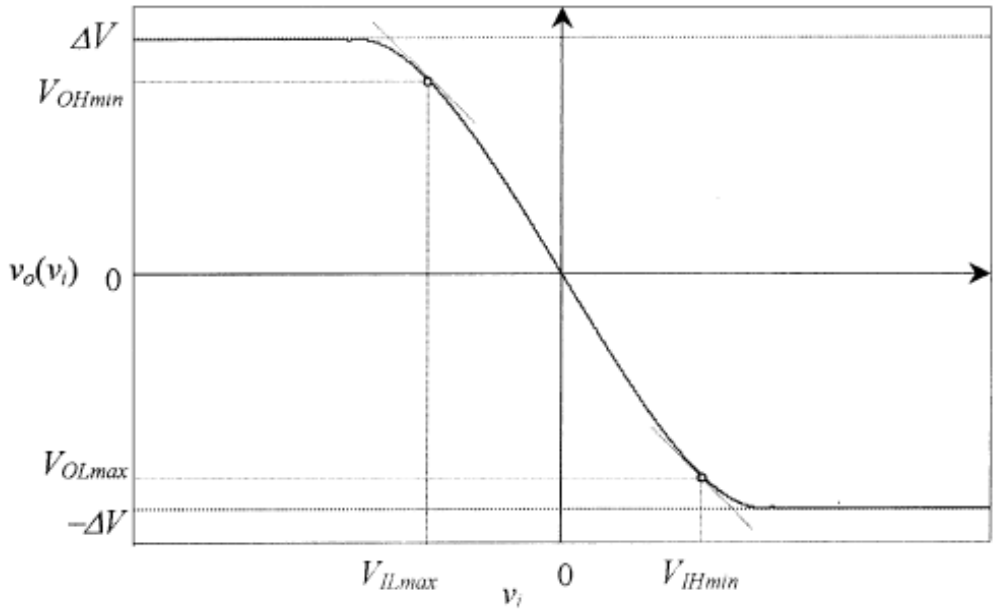


Figure 2.4: DC transfer characteristic of an MCML gate
(ALIOTO e PALUMBO, 2003b)

Mathematically the noise margin of an MCML inverter gate can be obtained from the expressions of currents on each branch of the gate as a function of differential input voltage v_i as follow:

$$i_{D1}\ v_i\ = \begin{cases} 0 & \text{If}\quad v_i < -\sqrt{\frac{2I_B}{\mu_n Cox\frac{W_n}{L_n}}} \\ \frac{I_B}{2}+\frac{v_i}{2}\sqrt{\mu_n Cox\frac{W_n}{L_n}I_B - \left(\mu_n Cox\frac{W_n}{L_n}\frac{v_i}{2}\right)^2} & \text{if}\quad v_i \le \sqrt{\frac{2I_B}{\mu_n Cox\frac{W_n}{L_n}}} \\ I_B & \text{if}\quad v_i > \sqrt{\frac{2I_B}{\mu_n Cox\frac{W_n}{L_n}}} \end{cases} \tag{2.6}$$

where: i_{D1} is the current flowing on a MCML gate branch, μ_n is the charge mobility of PDN transistors, Cox is the gate oxide capacitance, W_n and L_n is the width and length of PDN transistor and I_B is the MCML gate bias current.

Differentiating (2.6) with respect to v_i, setting it to -1 and considering the equation (2.2), is possible find the value of V_{IHmin}. Approximating V_{OHmin} to the voltage swing, ΔV, leads to the following expression of noise margin:

$$NM = \Delta V \left(1 - \frac{\overline{2}}{A_V}\right) \sqrt{1 - \frac{1}{\overline{2}A_V}} \cong \Delta V \left(1 - \frac{\overline{2}}{A_V}\right) \tag{2.7}$$

where A_V is the small-signal voltage gain of the gate. This mathematical process can be found more detailed in (ALIOTO, PALUMBO e PENNISI, 2002).

The small-signal gain of the inverter gate is the gain of a basic differential pair, which is approximated by (RAZAVI, 2001):

$$A_V = R_D \sqrt{\mu_n Cox \frac{W_n}{L_n} I_B} \tag{2.8}$$

where R_D corresponds to the output resistance of the gate, which is equivalent to the ratio between the gate voltage swing and the bias current. Therefore, considering equation (2.2) the voltage gain becomes:

$$A_V = \Delta V \sqrt{\mu_n Cox \frac{W_n}{L_n} \frac{1}{I_B}} \tag{2.9}$$

2.2.3 Propagation Delay

The understanding of the propagation delay behavior and the contributions of design parameters on it is fundamental to achieve an efficient MCML gate design. As already explained in section 2.1, during the switching the complementary outputs undergo an opposite change in voltage. By the symmetrical operation of MCML gates, it is common study the propagation delay based on a half circuit analysis (ALIOTO e PALUMBO, 2003b).

The Elmore delay model can approximate the propagation delay in a digital circuit. In MCML inverter gate, the resistance of the delay model is represented by the ratio between voltage swing (ΔV) and bias current (I_B), that is equivalent to the pull-up gate resistance. Therefore, the general form of Elmore's approximation applied for MCML inverter (Figure 2.2) is the following (ALIOTO e PALUMBO, 2003b):

$$\tau_{PD} = 0{,}69 \frac{\Delta V}{I_B} \, x \, C_{out} \tag{2.10}$$

where C_{out} is the lumped capacitance of output node and is represented by:

$$C_{out} = C_{gd,n} + C_{db,n} + C_{db,p} + C_{gd,p} + C_L \tag{2.11}$$

where, $C_{gd,n}$ and $C_{db,n}$ are the gate-drain and the drain-bulk capacitances of NMOS differential pair respectively. Analogously $C_{gd,p}$ and $C_{db,p}$ are the relative capacitances of PMOS pull-up resistances and C_L is the load connected to the gate.

2.2.4 Power

Once the MCML gates work with a constant bias current, which is steered to the left or right pull-up resistance, these gates present static power consumption. The relation between the power and bias current is given by the following equation:

$$Power = V_{DD} I_B \tag{2.12}$$

Note that the power dissipation of an MCML gate is independent of frequency switching. This power characteristic makes MCML cells more attractive in high-speed applications. Another advantage of static power consumption is the low switching noise obtained. Therefore, it makes MCML circuits attractive for circuits responsible for the interface between the analog and digital world.

2.3 MCML Complex Gates

Now that the functionality of the simplest MCML gate is understood, more complex gates, like combinational logic function and sequential gates can be introduced. Knowing that the PDN is responsible for implement the logic function of MCML gates and these networks are constructed by the association of differential pairs, a binary decision diagram (BDD) may support to find the differential PDN topologies (DA ROSA JUNIOR, SCHNEIDER e RIBAS, 2009). Observing Figure 2.5, each BDD

node is a differential pair, and each branch corresponds to a connection between one transistor drain and the source of another differential pair or an output.

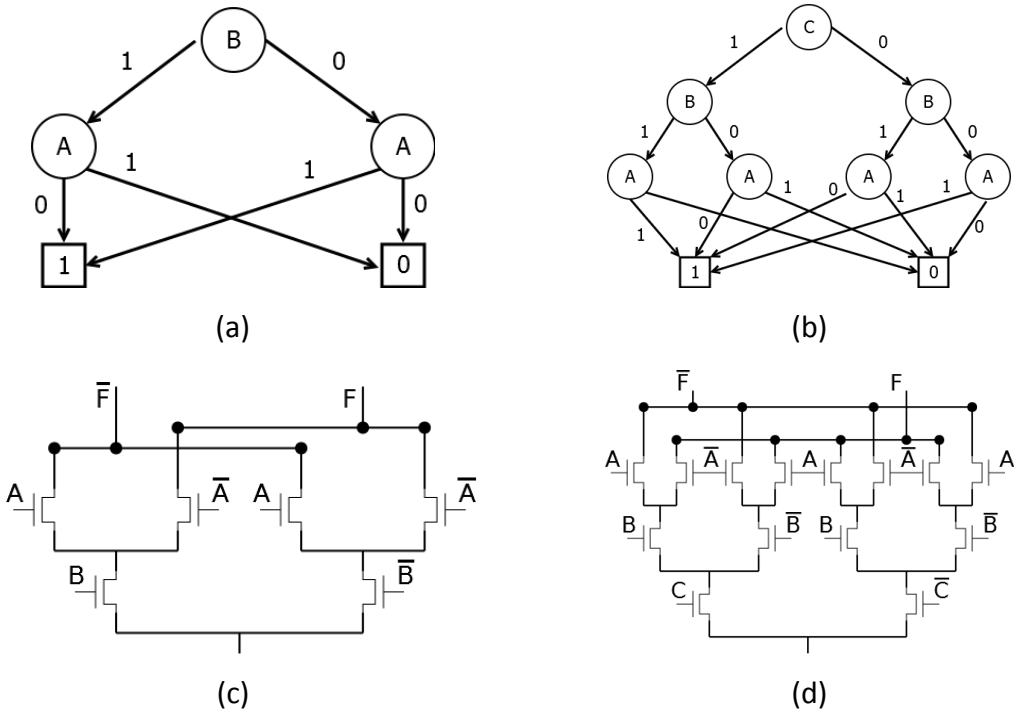


Figure 2.5: Binary decision diagram and pull-down network of exclusive-OR gates: (a) XOR2 BDD,(b) XOR3 BDD, (c) XOR2 PDN, (d) XOR3 PDN.

The number of levels in the logic network increases according to the number of inputs in the target function. For instance, the BDD of a 2-input exclusive-OR (XOR2) is shown in Figure 2.5(a), whereas Figure 2.5(b) represents a BDD of the 3-input exclusive-OR (XOR3). Notice that XOR3 function has three levels in the BDD whereas the XOR2 results in a BDD with only two levels. Figure 2.5(c) and Figure 2.5(d) show the logic network of XOR2 and XOR3 gates, respectively.

PDN uses the reduced ordered BDDs (ROBDDs) to optimize the numbers of transistors in the network. Figure 2.6(a) show the BDD of an AND2 function. Its ROBDD is represented in Figure 2.6(b) and the resultant transistor network in Figure 2.6(c).

The simplification made by ROBDDs can introduce a mismatch of propagation delay and DC output levels, between the two differential outputs. The difference of stacked transistors on the paths of PDN produces this divergence. To overcome this fact, the topology illustrated in Figure 2.7 is proposed by (ABDULKARIM e SHAMS,

Mar 2007). A transistor in the simplified branch is included, and its gate is connected to V_{DD}. The cost of stacking symmetry is the internal capacitances added in the gate.

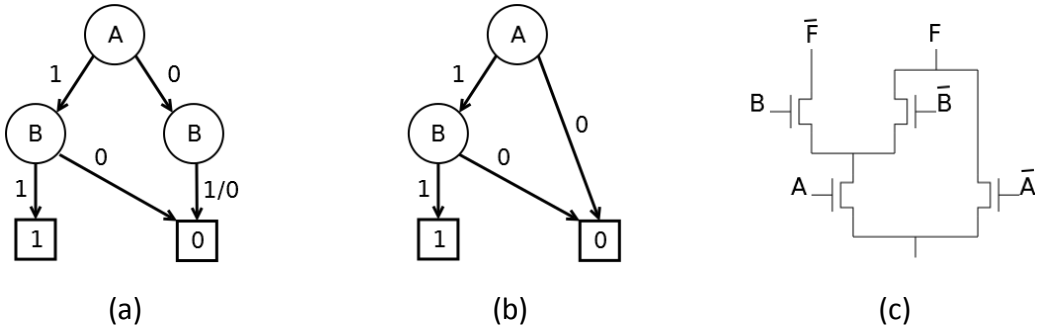


Figure 2.6: (a) BDD of AND2, (b) ROBDD of AND2, (c) corresponding PDN.

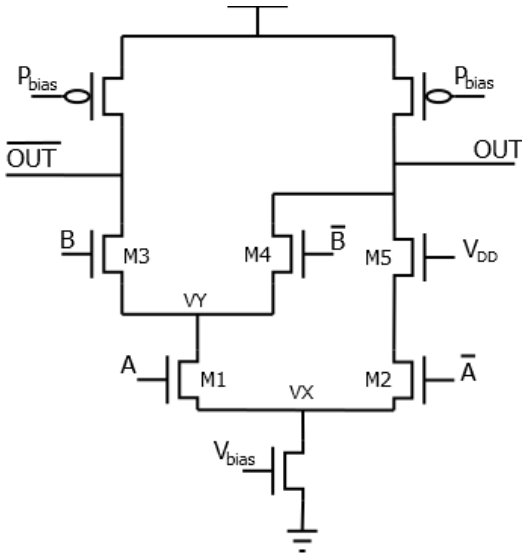


Figure 2.7: AND2 MCML gate topology.

Observe that as in the case of inverter and buffer gates, presented in section 2.2, the negated and direct function present the same topology. To change its function is only necessary change the complementary output nodes. Moreover by De Morgan's Law, the topology of Figure 2.7 implements the functions AND, NAND, OR and NOR gates. The logic function configuration is defined just changing the (in)outputs polarities. This logic function flexibility makes that gate being known as universal MCML gate (KHABIRI e SHAMS, 2004).

2.3.1 Voltage Swing

Section 2.2.1 shows that the voltage swing of an MCML inverter is a function of the differential pair overdrive voltage. Extending the analysis made in that section to a multi-input gate, take as an example the Figure 2.8. Consider that all inputs, A, B and C, are in logic level one (V_{DD}). The bias current will flow through the transistors M1, M2 and M3. In this situation, equation (2.13) calculate the voltage at node Vx.

$$V_X = V_{DD} - (V_T + V_{OV} + V_{ds1} + V_{ds2}) \tag{2.13}$$

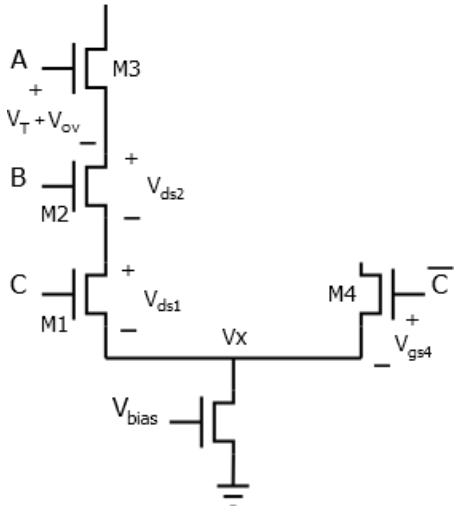


Figure 2.8: Stack transistor effect on voltage swing

Analyzing the opposite branch of Figure 2.8, the complementary input C, that in this case is the logic level zero voltage (V_{Low}), controls the transistor M4. Therefore, its gate should have a voltage that makes the $V_{gs4} < V_T$ to cut-off the transistor, resulting in the inequality (2.14).

$$V_{Low} - V_X < V_T \tag{2.14}$$

Replacing (2.13) in (2.14) and rearranging the equation, results in (2.15). As $\Delta V = V_{DD} - V_{Low}$ the inequality (2.16) gives the lower voltage swing bound for multi input gates (in this case, 3 inputs).

$$V_{Low} < V_{DD} - (V_{OV} + V_{ds1} + V_{ds2}) \tag{2.15}$$

$$\Delta V > V_{OV} + V_{ds1} + V_{ds2} \tag{2.16}$$

Remember that as the voltage overdrive (V_{OV}), the drain-source voltage (V_{ds}) is function of transistor sizing too. Therefore, in a general case the voltage swing lower bound is dependent of the quantity of stacked transistors and its sizing.

The upper bound of voltage swing is the same as for the inverter gate. It depends on the pull-up resistance linearity and the bias current mirror saturation. Note that if is used a voltage swing greater than the NMOS threshold voltage the equation (2.16) changes a little bit. The transistor M3 also operates in a linear region and its source voltage is a function of drain voltage. Therefore, equation (2.13) becomes:

$$V_X = V_{DD} - \Delta V - (V_{ds1} + V_{ds2} + V_{ds3}) \tag{2.17}$$

considering the equation (2.14) and rearranging (2.17) the following inequality is found:

$$V_{Low} < V_{DD} - \Delta V + V_T - (V_{ds1} + V_{ds2} + V_{ds3}) \tag{2.18}$$

Therefore, being $V_{Low} = V_{DD} - \Delta V$, an association between the threshold voltage and drain source of differential pairs voltages must be satisfied:

$$V_T > V_{ds1} + V_{ds2} + V_{ds3} \tag{2.19}$$

hence, for the case where the voltage swing is higher than the threshold voltage, the sum of voltage drop of PDN transistors must be lower than the threshold voltage of these transistors. It agrees with the assertion did before that voltage swing is dependent of the quantity of stacked transistors and its sizing.

2.3.2 Robustness

For complex MCML gates, for example, an XOR2 (Figure 2.9), the noise margin is evaluated considering the voltage characteristic associated with the change of value in one input while the others are maintained constants. Since the other inputs are statics, their correspondent transistors can be considered as an open or short circuits. Therefore, they do not affect the DC analysis of the circuit. For this reason, the noise

margin of a generic MCML gate is the same of an MCML inverter, as presented in equation (2.7) (ALIOTO e PALUMBO, 2003b).

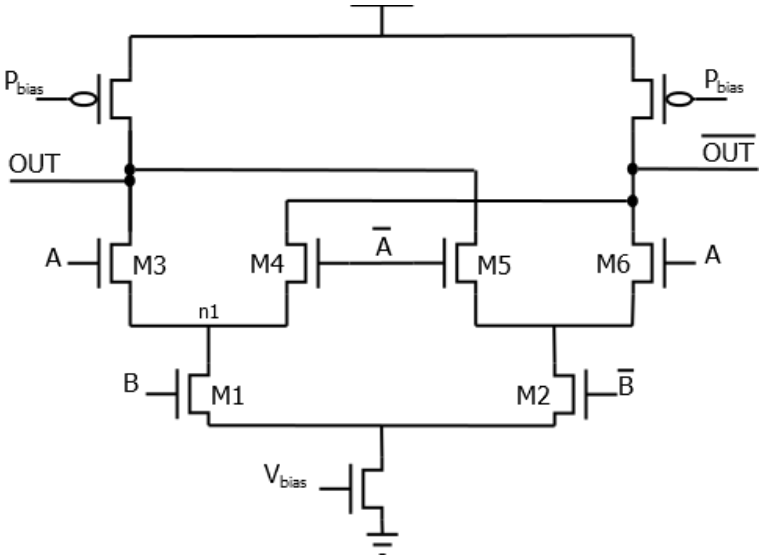


Figure 2.9: Schematic of MCML XOR2 gate.

It is worth noting that all noise margin model presented in this chapter consider the differential pairs operating in the saturation region. It limits the voltage swing to be lower than the threshold voltage. The consequence of the transistors not being saturated is the gain degradation of the gate. When the transistor leaves the saturation region, its transconductance drops, slowly in the beginning and more sharply when entering deeper in the linear region. As consequence degradation on the cell's noise margin happens. This loss in noise margin can be compensated by increasing the size of the PDN leading in a reducing speed and increasing area (BADEL, 2008).

For the case of complex gates, the operation of all differential pairs in the saturation region requires the use of level shifters to access the lower differential pairs' inputs. This insertion adds more power dissipation, an extra propagation delay and an area overhead. These practices are too conservative for high-speed MCML design (CHENG, MUSA e CARUSONE, 2009). Furthermore, the limitation on voltage swing is not beneficial to the MCML standard cell gates as will be discussed in section 2.4.3. Although the operation of the transistors in the triode region reduces the accuracy of the square-law MOS model, the noise margin model presented is a good start point for a simulation based design methodology.

2.3.3 Propagation Delay

In multi-input gates, the stacking of differential pairs adds parasitic capacitances that must be considered on the propagation delay model. Beyond of these parasitic capacitances, the charge and discharge current paths present additional resistances increasing the propagation delay time.

Taking as an example the MCML XOR2 gate, depicted in Figure 2.9, which half small-signal circuit is illustrated in Figure 2.10, the worst case delay is obtained fixing the A input, suppose $A = 1$, and toggle the B input, suppose from 1 to 0. In this case, the current is switched from transistors M3 and M1 to M2 and M6. Note that the capacitance of internal node n1 must be charged up to V_{DD}. There is an additional transistor (M3) that adds an equivalent resistance equals to $1/g_{m3}$ on the path responsible to charge this node. Therefore the propagation delay equation can be expressed by (CARUSO e MACCHIARELLA, 2008):

$$\tau_{PD} = 0{,}69 \left[\frac{1}{g_{m3}} \left(C_1 + C_2 + C_3 \right) + \frac{\Delta V}{I_B} \left(C_4 + C_5 + C_L \right) \right] \tag{2.20}$$

where g_{m3} is the transconductance gain of transistor M3 and:

$$C_1 = C_{gd,1} \tag{2.21}$$

$$C_2 = C_{db,1} + C_{sb,3} + C_{gs,3} + C_{sb,4} + C_{gs,4} \tag{2.22}$$

$$C_3 = C_{gs,3} \tag{2.23}$$

$$C_4 = C_{gd,3} \tag{2.24}$$

$$C_5 = (C_{db,3} + C_{gd,3} + C_{db,5} + C_{gd,5} + C_{gd,p} + C_{db,p}) \tag{2.25}$$

In equations, (2.21) - (2.25) the capacitances index identifies which parasitic capacitance is referred, and the number identify the transistor. More detail of parasitic MOSFET capacitances can be found in (RAZAVI, 2001).

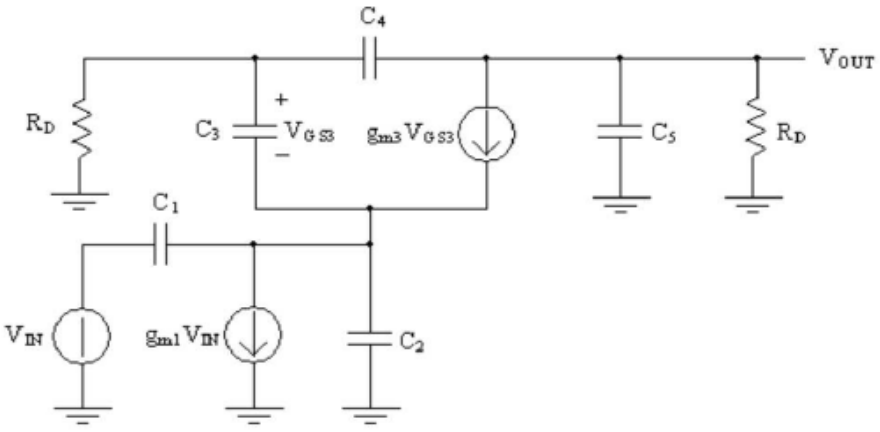


Figure 2.10: MCML XOR2 gate half-circuit small signal circuit (CARUSO e MACCHIARELLA, 2008)

2.3.4 Sequential Logic Gates

Besides the combinational logic, is possible implement sequential logic functions using MCML circuits. A current mode logic latch consists of a sample and a hold stage as illustrated in Figure 2.11. Note that the MCML latch schematic has two levels in the PDN. Therefore, its designs parameters follow the tradeoffs of a MCML XOR2 gate.

The operation of the latch is according to the complementary signals of the clock that control the lower differential pair. When the CLK is high, the current passes through the upper differential pair that is switched by the inputs D and $\overline{D}$. If the CLK is low, the current is steered to the differential pair of cross-coupled transistors that store the data. This topology can be used to form a D Flip-Flop with a master-slave approach (USAMA e KWASNIEWSKI, 2004).

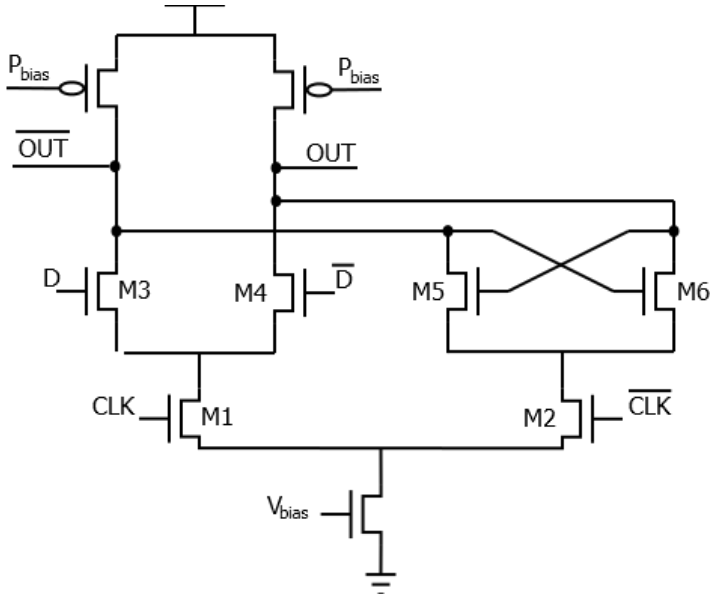


Figure 2.11: MCML Latch.

2.4 MCML Structures Sizing

Now that the MCML design parameters and functionalities were already explained, it is time to understand how to implement the three main structures of MCML gates, i.e. the bias current mirror, the pull-up resistance and the PDN.

2.4.1 Bias current mirror

A current mirror implements the bias current of the MCML gate. The current mirror uses the principle that if the gate-source potentials of two identical MOS transistors are equal, the channel currents should be equal (ALLEN e HOLBERG, 2012). The current of these transistors are different from the ideal situations for two facts: channel length modulation and mismatching between the transistors.

Different techniques can be used to reduce the second order effects of the current mirror. For example mirror cascade are implemented to reduce the channel length modulation effect, on another hand, it reduce the output swing range and represent an area overhead. As in a digital standard cell library the area is an important constraint, a single device implementation is commonly used.

All gates in a circuit share the same bias voltage. To use different bias current in a gate is possible to make transistors with a different aspect ratio from the reference

one. To overcome the mismatch problems is usually used multiple transistors with the same aspect ratio to get more bias current in a gate. This implementation is illustrated in Figure 2.12.

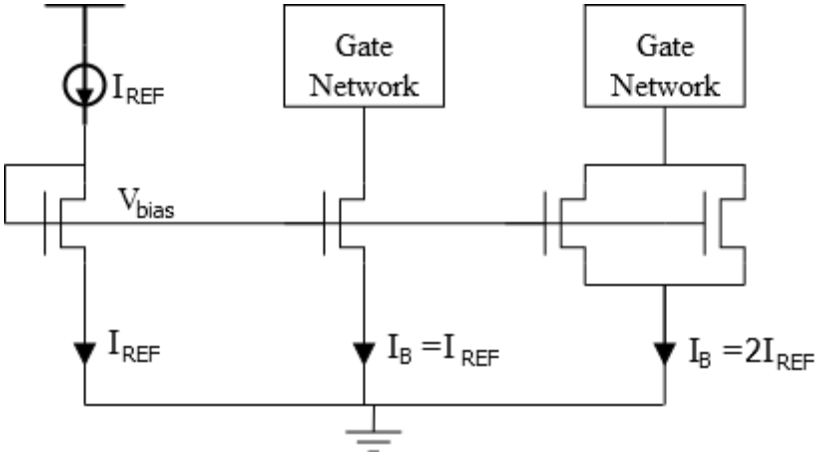


Figure 2.12: Current mirror representation

The current mirror design also is important to determine the common-mode rejection ratio (CMRR). A non-minimum length of NMOS device is used to increase the output resistance of current source, which in turns improves the CMRR and reduce the mismatching of bias current between the gates and the bias reference.

The characteristic equation of saturated transistor give the sizing for the bias current transistor of the gate as follow:

$$W_{Bias} = \frac{I_B L_{Bias}}{\mu_n Cox {V_{OV}}^2} \tag{2.26}$$

where two parameters are technology dependent, μ_n and Cox, that correspond to the charge mobility and gate oxide capacitance respectively. The L_{Bias} is the length of the transistor. The I_B is the bias current of the gate. Finally V_{OV} is the voltage overdrive of the transistor and it is a choice of the designer.

2.4.2 Pull-up resistance

A transistor operating in a triode region implement the pull-up resistances of the MCML gate. To model the resistance of the PMOS transistor, its gate is considered connected to the ground node. This connection imposes a high inversion level on the

gate resulting in mobility degradation. Therefore, the sizing of pull-up resistances take as reference the characteristic MOSFET device equation of the drain current at linear operation condition, considering the mobility degradation effect (RAZAVI, 2001):

$$I = \frac{\mu_p Cox W_P \quad V_{GS} - V_{Tp} \quad V_{DS} - \frac{{V_{DS}}^2}{2}}{L_p \quad 1 + \theta \; V_{GS} - V_{Tp}} \tag{2.27}$$

in which μ_p, Cox and V_{Tp} depends on the technology used, and correspond to the charge mobility and gate oxide capacitance and threshold voltage respectively. V_{GS} and V_{DS} are the gate-source and drain-source voltages. θ is the mobility degradation parameter. This parameter is extracted through a curve fitting process. L_p is the transistor length.

Rearranging (2.27) and taking into account that the gate-source voltage of PMOS transistor is the supply voltage, the drain-source corresponds to the gate voltage swing and the total current is the bias current of the gate. The equivalent equation is the following:

$$W_P = \frac{I_B L_p \quad 1 + \theta \; V_{DD} - V_{Tp}}{\mu_p Cox \quad V_{DD} - V_{Tp} \quad \Delta V - \frac{\Delta V^2}{2}} \tag{2.28}$$

in which μ_p, Cox and V_{Tp} depends on the technology used, and correspond to the charge mobility and gate oxide capacitance and threshold voltage respectively. V_{DD} is the supply voltage of the gate. I_B and ΔV are characteristic parameters of the gate corresponding to the bias current and voltage swing respectively. θ is the mobility degradation parameter. This parameter is extracted through a curve fitting process. L_p is the transistor length. In order to reduce the mismatching between the two equivalent resistances, these transistors use non-minimal value of channel length.

To improve the physical implementation of the MCML circuits, the gate of PMOS transistors are connected to a bias voltage ($Pbias$) instead of to a ground node as cited before. This bias voltage comes from a feedback loop control circuit that compensates the PVT variations, Figure 2.13. The bias control circuit takes the drain

voltage of the PMOS transistor and compares it with the reference voltage (V_{REF}). The difference between these two voltage sets the output voltage of an operational amplifier. This output controls the PMOS gate to equalize the low logic level voltage with the reference one ($V_{REF} = V_{DD} - \Delta V$).

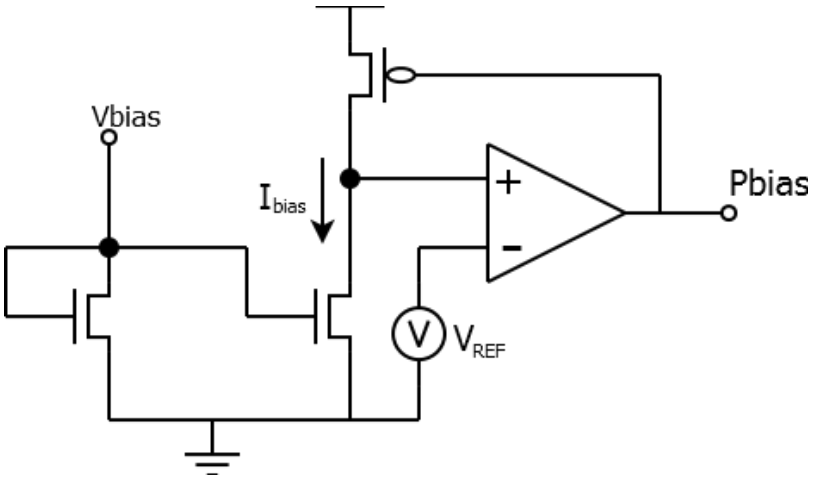


Figure 2.13: On-chip PMOS bias control circuit.

2.4.3 Pull Down Network

The topologies of PDN were present in section 2.3. This section gives some guidelines to the PDN sizing and the influence of design parameters on it.

Taking into account only the performances constraints, there is no advantage the use of a non-minimum length on these transistors. The increasing of these lengths degrades the propagation delay by adding parasitic capacitances in the gates. The chosen length influences the noise margin too. Bigger lengths reduce the voltage gain of the cell and as a consequence the noise margin. The only reason to use a non-minimum length on PDN transistors is to reduce the impact of possible process variations (HASSAN, ANIS e ELSMASRY, 2005). Since, in a standard cell library design, area is an important constraint, this work uses a minimum transistors length on the PDN. Fixing the transistors lengths, the aspect ratio of the transistors is controlled only by the width.

In a digital standard cell design, it is important noting that the PDN sizing influences not only the internal parasitic capacitances of the gate but also the output capacitances connected to them. Digital circuits are composed of several chains of digital standard cells. Therefore, the load of one gate are other gates. Usually digital

standard cell gates are designed taking into account a load of fanout four. It is equivalent to say that one gate has as load another four gates equal to them.

According to the equations (2.7) and (2.9), beyond of the technology parameters, the PDN sizing is a function of the bias current, voltage swing and noise margin of the cell. All these parameters are a designer choice. In general terms, a reduction in the voltage swing requires an increasing on the transistor width to achieve a higher small-signal voltage gain and, as a consequence, reach the required noise margin. The same behavior occurs for an increase in the bias current.

On the other hand, equations (2.10) and (2.20) demonstrate that the cell's propagation delay is a function of PDN sizing. Larger transistors imply in a higher output capacitance load for the gate increasing the propagation delay.

Therefore, the goal of PDN sizing is: find the smallest transistors width that is capable of achieving the required gain and as a consequence the specified noise margin of the cell. This minimum sizing is desirable to add the lowest amount of load and internal parasitic capacitance to the gate.

3 DESIGN METHODOLOGY

As cited in chapter 2, the MCML digital gates design has three main design parameters that are the bias current, output voltage swing and noise margin. These design parameters are correlated among themselves. This MCML characteristic makes the MCML design complex and time consuming. In order to reduce design time and complexity, it is possible to create an MCML standard cell library for synthesizing complex designs through pre-characterized gates and available EDA tools. On the other hand, an efficient design methodology must be used to generate a cell library that reaches the circuit specifications.

Previous works already made studies in that way. (MUSICER, 2000) presents a simulation-based design methodology without the use of analytical formulations. Although this methodology provides accurate results, the designer must try a range of design parameters and test if each parameter reaches the target design.

In (ALIOTO e PALUMBO, 2003b), analytical expressions were developed for the MCML inverter gate and the correlations between the circuit performance and circuit design parameters were addressed. Their work was extended to a two-level MCML gates in (ALIOTO e PALUMBO, 2003a).

The challenge of design two-level MCML gates was also addressed by (HASSAN, ANIS e ELSMASRY, 2005) and (OSMAN e MAITHAM, 2010). Those works explore the best relation between bias current, voltage swing and PDN differential pairs sizing to optimize the propagation delay and power consumption of the gates. The optimizations consider that each level of differential pairs can be sized with a different width. These works are based on analytical formulations, and the design solution is obtained through a mathematical solver software. The drawback of the design optimization based on analytical models is the precision of the solution. The first work presents an accuracy of 11% and the second one an average error of 3.6% with a maximum error of 12%. Note that these precisions are dependent of the technology parameters extractions and some parameters should be added to consider the process variability in the advanced technology nodes.

3.1 Proposed Methodology

The proposed methodology focuses on an easy adaptability for different technology nodes. All works cited before did an analysis on a large space of choice of bias current and voltage swing, in other words, for each combination of bias current and voltage swing a solution of transistor sizing is found. Therefore, the solution is the best power-delay trade-off.

Some technology parameters are operating transistors functions. For example, the charge mobility and threshold voltage change according to the inversion channel level, transistor sizing, source-bulk (body effect) voltage, among others. For a large space of choice analysis, analytical models are complex and dependent on some fitting curves parameters, which in sometimes, cannot satisfy all design cases. The consequence is a decreasing on the accuracy of the model. In order to overcome this problem, the proposal is a simulation-based methodology.

In contrast on (MUSICER, 2000), this work takes into account simple mathematical models to find the initial values of MCML gates sizing. After that, according to the simulation results, the method defines the transistor which must be resized to a lower or greater value. Next, the methodology re-simulate the circuit and check some parameter results. These iterations are done until finding the target specifications. At the end, the solution is already validated with BSIM models. Figure 3.1 illustrates the steps of the proposed design methodology.

The following sections describe each methodology step, pointing the boundary specifications and the testbenches circuits used. Note that the boundary values are associated with some error tolerances. These tolerances are necessary once that the methodology use discrete transistors sizing values. Therefore, the methodology is not able to achieve any value. The tolerance values are chosen through a calibration process that take into account the methodology input values and circuit performance results that not are prejudicial to the correct circuit functionalities.

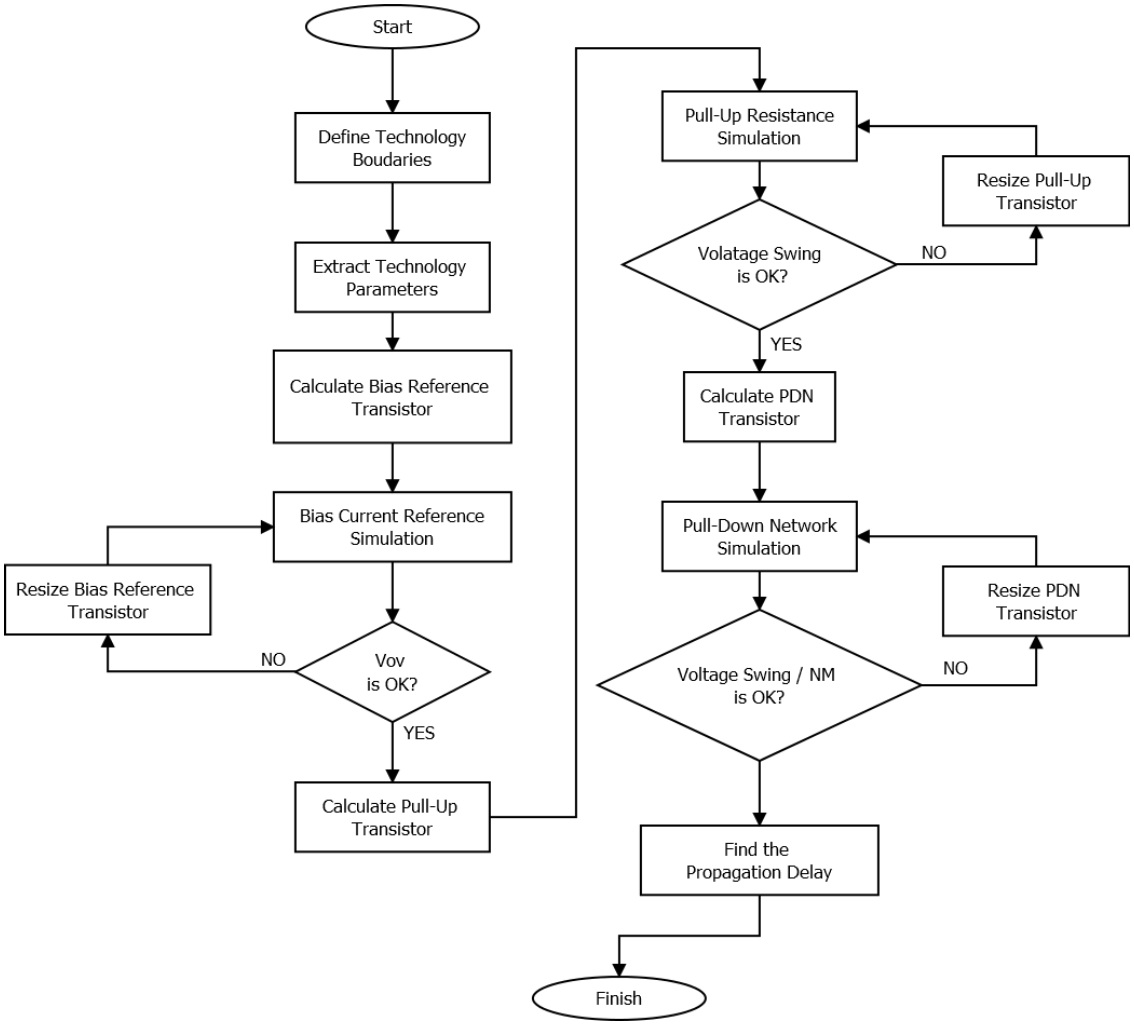


Figure 3.1: Design methodology flow chart.

3.1.1 Technology Parameters

The proposed methodology depends on some limitations determined by the used technology. The user set the voltage supply, minimum transistor sizing and the range of bias current and voltage swing that must be analyzed. Another parameter that depends on the designer experience is the voltage overdrive of the current mirror transistor. Therefore, this value should be previously defined.

Based on the technology parameters specified by the designer, the methodology uses the transistor quadratic model to find the first iteration sizing parameters. According to the models presented in chapter 2, some technology parameters are required. In order to obtain a better first circuit sizing approximation, the methodology

perform an SPICE simulation to extract the transistor gain parameter ($\mu_n Cox$) and threshold voltage (V_T).

The simulation takes as reference a length three times larger than the minimum one and a width ten times 10 larger than the minimum value. This length value approximates the values used in the current bias mirror and pull-up network transistors. Note that the transistors of PDN use minimum length transistors. Therefore, although this parameter extraction does not satisfy all transistors of the circuit, the extracted parameter gives an approximation for the first transistors sizing of the circuit. The imprecision of the values will be compensated by the methodology iterations as will be explained in the following chapters.

The gate and drain of the NMOS transistor are excited by the supply voltage, and the NMOS source is connected to the ground node. This configuration extract the parameters for a nom minimum sizing for the NMOS transistors and a high inversion channel level because of the supply voltage applied to the gate terminal. Similarly the technology parameters of PMOS transistor also are extracted connecting the transistor in a diode configuration and applying a source-gate voltage equal to the supply voltage.

A SPICE simulation is performed, and the operational point response (.OP) provides the gain parameter, which corresponds to the “beta” parameter of SPICE results, over the transistor aspect ratio $\frac{beta}{(W/L)}$. The threshold voltage of transistors is directly found as the "V_{th}" parameter in SPICE solutions. Note that there are other methods to extract the cited parameters. This work uses the extraction through spice simulation due to the quickly and easily extraction process that is not affected by the technology node changes.

3.1.2 Bias Current reference

After determining the technology parameters, the proposed methodology starts from the bias current design. As cited in section 2.4.1 a current mirror implements the bias current source of the MCML gate. Equation (2.26) defines the first sizing of the bias current transistor. Notice that for the L_{Bias} is considered a non-minimum value. The gain parameter, $\mu_n Cox$ was previously obtained and the voltage overdrive, V_{OV} is a choice of the designer, usually is a few cents of millivolts (100mV ~ 200mV). This

value guarantees an acceptable transistor inversion level to reduce the mismatching effects of current mirrors.

The procedure uses some iteration to obtain the desired voltage overdrive of the reference bias transistor. According to (2.26) if the voltage overdrive is higher than the target the transistor width should be increased, otherwise the transistor sizing is reduced. This iteration happens until the voltage overdrive achieves an error lower than 10% of the desired one. The indicated percentage gives a tolerance in relation to the exact value once that the methodology uses discrete values of transistor width. Therefore, this tolerance is not prejudicial to the circuit performance and is able to be achieved by the methodology.

The testbench circuit consists of an ideal current source injecting the desired current into the drain of NMOS diode connected transistor, which makes its drain and gate-source voltage equals and guarantees the operation in the saturation region.

As explained in section 2.4.1 this transistor sizing is a reference to design the bias current mirror of the MCML logic gates. Different bias currents are obtained in a gate connecting multiple transistors, with the same sizing of this reference, in parallel. The gate of these transistors receive the bias voltage created by this reference.

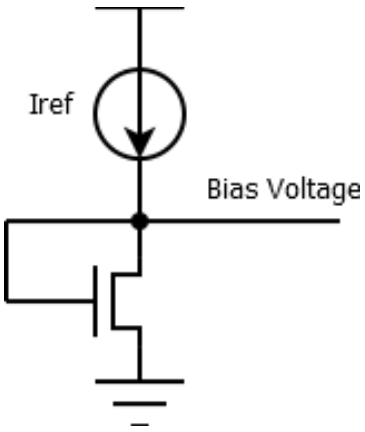


Figure 3.2: Testbench circuit for current mirror reference.

3.1.3 Pull-up Resistance

According to section 2.4.2, a PMOS transistor operating in a triode region implements the pull-up resistance of the MCML gates. This resistance is responsible for

determining the voltage swing of the cell. Since the voltage swing is the voltage drop on this transistor, its sizing is obtained through the characteristic equation of the transistor operating in a linear region where its V_{DS} is the desired voltage swing. Therefore, given a bias current and the technology parameters, the first transistor sizing approximation is calculated by equation (2.28). It is worth noting that if the resultant transistor width is lower than the minimum one, the minimum value is set to the transistor width and a new length is calculated to the transistor by a rearrange equation.

The testbench circuit for the pull-up transistor, depicted in Figure 3.3, consists of the PMOS transistor which source is connected to the supply voltage. Its gate is controlled by the *Pbias* voltage that comes from the output of the operational amplifier present in the swing control circuit. The drain terminal is connected in an ideal current source that generates the chosen bias current. The inputs of the operational amplifier are the PMOS drain voltage, which corresponds to the low logic level voltage produced by the voltage drop of the pull-up transistor, and a reference voltage that comes from an ideal voltage source. This ideal voltage source gives the desired low logic level voltage. Focusing in an easily adaptable of methodology among different technologies, the operational amplifier is a Verilog model.

The proposed design flow analyzes two parameters of the testbench circuit: the *Pbias* node voltage and the transistor drain voltage V_{Low}. The first parameter must be maintained in a low value, closer to ground voltage. This polarization guarantees a larger range of linear operation region. It is worth noting that for a non-ideal operational amplifier this voltage does not achieve the absolute zero value because of his circuit topology. On other hand if, on a real application, the *Pbias* voltage is greater than the desired one, the pull-up transistor performs a higher resistance than the target resistance. This increase in the equivalent pull-up resistance can be prejudicial to the propagation delay of gates, but this behavior plays a more reliable operation with a higher voltage swing and cell's gain.

The boundaries used in the proposed methodology, to the *Pbias* voltage, are the ground and a percentage of the supply voltage, in the studied case 10%. Note that the Verilog amplifier model is able to output a negative *Pbias* voltage if the pull-up transistor width is smaller than the desired value. In this case the proposed methodology increases the transistor width to a value that produces a positive *Pbias* voltage. In the opposite case, greater transistor width, the *Pbias* present a value higher than the

boundary case. Hence, the procedure sets the transistor width to a lower value. This analysis continues until the *Pbias* voltage reach a value that satisfy the boundaries of the proposed methodology.

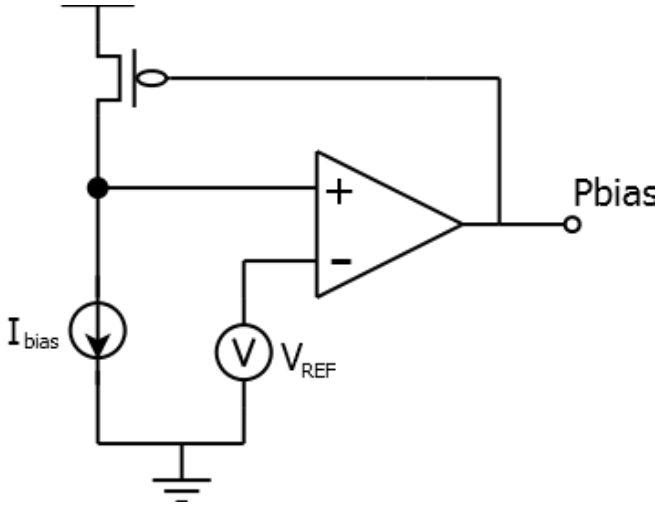


Figure 3.3: Pull-up resistance sizing circuit

The second analyzed voltage (V_{Low}) represents the lower output logic level voltage and must satisfy the equation (3.1)

$$V_{Low} = V_{DD} - \Delta V \pm \varepsilon \tag{3.1}$$

where, ΔV is the target voltage swing and ε is an error margin. In the studied case this margin is set to a value equals to a 5% of voltage swing.

A V_{Low} lower than the required voltage means that the transistor performs a resistance greater than the desired value. Then, the design routine increase the transistor size. The opposite case, V_{Low} greater than the target, produces an MCML output voltage swing smaller than the desired value. In this case the PMOS transistor width is lowered. Notice that if the PMOS transistor width achieve the minimum technology value an increasing on the transistor length becomes necessary.

3.1.4 Pull-down Network

The MCML gate sizing methodology analyzes a PDN sizing for each desired combination of bias current and voltage swing. According to section 2.2.2, the PDN sizing must be sized to achieve the required cell's noise margin. Taking into account that the noise margin is proportional to the transistors width, an excessive noise margin imply an increasing in the gate's capacitances, and according to the equations (2.10) and (2.11), it is prejudicial to the frequency response of the gate.

The methodology takes as reference the equation (2.7) to find the initial sizing of the PDN transistors. Note that independent of the numbers of cell's inputs, the first sizing approximation is the same. On the other hand, equation (2.5) and (2.16) show that it is not true. This difference is taken into account during the methodology simulations.

A DC analysis gives the gate's sizing performance. This simulation performs a DC-sweep in one input of the gate maintaining the others at fixed level. Note that the static inputs must be excited by the MCML logic level that depends on the gates sizing. Therefore, a chain of three MCML gates, with the same sizing of the gate that is under simulation, produces these voltages levels. Figure 3.4 illustrates this chain, where the signals POS and NEG are the static signals that are applied in the DC analysis.

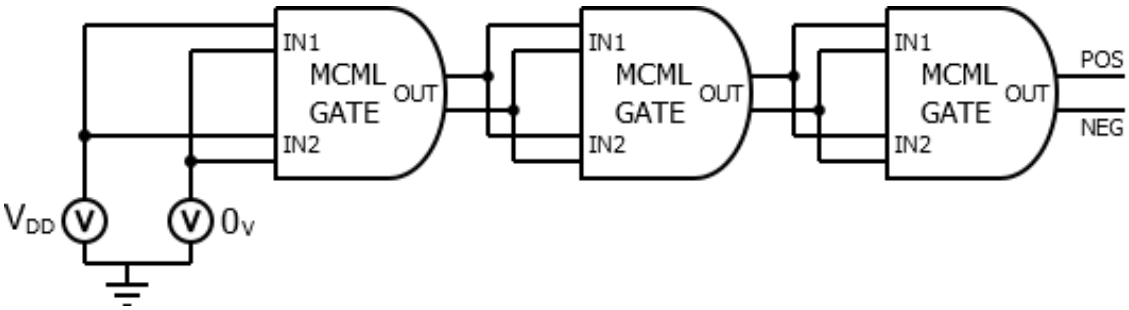


Figure 3.4: Circuit of the static voltage levels signals.

The analyzed input receives the signal from ideal voltage sources that changes its value from V_{DD} to V_{Low} in an input and from V_{Low} to V_{DD} in the complementary one. Figure 3.5 depicts this testbench circuit. The DC waveform gives the characteristic gain, noise margin and effective voltage swing of the gate.

At this step, the MCML gate under analysis has already sized its bias current and the pull-up transistors. The methodology uses some boundaries to find the required sizing of the PDN. The first boundary is the effective voltage swing. This boundary represents the minimum voltage swing that the designed gate must achieve in a static operation. An ideal MCML gate is able to mirror the desired bias current and steer all this current to one of the pull-up transistors.

Note that this behavior does not occur in a real application. The channel length modulation of the bias current mirror transistor has as effect a different value of current bias produced in the gate. Another fact considered in the effective voltage swing value is the amount of current that really is steered in each gate branch. It is known that the transistors in the cut-off branch are not ideally off. Therefore, this branch can conduct a few percentage of the bias current. These two facts degrade the effective voltage swing of MCML gates. In the studied case the effective voltage swing boundary is 80% of the target output voltage swing. This value guarantees that the MCML gate is able to output the correct DC behavior. This output is important to the correct analysis of the next PDN boundaries that appear in this section.

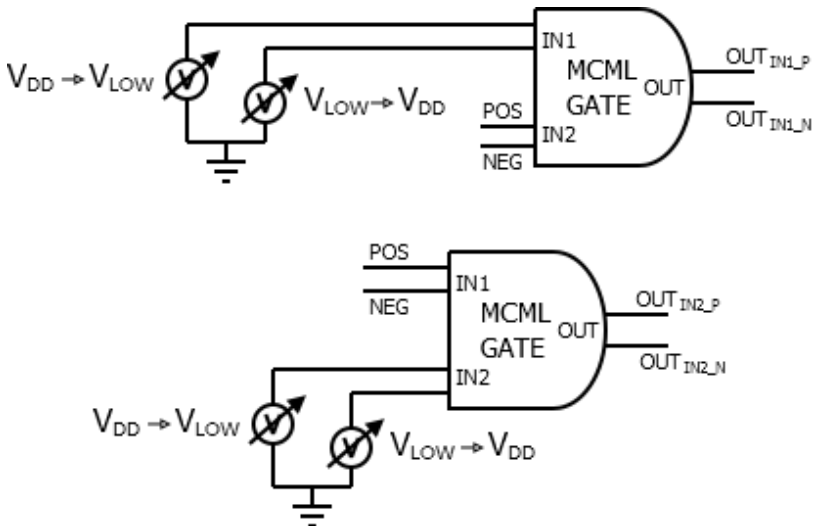


Figure 3.5: Testbench for the DC analysis of MCML gate.

Another boundary to the PDN sizing is the derivative of output waveform. The derivative of DC waveform corresponds to the gain of the gate. Therefore, the gain at the point where both inputs are equal, i.e. the differential input is zero should be higher than the unity in order to reliably propagate the signal. The gain is also correlated to the

gate noise margin. When the input is equal to V_{IHmin} and V_{ILmax} the derivative must be closer to one. Note that if this value is lower than one, the MCML logic gate presents an excessive noise margin and its PDN transistors can be reduced. A poor noise margin occurs in the opposite case, when the transistors sizing must be increased.

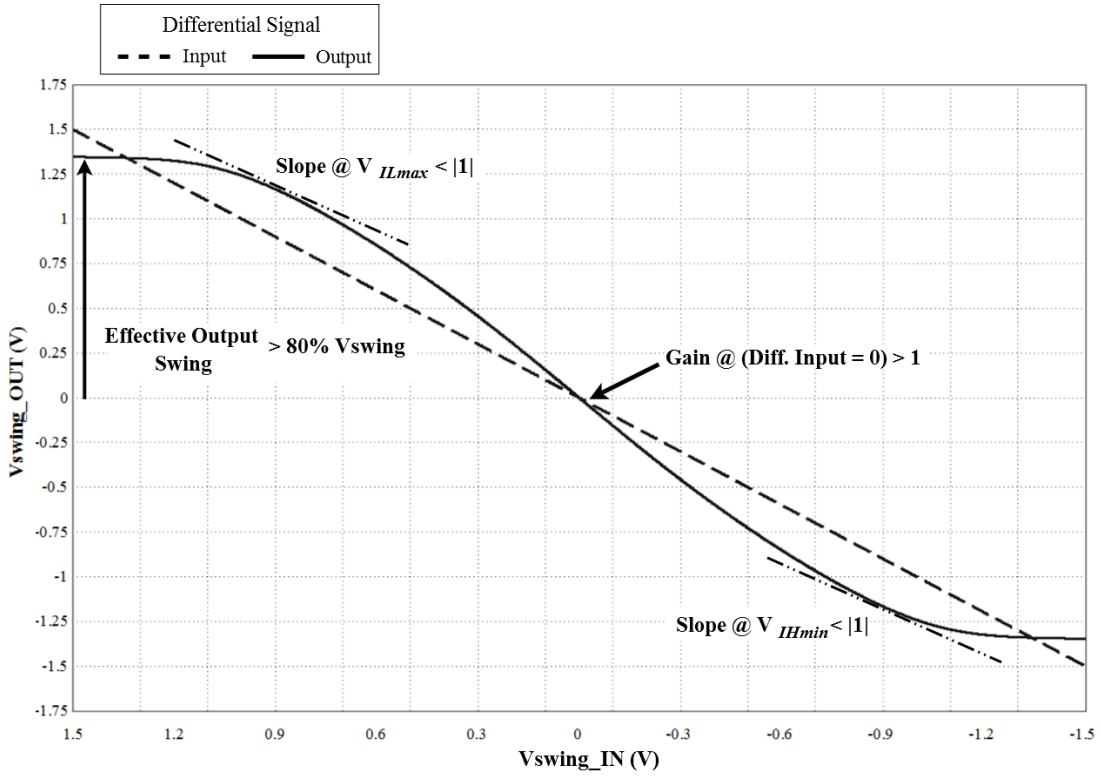


Figure 3.6: Waveform boundaries for PDN sizing.

Note that this methodology considers the same sizing for all PDN transistors. Although it could degrade the propagation delay performance, it brings symmetry to the physical implementation. The standardization of structures helps to apply the layout mismatching aware techniques and in some cases resulting in a smaller gates layout.

3.1.5 Propagation Delay Analysis

This routine analyze the propagation delay of the gate, after that the methodology finishes the gate sizing for a predefined robustness. As cited before, usually a standard cell library design take as reference a gate load equal to four times it input capacitance. Therefore, the testbench for the propagation delay extraction of the

combinational cells consists of a chain of five designed MCML logic gates. Each chain stage presents a fanout four. Figure 3.7 illustrates this topology.

Two ideal voltage sources excite the chain circuit with complementary signals. These signals consist of an ideal square wave. The signals are applied to one input while the others input are static. The static level comes from another chain of gates as represented in Figure 3.4. The propagation delay time of the fourth gate is extracted.

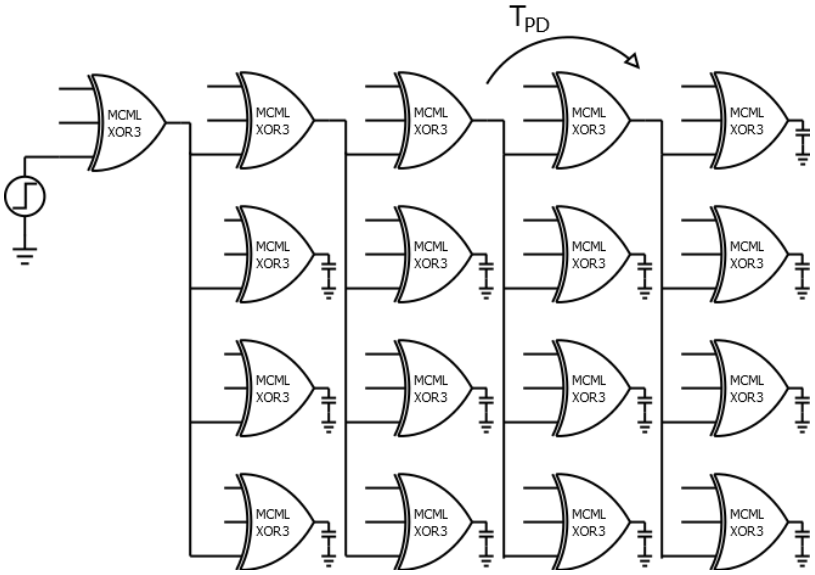


Figure 3.7: Testbench for propagation delay analysis, this is an XOR3 example.

The propagation delay performance of the Flip-Flop gate is different from the combinational gates. The main propagation delay of this gate is the time between the transition at the input clock signal to the output transition. This propagation delay is known as the clock-to-q (CK2Q) delay. The application of Flip-flop in logic circuits also is different from the combinational cells, generally, FF gates are used as registers between logical paths. Therefore, in digital circuits, the FF has as loads combinational gates, and not others FFs. Note that it could be not true in the case of preescalers.

The proposed strategy takes as metric the use of the gates in digital circuits. Therefore, the testbench constructed to obtain the FF gate propagation delay uses, as the excitation of the FF, a clock signal that pass through a MCML buffer gate. An XOR2 gate provides the signal of the D input, and the load is four buffer gates. Figure 3.8 illustrates this testbench. The circuit of Figure 3.4 provides the POS and NEG signals connected in the XOR2 gates.

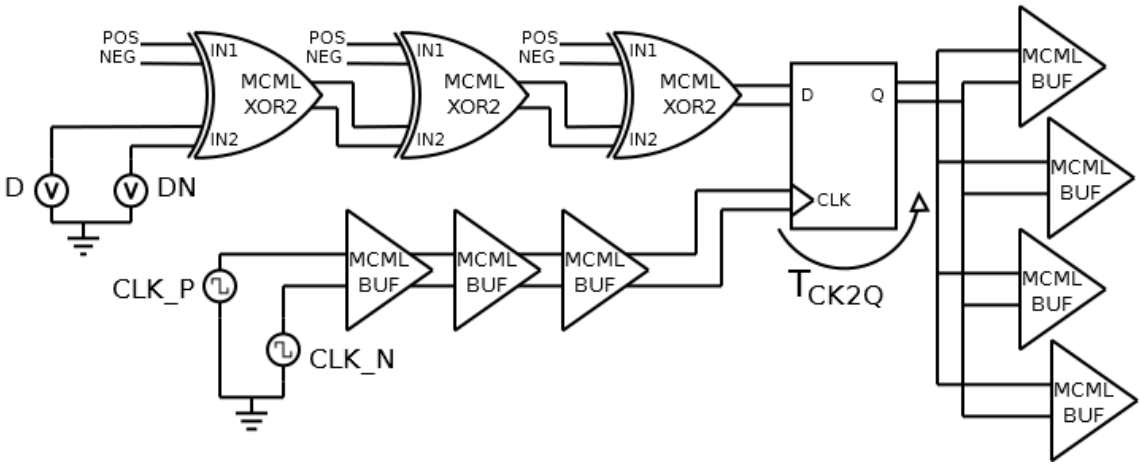


Figure 3.8: Flip-Flop propagation delay testbench.

3.2 Sizing Analysis and Results

The proposed methodology was applied to three different technologies: XFAB06, IBM130 and an predictive model PTM45. This section show the results obtained for each technology. A comparison with an optimizer software is done.

3.2.1 XFAB XC06

The XFab XC06 technology is a mature technology. Table 3.1 display the MOSFETs technology parameters of this technology. The procedure size the gates with a range of current bias that goes from 15µA up to 150µA, and analyze the output voltage swing from 500mV up to 1.8V. These ranges are able to demonstrate the behavior of the MCML gates as function of bias current and voltage swing in this technology. The minimum length specified for the bias current mirror and pull-up transistors was 1µm to overcome the process variability.

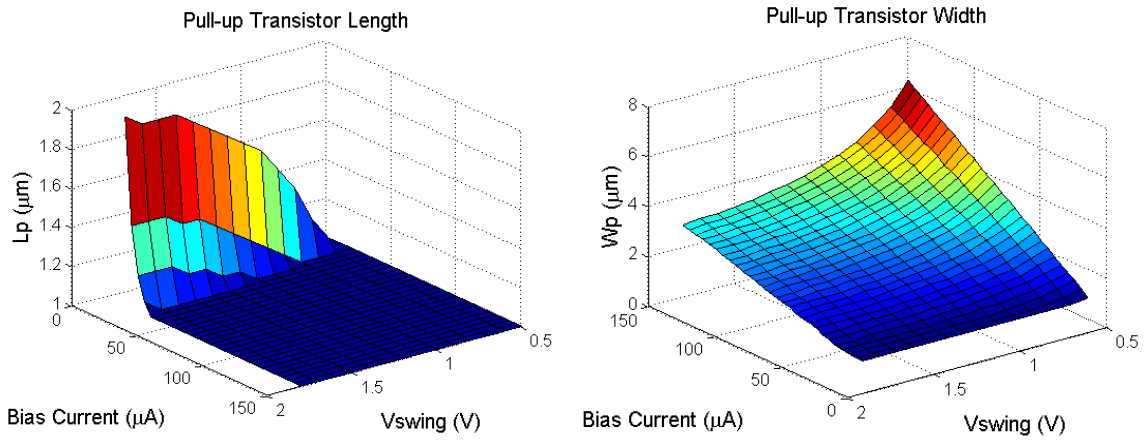
Table 3.1: XFab XC06 technology parameters.

V_{DD}	3.3V
Vth0n	0.87 V
µnCox	117 µA/V²
Vth0p	- 0.9 V
µpCox	40 µA/V²
Lmin	0.6 µm
Wmin	0.8 µm

Figure 3.9 shows the pull up transistor sizing. This sizing has as objective to achieve the required pull-up resistance. It is well known that small resistances correspond to a high W/L ratio. High resistances are achieved in the opposite case. Pay attention that the graph of Figure 3.9 (a) and Figure 3.9(b) has the bias current axis inverted between them for a better presentation.

Note in Figure 3.9(a) that for greater bias current the transistor length is the lowest value indicated in the methodology. This parameter only change in the case of transistor width achieves the minimum value, and the equivalent resistance needs a further increasing. This only occurs for a small bias current.

According to Figure 3.9(b) the pull-up transistors width changes linearly with the bias current change. In other point of view, the width decreases with the voltage swing increasing, but it seems to saturate the decreasing when voltage swing achieves high values. Referring to equation (2.28), note that there is a term associated with the square of voltage swing in the denominator, which causes this behavior.



(a) (b)

Figure 3.9: Pull-up resistor (a) length (b) width of buffer gate versus bias current and voltage swing parameters.

The Figure 3.10 illustrates the pull-down network sizing of the gates. All graph present the same behavior, greater transistor width for high current, small voltage swing gates. The smallest sizing occurs in the opposite case. The noise margin of the gates leads to this sizing behavior. Therefore, as referred in equations (2.7) and (2.9) the width has a linear correlation with the bias current, and an almost quadratic relation with the voltage swing. Furthermore, as cited in section 3.1.4, each graph present

different values of transistors width. The lowest values occurs for one input gate, these width increases in the two input gates and achieve the greatest values for three input gates.

The methodology presented, after the gate sizing, makes a simulation to extract the propagation delay of each logic cell. These simulations take as reference a fanout of four. The graphs below present these results.

Figure 3.11 presents the results for the buffer/inverter gate. According to Figure 3.11(a) the use of greater voltage swings associated with small bias current is not a good practice. The reason for this behavior is that, although greater voltage swings lead a small PDN transistors and load capacitances, the increase in the length of the pull-up transistors makes its parasitic capacitances be dominant over the load capacitances. Therefore, the pull-up transistors sizing increases the propagation delay. When is taking into account gates with large bias current, the PDN sizing has more impact on the propagation delay and as a consequence higher voltage swing is preferred.

Figure 3.11(b) presents the best gate propagation delay versus the bias current used. Note that this graph shows results independent of the voltage swing. In other words, for each bias current was found the voltage swing that produces the best propagation delay response and this delay is printed in the graph. In resume, bias currents below 50µA present delays much higher than the delays founded in larger bias current. Changing the bias current from 15µA to 50µA the propagation delay gain is around 15%. But, above 50µA, the improvement is no more significantly. A bias current of 150µA only produces a gain of 5% in the propagation delay when compared with the same performance at a bias current of 50µA.

The Figure 3.12 presents the results for the exclusive-OR2 gate. The Figure 3.12(a) presents the delay as a function of bias current and voltage swing. The graph presents two surfaces; the lower one illustrates the propagation delay of the input that controls the upper gate differential pairs, the upper surface is the propagation delay of the lower input, i.e. the input that controls the lower gate differential pair. As expected the lower differential input presents higher propagation delay. The behavior according to the bias current and voltage swing is almost the same of the buffer gate. It is advantageous to use smaller voltage swings to a low bias current and greater voltage swing for high bias currents.

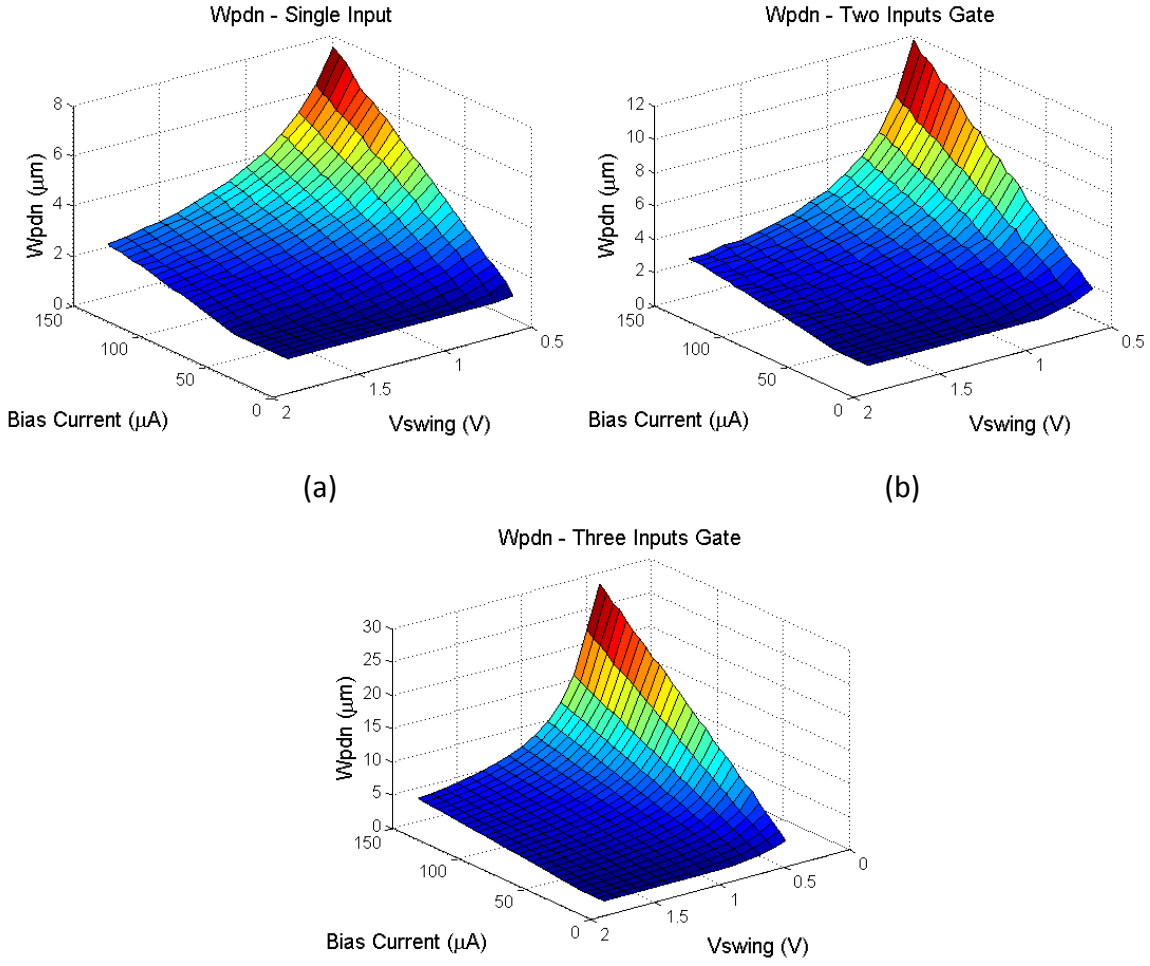


Figure 3.10: PDN width of MCML gates with (a) one; (b) two; (c) three inputs versus bias current and voltage swing parameters.

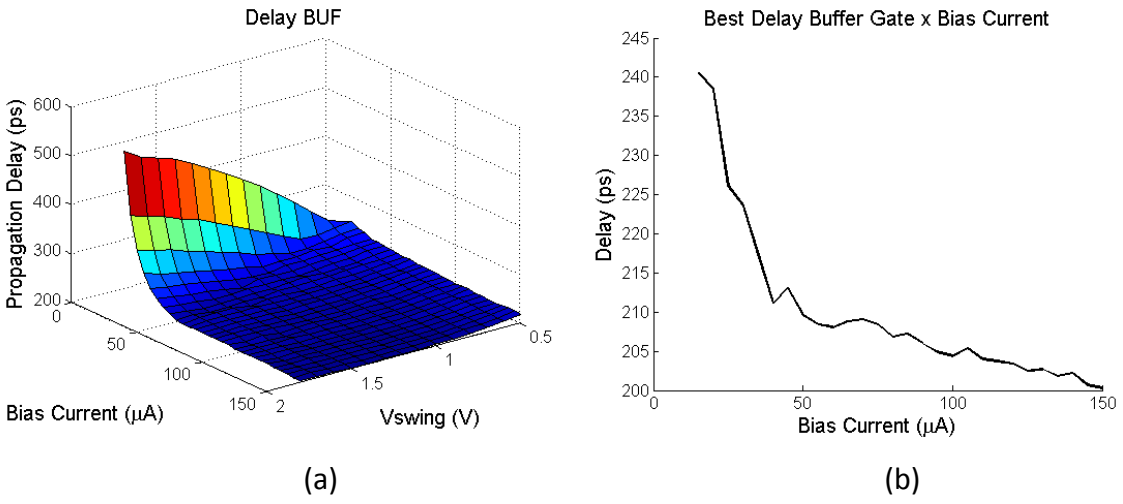
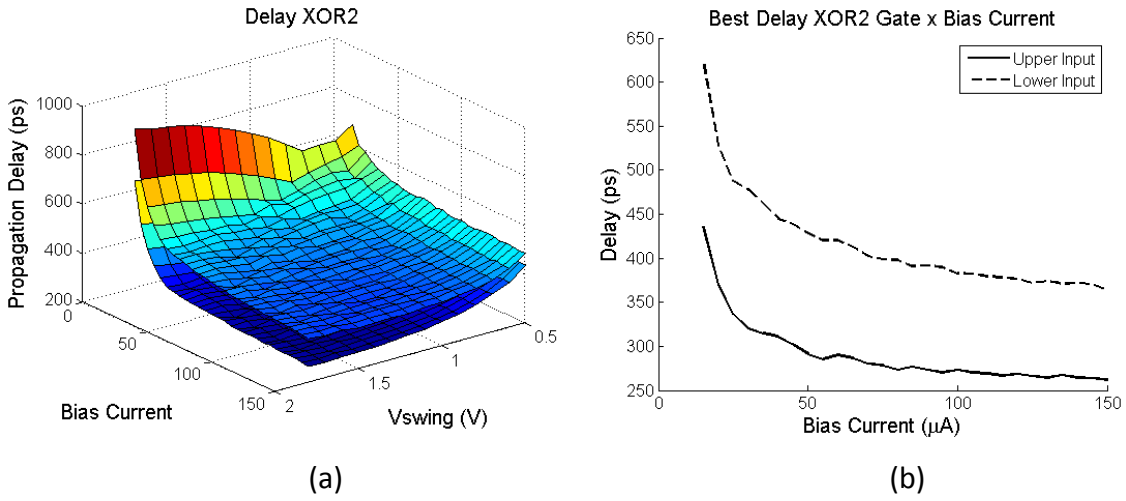


Figure 3.11: (a) Delay of buffer gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the buffer gate.

Analyzing the best propagation delay achieve for each bias current, Figure 3.12(b), the increase in bias current present a gain in the propagation delay up to a value around 50µA. Above this value, the propagation delay gain is no more so significant.

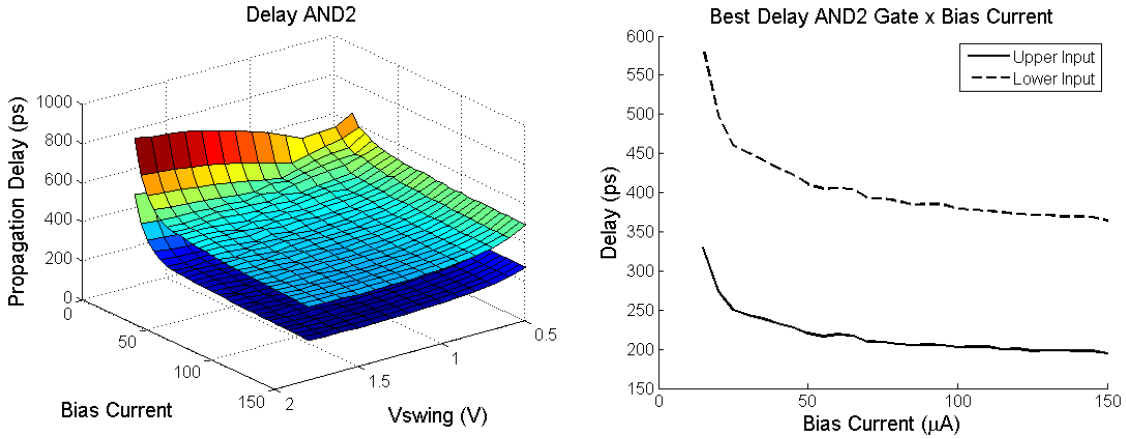


(a) (b)

Figure 3.12: (a) Delay of exclusive-OR2 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR2 gate

The Figure 3.13 presents the results for the AND2 gate. The Figure 3.13(a) presents the delay as function of bias current and voltage swing. As in the Figure 3.12 it presents two surface, one for each input of the gate. The behavior of AND2 gate propagation delay is almost the same of XOR2 gate. The difference came from the simplification done on the PDN sizing, as presented in section 2.3. The optimization changes a differential pair by a transistor, as consequence the internal gate capacitances are reduced and the gate achieve a better propagation delay.

Furthermore, the methodology study the propagation delay connecting the gate output in the same input of other gate, as consequence the upper input must charge only one differential pair instead of two as in the XOR2 gate. Note that, comparing the upper input curves of Figure 3.12 and Figure 3.13, the second one presents a better propagation delay.

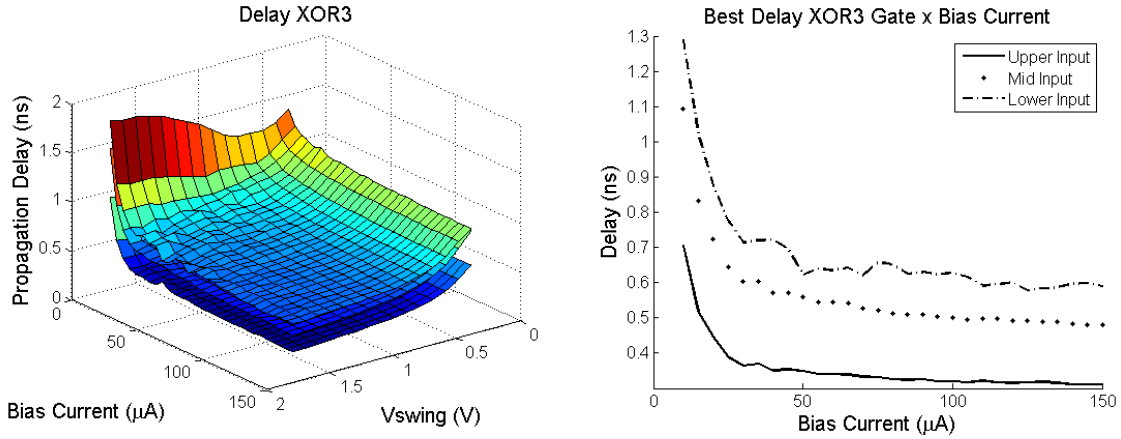


(a) (b)

Figure 3.13: (a) Delay of AND2 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the AND2 gate

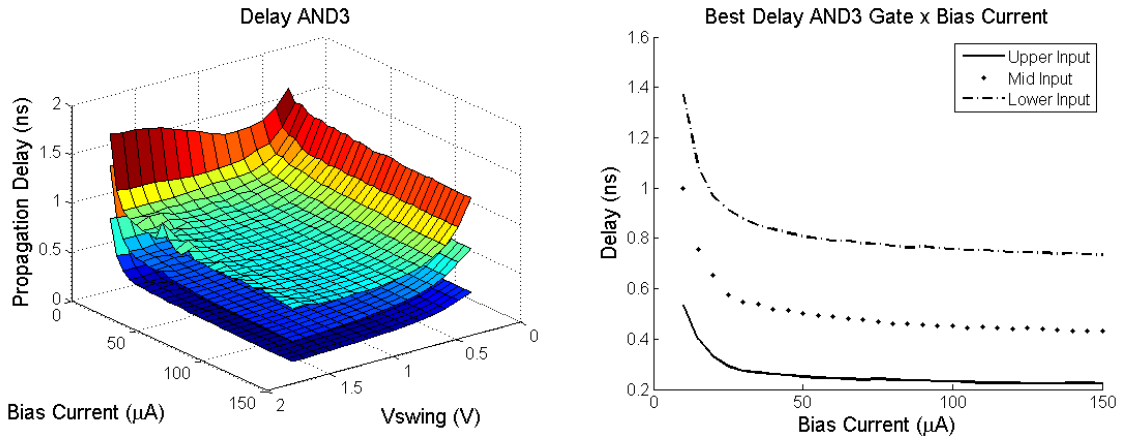
The Figure 3.14 presents the results for the exclusive-OR3 gate. The Figure 3.14(a) presents the delay as function of bias current and voltage swing. The graph presents three surfaces. The lower one illustrates the propagation delay of the input that controls the upper gate differential pairs. The middle surface represents the propagation delay of the input that controls the middle gate differential pairs. Finally, the upper surface is the propagation delay of the lower input, i.e. the input that controls the lower gate differential pair. All inputs presents the same behavior as function of the bias current and voltage swing. The small voltage swing is not a good choice for the majority of the bias current cases. According Figure 3.14(b) the bias current increasing presents a gain in propagation delay up to a value around of 40μ, above this value the gain in propagation delay decreases significantly.

The graph for propagation delay is presented also to the AND3 gates, as depicted in Figure 3.15. The same behavior of XOR3 in relation of the chosen bias current and voltage swing is saw.



(a) (b)

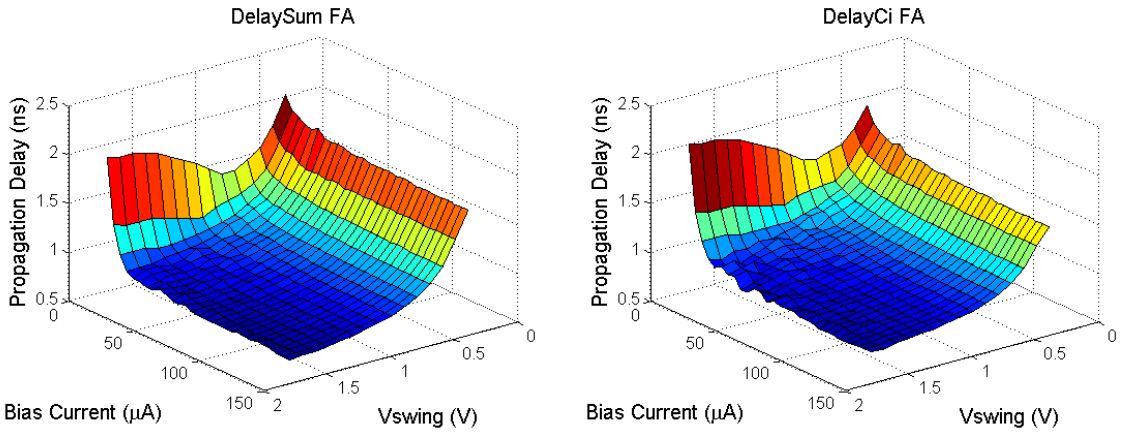
Figure 3.14: (a) Delay of exclusive-OR3 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR3 gate.



(a) (b)

Figure 3.15: (a) Delay of AND3 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the AND3 gate.

Figure 3.16 shows the propagation delay of the Full Adder gate. The left graph, Figure 3.16(a), represent the propagation delay of the slowest sum bit. The right one, Figure 3.16(b), illustrates the performance of the Carry bit. The difference of these graphs for the previous, XOR3 for example, came from the impact of voltage swing. Lower voltage swing impacts hardly the propagation delay degradation in the FA gate. Note that the FA gate is a association of two gates, the XOR3 and a MAJ3. Therefore, as small voltage swings leads an increase in the PDN transistors, at this time there are more transistors connected to the output node. The result is a bigger influence on the output capacitance because of the PDN sizing.

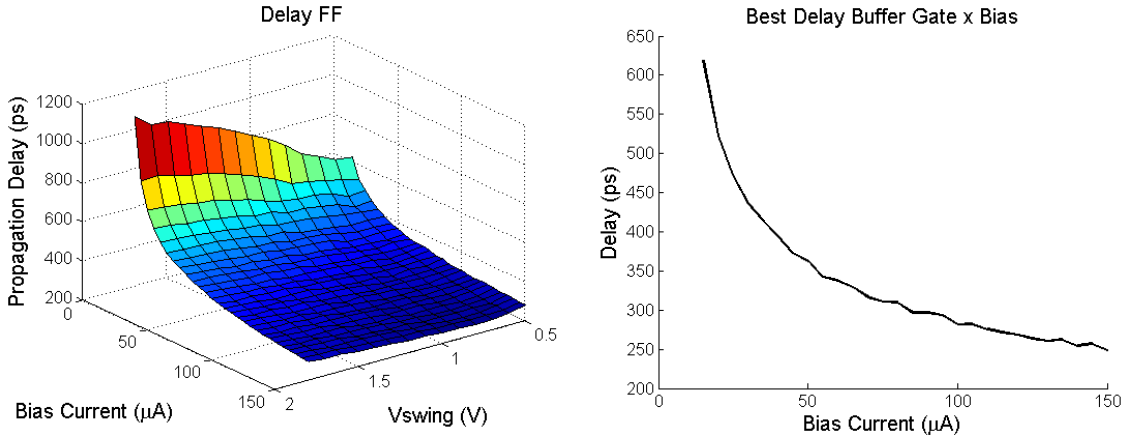


(a) (b)

Figure 3.16: Delay of FA (a) Sum and (b) Carry bit versus bias current and voltage swing parameters.

In the methodology used, the Flip-flop gate has a little bit different propagation delay behavior as function of the bias current and voltage swing parameters. Remember that the propagation delay testbench is different of that used for the combinational gates, section 3.1.5 explain it.

According to Figure 3.17(b) the behavior of Clk2q delay as function of bias current also presents a saturation result. Taking into account the Figure 3.17(a) the influence of voltage swing demonstrates that small values of this parameter seems to be attractive, what do not appear in the analysis of combinational gates. In order to understand it, note that in Figure 3.10 the increasing of the PDN sizing is dependent of the gate complexity. In other words, for a buffer gate, the reduction in the voltage swing requires a lower increasing on the PDN transistors sizing if compared with the sizing of the two or three input gates. As a consequence the output capacitance load of the FF gate on this testbench does not impact significantly on the propagation delay analysis as function of the voltage swing.



(a) (b)

Figure 3.17: (a) Delay of Flip-Flop gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the Flip-flop gate.

As already said, the methodology uses the same sizing for all transistors that compose the PDN of a MCML gate. An evaluation of the impact of use a standard value for the PDN transistor width becomes necessary to know how much it degrades the gate performance. In order to find this performance loss some gates were sized through the optimization circuit software Wicked.

The Table 3.2 shows the results of the XOR2 sizing. The first column point the methodology used, the second and third column explicit the static parameters of the analyzed gate. Note that three combinations of bias current and voltage swing were studied. The results of sizing are in the PDN sizing column and the last three columns give the propagation delay response being the last one the average delay of the two gate inputs. A more detailed analysis of results shows that the optimization software increase the sizing of the upper input transistors and make the lowers one smaller than the sizing achieve by the proposed methodology. This procedure led to an improvement of 11% in average for the worst case delay, which correspond to the lower input delay. Analyzing the two inputs together, the average gain was 4%. Therefore, it is possible conclude that the Wicked penalizes the upper input to give a better delay response to the lower one.

Table 3.3 gives the results of the same comparison for the XOR3 gate. This table shows the results for the same bias current and voltage swing of the previous table. The table organization give the methodology used in the first column, the bias current and voltage swing in the second and third columns respectively. The PDN Sizing columns give the sizing of the differential pairs correspondent to the three inputs of the gate and

its propagation delays are presented in propagation delay columns. The last column gives the average delay of the three gate inputs.

Table 3.2: XOR2 pull-down network sizing and propagation delay achieve by the proposed methodology and by the optimization software Wicked.

Methodology	Bias Current (µA)	Voltage Swing (V)	PDN Sizing		Propagation Delay (ps)		
			Wn_up (µm)	Wn_dw (µm)	Upper Input	Lower Input	Average
Proposed	50	1.5	1.04	1.04	297.5	440.4	368.95
Wicked			1.05	0.8	301	398.7	349.85
Proposed	20	0.6	1.52	1.52	428	576	502
Wicked			1.55	1.05	474	482.7	478.35
Proposed	130	1	3.69	3.69	296	383	339.5
Wicked			4	3.15	316	355.3	335.65

The Wicked results demonstrate that the sizing follows the same principle of the used in the XOR2 case. Lower differential pair uses smaller transistors and for each upper differential pair input level the transistors become larger. The Wicked sizing performance response presents an improvement for the lowest and the middle input, and degradation for the upper input when compared with the proposed methodology. In resume, the Wicked presents the worst case delay with an average improvement of 20%, while the average propagation delay of the gate has a result 10% better of the proposed methodology.

Table 3.3: XOR3 pull-down network sizing and propagation delay achieve by the proposed methodology and by the optimization software Wicked.

Methodology	Bias Current (µA)	Voltage Swing	PDN Sizing (µm)			Propagation Delay (ps)			
			Wn_up	Wn_mid	Wn_dw	Upper Input	Middle Input	Lower Input	Average
Proposed	50	1.5	1.55	1.55	1.55	360.4	572.2	723.3	552
Wicked			1.9	1.3	0.85	414	533	586	511
Proposed	20	0.6	2.4	2.4	2.4	574.2	907.3	1038	840
Wicked			2.55	2.1	1.3	598	831	772	734
Proposed	130	1	6.03	6.03	6.03	379.4	580	678	546
Wicked			6.45	5.15	4.05	396	521	540	486

3.2.2 IBM130

The Table 3.4 displays the MOSFET technology parameters of this technology. The procedure size the gates with a range of current bias that goes from 10µA up to 80µA, and analyze the output voltage swing from 300mV up to 800mV. The minimum length specified for the bias current mirror and pull-up transistors was 400nm to overcome the process variability.

Table 3.4: IBM130 technology parameters.

V_{DD}	1.2 V
Vth0n1	0.355 V
µnCox	390 µA/V2
Vth0p1	-0.325 V
µpCox	80 µA/V2
Lmin	120 nm
Wmin	160 nm

[1]Consider gates with W/L=5/0.12µm

The Figure 3.18 shows the pull up transistor sizing. This sizing has as an objective achieve to the required pull-up resistance. Note that the pull-up transistors width changes linearly with the bias current change. The relation of transistor width and voltage swing is inversely proportional, and not linear. This is the same behavior of the

XFab XC06 technology. The transistor length used on these transistors is always the minimum set in the methodology (400nm). Therefore, its graphic is not shown.

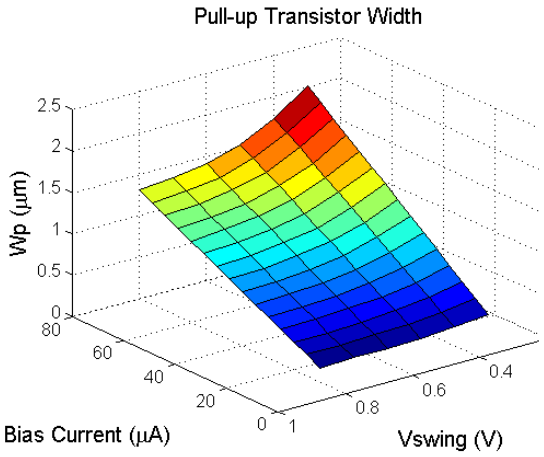


Figure 3.18: Pull-up resistor width of buffer gate versus bias current and voltage swing parameters.

The Figure 3.19 illustrates the pull-down network sizing of the gates. All graph present the same behavior, greater transistor width for high current, small voltage swing gates. As in the previous technology analyzed, the width has a linear correlation with the bias current, and an almost quadratic relation with the voltage swing. Comparing Figure 3.19 (a), (b) and (c), the complexity of the gate increases the PDN transistors width because of the transistor stacking in the gate PDN.

The next graphs of this section present the propagation delay for a fanout of four of combinational cells leads by the sizing presented in Figure 3.18 and Figure 3.19. The Figure 3.20 presents the results for the buffer/inverter gate. According to Figure 3.20(a), the use of high values of voltage swings associated with small bias current hardly degrades the buffer speed performance. When is taken into account gates with large bias current, small voltage swing are still preferred. Although for large bias currents, the use of large voltage swing is not as prejudicial to the gate performance as in the small bias current cases.

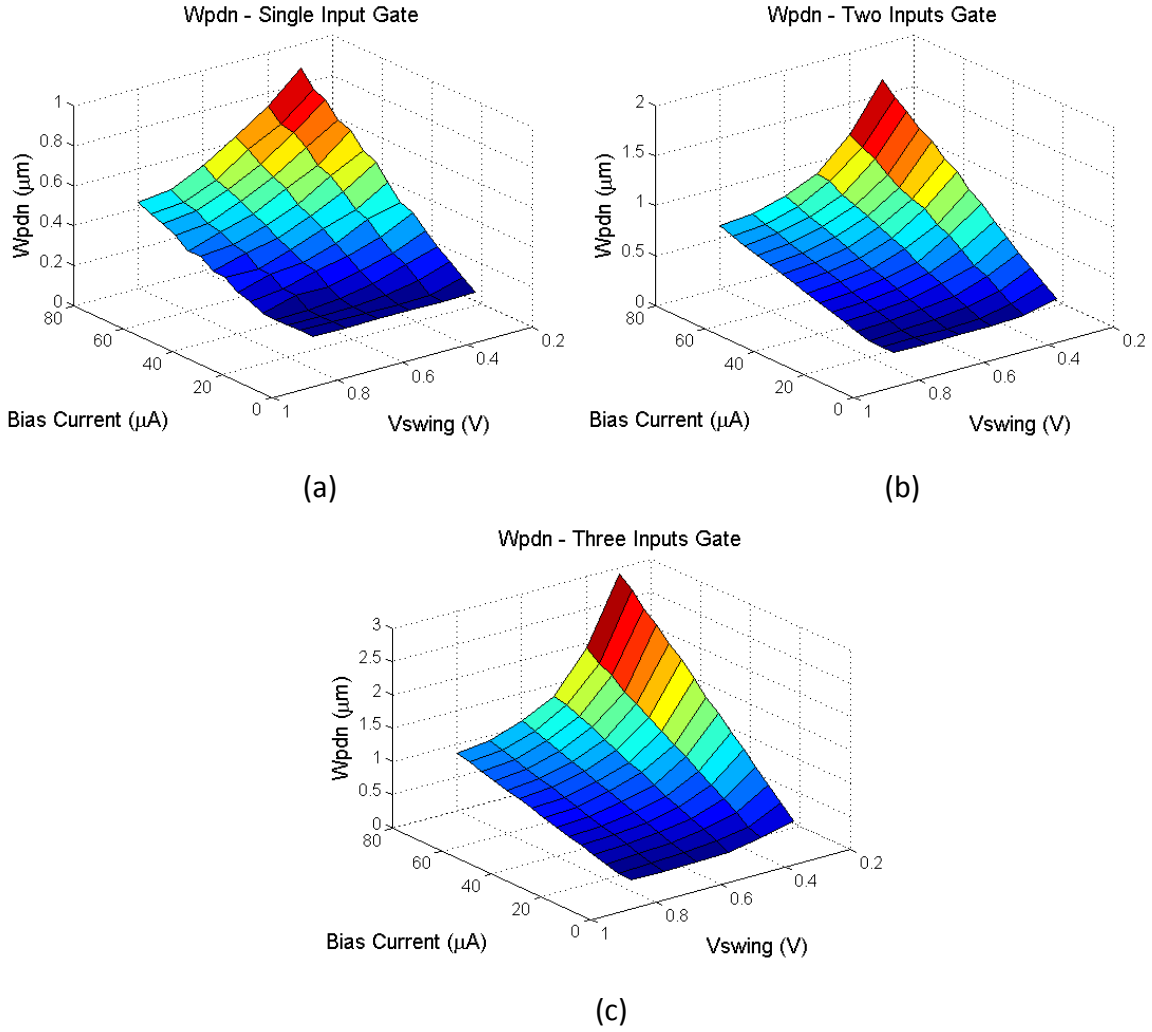
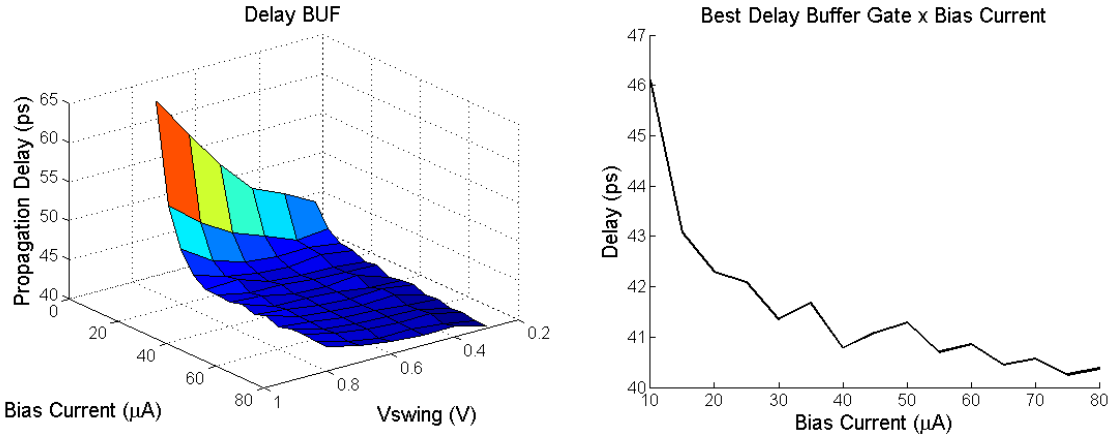


Figure 3.19: PDN width of MCML gates with (a) one; (b) two; (c)three inputs versus bias current and voltage swing parameters.

The Figure 3.20(b) presents the best gate propagation delay versus the bias current used independently of the voltage swing used. Note that the propagation delay gain achieves better values according to the increase of bias current. The graph presents a saturation tendency observed for bias current higher than 30 µA.

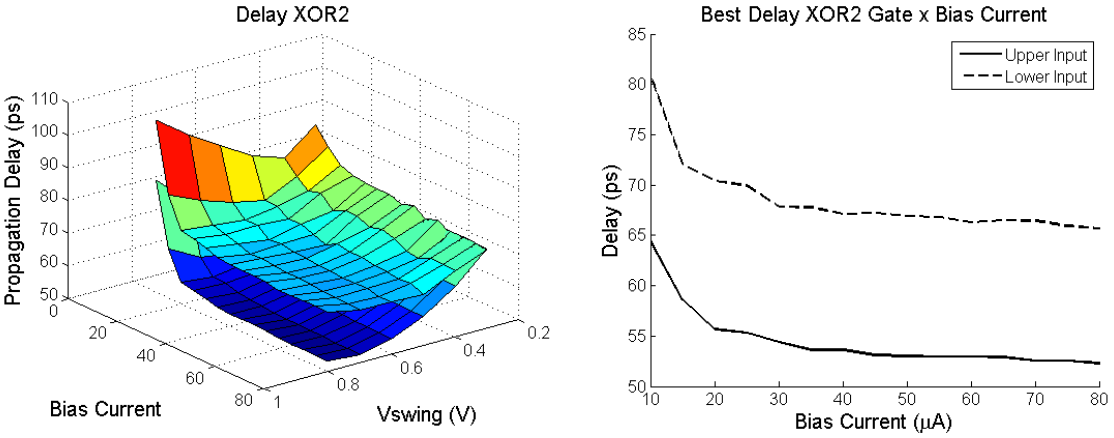
The Figure 3.21 presents the results for the exclusive-OR2 gate. The Figure 3.21(a) presents the delay as function of bias current and voltage swing. As in the previous technology, the graph presents two surfaces one surface for each gate input. The behavior according to the bias current and voltage swing give the idea that is advantageous use small voltage swings for small bias currents. The increasing of bias current leads to an increasing on the voltage swing to achieve the best delay performance.



(a) (b)

Figure 3.20: (a) Delay of buffer gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the buffer gate.

Analyzing the best propagation delay achieve for each bias current, Figure 3.12(b), the increase in bias current present a gain in the propagation delay up to a value around 20μA. Above this value the propagation delay gain is no more so significant.



(a) (b)

Figure 3.21: (a) Delay of exclusive-OR2 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR2 gate (b) Best delay achieve for each bias current of the buffer gate.

The Figure 3.22 presents the results for the AND2 gate. The Figure 3.22(a) presents the delay as function of bias current and voltage swing for the two gate inputs. As in the XOR2 gate, the behavior of AND2 gate propagation delay according to the

bias current and voltage swing parameters show that is advantageous use small voltage swings for small bias currents. The increasing of bias current leads to an increasing on the voltage swing to achieve the best delay performance. Note that for the cases of bias current above 20µA, the improvement on propagation delay is almost null for gates with voltage swing between 500mV and 800mV. Take as reference the Figure 3.22(b), the saturation on the delay performance appear for bias current above 20µA too.

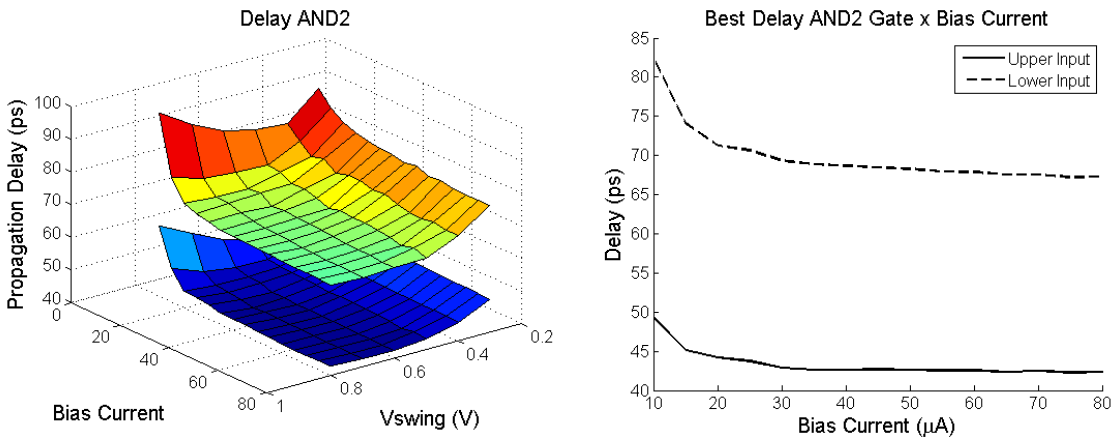
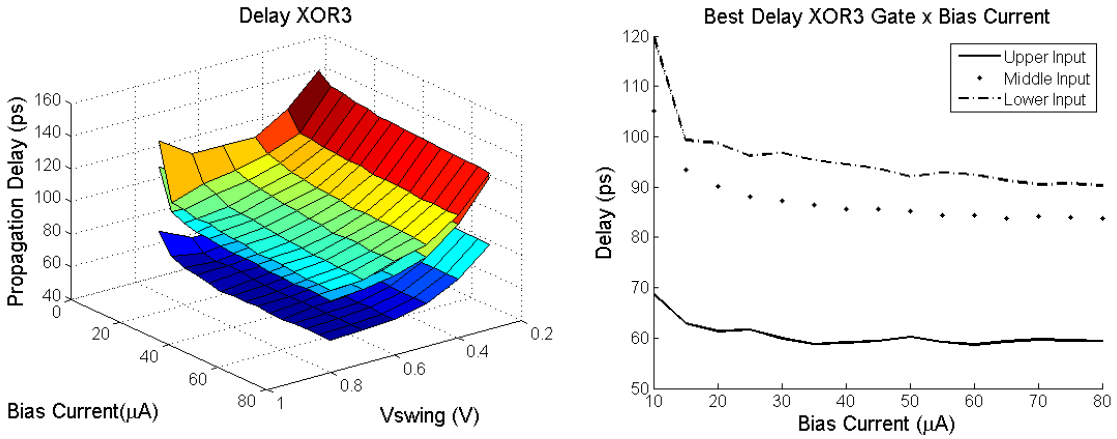


Figure 3.22: (a) Delay of exclusive-OR2 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR2 gate

The Figure 3.23 presents the results for the exclusive-OR3 gate. The Figure 3.14(a) presents three propagation delay surfaces. The lower one illustrates the propagation delay of the fastest input, the input that controls the upper gate differential pairs. The middle surface represents the propagation delay of the input that controls the middle gate differential pairs. Finally, the upper surface is the highest propagation delay, that corresponds to the input that controls the lower gate differential pair.

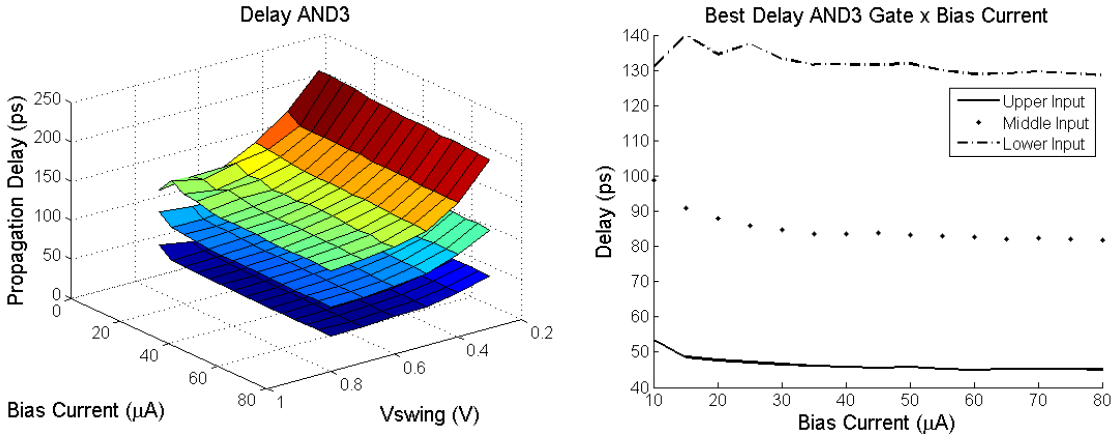
All XOR3 gate inputs presents the same behavior as function of the bias current and voltage swing. The small voltage swing is not a good choice for the majority of the bias current cases. According Figure 3.23(b) the bias current increasing presents a gain in propagation delay up to a value around of 20µ, above this value the gain in propagation delay decreases significantly.



(a) (b)

Figure 3.23: (a) Delay of exclusive-OR3 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR3 gate.

The graph for propagation delay of AND3 gate is presented in Figure 3.24. Notice in the Figure 3.24(a) that the bias current has a little influence on the propagation delay. The possible cause of this effect is that the analyzed range is at the saturation region of propagation delay in function of bias current. The graph of Figure 3.24(b) confirms this idea. Analyzing the propagation swing as function of voltage swing, note that low voltage swings are prejudicial for the gate delay performance.

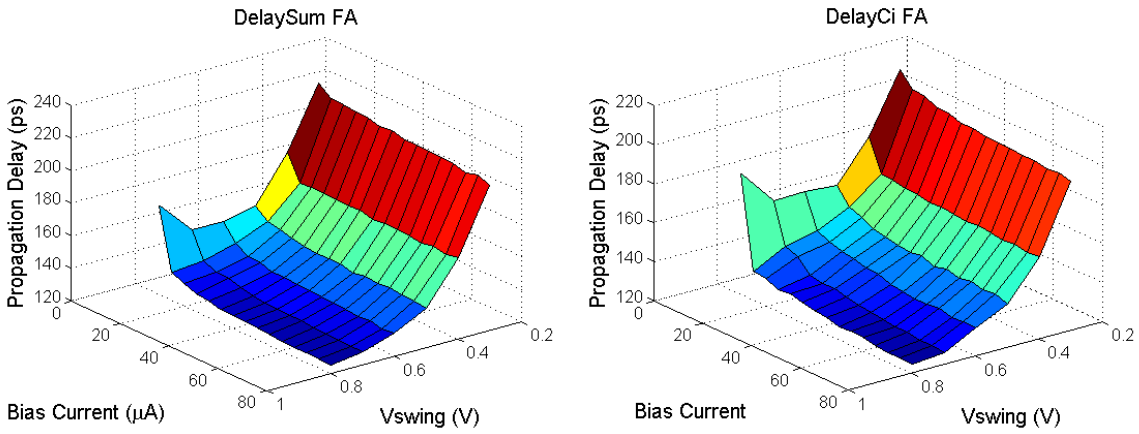


(a) (b)

Figure 3.24: (a) Delay of AND3 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the AND3 gate.

The Figure 3.25 shows the propagation delay of the Full Adder gate. The left graph, Figure 3.25(a), represent the propagation delay of the slowest sum bit. The right

one, Figure 3.25(b), illustrates the performance of the Carry bit. Remember that an XOR3 gate, to process the sum bit and a MAJ gate to process the Carry bit compose the FA gate. Therefore, as small voltage swings leads an increase in the PDN transistors, at this time there are more transistors connected to the output node. The result is a bigger influence on the output capacitance because of the PDN sizing.



(a) (b)

Figure 3.25: Delay of FA (a) Sum and (b) Carry bit versus bias current and voltage swing parameters.

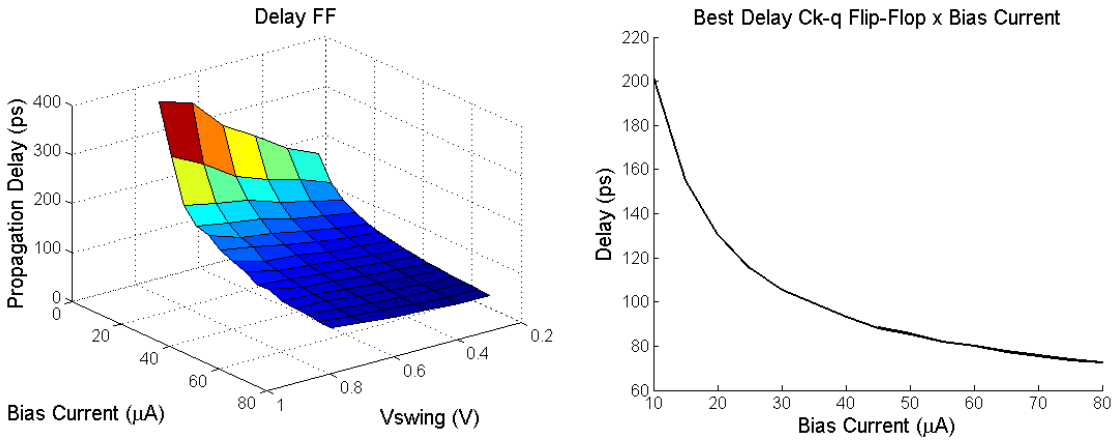
The Figure 3.26(a) demonstrates that the delay of Clk2q of FF gate decreases as decrease the voltage swing used. Remember that the output load of the FF in the used testbench is four inverter gates. According to the Figure 3.19 the influence of voltage swing on the inverter gate is lower than the influence on the two input gates. Therefore, the impact on the output load is not so significant on this testbench.

Note that Figure 3.17(b) shows the behavior of Clk2q delay as function of bias current. This curve also presents a saturation characteristic, but is less abrupt them the occurred in the combinational gates.

In order to evaluate the cost of use a standard value for the PDN transistor on the propagation delay performance the Table 3.5 presents the comparison of three XOR2 gates designed by the proposed methodology and by the optimization software Wicked.

The first column of Table 3.5 shows the methodology used, the second and third column explicit the static parameters of the analyzed gate. Note that three combinations of bias current and voltage swing were studied. The results of sizing are in the PDN Sizing column and the last three columns give the propagation delay response being the

last one the average delay of the two gate inputs. A more detailed analysis of results shows that the optimization software increase the sizing of the upper input transistors and make the lowers one smaller than the sizing achieve by the proposed methodology. This procedure led to an improvement of 2% in average for the worst case delay, that correspond to the lower input delay. Analyzing the two inputs together, the average gain was 4%. Therefore, it is possible conclude that the Wicked penalizes the upper input to give a better delay response to the lower one.



(a) (b)

Figure 3.26: (a) Delay Ck-q of Flip-flop gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current.

Table 3.5: XOR2 pull-down network sizing and propagation delay achieve by the proposed methodology and by the optimization software Wicked.

Methodology	Bias Current (μA)	Voltage Swing (V)	PDN Sizing		Propagation Delay (ps)		
			Wn_up (μm)	Wn_dw (μm)	Upper Input	Lower Input	Average
Proposed	15	0.5	210	210	62.4	72.1	67.25
Wicked			200	230	59.5	72	65.75
Proposed	30	0.6	280	280	52.1	67.8	61.95
Wicked			330	250	55.2	62.8	59
Proposed	65	0.7	530	530	52.9	66.5	59.7
Wicked			680	480	54.2	62.7	58.45

The Table 3.6 gives the results of the same comparison for the XOR3 gate. This table shows the results for the same bias current and voltage swing of the previous table. The table organization give the methodology used in the first column, the bias current and voltage swing in the second and third columns respectively. The PDN Sizing columns give the sizing of the differential pairs correspondent to the three inputs of the gate and its propagation delays are presented in propagation delay columns. The last column gives the average delay of the three gate inputs.

The Wicked results demonstrates that for this technology the results of the proposed method leads to a degradation of 3% for the worst case delay, and 2% if is considered the average delay of three inputs. These results are better than the results demonstrates for the XFab XC06 technology.

Table 3.6: XOR3 pull-down network sizing and propagation delay achieve by the proposed methodology and by the optimization software Wicked.

Methodology	Bias Current (µA)	Voltage Swing	PDN Sizing (nm)			Propagation Delay (ps)			
			Wn_up	Wn_mid	Wn_dw	Upper Input Delay	Middle Input Delay	Lower Input Delay	Average
Proposed	15	0.5	285	285	285	72.5	109.5	108.5	96.8
Wicked	15	0.5	300	260	290	74.8	104.5	105	94.8
Proposed	30	0.6	415	415	415	64.5	96	95	85.2
Wicked	30	0.6	430	420	410	64	94	92	83.3
Proposed	65	0.7	760	760	760	64	93	94	83.7
Wicked	65	0.7	1000	820	680	67	91	92	83.3

3.2.3 PTM45

The Table 3.4 displays the MOSFETs technology parameters of the predictive technology model PTM45. The procedure size gates with a range of current bias that goes from 7µA up to 45µA, and analyze the output voltage swing from 300mV up to 700mV. The minimum length specified for the bias current mirror and pull-up transistors was 150nm to overcome the process variability. Observe that there are three

different types of transistors in this process. This work uses the low threshold voltage devices.

Table 3.7: PTM45_VTL MOSFET specifications.

V_{DD}	1 V
Vth0n	0.322 V
µnCox	510 µA/V²
Vth0p	-0.302 V
µpCox	202 µA/V²
Lmin	50 nm
Wmin	90 nm

The Figure 3.27 shows the pull up transistor sizing. Note that, for a better presentation, the graphs of Figure 3.27 (a) and (b) has the bias current axis inverted between them. As the previous works the pull-up transistors width changes linearly with the bias current change. The relation of transistor width and voltage swing is inversely proportional, and not linear. For bias currents below 20µA the methodology uses larger transistors length than that pointed as boundary case.

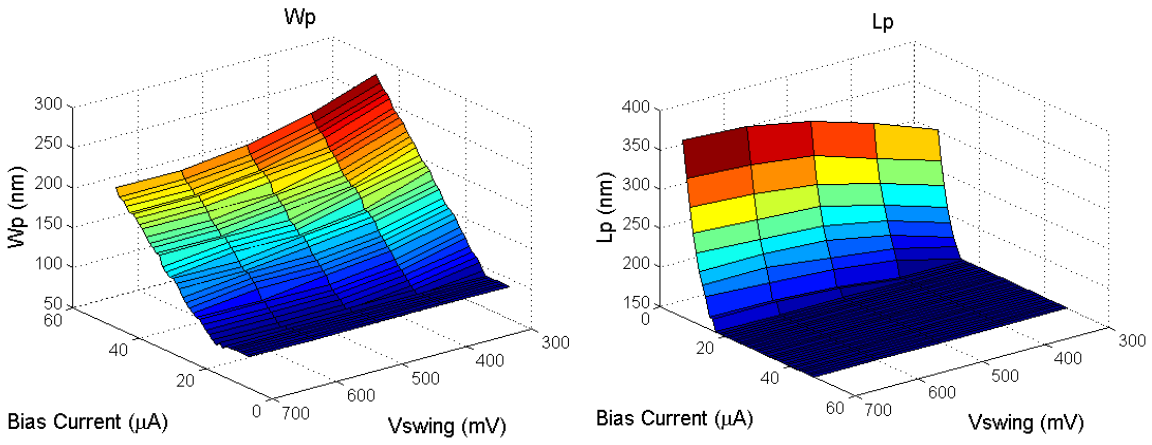


Figure 3.27: Pull-up resistor (a) width (b) length of buffer gate versus bias current and voltage swing parameters.

The Figure 3.28 illustrates the pull-down network sizing of the gates. The behavior seen on the previous technologies nodes presented happens on this technology too, i.e. transistors width proportional to the bias current used and inversely proportional to the voltage swing. Note that for lower values of bias current the PDN the gates achieve the minimum PDN transistors sizing.

Following the graphs of the propagation delay analysis as function of the bias current and voltage swing used on the gates sizing. Observe that in all graph the propagation delay of gate with a low bias current, bellow 10µA, the behavior well approximate the sketch of Figure 3.27(b), the length of the pull-up transistors. As the PDN sizing on these cases achieves the minimum values, there is not difference on the output load o the gates. Therefore, the dominant effect is the parasitic capacitance of the pull-up resistance.

The Figure 3.29 shows that the buffer delay is few influenced by the voltage swing used. The main effect comes from the bias current used. The Figure 3.20(b) presents the best gate propagation delay versus the bias current used independently of the voltage swing used. Note that graphs present a saturation tendency observed for bias current higher than 20 µA.

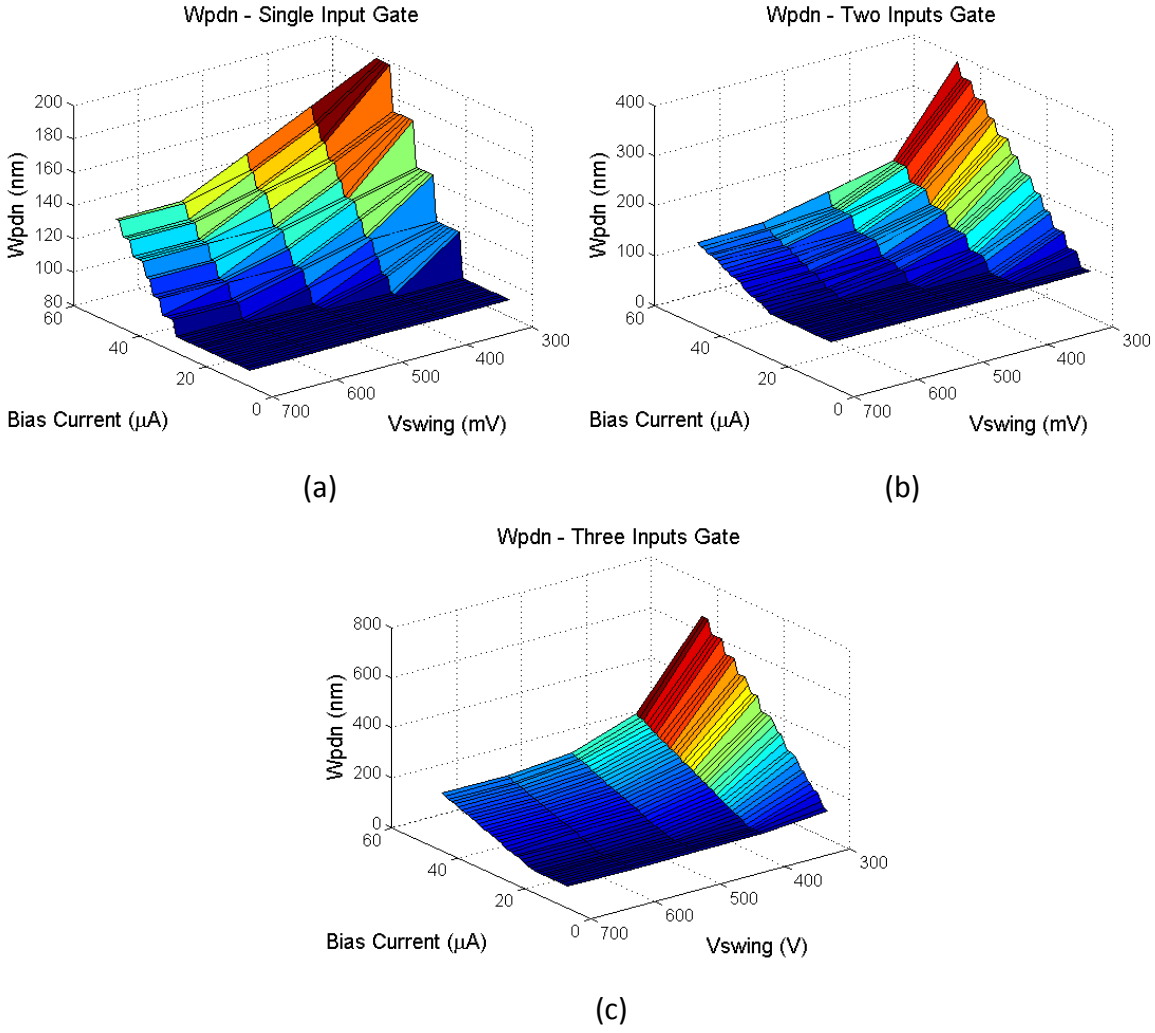
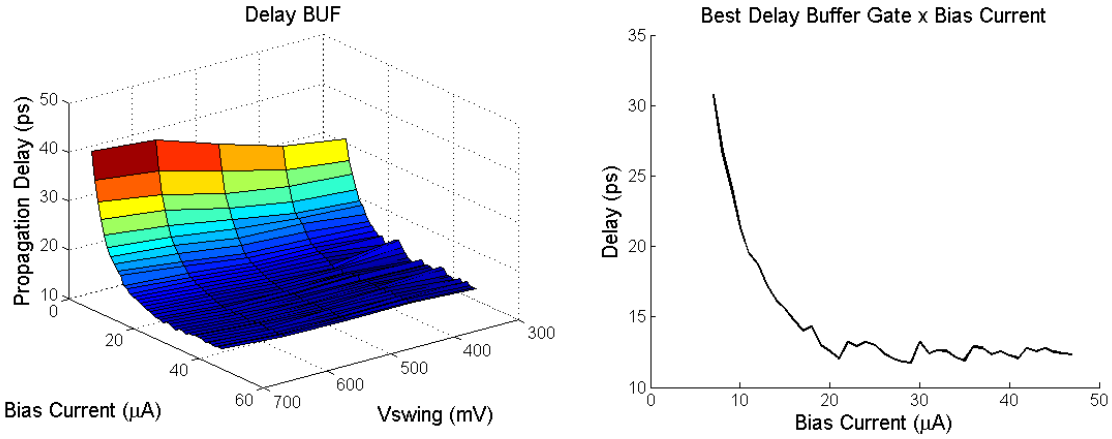


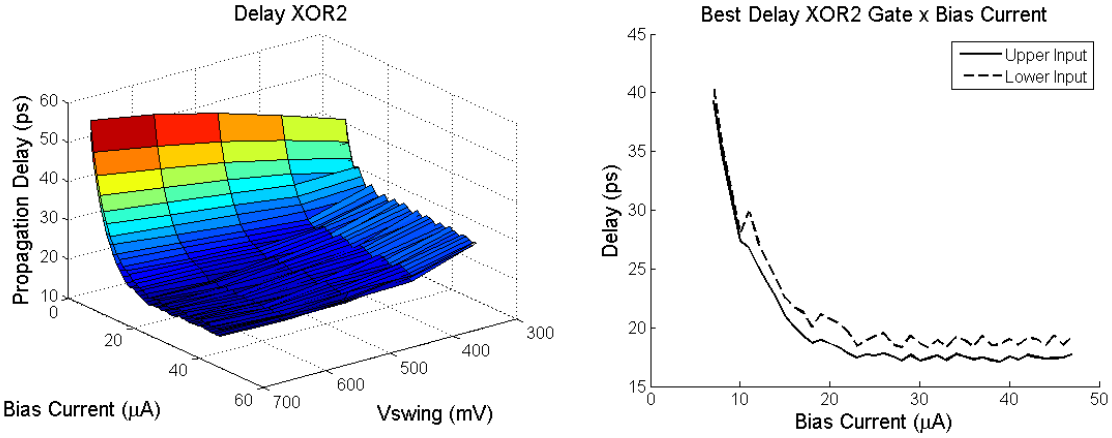
Figure 3.28: PDN width of MCML gates with (a) one; (b) two; (c)three inputs versus bias current and voltage swing parameters.



(a) (b)

Figure 3.29: (a) Delay of buffer gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the buffer gate.

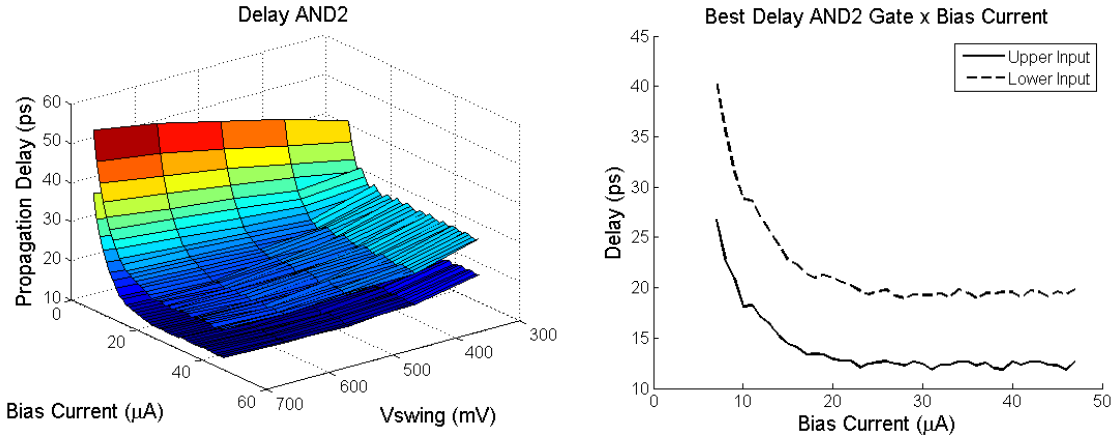
The propagation delay of gates with two inputs, represented by Figure 3.30 and Figure 3.31, shows that for higher values of bias current (above 20μA) a small voltage swing is not advantageous. This behavior comes from the sizing of PDN sizing.



(a) (b)

Figure 3.30: (a) Delay of exclusive-OR2 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR2 gate

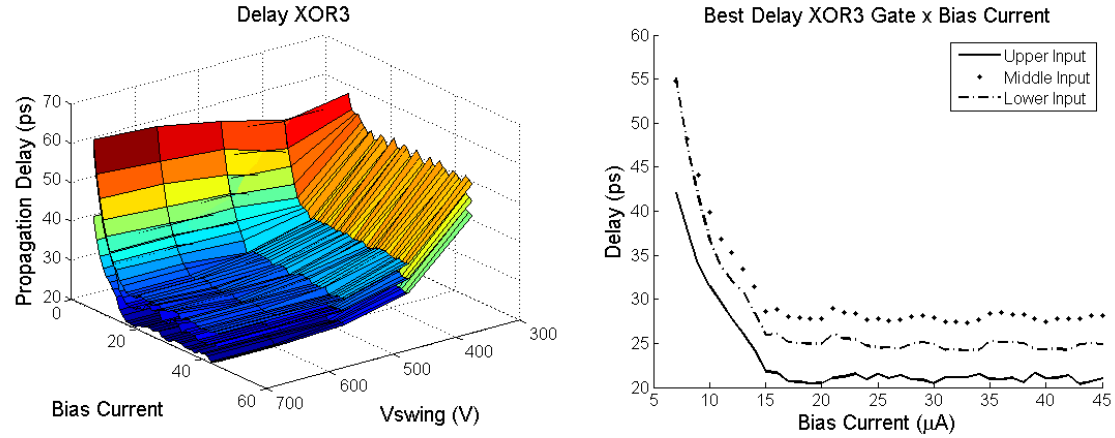
(b) Best delay achieve for each bias current of the buffer gate.



(a) (b)

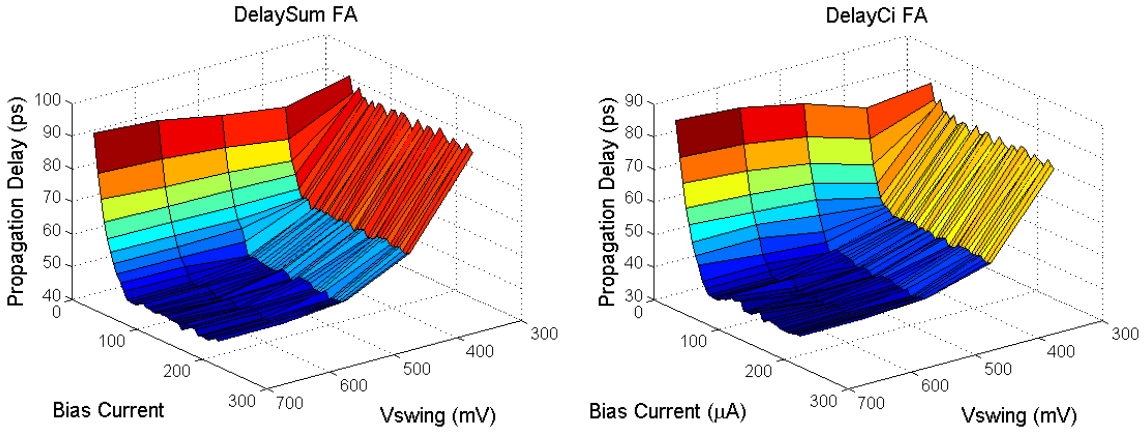
Figure 3.31: (a) Delay of exclusive-OR2 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR2 gate

The Figure 3.32 and Figure 3.33 show that the influence of voltage swing on the three inputs gates is more significant. Observing Figure 3.28 is possible see that the PDN sizing increases more for complex gates resulting in higher output capacitance.



(a) (b)

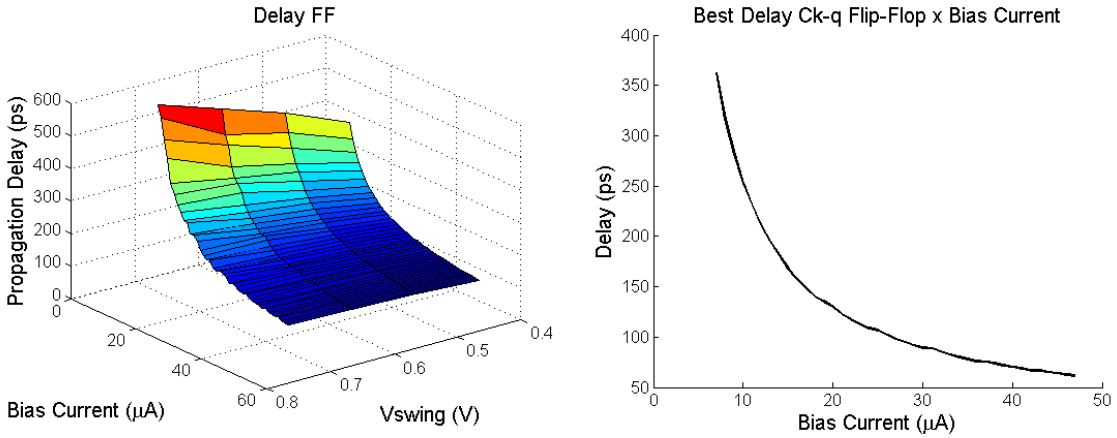
Figure 3.32: (a) Delay of exclusive-OR3 gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current of the XOR3 gate.



(a) (b)

Figure 3.33: Delay of FA (a) Sum and (b) Carry bit versus bias current and voltage swing parameters.

The Flip-flop delay analysis, Figure 3.34, take as load buffer gates. Therefore, for a low bias current small voltage swing is preferred, while for high values of bias current it does not influence significantly on the clock-to-q delay.



(a) (b)

Figure 3.34: (a) Delay Ck-q of Flip-flop gate versus bias current and voltage swing parameters (b) Best delay achieve for each bias current.

4 PERFORMANCE AND CONSTRAINTS OF MCML AND CMOS

This chapter presents the constraints and performances tradeoffs between MCML and CMOS gates. This study takes into account the design challenges of standard cell library on both topologies, how the scaling effects act on its circuits and as conclusion the performance of the gates is analyzed for three different technologies.

4.1 Design Challenges

The use of high-level hardware description languages (HDL) for describing circuit functionalities followed by the synthesis and mapping processes in standard cell design flow is the most applied methodology for designing digital integrated circuits (ICs). Standard cells are pre-designed and pre-characterized gates compatible with automated design flow requirements. This methodology guarantees a reliable and short time-to-market relationship for new designs. Therefore, in order to be successfully adopted, a logic style should be suitable to the conventional top-down design flow supported by the available EDA environments. Hence, the building blocks should bear the form of standard cell.

This section makes a review of static CMOS standard cell library design and compares it with the MCML standard cell design. The differences between the logic network, output swing, power delay trade-off and the standard cell template is addressed.

4.1.1 Logic Network

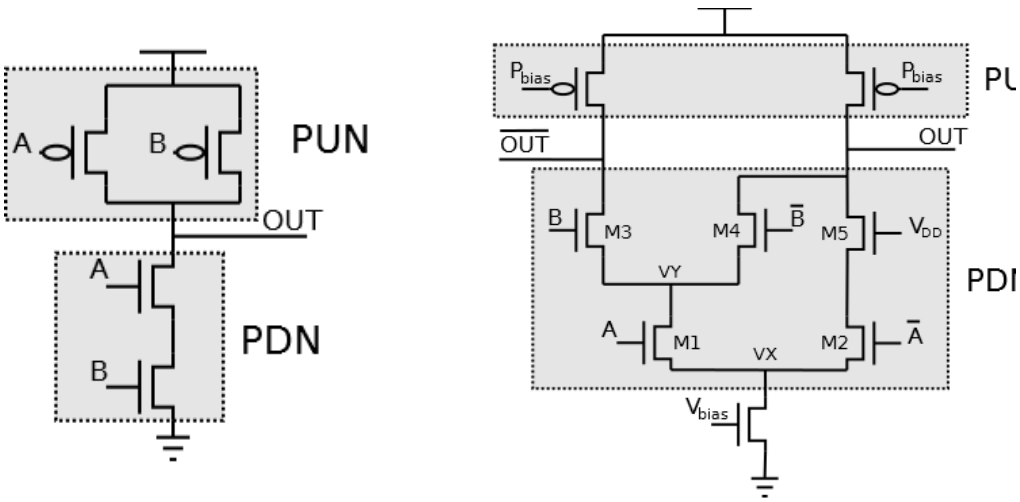
A static CMOS gate is a combination of two networks, the pull-up network (PUN) and the pull-down network (PDN). The function of the PUN is to provide a connection between the outputs and V_{DD} anytime the output of the logic gate is meant to be 1. This network is constructed using PMOS transistors. Similarly, the function of the PDN is to connect the output to GND when the output of the logic gate is meant to be 0. Complementary to the PUN, the PDN is implemented with NMOS transistors. This construction gives to the PUN and PDN networks a mutually exclusive operation.

Note that the static CMOS logic gates present a complementary networks and this implementation is naturally inverting. Therefore, in a single stage, the static CMOS is able to construct only functions such as NAND, NOR, and XNOR. The realization of a non-inverting Boolean function (such as AND OR, or XOR) requires the addition of an extra inverter stage (RABAEY, CHANDRAKASAN e NIKOLIC, 2003).

Complex CMOS gates are formed using a combination of series and parallel transistors associations. Remember that a series association corresponds to an AND function and an OR function can be constructed with a parallel association.

The logic network of MCML gates was present in section 2.3, the logic function is implemented by the PDN that is constructed with NMOS differential pairs. It provides two complementary outputs, therefore the inverting (NAND, NOR, XNOR) functions are constructed with the same network of the non-inverting ones (AND, OR, XOR). The logic output result is provided by the voltage drop on the pull-up network.

Although the static CMOS gates take advantages in transistors numbers if is taken in to account one stage CMOS gates. More complex gates can be advantageous for MCML topology once it is able to implement these gates in a single stage, specially a XOR3 and the LATCH that are largely used in digital circuits, the first one in adder circuits and the second in sequential circuits.



(a) (b)

Figure 4.1: Logic Network of a NAND2 (a)CMOS (b)MCML

4.1.2 Logic Swing

Considering the logic network of static CMOS presented in the previous section, once the transients have settled, a path always exists between V_{DD} and the output OUT, providing a high output (“one”), or, alternatively, between GND and OUT for a low output (“zero”) (RABAEY, CHANDRAKASAN e NIKOLIC, 2003). Therefore, the output logic swing of the static CMOS topology always is equal to the supply voltage of the circuit.

In MCML the logic swing is a design parameter and it is one of the main advantages of the MCML circuits when compared to conventional CMOS topology. As already cited in section 2.3.1, while the CMOS presents a logic swing equals to the circuit voltage supply, the MCML is able to work with a reduced output voltage swing. The consequence is a reduction on the charge amount necessary to change the logic level of a certain load.

The behavior of MCML gates performance in relation to the chosen voltage swing depends on the load consideration. Considering fixed capacitance loads, generally the best propagation delay performance is found with small voltage swing. More precisely it is valid for the case where the load capacitance is dominant if compared with the internal gate capacitances. On the other hand, for digital standard cell library, the output signal from a gate must be able to transfer its logic value to the following gate. This behavior is only possible if the voltage levels of logic zero and logic one are uniform for all cells. Note that on this situation larger voltage swing is preferred. Larger voltage swing implies in a small transistor size of the gate, as commented in section 2.4.3, and it is beneficial to the circuit performance.

4.1.3 Power

The static CMOS power dissipation comes from two components: static and dynamic dissipation. The dynamic dissipation is represented by the charge amount spent to charge and discharge a load capacitance over any given interval of time. This power can be approximated by:

$$P = \alpha \, C_L {V_{DD}}^2 f \tag{4.1}$$

where the C_L is the load capacitance, V_{DD} is the supply voltage, f is the operating frequency and α the is the switching probability (WESTE e HARRIS, 2005).

The static portion comes from the subthreshold conduction, tunneling current through the gate oxide and leakage through reverse-biased diodes. In the older process these components were small enough to be neglected. In 130nm process and beyond, the static power becomes significant and must be taken into account (WESTE e HARRIS, 2005).

As referred in section 2.2.4, opposite of static CMOS, the MCML gates has static power dissipation that is dominant for the topology. The power is only function of its bias current and the supply voltage and no dependency of operating frequency. Therefore at high operation frequency MCML can be advantageous if compared to static CMOS topology.

4.1.4 Standard Cell Template

The physical synthesis is the step of the digital standard cell design flow responsible to translate the netlist circuit into a physical layout. This translation is only possible if a gate physical representation is provided to the place and route (PNR) tools. These physical structures are the gate's layout that should be constructed taking into account some standard parameters.

In the placement step, the standard cells are arrayed in rows across the chip. To make it possible the gates layout must present a constant height (WESTE e HARRIS, 2005). The design rules should consider the placement of the cell side-by-side. Therefore, a template of cell's layout is necessary.

Most simple standard cell CMOS layout template has two supply rails at the top (V_{DD}) and bottom (GND) of the cell. Between these rails are disposed the PMOS and NMOS transistors, closer to the V_{DD} and GND respectively. The supply lines are sized according to the average and peak current performed by the library gates in the possible circuit applications. The distance between the rails take into account the number of metal lines necessary to the internal cell routing and the transistors sizing. The total height of the cells considers the supply rails width and the distance between them.

The space between of the supply rails must be divided to define the portion where the pull-up (PMOS) and pull-down network (NMOS) will be disposed. Note that

the pull-up region depends of the N-Well diffusion and generally is bigger than the pull-down network region once the PMOS transistors are larger than NMOS to compensate the charge mobility. Figure 4.2(a) show a static CMOS standard cell template.

When compared with CMOS templates, the MCML template, beyond of the supply lines presents the bias voltages of current mirrors and pull-up resistances that are shared by all circuit gates. The current mirror bias voltage ($Vbias$) is located on the bottom of gate layout, and the pull-up bias voltage ($Pbias$) at the top. Opposite to the CMOS layout, the MCML has only two PMOS transistors independently of the gate logic function. Therefore, the PMOS portion is smaller than the NMOS area. Furthermore, the NMOS portion is responsible to allocate the PDN and the bias current transistors.

The pull-up resistances and bias current transistors define the output voltage swing of the gate. A mismatch of these transistors between the gates can takes the circuits to fail because of insufficient output voltage swing propagation. Therefore, is important the use of regular structures to reduce the mismatch effects. Thus, the template also defines portions to allocate these structures. Figure 4.2(b) depicts the template definitions of MCML digital standard cell.

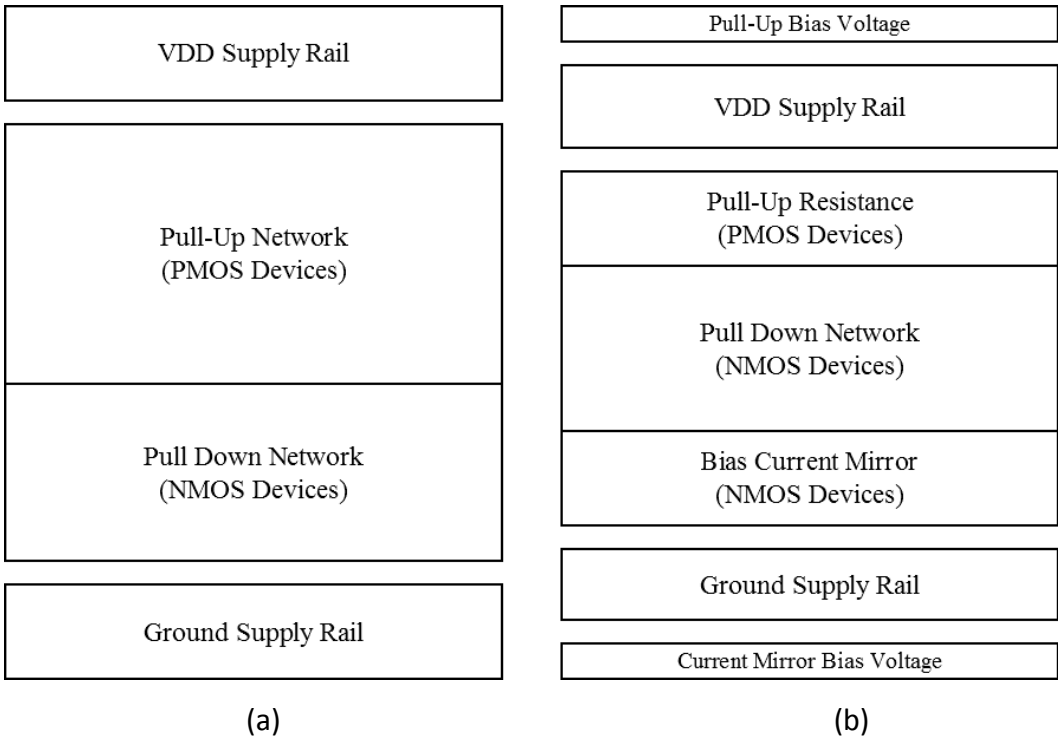


Figure 4.2: Cell Template (a)CMOS (b)MCML

4.2 Scaling Effects

The optimization of MOSFETs has different effects to analog and digital circuits. For digital CMOS circuits, the main performance requirement is the I_{on}/I_{off} ratio. While for analog circuits cutoff frequency (f_T), intrinsic gain (g_m/g_{ds}), linearity, noise, and device mismatches are the main requirements (LEWYN, YTTERDAL, *et al.*, 2009). Although MCML gates have a digital application, they have an analog operation behavior. Therefore the understanding of the analog requirements behavior with the process scaling is important to compare the logic topologies presented.

The maximum cutoff frequency that is represented by:

$$f_{Tmax} = \frac{v_{sat}}{2\pi L_{eff}} \tag{4.2}$$

note that it is function of saturation velocity (v_{sat}), and it increases with the decreasing of the channel length (L_{eff}). In a real case this frequency will not be achieve due to, for example, parasitic capacitances. But taking into account only a transistor without interconnects, the intrinsic speed transistor, f_i, is approximated as:

$$f_i \cong \frac{g_m}{2\pi(C_{gs} + C_{db})} \tag{4.3}$$

where g_m is the transistor transconductance, C_{gs} and C_{db} are the gate-source and drain-bulk capacitances.

For a given current density, the transistor scaling does not change the transconductance. It can be understood by observing the following expression of the strong-inversion drain current in the case of a fully velocity saturated transistor channel:

$$I_D = WC_{ox}(V_{gs} - V_t)v_{sat} \tag{4.4}$$

where W is the transistor width, C_{ox} is the gate oxide capacitance, V_{gs} is the gate-source voltage, V_t the threshold voltage and v_{sat} is the charge carriers saturation velocity.

Hence, considering that the threshold is independent of gate-source voltage and that in an ideal scaling $W\ \alpha\ L$ and $C_{ox}\ \alpha\ 1/L$, the transconductance is independent of L and is given by:

$$g_m = WC_{ox}v_{sat} \tag{4.5}$$

It is clearly that the transistors capacitance reduces with the process scaling. Therefore if the transconductances does not change the transistors intrinsic speed will increase with the technology scaling (LEWYN, YTTERDAL, *et al.*, 2009).

The degradation of transistor's intrinsic gain is the major challenge of analog design in earlier technologies. Figure 4.3 show the intrinsic gain versus the drain current of NMOS transistor for three technologies nodes. These curves were extracted through a SIPCE simulation considering the minimum transistor length and a fixed width of 2µm. Note that a degradation of almost 70% can be achieved on the intrinsic gain for a given drain current when comparing the 0.13µm and 65nm technologies.

Another electrical characteristic that is affected by the transistor scaling is the subthreshold and leakage currents. These currents mainly affect the I_{off} current on static CMOS circuits, resulting in static power consumption. Subthreshold currents increase exponentially as V_t decreases, so it is a major problem for circuits using low supply and threshold voltages. Subthreshold conduction is intensified by drain-induced barrier lowering (DILB) in which a positive V_{ds} reduces the threshold voltage.

The leakage current comes from two effects, the gate leakage and junction leakage; the second one is not a significant effect if compared with the first one. In modern state-of-art CMOS technologies the main mechanism of gate leakage current is the tunneling through the thin gate oxide. Therefore, this current is extremely sensitive to the oxide thickness (CHOI, NAM, *et al.*, 2001).

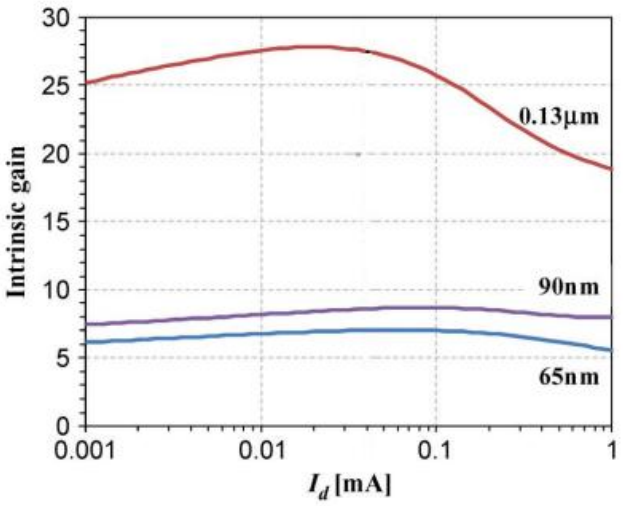


Figure 4.3: NMOS transistor intrinsic gain versus drain current for three different CMOS technologies nodes (LEWYN, YTTERDAL, *et al.*, 2009).

Considering MCML logic circuits, these currents do not appear in the power dissipation results. The only current that can affect the gate performance is the subthreshold voltage that represents a current flowing on the off MCML branch and it degrades the voltage swing output.

The scaling of CMOS process brings also the challenge of the variability effects. For MOSFETs devices, the most important variations are channel length, oxide thickness and threshold voltage. The first one is a result of photolithography, plasma and etching effects. Oxide thickness is well controlled and generally is more significant between wafers. Threshold voltage vary because of different doping concentration and annealing effects, mobile charge in the gate oxide, and discrete dopant variations caused by the small number of dopant atoms in tiny transistors (WESTE e HARRIS, 2005).

Due to the process variability the devices with the same specifications can achieve different electrical characteristics. Device matching has always been a major concern for analog CMOS circuit designer. Opposite to static CMOS logic gates, which are robustness to process variations, the MCML logic gates works based on differential pair networks, the mismatching between its devices can affect the gate functionality.

Thinking in a MCML digital standard cell, is not possible predict which circuit will be located around a specific cell. Therefore, is important the use of regular structures for the bias current mirror transistor and the pull-up transistors once these structures hardly affect the gate functionality. Some dummy structures can be used such that all current mirrors or pull-up resistors presents the same neighborhood. The cost of insert these dummy structures is the area overhead.

4.3 Circuits Performances

This chapter makes an evaluation of the performances of MCML against CMOS gates. This evaluation take as reference the power dissipation and speed performance of these topologies in a schematic level simulations. The post-layout comparison between these topologies are addressed in chapter 5.

Once the main goal of this work is design a high speed MCML gates, the CMOS gates used on this comparison also focus on it. Therefore, for the process technologies of XFab XC06 and IBM130, the design of the CMOS gates uses a study of the PN ratio

and the drive strength that give the best frequency operation of a ring oscillator. The sizing of the predictive technology model, PTM45, comes from the library available from NanGate. The Table 4.1 presents the values of PN ratio and the minimum width for each process technology.

Table 4.1: Sizing parameters of CMOS gates

Parameter	XFab XC06	IBM130	PTM45
PN Ratio	1.8	1.8	2
Minimum Width	4µm	1.6µm	250nm

Until this moment, the analysis of MCML gates considers that these gates have a free choice of bias current and voltage swing. Note that as discussed in section 4.1.2 for a MCML standard cell library the voltage swing of all logic cells must be standardized. Observing the results presented in section 3.2, is possible see that the voltage swing for high values of bias current presents a saturation tendency. This trend is mainly observed on the three inputs gate. Therefore, the following analysis standardize the voltage swing of each technology according to the voltage swing behavior commented. The Table 4.2 detail the voltage swing used for each technology.

Table 4.2: Standard voltage swing used on MCML gates

Technology	XFab XC06	IBM130	PTM45
Voltage Swing	1.5V	600mV	500mV

4.3.1 Ring Oscillator

The first evaluation between the two logic styles is the performance of ring oscillators. The ring oscillators can evaluate the performance of the gates once it is self-excited. Therefore, no external signal sources are used to generate the propagated signal.

The testbench constructed is a ring oscillator with 13 stages made for each gates input. The propagated signal passes always by the same input. The others gate inputs remain in a static value. In the CMOS case, the static values come from ideal sources that generate a zero or supply voltage levels according to the logic input value. The

MCML ring oscillators obtain the static inputs from the circuit represented in Figure 3.4.

The performances evaluation takes as reference the slowest input of the gate. The Figure 4.4 depicts the AND2 ring oscillator frequency achieved by the CMOS and the MCML. Notice that the MCML frequency is function of bias current used. The evaluation takes the CMOS speed performance as the target specification. Therefore, the MCML gate bias current is set to the value that achieves the same frequency response.

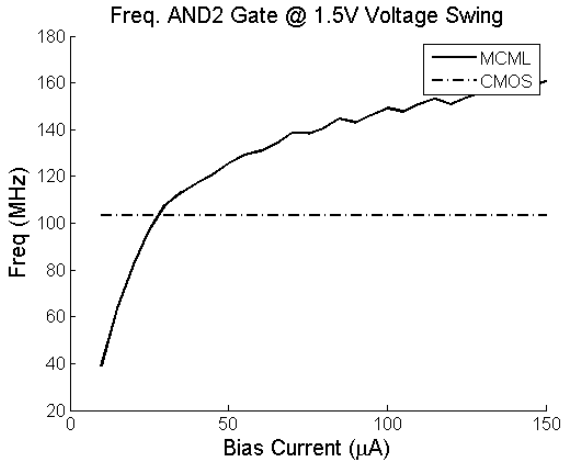


Figure 4.4: MCML oscillator frequency as function of bias current

The Table 4.3 shows the bias current necessary to the MCML gates reach the same frequency performance of CMOS gates in the ring oscillator circuit. Observe that the bias current of buffer and NAND gates for the IBM130 and PTM technology are not available. These gates present a frequency response out of the range analyzed by the MCML design.

Through an HSPICE simulation, the testbench extracts the charge spent by one gate, in a charge and discharge cycle of the CMOS ring oscillator. Assuming that CMOS circuit only consumes energy during the switching process, the power of the circuit is approximated by the multiplication of this charge, the oscillation frequency and supply voltage. In the case of MCML ring oscillator, the power is the bias current of the gate times the gates quantity and the supply voltage. With these assumptions, is possible estimate the number of ring oscillator stages in which the power dissipation equalize for CMOS and MCML gate.

Table 4.3: Bias current necessary to reach the CMOS frequency.

Analyzed Gate	MCML Bias current per gate (μA)		
	XFab XC06	IBM130	PTM45
XOR3	10	5	7
OR2	17	8	13
OR3	18	8	11
XOR2	23	10	15
AND2	30	15	16
NOR3	37	10	15
NOR2	40	40	46
AND3	44	10	41
Buffer/Inv.	110	N/A	N/A
NAND2	193	N/A	N/A
NAND3	225	N/A	N/A
FA (SUM)	10	5	7
FA (Carry)	15	7	10

Figure 4.5 illustrates the behavior of CMOS and MCML power dissipation in a ring oscillator according to the number of stages. The example considers ring oscillators constructed with AND2 gates of IBM130 technology. The CMOS ring oscillator uses gates with the sizing indicated in Table 4.1 and the MCML presents a bias current of 15μA as indicated in Table 4.3. The maximum frequency operation obtained for a single AND2 gate at schematic simulation in typical case was 8.74GHz. Note that the number of stages in a ring oscillator is inversely proportional to its operation frequency. Therefore, according to equation (4.1) the power dissipation of CMOS decreases as the stage number of ring oscillator increases. On the other hand, the power dissipation of a MCML ring oscillator increase linearly with the number of stages, it is well explained by the constant bias current that flow in each MCML gate.

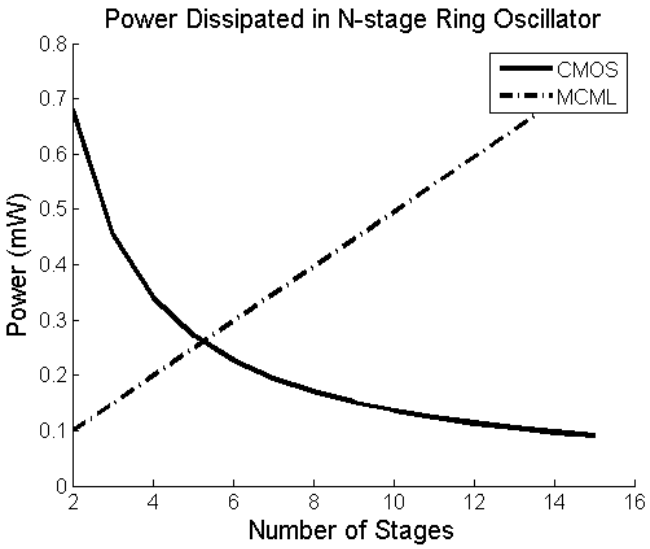


Figure 4.5: Power dissipation of a AND2 ring oscillator versus the number of stages

This study can be approximated as the optimum number of stage that is advantageous use MCML or CMOS gates. Less stages corresponds to a higher operating frequencies therefore MCML is preferred. The Table 4.3 presents in the first column the gates analyzed and the following columns show the number of stages where the MCML and CMOS power curves crosses, and the correspondent operating frequency.

Making an analysis on the Table 4.4, remember that all MCML gates compared process its logic function in one stage, then the gates that need more stages to compute the logic function in CMOS, i.e. XOR, OR, AND dissipates more power and the ring oscillators that equalizes the power have more stages. The second fact that call attention is CMOS gates that use transistors staking in the pull-up network (OR, NOR). This construction makes the CMOS gates slower than AND and NAND gates. Therefore, as in the MCML circuits all logic function is performed by PDN with NMOS transistors, the ring oscillators that equalizes the power of OR gates have more stage than that constructed by ANDs.

Analyzing the performance of the different technologies, notice that small supply voltage and MOSFET capacitances provide more efficient circuits to the static CMOS style. Therefore, the operation frequency that equalizes the power dissipation of both logic styles increases with the technology advance. Note that, for the PTM45 technology, the ring oscillators constructed with gates up to two inputs only present better power performance in MCML for frequencies above 5 GHz.

Table 4.4: Number of stage and consequently operation frequency that equalizes the dissipated power of ring oscillators.

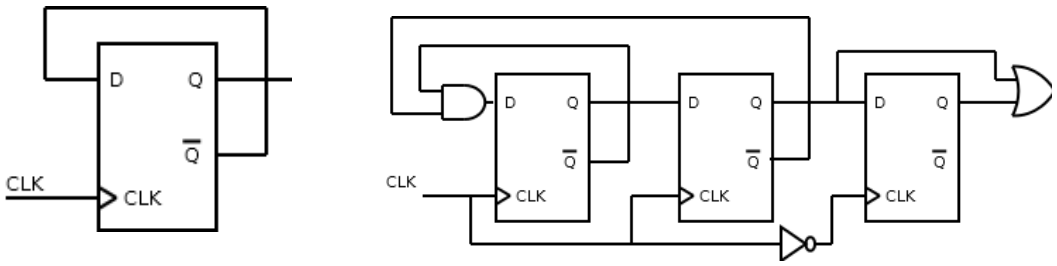
Analyzed Gate	XFab XC06		IBM130		PTM45	
	Nº stage	Equivalent Frequency	Nº stage	Equivalent Frequency	Nº stage	Equivalent Frequency
FA (SUM)	9	35MHz	11	198MHz	7	1.28GHz
XOR3	9	38.5MHz	11	215MHz	7	1.4GHz
FA (Carry)	9	51.2MHz	12	262MHz	8	1.7GHz
OR3	7	97MHz	8	622MHz	6	3.28GHz
XOR2	7	164MHz	8	976MHz	6	5.6GHz
OR2	6	176MHz	8	936MHz	5	6.12GHz
NOR3	5	168MHz	7	874MHz	5	5.16GHz
AND2	5	268MHz	6	1.45GHz	4	9.45GHz
AND3	4	238MHz	7	882MHz	3	9.33GHz
NOR2	4	380MHz	4	2.7GHz	3	15.2GHz
Buffer	3	1.26GHz	N/A	N/A	N/A	N/A
NAND2	2	1.11GHz	N/A	N/A	N/A	N/A
NAND3	2	690MHz	N/A	N/A	N/A	N/A

4.3.2 Frequency Divider

PLLs, which are widely used in communication systems, depend on high-speed frequency dividers for their proper operation. The frequency divider takes the reference clock and divides it by some value to reach the target clock frequency used in the circuit. Note therefore those frequency dividers are in a continuous switching, and it configures a good MCML application.

In order to evaluate the performance of CMOS and MCML gates in a frequency divider, three of them are simulated. The first one is a divider by two that consists of a master-slave flip-flop with a feedback loop from the negate output to its input, see Figure 4.6(a). The second one is a divider by three, represented in Figure 4.6(b), this topology provides a 50% duty cycle. And the last implementation is divider of four that consist of a chain with two dividers of Figure 4.6(a).

The testbench receives the input clock of ideal voltage sources, and consider as output load an inverter gate. The test has as objective find the highest input clock frequency that the divider is still able to do his correct function. The boundaries consider is the correct output frequency value, and in the MCML case, the output voltage swing must satisfy a value of 60% of the design one. The test also extracts the average bias current of the frequency divider.



(a) (b)

Figure 4.6: Frequency divider by (a) two, (b) three

The Figure 4.7 illustrates the maximum frequency achieve by the MCML gates of XFab XC06 technology as function of the bias current used. Note that as observed in the propagation delay extraction, section 3.2, there is a saturation of speed performance of the gates according to the increasing of bias current. Therefore, the MCML gates that compose the testbench uses a bias current that characterizes the saturation point, that are 50µA, 15µA and 20µA for XFab, IBM and PTM technologies respectively.

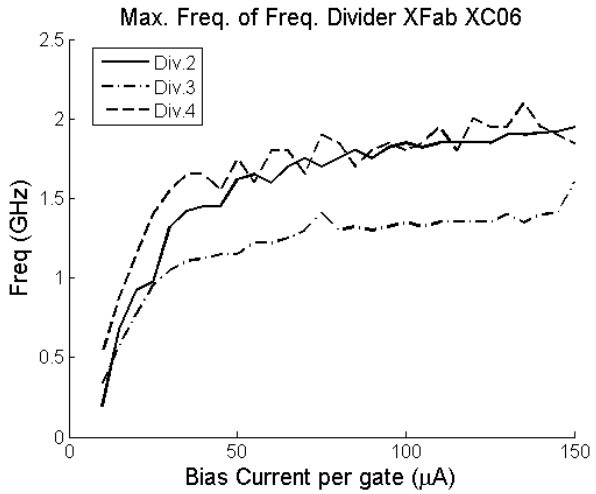


Figure 4.7: Maximum frequency achieved in the frequency divider of XFab XC06 gates.

Follows in the Table 4.5, 4.6 and 4.7 the results of the frequency divider circuits for the technologies XFab XC06, IBM130 and PTM45 respectively. In the tables the first column indicates which the circuit divider is analyzed. The second and third columns shows the maximum frequency achieve by the CMOS and MCML circuits respespectively. The average current of the circuits are present in the last two columns.

The results show that generally the MCML gates can achieve approximately a twice maximum frequency that accomplished by the CMOS gates. Furthermore, considering the XFab XC06 and PTM45 technology, the current used by MCML circuits to reach these frequencies is almost 8% of the CMOS circuit for the half frequency generator, 5% for the divisor by four and 15% for the divider by three. Taking into account the IBM130 technology these percentages are 3.5%, 6% and 5% for the divider by two, three and four respectively.

Table 4.5: Max. Freq. and Avg. current achieves in the Freq. divider circuits using XFab XC06 technology.

Freq. Divider	XFab XC06			
	Max. Frequency		Average Current	
	CMOS	MCML	CMOS	MCML
CLK/2	600MHz	1.5GHz	1.19mA	100µA
CLK/3	500MHz	1.1GHz	2.7mA	400µA
CLK/4	550MHz	1.5GHz	1.75mA	200µA

Table 4.6: Max. Freq. and Avg. current achieves in the Freq. divider circuits using IBM130 technology.

Freq. Divider	IBM130			
	Max. Frequency		Average Current	
	CMOS	MCML	CMOS	MCML
CLK/2	4.2GHz	7GHz	846µA	30µA
CLK/3	3.5GHz	6.5GHz	1.9mA	120µA
CLK/4	3.9GHz	9GHz	1.24mA	60µA

Table 4.7: Max. Freq. and Avg. current achieves in the Freq. divider circuits using PTM45 predictive model.

Freq. Divider	PTM45			
	Max. Frequency		Average Current	
	CMOS	MCML	CMOS	MCML
CLK/2	17.7GHz	30GHz	551µA	40µA
CLK/3	14.9GHz	25GHz	1mA	160µA
CLK/4	15.8GHz	32GHz	782µA	80µA

Considering that the frequency of CMOS is linearly dependent of the frequency, another study done is the frequency reached by the CMOS circuits if the average current is equalized between the MCML and CMOS logic styles. Therefore, Table 4.8 shows the CMOS resultant frequency for this case. Note that the less affect circuit is the divider by four, although the best case represent only 9% of the frequency operate by the MCML circuit.

Table 4.8: Working frequency of frequency divider circuits for a equalized average current.

	XFab XC06			IBM130			PTM45		
	CMOS (MHz)	MCML (GHz)	$\frac{CMOS}{MCML}$	CMOS (MHz)	MCML (GHz)	$\frac{CMOS}{MCML}$	CMOS (MHz)	MCML (GHz)	$\frac{CMOS}{MCML}$
CLK/2	50	1.5	3%	148	7	2%	1.28	30	4%
CLK/3	74	1.1	2%	221	6.5	3.5%	2.34	25	2%
CLK/4	62.8	1.5	4%	188	9	9%	1.61	32	5%

In general terms the frequency divider is prejudicial for CMOS gates. The Flip-flop gates in the conventional CMOS style comprises several internal switching stages to output the resultant signal. Other element that benefits the MCML gates in these circuits is the complementary output. Notice in Figure 4.6 that the flip-flop needs a negate output and in the MCML gates it is generate for all gates by its functionality.

5 SILICON IMPLEMENTATION

This chapter describes the physical implementation of a set of MCML gates in order to analyze the behavior and requirements necessary to use them with PNR tools of digital circuit designs. The technology used to the physical implementation is the XFab XC06. The physical implementation consists of eight MCML structures. Each structure is a ring oscillator constructed with the MCML designed gates. The oscillators propagate the signal of the inputs that present the worst propagation delay of each cell. The gates analyzed are AND2, XOR2, AND3, XOR3 and FA. Note that AND2 and AND3 MCML cells topologies are the universal MCML gates as explained in section 2.3.

The MCML full adder gate (FA) was analyzed with two different topologies, and for each topology, the signal of sum bit and the carry bit were analyzed. Therefore, four different ring oscillators compose the physical implementation of the FA gates. The Figure 5.1 depicts the two FA topologies. Gates with two inputs compose the first topology, as illustrated in Figure 5.1(a). This topology uses simpler, and faster, gates but needs more stages to process the add function. This chapter makes the reference to this topology calling this full adder as FA1. The second topology, referred as FA2 in this chapter, uses only one stage to process the logic function. However, it depends on gates that are more complex, i.e. an XOR3 is responsible for processing the sum output, and a majority gate gives the output carry. Figure 5.1(b) shows the second FA implementation.

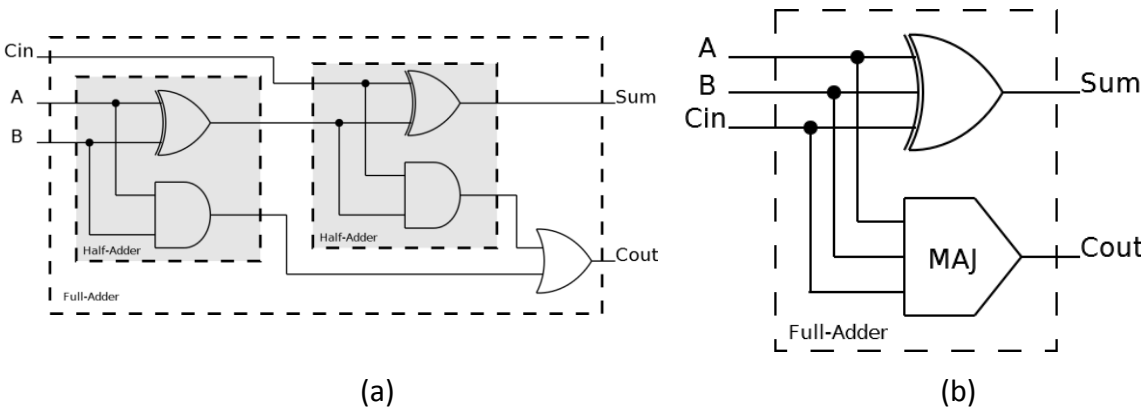


Figure 5.1: Full Adder Topologies (a) FA1 (b) FA2.

The results obtained in the section 3.2.1 give a large number of designed MCML gates. Hence, a choice of which bias current and output voltage swing must be done. The physical implementation takes into account the saturation behavior of the propagation delay as a function of the output voltage swing and bias current of the gates. Therefore, the gates used in the ring oscillators consider an output voltage swing of 1.5 V and a bias current of 50 µA for each stage of the gate.

Note that the AND and XOR gates have only one stage to processing the logic function. Therefore, the total bias current of each cell is 50 µA. In another hand, FA uses more stages to compute the logic function. Hence, the total bias current of each FA1 presented in Figure 5.1(a) is 250 µA while the FA2, Figure 5.1(b), is 100 µA. Focusing in compare the performance of designed MCML gates against the CMOS gates, the ring oscillators were also implemented with a commercial CMOS standard cell library of XFAB XC06 technology. Table 5.2resume the design parameters used in the MCML gates design of this chapter.

Table 5.1: MCML Design parameters used in the silicon implementation

	Voltage Swing (V)	Bias Current per Gate (µA)
FA1_CI	1.5	250
FA1_SUM	1.5	250
FA2_CI	1.5	100
FA2_SUM	1.5	100
AND2	1.5	50
AND3	1.5	50
XOR2	1.5	50
XOR3	1.5	50

The MCML ring oscillators need static voltage values at the inputs that do not propagate the signal. Therefore, two circuits similar to that represented in Figure 3.4 provide these voltage levels. MCML XOR2 gates compose the first circuit, given static signals from two input gates. The second static circuit is a chain of XOR3 gates that gives the static signals from three input gates.

5.1 Reliability Design

The analog behavior of MCML style makes this logic family susceptible to PVT variations. Opposite to the CMOS logic gates that are almost insensitive to device variations, a variation on the device characteristics in the MCML logic cells can lead them to fail on its functionalities.

In order to overcome the PVT variations, gate simulations were performed at corners situations. On these simulations, it is possible to note that the most prejudicial case for the gate robustness happens when the MCML logic gate performs a small voltage swing and a small current capability in the PDN. Therefore, the worst case is at low supply voltage, worst zero MOSFETs condition (fast PMOS and slow NMOS) and high-temperature case. On the other hand, the worst propagation delay occurs in the corner that presents a high output voltage and low current capability, which corresponds to a high voltage supply and worst speed MOSFETs conditions.

The output swing control circuit illustrated in Figure 2.13 compensates the global process variations on the PMOS devices. Note that this circuit does not provide a negative $Pbias$ voltage. Therefore, in the worst-case design, the designer should consider a slowest PMOS device. This PMOS condition provides the highest voltage drop on the pull-up network. Hence, the control circuit supplies the lowest $Pbias$ voltage given to the pull-up device the highest possible gate-source voltage. In the cases where the PMOS device has less resistive characteristics, the control circuit is able to output a positive $Pbias$ voltage that compensates the resistive characteristics to the device. Considering this PMOS sizing, the worst-case design, to reach the robustness of the gate, results in a wider PMOS device than the typical design.

Taking into account the effect of worst-case design on the PDN, there is no control to compensate the loss on the transistors gain. Hence, the slowest NMOS should be considered, and the sizing of the gate for this case must achieve the gain necessary to propagate the MCML logic signal. Moreover, in this case, occurs the highest voltage drop on the PDN. High values of PDN voltage drop pulls drain voltage of bias current mirror transistor down. This fact corresponds to the worst operation case to the bias current mirror transistor. Sizing the gate for this case guarantees that the gate will work well for other corners cases, with a sufficient gain and an enough voltage overdrive on

the bias current transistor. The drawback of design for this condition is that it requires an increase on the PDN transistor, degrading the propagation delay because of the parasitic capacitances addition.

Corners simulations are the extreme operating cases. In those situations all devices of the design are working in the same condition. Hence, the occurrence probability of this scenario is very low. In order to obtain a yield probability of the circuits, a Monte Carlo analysis considering only the PVT variations without mismatch between devices is performed. Table 5.2 and Table 5.3 present this the Monte Carlo analysis results for the designed XOR2 and XOR3 gate respectively. The presented Monte Carlo analyzes consider 1000 samples. The table organization gives, in the first column, the parameter analyzed follow by the mean value of these parameters in the second column and the standard deviation in the third column. The fourth and fifth columns present the perform parameters for the cases of three sigma operation, which corresponds that approximately 99.7% of the IC designed will achieve a performance between these two values.

Notice that the Monte Carlo analyzes were done with the cells designed to achieve a sufficient gain in the logic cell at the corners operation. Hence, even the - 3σ condition of XOR2 gate results in a gain equals to two, i.e. when the input achieve a half of voltage swing the output already perform the entire transition. This value is even greater in the XOR3 gate. This fact demonstrates that the more complex gates are more sensitive to the global process variations effects.

Making an analysis of the PVT variations on the worst input propagation delay, the design in typical condition gives a result of 440ps for XOR2 gate and 723ps for the XOR3, as presented in Table 3.2 and Table 3.3. Therefore, the design for the corners conditions penalizes the speed response of the gate in 48% the XOR2 gate and 56% the XOR3.

Note that the above results, Table 5.2 and Table 5.3 show the influence of PVT variations without consider the mismatching of the devices. The MCML topology works with a series of structures that are susceptible to the mismatching effects, the bias current mirrors, the differential pairs of the PDN and even the pull-up resistances are affected by the mismatching. The Pbias control circuit is able to compensate a global process variation, the same happen with the bias current mirror, but these circuits do not provide a protection against the local variations, or in other words, against the mismatch

effects. Therefore, another Monte Carlo analysis was done taking into account also the mismatch effects. Table 5.4 and Table 5.5 show the results of this analysis for the XOR2 and XOR3 MCML gates respectively. In these tables were added in the sixth column the gate yield. The yield consider as boundaries a gate gain higher than the unity, a positive noise margin and an output voltage swing higher than 60% of nominal value, in this case 0.9V.

Table 5.2: Monte Carlo analysis of MCML XOR2 logic gate

XOR2	Mean	Standard Deviation	- 3σ	+ 3σ
Upper Input Gain	2.29	0.07	2.09	2.49
Lower Input Gain	2.26	0.07	2.04	2.49
Upper Input NM	47%	0.8%	44%	49%
Lower Input NM	48%	1.0%	45%	51%
Upper Input Delay (ps)	500.00	17.16	448.52	551.48
Lower Input Delay (ps)	655.00	22.00	589.00	721.00
Output Swing (V)	1.31	0.01	1.28	1.35

Table 5.3: Monte Carlo analysis of MCML XOR3 logic gate

XOR3	Mean	Standard Deviation	- 3σ	+ 3σ
Upper Input Gain	2.97	0.07	2.76	3.18
Middle Input Gain	3.02	0.09	2.75	3.29
Lower Input Gain	2.94	0.09	2.68	3.20
Upper Input NM	54%	0.4%	53%	55%
Middle Input NM	56%	0.5%	54%	58%
Lower Input NM	56%	0.7%	54%	58%
Upper Input Delay (ps)	663.00	23.05	593.85	732.15
Middle Input Delay (ps)	1021.00	34.50	917.50	1124.50
Lower Input Delay (ps)	1131.00	36.65	1021.05	1240.95
Output Swing (V)	1.33	0.01	1.30	1.37

The comparison between the results achieved with and without mismatch effects show that, as expected, the MCML gates are tolerant to global effects but susceptible to mismatch effects. The variation on the bias current mirrored to the cell associated with the mismatch of the gate branches degrades the yield of the gates. It is possible note that gates with more inputs are more affected by the mismatch effect.

Table 5.4: Monte Carlo analysis of MCML XOR2 logic gate considering mismatch

XOR2	Mean	Standard Deviation	- 3σ	+ 3σ	Yield
Upper Input Gain	2.11	0.38	0.98	3.24	99.9%
Lower Input Gain	2.27	0.11	1.93	2.61	100%
Upper Input NM	47%	19%	-9%	103%	99.9%
Lower Input NM	51%	17%	-1%	103%	100%
Upper Input Delay (ps)	519.7	98.00	225.70	813.70	
Lower Input Delay (ps)	670.45	88.12	406.09	934.81	
Output Swing (V)	1.36	0.31	0.43	2.3	98.1%

Table 5.5: Monte Carlo analysis of MCML XOR3 logic gate considering mismatch

XOR3	Mean	Standard Deviation	- 3σ	+ 3σ	Yield
Upper Input Gain	2.71	0.56	1.05	4.38	98.6%
Middle Input Gain	2.88	0.36	1.79	3.98	100%
Lower Input Gain	2.95	0.14	2.54	3.36	100%
Upper Input NM	54%	18.7%	-2%	110%	99.9%
Middle Input NM	57%	17.7%	4%	110%	100%
Lower Input NM	59%	17.3%	7%	111%	100%
Upper Input Delay (ps)	697.00	140.00	277.00	1117.00	
Middle Input Delay (ps)	1052.00	182.00	506.00	1598.00	
Lower Input Delay (ps)	165.00	147.50	722.50	1607.50	
Output Swing (V)	1.38	0.32	0.41	2.35	98.7%

5.2 Layout Implementation

The layout of MCML gates follows the template guidelines presented in section 4.1.4. For the designed gates the supply rails present 4µm of height, the technology has specification give a conductibility of 1mA/µm o metal 1. Therefore, this rail height can supply up to 80 MCML gates in the same array. The bias lines ($Pbias$ and $Vbias$) have the minimum width to insert a contact from metal 1 to poly. Ignoring the circuit start-up, there is no current flowing on these lines; hence the voltage drop and current density are not a problem on the bias lines. The Figure 5.2 illustrates the template pointing the common metal rails of gates. The figure also highlights the three regions of the template (PUN, PDN and Bias Current Source).

Notice that the bias current source of the XOR2 gate has two transistors in parallel. This current mirror doubles the bias current of the reference bias transistor. In the case of a gate with a larger strength, parallel transistors are added to the bias current source. A gate with larger bias current requires that the pull-up devices reduce its resistance by the same factor to guarantee the same voltage swing. This reduction comes adding parallel pull-up transistors too. The strategy of use parallel transistors on the bias current source and PUN to achieve a higher gate strength does not change the height of the cell

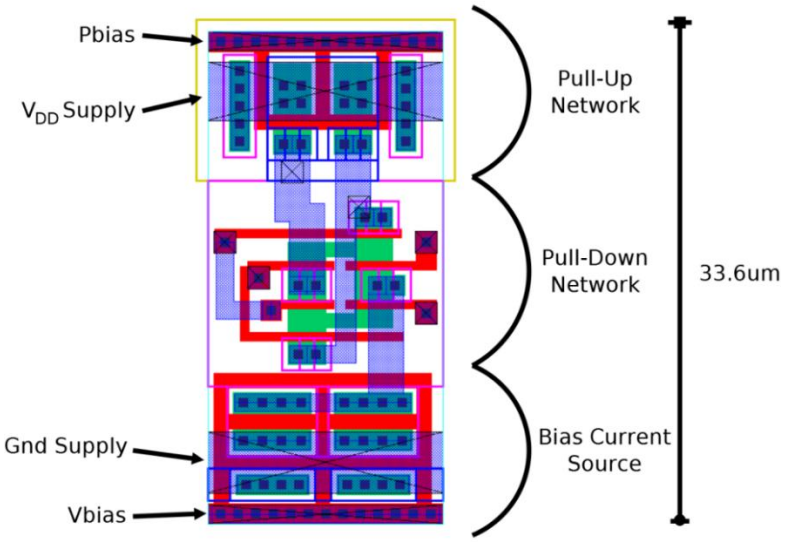


Figure 5.2: MCML XOR2 Layout and the template specifications

In a general form, the MCML XOR2 gate is a simple MCML gates layout, there are only two levels of differential pairs and the inputs controls only one or two differential pairs. Figure 5.3 depicts the layout of the MCML XOR3 cell. Observe that the strategy used in the PDN layout makes the signal propagate from the left to the right side. Hence, the addition of a differential pair level creates wider gates and does not increase the cell height.

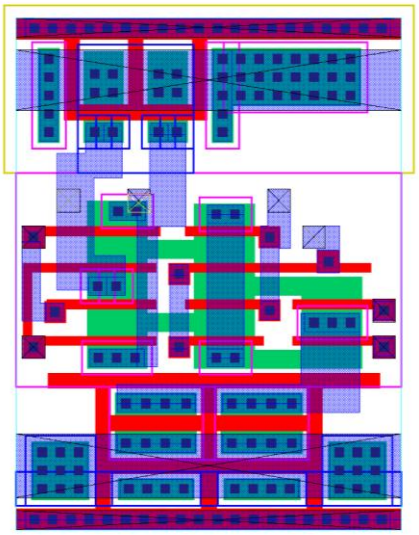


Figure 5.3: Layout of MCML XOR3 gate.

The height limitation of the set of designed gates comes from the FA1 gate. Figure 5.4 shows this layout. This gate needs two PUN and bias current source to process its functionality, which in this case are two logic functions (XOR3, MAJ). In order to increase the matching between these structures, dummy devices were added. The limitation on the height occurs because of the interconnections between the inputs of the two logic functions. These connections take place through the horizontal polysilicon lines. Comparing to a commercial CMOS library the resultant cell height is almost 30% greater, 26.4µm in the CMOS and 33.6µm in MCML.

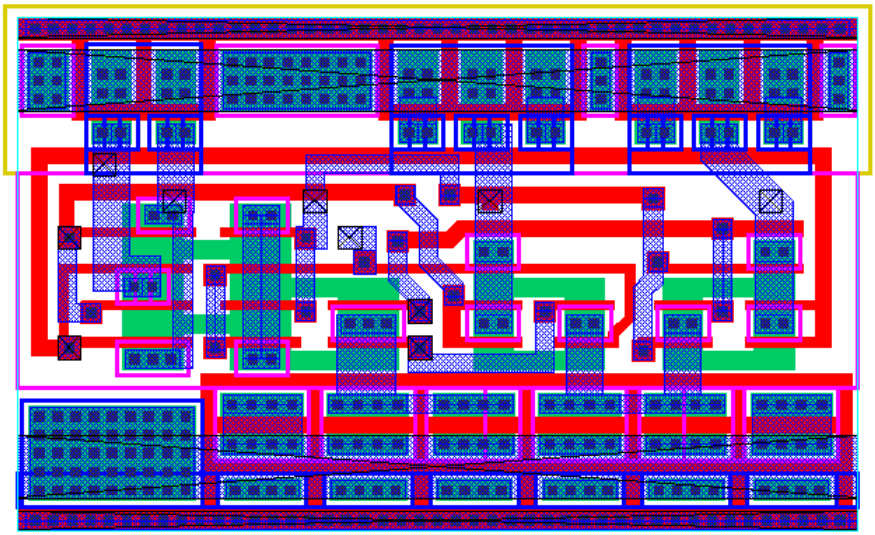


Figure 5.4: Layout of MCML Full Adder (FA1)

5.3 Special MCML Cells

The analysis of the ring oscillator signal comes from the extraction of the propagated signal in a stage of the oscillator. A CMOS multiplexer select the ring oscillator that sends the signal to the output of the IC. Therefore, the MCML signal of ring oscillators should be converted to a CMOS level before the analysis. The conversion from MCML to CMOS circuit can be performed by using a differential single-ended amplifier follow by a CMOS inverter, Figure 5.5. The amplifier only requires enough gain to amplify the MCML signal beyond of the inverter threshold voltage. Hence, the inverter output presents the CMOS output levels. Note that the opposite direction of conversion, CMOS to MCML, is possible directly applying the CMOS signal with his complementary in an MCML buffer gate.

In order to be feasible the use of MCML cells on the PNR tools, all gates should bear the form of the standard cells. Therefore, the layout of the reference transistor of the bias current mirror and the reference pull-up transistor must be designed with the template of the gates. Furthermore, these structures should present the same design layout of the PUN and bias current source of the logic gates reducing the mismatch problems. The PNR tools also use the insertion of fillers cells to fill the empty spaces in the layout design. The fillers are responsible by the link of standard layers of the cell

template between all cells. The bias and supply rails together with the n-well, P and N implant area compose the filler designed for the MCML library.

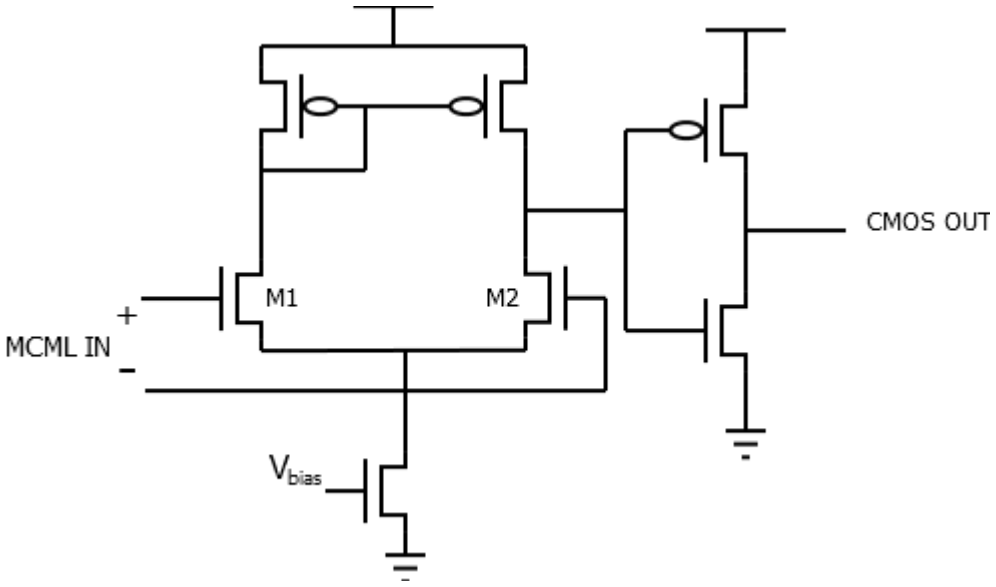


Figure 5.5: MCML to CMOS signal converter.

5.4 Physical Synthesis

The PNR tools use a Library Exchange Format (.LEF) file to correct place the cell and interconnect them. The LEF file describes the physical attributes of library cells, including port locations, layers, and vias definitions. LEF specifies enough information to allow the PNR tools connect the cells without generating conflicts with the internal cell constraints. This work uses the Abrastract Generator to obtain the LEF file. Figure 5.6 shows the abstract view generated for the MCML XOR2 cell. Each graphical representation indicates a blockage for a certain design layer.

The LEF file also identifies the supply rails of the cell; this is the point that the MCML LEF generation differs from the static CMOS ones. The MCML LEF generation takes into account that the lines responsible for the bias voltages of the cell have the same configurations of the supply rails. In the LEF file, these lines are specified as global nets, it gives the possibility of defined previously in the physical synthesis the distribution of bias signals as the supply voltages.

With the layout, LEF file and a circuit netlist that already define the cell that should be used in the synthesis is possible make a physical synthesis. The higher levels

of the digital design flow depend on the generation of others files, for example, the Liberty file (.LIB) that give the delay specifications of the cells.

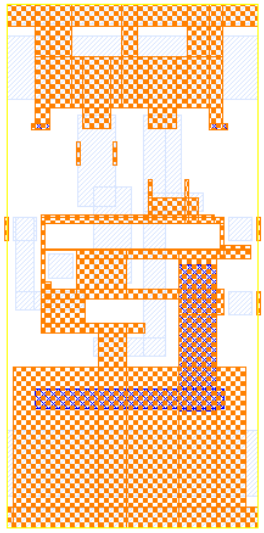
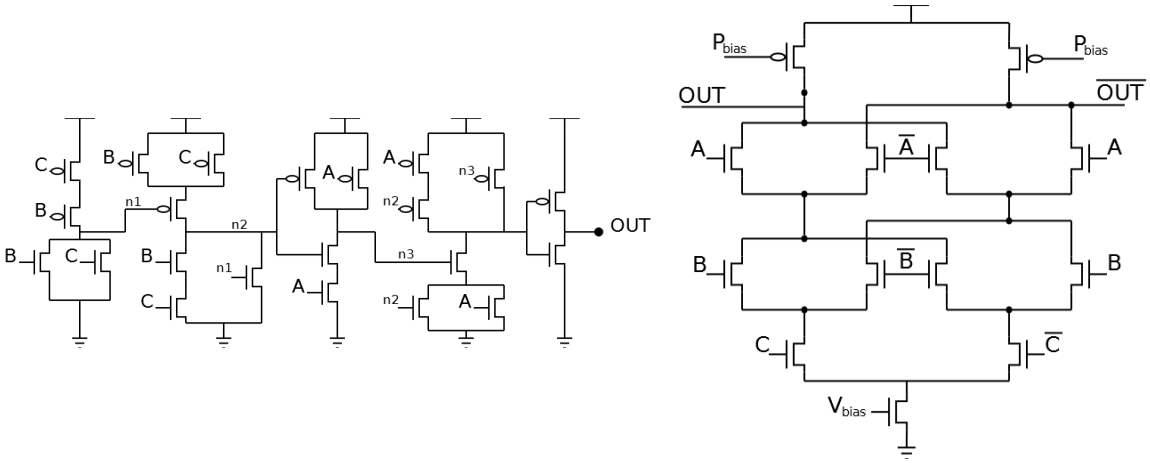


Figure 5.6: Abstract view of MCML XOR2 cell.

5.5 Analysis and Results

In order to compare the area performance of the MCML against the CMOS gates, Table 5.6 presents an analysis of the resultant area of both topologies design. As already cited in section 5.2 the height of designed MCML cells presents an increase of almost 30% if compared with the CMOS cells. The cell's width also demonstrates that CMOS gates present a better area performance. Only the XOR3 gate presents a smaller width in the MCML style. The static CMOS logic style depends on several logic stages to implements the XOR3 logic function. Figure 5.7 shows that the MCML topology can implement the XOR3 function with a simpler network. However, the total area still is smaller in CMOS gate. In general terms, the conclusion is that the standard structures, as the bias current source and the bias voltage lines, of MCML cells makes the total area prejudicial to this topology.



(a) (b)

Figure 5.7: XOR3 topology using (a)static CMOS and (b) MCML topologies

Table 5.6: Cell area analysis

Gate	CMOS		MCML		% Area Increase
	Width (μm)	Area (μm^2)	Width (μm)	Area (μm^2)	
AND2	9.2	242.88	16.1	540.96	123%
OR2	9.2	242.88	16.1	540.96	123%
NAND2	6.9	182.16	16.1	540.96	197%
NOR2	9.2	242.88	16.1	540.96	123%
XOR2	16.1	425.04	16.1	540.96	27%
AND3	11.5	303.6	27.6	927.36	205%
OR3	11.5	303.6	27.6	927.36	205%
NAND3	13.8	364.32	27.6	927.36	155%
NOR3	13.8	364.32	27.6	927.36	155%
XOR3	29.9	789.36	25.3	850.08	8%
FA*	36.8	971.52	55.2	1854.72	91%
MUX2	16.1	425.04	16.1	540.96	27%

*The comparison take as reference the MCML FA2

The second analysis done is about the layout efficiency. The layout design includes parasitic capacitances and resistances. These parasitic degrade the speed performance of the cells. With the goal of analyzing this performance loss, Table 5.7

presents the frequency achieved by the designed MCML ring oscillators at schematic level and at layout extraction simulation. The first column of this table details the gate analyzed. Note that the full adder ring oscillators names in this columns have a suffix in the name. This suffix identifies which is the propagated port signal in the ring oscillator. The CI suffix indicates the propagation of the carry signal in the ring oscillator, while the SUM suffix corresponds to the SUM bit propagation. The second and third columns show the frequency achieve by the ring oscillators and the last column presents the percentage of the frequency decreased from the schematic to the layout extraction simulation.

The results of Table 5.7 demonstrate that the usage of basic logic gates to construct the FA1 adds more parasitic. So, the frequency of the sum bit presents the worst speed performance degradation, 39%. According to Figure 5.1, this is the input that has more interconections in the propagation path. Furthermore, the second full adder topology achieves an absolute maximum frequency higher than the first one with less power dissipation once that the FA1 consumes 250μA by each gate while the FA2 only consumes 100μA by gate as presented in Table 5.1.

The ANDs and XORs gates analyses show that the difference of speed performance between the schematic and layout simulations is lower in the three inputs gates. Note that the layout constructions use abutment techniques. The schematic simulation considers no sharing of the transistors diffusions. Then, the abutment technique can reduce the source and drain capacitances of the cells transistors. This fact appears with more impact in three input gates once there are more transistors in the network of these cells. In another hand, the interconnections of the gates degrade the speed performance in both cases.

With the regard to the speed and power dissipation of the designed MCML gates and the commercial static CMOS gates, Table 5.8 presents the working frequency of the analog extracted simulation of the ring oscillators constructed as well the power dissipated by them. The first table column presents the gate analyzed. The frequency results can be seen in the second and third columns for CMOS and MCML topologies respectively, followed by the percentage relation between these results in the fourth column. The last three columns show the power dissipation results, being the fifth column the power of CMOS ring oscillators followed by the MCML power in the sixth

column. The last column details the relation between the power dissipation of the studied topologies.

Table 5.7: Frequency response of ring oscillators

	Frequency (MHz)		% Frequency Reduction
	Schematic	Layout	
FA1_CI	15.10	11.59	23%
FA1_SUM	19.10	11.69	39%
FA2_CI	25.11	18.35	27%
FA2_SUM	23.19	17.95	23%
AND2	35.39	29.10	18%
AND3	21.33	20.55	4%
XOR2	31.52	28.48	10%
XOR3	17.80	17.68	1%

Note that the FA1 implementation as already demonstrated in Table 5.7 is not the best full adder implementation. This implementation presents only 61% of the frequency performed by the carry propagation of the CMOS implementation. Note that the CMOS full adder implementation has a carry frequency response that almost doubles his sum output frequency. The MCML FA2 presents an advantage over the CMOS implementation on the sum bit output speed performance. This parameter is 68% greater than the CMOS implementation. The two inputs gates also present better performance in MCML topology comparing to the static CMOS one. Note that this advantage is only 9% in the NAND2 gate, but the XOR2 gate presents 25% of frequency increasing. This highlights the advantage of MCML over CMOS gates that are composed by multi stages circuit and depend on more complexes pull-up networks. The implementation of three inputs gate in MCML topology fails in achieve higher frequency than the CMOS topology. The transistor sizing increasing required to overcome the PVT variations presents more impact on the performances than the cases of two input gates. It is possible that a resizing of these gates with a higher bias current perform a better frequency response than CMOS gates.

The power dissipation result demonstrates that MCML gates are power hungry for low frequency circuits comparing with the static CMOS family gates. The

implemented ring oscillators have 29 stages; the study of section 4.3.1 demonstrates that MCML is advantageous for short logic paths that operate at high frequencies. On that analysis, the best case indicates ring oscillators up to 9 stages are advantageous for this technology. Therefore, the high power dissipation of the implemented ring oscillators was expected.

Table 5.8: Analog extracted simulation results

Gate	Frequency (MHz)			Power (mW)		
	CMOS	MCML	$\% \frac{\text{MCML}}{\text{CMOS}}$	CMOS	MCML	$\frac{\text{MCML}}{\text{CMOS}}$
FA1_CI*	19.01	11.59	61%	3.07	24.74	8.1
FA1_SUM*	10.68	11.69	109%	1.80	24.76	13.8
FA2_CI*	19.01	18.35	97%	3.07	10.38	3.4
FA2_SUM*	10.68	17.95	168%	1.80	10.39	5.8
NAND2	26.71	29.10	109%	1.68	5.571	3.3
NAND3	24.58	20.55	84%	1.73	5.591	3.2
XOR2	22.87	28.48	125%	1.87	5.562	3.0
XOR3	22.43	17.68	79%	1.87	5.583	3.0

*The full adder CMOS implementation is the same for FA1 and FA2.

6 CONCLUSIONS

The design of MCML standard cell represents a complex task since the gate has an analog topology and MCML digital gate design presents several design parameters correlated with each other. Therefore, the design methodology requires imposing constraints to guarantee the gate functionalities. The proposed design methodology demonstrates its applicability and accuracy for designing MCML gates in three different process technologies, from mature nodes to deep submicron nodes.

The propagation delay extraction methodology used in the work focus in digital logic path and considers a chain of gates in which each stage has a fanout of four. Once that the output voltage swing of MCML gates represents the difference between the low and high logic values, the design of an MCML standard cell library requires the standardization of the output voltage swing. It is well kwon that the reduction of voltage swing implies in fewer charges required to charge a certain load amount. Furthermore, this reduction is beneficial to the speed performance of the gate. However, in order to guarantee a defined gates noise margin, a voltage swing decrease in MCML gates leads to wider PDN transistor. According to the propagation delay extraction method used, wider PDN transistors imply in greater output load to the gates. Hence, below a certain value the voltage swing reduction degrades the propagation delay of MCML gates.

The bias current represents the current capability of the gate to discharge the output node. Therefore, the use of reduced bias current results in slower gates. However, the increase of this current also requires wider PDN transistors to achieve the required noise margin. Hence, this improvement of propagation delay through the increase of bias current works well up to a certain value, and above this value it is no more advantageous due to the excess of capacitances added in the circuit.

The proposed methodology uses a standard sizing for all PDN transistors. Although this procedure is not the best solution for the propagation delay, this standardization helps in the layout implementations. In order to evaluate the lost in the speed performance of the gate, this work show the optimization done by commercial circuit optimization software for two technologies, XFab XC06 and IBM130. The Wicked optimization presents an improvement in the propagation delay performance of 20% on the XFab XC06 technology. The software solution sizes the upper transistors (closer to the output) wider than the lowers one. This procedure equalizes the current

capability of the stacked transistors, once that the upper devices have lower gate-source voltages. On the other side, the optimization of the gates designed in the IBM130 technology had an improvement of only 3% for the worst-case delay of the gate. Therefore, it demonstrates that the standardization of the PDN width is not prejudicial for advanced technologies. The scaling of technologies reduces the parasitic capacitances of the devices. Therefore, wider transistors have less impact in the speed degradation.

The simulations of the ring oscillators also demonstrate that small logic paths are desired in MCML applications. The power dissipation of MCML style comes from the constant bias current of each gate that composes the circuit. Hence, this dissipation has a linear dependence of gates numbers in the logical path. Moreover, MCML gates operating in high frequency can dissipates less power than CMOS gates mainly on the XOR, AND and OR gates. These CMOS gates are implemented with multi-stage logic computations, while in MCML style, a single stage can process these logic functions. The technology scaling does not influence significantly the number of stages that equalize the power dissipation. In another hand, the frequency achieved by the ring oscillators, at the power equalized condition, increase notably. In a general form, the MCML logic gates perform a better response to the power-frequency tradeoff with pipeline circuits.

The comparison between the MCML and static CMOS topologies in frequency divider applications take into account the MCML gates designed with the bias current that characterize the saturation behavior of speed performance. The CMOS flip-flops are constructed with the traditional master-slave topology. The CMOS sizing focus in PN ratio that achieve the highest frequency operation of a inverter ring oscillator. The results demonstrate that, in this design condition, the MCML topology can achieve frequencies that almost double that accomplish by CMOS gates. The complexity of flip-flops constructed with static CMOS topology makes the MCML attractive on these applications. The characteristic of constant switching of frequency dividers also benefits the power dissipation performed by the MCML gates, regardless the technology used.

The layout implementation demonstrates that the requirement of bias current mirror and pull-up standard structures in the MCML gates makes the MCML cells area disadvantageous compared to gates of a commercial CMOS digital standard cell library. The reliability design shows that the global process variations can degrade the MCML

cell gain. Therefore to overcome this situation the design requires wider PDN transistors sizing to compensate the robustness loss of the gate. When the local variations are analyzed, it is possible note that the control bias circuits do not present a compensation for this kind of variability. Therefore, the reliability of the circuit is degraded. The increase of PDN transistors size increases the propagation delay due to the addition of parasitic capacitances in the gate. The full adder implementations demonstrate that internal gate routing also degrades the cell speed performance. The studied case demonstrates that implement a full adder with simpler gates and more logic stages is not advantageous if compared with the single stage construction. The comparison between the frequency performance achieved by layout extracted simulations of the CMOS and MCML ring oscillators shows that MCML applications are advantageous for gates with lower inputs number. The power dissipation of the implemented MCML ring oscillators is higher than the CMOS one due to the long logic path, 29 stages, and low-frequency operation.

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APPENDIX A: PUBLICATIONS

- CANAL, B., NUNES, C. S., RIBAS, R. P. and FABRIS, E. E. *"MCML Gate Design for Standard Cell Library".* Proceedings of 28th Symposium on Integrated Circuits and Systems Design **(SBCCI'15).** Salvador, Brazil. September 2015.

APPENDIX B: SUMMARY IN PORTUGUESE

Metodologia de Projeto de Portas Lógicas MCML e a Comparação entre Portas Lógicas CMOS e MCML

B.1 INTRODUÇÃO

Este capítulo contextualiza a evolução dos componentes eletrônicos devido à miniaturização dos transistores, o que possibilita uma maior integração dos circuitos. Isso leva a um aumento da complexidade dos circuitos e dos desafios de projetar um circuito integrado que atenda às diversas funções de custo requeridas. São apresentadas resumidamente durante o capítulo as famílias lógicas CMOS, pseudo-NMOS, Lógica Dinâmica, DCVSL e MCML. As metodologias de projetos *full-custom*, *semi-custom* e *standard cell-based* são explicadas brevemente chamando atenção para a padronização dos circuitos necessária à medida que o fluxo de projeto se torna mais automatizado.

B.1.1 Motivação

O capítulo versa sobre a motivação do trabalho, o qual visa estudar uma família lógica, alternativa à CMOS estática, que possua características atrativas para ser aplicada em circuitos de alta frequência. Desta forma, a família lógica MCML demonstra ser uma alternativa a ser estudada. Dentre as características que a fazem atrativa para esta aplicação estão a baixa diferença de tensão entre seus níveis lógicos alto e baixo e seu funcionamento que provém do direcionamento da corrente de polarização, sendo assim não há um chaveamento total dos transistores que compõem a sua rede lógica, o que aumenta a velocidade do processamento lógico. Ainda chama-se a atenção para o fato da dissipação de potência de circuitos MCML ser independente da frequência de operação.

Nota-se que para ser largamente utilizada na síntese de circuitos digitais, uma família lógica deve se adaptar ao máximo ao fluxo de projeto baseado em células padrões. Esse fato faz com que seja necessário desenvolver uma metodologia de projeto de células lógicas MCML. O projeto de células MCML representa uma tarefa complexa devido aos diversos graus de liberdade na parametrização das células, e a necessidade da padronização de certos parâmetros para que seja possível a inserção das células no fluxo *standard cell*. Outro fato motivador é a análise do comportamento da família lógica, frente ao estilo lógico CMOS estático, de acordo com o avanço do nodo tecnológico utilizado.

B.1.2 Objetivo

Devido à necessidade de estudar famílias lógicas alternativas à topologia CMOS estática e a complexidade de gerar diversas células lógicas MCML, este trabalho tem por objetivo desenvolver uma metodologia de projeto de células lógicas MCML. A metodologia deve ser capaz de dimensionar diversas células MCML, analisando os efeitos da combinação entre valores da corrente de polarização e da variação de tensão entre os níveis lógicos alto e baixo. Para analisar o comportamento da topologia MCML em diferentes nodos tecnológicos a metodologia deve prover uma fácil migração de tecnologia e por fim o trabalho ainda tem o objetivo de fazer uma análise das células desenvolvidas pela metodologia contrapondo-as às células CMOS estáticas.

B.1.3 Organização da Dissertação

A dissertação está organiza da seguinte forma:

Capítulo 2: Fundamentos de Projeto MCML – Operação básica de células lógica MCML, e discussão sobre características elétricas das mesmas.

Capítulo 3: Metodologia de Projeto – Descreve a metodologia de projeto proposta e apresenta e discute os resultados obtidos.

Capítulo 4: Desempenho e Restrições de Células MCML e CMOS – Comparação do projeto de bibliotecas CMOS e MCML. Descrição dos efeitos da escalabilidade dos transistores em ambas as famílias lógicas.

Capítulo 5: Implementação em Silício – Apresenta os passos da implementação física para teste das células MCML.

Capítulo 6: Conclusões – Apresenta as conclusões e contribuições do trabalho desenvolvido.

B.2 FUNDAMENTOS DE PROJETO MCML

O capítulo dois apresenta a composição de uma célula lógica MCML bem como o seu princípio básico de operação. Mais detalhadamente, a célula é composta por três principais partes: espelho de corrente que gera a corrente de polarização; rede de *pull-*

down, responsável pela identificação da função lógica da célula; resistências de *pull-up* que convertem a corrente drenada em um valor de tensão nos nós de saídas da célula.

O funcionamento da célula é baseado no direcionamento da corrente de polarização a uma das resistências de *pull-up*. O braço da célula que está drenando a corrente apresentará o valor lógico baixo devido à queda de tensão presente no resistor de *pull-up*, como idealmente o outro ramo da célula não apresenta fluxo de corrente elétrica, a saída apresentará tensão igual a tensão de alimentação. Assim são definidos os valores de tensão das saídas diretas e complementar da célula.

O capítulo introduz os parâmetros de projeto das células MCML apresentando um Inversor/Buffer MCML. Esta é a célula MCML mais simples, a qual tem sua rede de *pull-down* composta somente por um par diferencial. Nas seções são apresentadas: as considerações a serem feitas para determinar a variação de tensão mínima das saídas da célula; o dimensionamento a ser feito para atingir a margem de ruído requerida e por fim as aproximações de atraso de propagação e dissipação de potência.

As análises feitas com a célula inversora são estendidas para o caso de células que desempenham funções lógicas mais complexas. Inicialmente é explicado como se define a rede de *pull-down* e em seguida como determinar os parâmetros de oscilação da tensão de saída, robustez e atraso de propagação. Ainda no mesmo capítulo é apresentada a topologia das células lógicas sequenciais.

Por fim o capítulo apresenta os princípios utilizados no dimensionamento das três partes principais da célula: espelho de corrente, rede de *pull-down* e rede de *pull-up.*

B.3 METODOLOGIA DE PROJETO

No capítulo três é apresentada a metodologia de projeto proposta. Esta metodologia busca projetar cada célula reduzindo seu consumo e atraso de propagação para uma dada margem de ruído. A metodologia é dividida em três etapas principais. Inicialmente há a caracterização da tecnologia na qual o projetista deve informar alguns dados da tecnologia, então através de simulações o método extrai os parâmetros necessários para o modelo utilizado. Tendo finalizado a caracterização da tecnologia o método passa a dimensionar a célula iniciando pelo espelho de corrente, depois há o dimensionamento dos transistores de *pull-up* seguido do dimensionamento da rede de *pull-down.* Todos esses dimensionamentos partem de um valor inicial encontrado

através dos equacionamentos apresentados no capítulo dois. Após cada dimensionamento inicial a metodologia segue uma rotina de simulações e redimensionamentos para que a célula atinja as especificações requeridas. Por fim a metodologia extrai o atraso de propagação da célula para um *fanout* igual a quatro.

A metodologia de projeto proposta foi aplicada a três diferentes nodos tecnológicos (XFAB XC06, IBM130 e PTM45) a fim de validar seu funcionamento. Os resultados desses dimensionamentos para células INV, (N)AND, (N)OR, X(N)OR de duas e três entradas assim como para *Flip-flops* estão apresentados no capítulo em questão através de gráficos 3D. Durante a apresentação desses gráficos, seus dados são analisados demonstrando a relação do dimensionamento e da resposta temporal das células com as características da corrente de polarização e da oscilação da tensão de saída da célula. Ao fim da análise dos resultados, o dimensionamento das tecnologias XFAB XC06 e IBM130 são confrontados com dimensionamentos obtidos por meio do software de otimização de circuitos integrados Wicked™.

B.4 DESEMPENHO E RESTRIÇÕES DE CÉLULAS MCML E CMOS

O capítulo quatro começa apresentando uma comparação entre a concepção de uma biblioteca de células digitais CMOS estática e a construção de uma biblioteca MCML. As análises da rede lógica, níveis de tensões de saída, potência dissipada e padronização de leiaute são apresentadas para ambas as topologias. Para verificar o desempenho da família lógica MCML, osciladores em anel e divisores de frequência foram desenvolvidos em nível de esquemático e então as análises da frequência de operação e dissipação de potência desses circuitos são apresentadas. Em resumo, a análise das simulações dos osciladores em anel mostra que circuitos que possuem menor profundidade lógica e alta frequência de operação apresentam melhor desempenho quando construídos com células MCML. A análise dos divisores de frequência, devido às características de constante chaveamento do circuito e a complexidade da implementação de *flip-flops* em circuitos CMOS estáticos, mostra que a topologia MCML é capaz de atingir frequências máximas de operação maiores do que a topologia CMOS dissipando menor potência.

B.5 IMPLEMENTAÇÃO EM SILÍCIO

Este capítulo aborda assuntos ligados ao processo de implementação de estruturas de teste das células MCML desenvolvidas na tecnologia XFAB XC06. Inicialmente são apresentadas as estruturas que foram desenvolvidas, sendo oito osciladores em anel desenvolvidos na topologia MCML, os quais são replicados na topologia CMOS estática, para fins de comparação de desempenho. O processo de implementação começa pela análise de confiabilidade das células projetadas, trazendo particularidades do funcionamento das células de acordo com variações de processo e descasamento dos dispositivos.

Na segunda etapa da implementação são apresentados detalhes do leiaute, demonstrando como foi definido o modelo padrão (*template*) das células MCML. Também segue neste capítulo detalhes sobre células físicas necessárias para a inserção das células lógicas na etapa de síntese física de circuitos digitais bem como a geração do arquivo *Library Exchange Format* (LEF) que é utilizado para esta síntese. Por fim os resultados obtidos nas simulações do leiaute extraído são apresentados.

B.6 CONCLUSÕES

O design de células lógicas MCML representa uma tarefa complexa, uma vez que estas células apresentam uma topologia utilizada em circuitos analógicos que possui diversos parâmetros de projetos correlacionados. O projeto destas células requer a definição de restrições para que a célula atinja suas funcionaliodades. A metodologia proposta demonstrou sua aplicabilidade no projeto de células de até três entradas para três diferentes tecnologias, desde nodos tecnológicos maduros até submicrométricos.

A metodologia utilizada neste trabalho para a extração do atraso de propagação foca na aplicação de circuitos digitais. Sendo assim, são consideradas cadeias de células lógicas em que cada estágio da cadeia apresenta um *fanout* igual a quatro. Como a variação da tensão de saída das células MCML representa a diferença de tensão entre os níveis lógicos alto e baixo, o projeto das células MCML requer que esta variação seja padronizada para todas as células desenvolvidas. Sabe-se que a diferença de tensão entre os níveis lógicos é proporcional a quantidade de carga necessária para alterar o nível lógico de uma dada capacitância. Logo, uma redução na oscilação de tensão de

saída corresponde em menos carga a ser drenada, o que levaria a uma redução no atraso de propagação. No entanto essa oscilação de tensão de saída está relacionada com a margem de ruído da célula, e uma redução dessa tensão requer um aumento no dimensionamento dos transistores da rede de *pull-down*. Logo, o aumento nos transistores da rede de *pull-down* implica em um aumento da carga de saída das células. Assim, abaixo de um dado valor, a redução da variação de tensão de saída das células MCML degrada o atraso de propagação das células.

A corrente de polarização representa a capacidade da célula de descarregar o nó de saída. Então, o uso de uma corrente de polarização baixa implica em células mais lentas. No entanto, o aumento da corrente de polarização também requer o aumento da largura dos transistores da rede de *pull-down* para atingir a margem de ruído especificada. Assim, a melhoria no atraso de propagação através do aumento da corrente de polarização funciona até certo valor de corrente, acima deste, o aumento na corrente não representa mais um ganho significativo devido ao excesso de capacitâncias adicionadas ao circuito.

A metodologia proposta utiliza um dimensionamento único para todos os transistores da rede de *pull-down*. Embora este procedimento não seja a melhor solução em termos de atraso de propagação, esta padronização auxilia na otimização do leiaute da célula lógica. Para avaliar a perda de desempenho de velocidade da célula, resultados obtidos através da metodologia proposta foram comparados com os de um software otimizador de circuitos integrados. Esta otimização via software apresentou uma melhora de 20% para a tecnologia XFAB XC06 e somente 3% no caso da tecnologia IBM130. De forma geral o dimensionamento dado como solução do software dimensiona os transistores superiores da rede de *pull-down* maiores do que os dos níveis mais baixos. Este procedimento equilibra a capacidade de corrente dos transistores empilhados, uma vez que os transistores superiores (mais próximos do nó de saída) possuem uma tensão fonte-porta menor do que os demais transistores. A diferença nos resultados demonstra que o avanço da tecnologia reduz as capacitâncias parasitas inseridas no circuito. Assim, o maior dimensionamento dos transistores utilizado pela metodologia proposta, frente à solução encontrada pelo software não impacta significativamente na degradação da velocidade da célula em tecnologias mais avançadas.

As simulações de osciladores em anel demonstraram que circuitos com profundida lógica menores são desejado para aplicações MCML. A dissipação de potencia do estilo lógico MCML provém unicamente da corrente de polarização utilizada em cada célula lógica. Assim, esta dissipação possui uma dependência linear com o número de células do circuito. Além do mais, circuito com células MCML dissipam menor potência do que circuitos CMOS estáticos em casos de alta frequência de operação, principalmente nos casos de células lógicas XOR, AND e OR. Estas células quando implementadas na topologia CMOS estática dependem de múltiplo estágios para computar sua função lógica. No entanto, quando se considera a topologia MCML, um único estágio é capaz de processar estas funções. A escalabilidade da tecnologia não demonstrou influenciar significativamente no número de estágios que iguala a dissipação de potência. De forma geral, células lógicas MCML, desenvolvem uma melhor relação consumo/frequência em circuitos que utilizem o conceito de *pipeline.*

A comparação entre as topologias MCML e CMOS estática em divisores de frequência levaram em conta células MCML projetadas com a corrente de polarização que caracteriza a saturação da velocidade de propagação. Os *flip-flops* CMOS estáticos foram construídos com base na topologia tradicional mestre-escravo e seu dimensionamento foi baseado em uma razão PN que atinge a máxima frequência de operação em um oscilador em anel formado por inversores. Os resultados demonstraram que, nestas condições de projeto, a topologia MCML pode atingir frequências de operação que aproximadamente dobram aquelas atingidas por células CMOS estáticas. A complexidade de *flip-flops* construídos com a topologia CMOS estática tornam atrativa a implementação destas aplicações com células MCML. A característica de constante chaveamento dos divisores de frequência também beneficia a dissipação de potência realizada por células MCML, independentemente da tecnologia utilizada.

A implementação do leiaute das células MCML demonstrou que a necessidade de estruturas padrão, para reduzir o descasamento dos espelhos de corrente e da rede de *pull-up*, tornam estes circuitos custosos em relação a área ocupada, quando comparados com o leiaute de células de uma biblioteca de células padrão comercial que utiliza a topologia CMOS estática. O projeto visando à confiabilidade dos circuitos demonstra que as células MCML requerem um maior dimensionamento dos transistores da rede de *pull-down*, para compensar a perda de ganho devido a possíveis variações globais de

processo. Apesar das estruturas de controle compensar variações globais nos espelhos de corrente e resistências de *pull-up*, as células MCML não apresentam proteção contra descasamentos. A comparação entre as frequências de operação atingidas nas simulações de leiaute extraído dos osciladores CMOS estáticos e MCML demonstraram que aplicações da topologia MCML são vantajosas para células com menor número de entradas. A dissipação de potencia dos osciladores em anel MCML é maior do que os mesmos osciladores implementados com células CMOS estáticas, fato explicado devido ao grande número de estágios, 29, e a baixa frequência de operação.