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Amplifier Topologies for Ultra Low Voltage Applications

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“If I have seen farther than others,
it is because I stood on the shoulders of giants.”
— Sir Isaac Newton

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ABSTRACT

Nomadic applications which cannot be recharged while at operation, such as biomedical sensors and Internet of Things applications, rely on energy harvesting from the environment. Typical supply voltages are usually higher than those achieved by energy harvesting methods and requires DC-DC conversion levels, which invariably results in energy loss proportionally to the step of voltage conversion. Consequently, designing at supply voltages closer to the nominal voltage of the energy source improves power efficiency. However, extremely low supply voltages bring design challenges, as circuit topologies for typical voltages employ techniques not suitable for extremely low supply voltages. In this work, single ended and fully differential amplifier topologies for voltage supplies in the range of few hundreds mV were proposed. The proposed approaches use the pseudo differential pairs with the transistor bulk terminals with forward biasing voltages for several purposes, including common mode rejection, output common mode voltage and DC current biasing. Additionally, a ring oscillator based in the same biasing techniques was proposed and designed for two main classes of applications: an intrinsically stable reference oscillator and a voltage controlled oscillator for analog-digital conversion with linearity improvements.

Keywords: Ultra Low Voltage. Voltage Amplifiers. Reference Oscillators. Voltage Controled Oscillators.

Topologias de amplificadores para aplicações com tensões de alimentação ultra baixas

RESUMO

Aplicações móveis que não podem ser recarregadas durante operação, como sensores biomédicos e aplicações da Internet das Coisas, dependem da extração de energia do próprio meio onde se encontram. Tensões de alimentação típicas são normalmente maiores que as disponiveis por métodos de extração de energia do meio e requerem uma conversão de nivel DC que invariavelmente resulta em perdas proporcionais ao fator de conversão. Consequentemente, aplicações projetadas para tensões de alimentação mais próximas da tensão nominal da fonte melhora a eficiência energética. Entretanto, topologias de circuitos elétricos para tensões típicas de alimentação sao impróprias para tensões extremamente baixas. Neste trabalho foram propostas topologias de amplificadores de saída unipolar e diferencial para tensões de alimentaçãoo na casa de centenas de milivolts. As técnicas propostas se baseiam no uso de pares pseudodiferenciais com terminais de corpo polarizados diretamente para vários propósitos, incluindo rejeição de modo comum e polarização de modo comum de saída e corrente DC. Adicionalmente, um oscilador baseado na mesmas técnicas de polarização foi proposto e projetado para duas classes de aplicações: um oscilador de referência intrinsicamente estável e um oscilador controlado por tensão para conversão analógica-digital com melhor linearidade.

Palavras-chave: Tensão de Alimentação Ultra Baixa, Amplificadores, Osciladores.

LIST OF ABBREVIATIONS AND ACRONYMS

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
CMOS	Complementar Metal-Oxide Semiconductor
CMRR	Commom Mode Rejection Ratio
CTAT	Complementary To Absolute Temperature
FSDM	Frequency-to-digital Sigma Delta Modulator
INL	Integral Non Linearity
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal Oxide Silicon Field Effect Transistor
NMOS	n-channel MOSFET
OTA	Operational Transconductance Amplifier
PMOS	p-channel MOSFET
PSRR	Power Supply Rejection Ratio
PTAT	Proportional To Absolute Temperature
PVT	Process, Voltage and Temperature
ULV	Ultra Low Voltage
VCO	Voltage Controlled Oscillator

LIST OF SYMBOLS

$A_{V_{cm}}$	Common mode voltage gain
$A_{V_{diff}}$	Differential voltage gain
g_{DS}	Drain-source conductance
g_m	Transistor transconductance
g_{mb}	Transistor bulk transconductance
g_{mg}	Transistor gate transconductance
G_o	Output transconductance
i_f	Transistor foward inversion level
I_Q	Push-pull pair quiescent current
i_r	Transistor reverse inversion level
I_{REF}	Reference current
I_S	Transistor intrinsic current
L	Transistor channel length
n	Slope factor
t_d	Inverter delay
V_A	Transistor Early voltage
V_B	Transistor bulk terminal voltage
V_bn	NMOS transistor bulk terminal voltage
V_bp	PMOS transistor bulk terminal voltage
V_{cm}	Common mode input voltage
V_D	Transistor drain terminal voltage
V_{DD}	Supply voltage
V_G	Transistor gate terminal voltage
V_{in}	Input voltage

V_{out}	Output voltage
V_P	Transistor pinch-off voltage
V_{REF}	Reference voltage
V_Q	Push-pull pair quiescent voltage
V_S	Transistor source terminal voltage
V_T	Transistor threshold voltage
W	Transistor channel width
γ	Transistor body effect factor
ϕ_t	Thermal voltage
μ	Transistor charge mobility

LIST OF FIGURES

Figure 1.1 Supply voltage and threshold scaling trend 15
Figure 1.2 18

Figure 2.1 Bulk input differential amplifier stage 20
Figure 2.2 Level shift biasing 21
Figure 2.3 Output common mode biasing 21
Figure 2.4 Biased error amplifier 22
Figure 2.5 Gate input differential amplifier stage 22
Figure 2.6 Cross coupled transistor gain enhancement biasing 23
Figure 2.7 Push-Pull Based OTAs with Common Mode Rejection 24
Figure 2.8 Push-pull quiescent voltage definition 24
Figure 2.9 Biasing Circuit 24

Figure 3.1 Push-pull CMOS pair configurations 27
Figure 3.2 Biased error amplifier 29
Figure 3.3 Proposed push-pull pair biasing circuits 30
Figure 3.4 Bulk-biased Nauta's transconductor 31
Figure 3.5 Nauta's transconductor small-signal circuit 32
Figure 3.6 Single ended self biased pseudo differential pair OTAs 33
Figure 3.7 Self biased push-pull based fully differential OTA 34
Figure 3.8 Proposed externally biased push-pull based single ended OTA 35
Figure 3.9 Externally biased push-pull based fully differential OTA 36

Figure 4.1 Single Ended OTAs - Testbenchs 39
Figure 4.2 Single Ended OTA - Mirrored - Simulation Results 41
Figure 4.3 Single Ended OTA - Self biased - Simulation Results 42
Figure 4.4 Single Ended OTA - Externally biased - Simulation Results 43
Figure 4.5 Fully differential OTAs - Testbenchs 45
Figure 4.6 Fully Differential Ended OTA - Self biased Nauta - Simulation Results 46
Figure 4.7 Fully Differential Ended OTA - Externally biased Nauta - Simulation Results 47
Figure 4.8 Fully Differential Ended OTA - Unbiased - Simulation Results 48
Figure 4.9 Fully Differential Ended OTA - Biased - Simulation Results 49
Figure 4.10 Fully Differential Ended 2 Stage Unbiased OTA - Simulation Results 52

Figure 5.1 Self biased push-pull pair based oscillator 54
Figure 5.2 Bulk biased push-pull pair based oscillator 55
Figure 5.3 Proposed biased oscillators 55
Figure 5.4 Proposed biasing circuit 56
Figure 5.5 PTAT self biased current reference 56
Figure 5.6 CTAT self biased current reference 56
Figure 5.7 VCO biasing scheme 59

Figure 6.1 Supply voltage frequency stability 61
Figure 6.2 Current reference supply voltage stability 61
Figure 6.3 Current reference temperature frequency stability 62
Figure 6.4 Temperature frequency stability 62
Figure 6.5 Voltage-to-frequency response 63
Figure 6.6 Integral Non Linearity Error 64

Figure 6.7 Loop AC response 64
Figure 6.8 DC response 65
Figure 6.9 Frequency temperature stability 65
Figure 6.10 Central frequency - Monte carlo simulation 66
Figure 6.11 Frequency-to-Digital Sigma Delta Modulator 66
Figure 6.12 FSDM output spectrum 67

LIST OF TABLES

Table 4.1 Single Ended OTAs - Simulation Results Summary 40
Table 4.2 Single Ended OTAs - Device Geometry 41
Table 4.3 Fully Differential OTAs - Device Geometry 44
Table 4.4 Fully Differential OTAs - Simulation Results Summary 46
Table 4.5 OTA Performance Comparison 51

Table 6.1 Transistor dimensions 60
Table 6.2 Design Specifications 63
Table 6.3 VCO - Summary of simulated performance 67

CONTENTS

1 INTRODUCTION **14**
1.1 Motivation **14**
1.2 The ideal and the non-ideal amplifier **16**
1.3 Limitations introduced by ultra low voltage supplies **17**
1.4 Organization **19**
2 ULV AMPLIFIER TOPOLOGIES REVIEW **20**
2.1 CHATTERJEE 2005 ..... **20**
2.2 VIERU 2011 ..... **23**
2.3 Topology Analysis **25**
3 PSEUDO DIFFERENTIAL AMPLIFIER TOPOLOGIES AND BIASING FOR ULV **26**
3.1 Push-Pull Pair Configurations and Analysis **26**
3.2 Push-Pull Pair Biasing **29**
3.3 Biased Nauta's Transconductor **31**
3.4 Operational Transconductance Amplifiers Based in Pseudo Differential Pairs **33**
3.4.1 Proposed self biased amplifiers 33
3.4.2 Proposed externally biased amplifiers 35
3.5 Section Summary **36**
4 SIMULATION RESULTS - AMPLIFIERS **38**
4.1 Amplifiers **38**
4.1.1 Single Ended 38
4.1.2 Fully Differential 44
4.2 Two stage amplifier **50**
5 APPLICATIONS FOR THE PROPOSED BIASING STRATEGY **53**
5.1 Ring Oscillator Analysis **53**
5.2 Current biasing scheme for a CMOS Based Reference Oscillator **54**
5.3 Biasing scheme for CMOS Ring Voltage Controlled Oscillator **57**
6 SIMULATION RESULTS - OSCILLATORS **60**
6.0.1 Reference Oscillator 60
6.0.2 VCO 63
7 CONCLUSION **68**
REFERENCES **70**
LIST OF PUBLICATIONS **72**
APPENDIX A — SUMMARY IN PORTUGUESE **73**
A.1 Introdução **73**
A.2 Topologias de Amplificadores Pseudo Diferenciais e Polarização para ULV **74**
A.3 Aplicações para a Estratégia de Polarização Proposta **75**
A.4 Conclusão **76**

1 INTRODUCTION

This chapter will contextualize the use of amplifiers in electronic circuits and its tradeoff for low power and low voltage applications, followed by a brief explanation of both ideal non-ideal amplifier operation and basic electric circuit topologies.

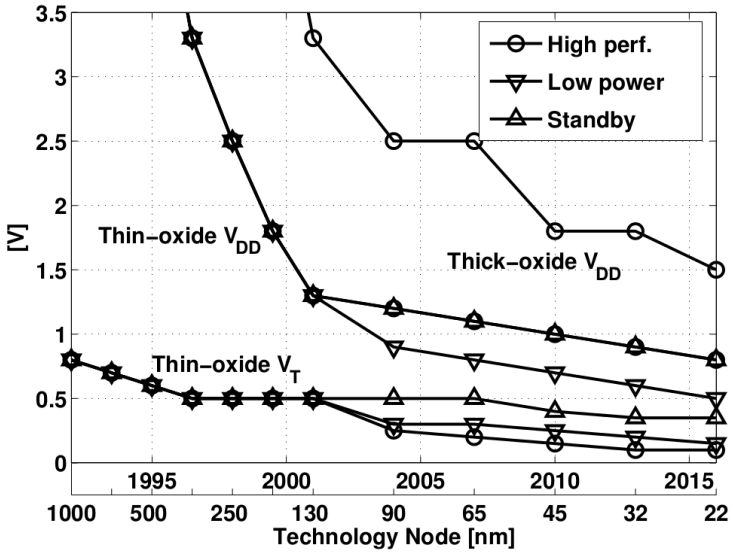
Motivation

With the advent and popularization of the transistor and integrated circuits, a new era emerged and since then electronics followed a trend of miniaturization and mass production which brought the computing power once exclusive to big business to the pocket of the ordinary citizen. The first mobile electronics were only portable versions of standard electronic topologies and applications. Well known examples were portable radios and digital watches. With integrated circuits technology further development, the transistor density grew exponentially and enabled the conception of increasingly smaller and more complex electronic applications. The most recent landmark of this trend is the popularization of wireless communications, which stated with basic voice calls functionalities and progressively added extra features as audio and video reproduction and recording and internet connectivity.

A shortcoming to the fast evolution of electronic devices in complexity and miniaturization was the slow evolution of energy storage technologies, a crucial point of mobile electronics, and it is currently one of the main concerns of its development. To solve the lack of available stored energy demanded by complex applications and the increasing desire for more autonomy by consumers, it is utterly necessary to design more efficient electronic circuits aiming less power consumption without performance drop. A design approach to this problem is to decrease the supply voltage of those electronics circuits, which reduces the power density resulted from the increasing transistor density in integrated circuits. As semiconductor technology matures and transistor length shrinks, the core supply voltage decreases, as predicted in (ITRS, 2004), as depicted in figure 1.1.

Some applications, as biomedical and remote sensors, despite being relevant, are not as widespread as wireless communications, one of the main targets of a major part of the electronics industry. Those applications must be adapted to manufacture processes not targeted to their specifications, since special processes are expensive and, in most cases, do not justify the demand, therefore are not feasible in a commercial perspective. One

Figure 1.1: Supply voltage and threshold scaling trend



Source: (KINGET, 2007)

of those adaptations to save power consumption while using common processes is the utilization of voltage supplies much below the nominal voltage. Throughout this thesis, state of art works will be referenced which operate with voltage supplies of a few hundreds milivolts, usually under 500 mV.

Mobile power supply can be provided by several sources as portable chemical batteries or the environment. Batteries have limited energy storage and must be replaced or recharged once fully depleted, while energy harvesting converts energy from the environment into electrical energy as long its available, which could extend device autonomy. Energy harvesting usually provide a low supply voltage which must be regulated to properly power electronic circuits. Although nominal supply voltages can be achieved by DC-DC voltage conversion from lower voltage power supplies, this conversion loses power efficiency proportionally to voltage upscaling, so, electric circuits must remain functional with a supply voltage as low as possible to save power. Additionally, voltage upscaling is accomplished by electric circuits and switches which must operate with the original low voltages in the earlier stages, which is a challenge itself.

Integrated circuits can be very complex systems, as digital processors with billions of transistors, or be simple and yet have tough operation conditions, as military grade ICs, and the usage of supply voltages bellow nominal has degrading effects in many of its characteristics. Systems on a chip have several modules, both in the analog and digital domain, and every one of them have their own challenges regarding to ULV operation. The scope of this thesis focuses on the design of amplifiers, a essential building block of

analog signal processing and data converters.

The ideal and the non-ideal amplifier

Amplifiers are composed by passive components as resistors and capacitors, and active components as transconductors and switches built with transistors. Real components deviate from the ideal models and, consequently, introduce non-idealities to the amplifier.

The main non-idealities of amplifiers are noise and distortion (RAZAVI, 2006). Noise is an unwanted signal shown at the amplifier output and is produced both externally by the environment or internally by its own components. Interference, also an unwanted signal, can be attenuated with the use of differential topologies and by the rejection of common mode and power supply signals. Noise is unavoidable, but can be reduced by proper device sizing for flicker noise in transistors, and proper biasing currents for thermal noise. Both interference and noise levels are defined by each application specification and are highly dependent of environment variables.

Distortion is the unwanted alteration of the signal and is mainly caused by the non-linearity of the amplifier components and by the limitation of signal excursion by supply voltages. Another source of amplifier nonlinearity is output hysteresis resulted from positive feedback, a common technique found in ULV amplifiers to improve voltage gain.

Ideal amplifiers should have a constant output gain and phase for all frequencies. The non-ideal amplifier has a limited operation bandwidth due to inherent parasitic loads, which results in attenuation of higher frequencies and unwanted filtering. Additionally, amplifiers usually have multiple stages to improve gain, which results in multiple phase inversions. Amplifiers used within closed loop circuits can introduce instability and oscillation.

After fabrication, many non-ideal amplifier key characteristics suffer from process, supply voltage and temperature variability, such as gain, bandwidth and power dissipation. The design must take this variability into account by defining tolerance margins or employing calibration in order to ensure proper operation of the higher level blocks.

Limitations introduced by ultra low voltage supplies

The design of amplifiers for typical supply voltages usually aims to use transistors operating in strong inversion (sometimes moderate and weak inversion for low power designs) and saturation region, since they offer greater gain, higher transconductances and less variability. Ultra low voltage supply strongly limit the use of high inversion levels for transistors, since their magnitude are very close to the threshold voltage of the transistors, consequently, transistors are actually operating at moderate or weak inversion.

The transistor inversion level i is mainly a function of the gate-bulk terminal voltage V_G and transistor threshold voltage V_T, as depicted in the equation 1.1 from the UICM model developed in (SCHNEIDER; GALUP-MONTORO, 2010), which will be the model used in this work. The transistor transconductance increases with the inversion level, accordingly to the equation 1.2. The transconductance in level of weak inversion is considerably lower than in strong inversion. As deducted from equation 1.2b, the gate transconductance is both function of both direct and reverse inversion levels i_f and i_r. When the transistors operates in the triode region, the reverse inversion level i_r is significant and it reduces the total gate transconductance.

$$V_P - V_{S(D)} = \frac{V_G - V_T}{n} - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + ln(\sqrt{1 + i_{f(r)}} - 1)\right] \quad (1.1)$$

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_{f(r)}} - 1\right) \quad (1.2a)$$

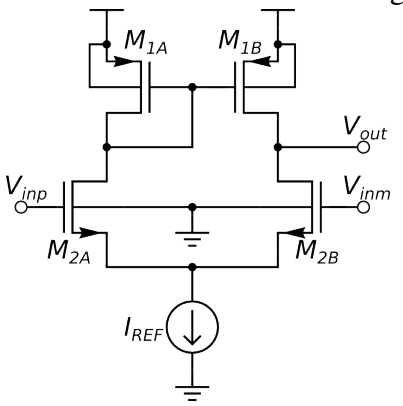
$$g_{mg} = \frac{g_{ms} - g_{md}}{n} \quad (1.2b)$$

In addition to the potentially lower transistor inversion level, ultra low voltage supply limit the output signal excursion. Transistors are expected to operate in the saturation region to achieve better linearity and higher voltage gain. In order to assure that the transistors operate in the saturation region, the voltage V_{DS} between drain and source terminals must be greater than the pinch off voltage V_P (also known as overdrive voltage) while operating in strong inversion and greater than $4\phi_t$ while operating in weak inversion. The use of stacked transistors decreases the output signal excursion for transistors designed to operate in the saturation region or it results in triode operation and, consequently, in lower gain and transconductance. Amplifier designs with ultra low voltage

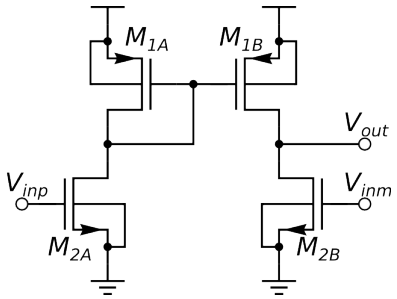
supplies seek to stack less transistors as possible to assure saturation operation.

One of the oportunities brought by the use of ultra low voltage is the safe use of forward body biasing without level shifting (CHATTERJEE et al., 2010). The pn junctions formed by the substrate and the source and drain diffusions can be biased in the forward region without conducting a considerable current relative to the drain current and it additionally control the drain current by altering the transistor threshold voltage, consequently, the transistor bulk terminal can be used to bias the transistor or as signal input.

Figure 1.2



(a) Mirrored load differential pair



(b) Mirrored load pseudo differential pair

A differential pair, as depicted in figure 1.2a is commonly composed of a transconductor pair, a current source and an active load, which results in at least three stacked transistors. A pseudo differential pair, as depicted in figure 1.2b, lacks a current source, as consequence, the biasing current is defined by the input voltage and common mode rejection is severely reduced. With ULV supplies, forward body biasing can be used to replace the current source to bias the pseudo differential pair improving its common mode and power supply rejection and process variability effects. Also, forward body biasing can be used for other functions in a pseudo differential pair, as input signal (FERREIRA; PIMENTA; MORENO, 2007), output common mode feedback (VIERU; GHINEA, 2011) and calibration (XU; YTTERDAL, 2010). The goal of this thesis is to study state-of-art amplifier topologies which employ forward body biasing, propose new ones and compare their perfomances.

Organization

This thesis is organized in the following manner. Chapter 2 will present state-of-the-art amplifier designs with ultra low voltage supplies. Chapter 3 will present some new forward body biasing circuits and pseudo differential topologies for ULV. Chapter 4 will present novel oscillator topologies based in previously proposed biasing schemes. Finally, Chapter 5 will present post-layout simulation results from designed prototypes.

2 ULV AMPLIFIER TOPOLOGIES REVIEW

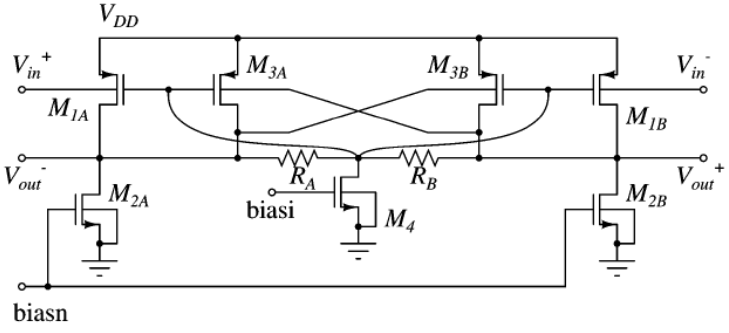
This chapter will present the state-of-the-art amplifier designs with ultra low voltage supply. They are mainly based on forward body biasing and have a maximum of two stacked transistors.

CHATTERJEE 2005

The amplifiers proposed by Chatterjee (CHATTERJEE; TSIVIDIS; KINGET, 2005), were implemented in 180 nm standard CMOS process and aims to work with a 500 mV power supply. Those amplifier topologies were based in three techniques commonly used when designing for ultra low voltage supplies: the use of the bulk terminal for input signal, a pseudo differential topology with two stacked transistors and the use of positive feedback to increase gain.

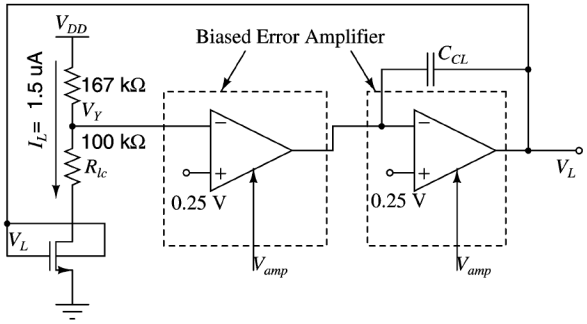
The body input amplifier is composed by amplifier stages shown in the figure 2.1. The PMOS transistors M_{1A} and M_{1B} are the transconductor elements of the input signal and, together with the NMOS transistors M_{2A} and M_{2B}, form the pseudodifferential pair. The forward biasing of the bulk terminal by a negative voltage V_{SB} decreases the transistor threshold voltage V_T. Decreasing V_T results in an increase of the inversion level. Forward biasing is only possible since V_{SB} is low enough that the current flow through the bulk terminal is negligible. The disadvantage of using the bulk terminal as input is a smaller transconductance g_{mb} by a factor of $(n-1)$ compared to gate transconductance g_{mg}, which means a smaller voltage gain, as result of body effect (SCHNEIDER; GALUP-MONTORO, 2010).

Figure 2.1: Bulk input differential amplifier stage



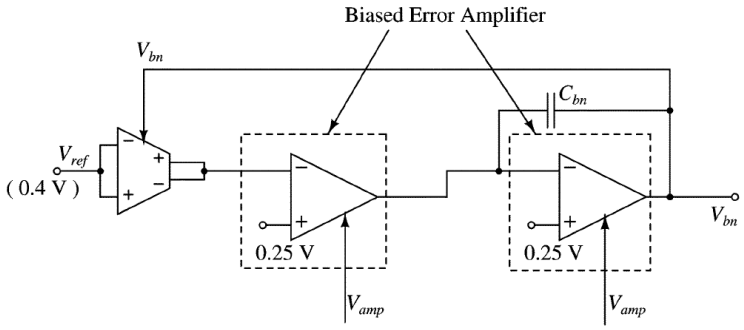
Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

Figure 2.2: Level shift biasing



Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

Figure 2.3: Output common mode biasing



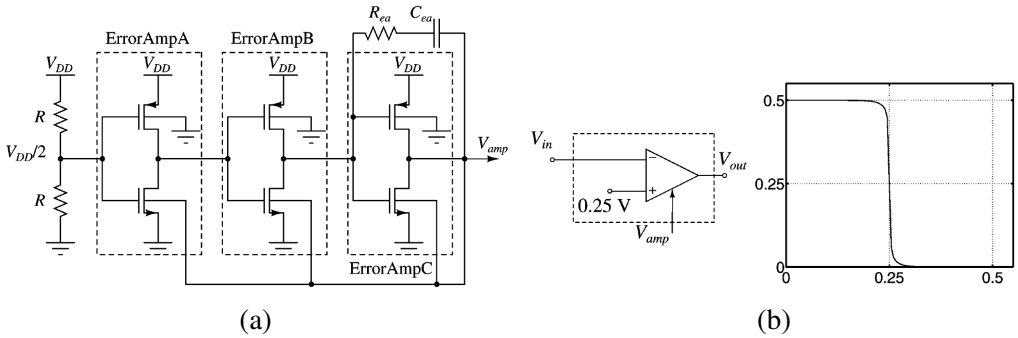
Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

The pseudo differential pair implemented with active load has only two stacked transistors for each branch, while the common differential pair needs a third transistor to act as a current source for the pair. The pseudo differential pair has a greater output range than the differential pair for the same supply voltage, however it lacks common mode rejection. The solution found for the proposed circuit is a feedback loop of the output common mode, detected by the resistors R_A and R_B, fed into the gate terminal of the transistors M_{1A}, M_{1B}, M_{3A} and M_{3B}.

In addition to the common mode rejection circuit, the transistor M_4 define the DC gate terminal voltage, which is itself biased by a voltage V_L, defined by the circuit shown in the figure 2.2. The common mode output voltage is defined by biasing the NMOS transistors with a voltage V_{bn}, defined by the circuit shown in figure 2.3. Both circuits are implementations of feedback loops employing push-pull based comparators, shown in figure 2.4. The comparator threshold voltage is set to a reference voltage by the use of forward body biasing and a feedback loop, which defines bulk terminal voltages for replicas of the push-pull pair.

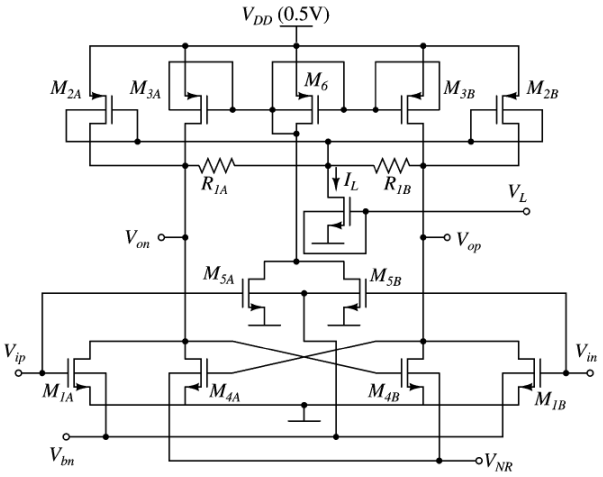
Ultra low voltage supplies limit the use of transistors in cascode configurations to increase the voltage gain, since it requires four stacked transistors. In order to increase

Figure 2.4: Biased error amplifier



Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

Figure 2.5: Gate input differential amplifier stage



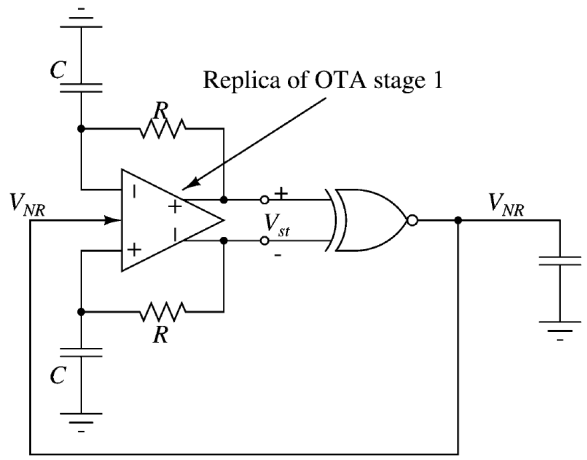
Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

gain without stacking extra transistors, the transistors M_{3A} and M_{3B} are inserted in parallel to the output terminals as a cross-coupled pair, implementing a negative resistance for differential signals. For further gain increase, two amplifiers stages were cascaded.

The same work proposes another similar amplifier, depicted in figure 2.5, however with gate terminals used for input signals, a feed-forward common mode cancellation and an additional gain enhancement scheme. NMOS transistors M_{1A} and M_{1B} are the transconductor elements of the input signals. NMOS transistors M_{5A} and M_{5B} sense the common mode input signal, producing a output current which is mirrored to the outputs by the PMOS transistors M_{3A} and M_{3B}, which implements the common mode cancellation path.

The cross-coupled pair M_{4A} and M_{4B} implements the negative resistance, but they are additionally biased by a gain enhancement circuit, shown in figure 2.6. The use of negative resistances can add hysteresis to the amplifier transfer function, which results in distortion. The circuit bias the cross-coupled pair to a threshold condition when the

Figure 2.6: Cross coupled transistor gain enhancement biasing



Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

negative resistance cancels out the output conductance and the circuit just start to show hysteresis, so the circuit provides optimal gain.

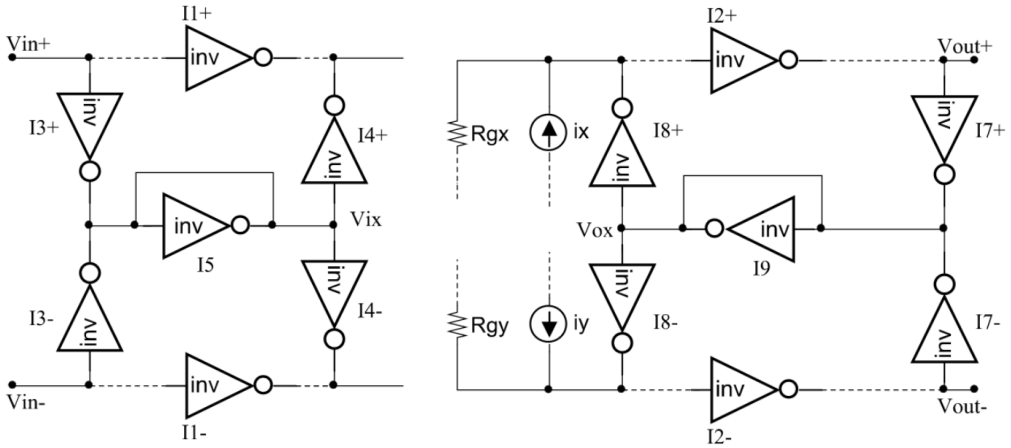
VIERU 2011

Push-pull pairs have greater transconductance and voltage gain than common source amplifiers with active load of similar size in the same process. Pseudo differential pairs based in push-pull pairs are highly efficient, however they require some kind of circuit to reject common mode signals and define a common mode output voltage.

Vieru (VIERU; GHINEA, 2011) proposed two pseudo differential amplifier topologies entirely based in push-pull pairs which employs feedforward and feedback paths to reject common mode signals, as shown in figures 2.7a and 2.7b.

The amplifier common mode output voltage is the push-pull pair quiescent voltage V_Q, which is the push-pull input voltage that outputs itself ($V_{in} = V_{out}$), as depicted in figure 2.8. The push-pull pair quiescent voltage is function of process parameters and, consequently, is intolerant to process, voltage and temperature variations. The topology uses adaptive body biasing, as the previous biasing circuit (CHATTERJEE; TSIVIDIS; KINGET, 2005), but uses a variation with a single-ended differential amplifier, as shown in figure 2.9

Figure 2.7: Push-Pull Based OTAs with Common Mode Rejection



(a) Feedforward (b) Feedback

Source: (VIERU; GHINEA, 2011)

Figure 2.8: Push-pull quiescent voltage definition

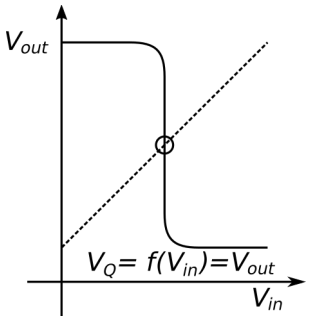
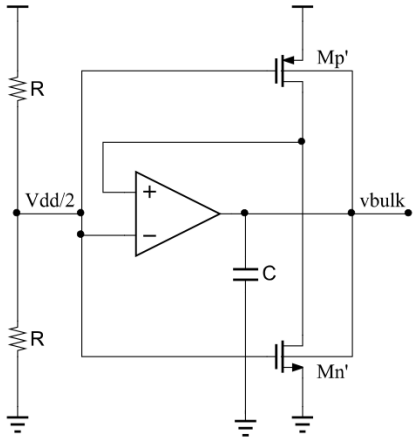


Figure 2.9: Biasing Circuit



Source: (VIERU; GHINEA, 2011)

Topology Analysis

The topologies proposed in (CHATTERJEE; TSIVIDIS; KINGET, 2005) differ from each other by using the gate or the bulk terminals for input signals. Bulk driven amplifiers show smaller transconductance per current consumption than gate driven ones and are less efficient, however, the bulk driven topology is simpler and the gate terminals are used for biasing and for common mode rejection, which is improved in comparison with the gate driven amplifier. Both topologies employ cross-coupled pairs for gain enhancement, which can produce hysteresis and distortion. Both topologies use a very complex biasing scheme which reduces efficiency, even if the same biasing circuit is used to bias several replicas of the same amplifier.

The topologies proposed in (VIERU; GHINEA, 2011) are based in the push-pull pair, which increases the transconductance and gain of the pseudo differential pair in comparison with common source amplifiers with active load with same current consumption. However, the common mode rejection circuit decreases the differential voltage gain, since it reduces the output or input resistance of the pseudo differential pair.

All topologies presented in this review rely in adaptive biasing schemes for the push-pull pair. Those bias circuits are inherently unstable, therefore they require some sort of stability compensation.

This work will present alternative amplifier stages for ULV based in the push-pull pair and biasing circuits, aiming to reduce the complexity of the design and improve efficiency.

3 PSEUDO DIFFERENTIAL AMPLIFIER TOPOLOGIES AND BIASING FOR ULV

The push-pull CMOS pair is often used in ultra low voltage as a building block for pseudo-differential pairs because it enables output voltage ranges similar to the common-source amplifier with active load with same dimensions and it achieves greater transconductance and gain. Biasing the gate terminal of the active load enables common-mode input rejection and common output voltage biasing.

Push-Pull Pair Configurations and Analysis

The push-pull CMOS pair, depicted in the figure 3.1a, consists in a PMOS staked over a NMOS and the input signal is connect to both gate terminals. The push-pull quiescent output voltage V_Q, which is the input voltage that results in an equal output voltage with quiescent current I_Q. Considering operation in weak inversion, they are defined by the equations 3.1 and 3.2, formulated in (SCHNEIDER; GALUP-MONTORO, 2010).

$$V_Q \approx \frac{V_{DD} + V_{T_P} + V_{T_N}}{2} - \frac{n\phi_t}{2} ln\left(\frac{I_{S_P}}{I_{S_N}}\right) \tag{3.1a}$$

$$I_{S_{P(N)}} = \mu_{P(N)} C'_{ox} n_{P(N)} \frac{{\phi_t}^2}{2} \frac{W}{L} \tag{3.1b}$$

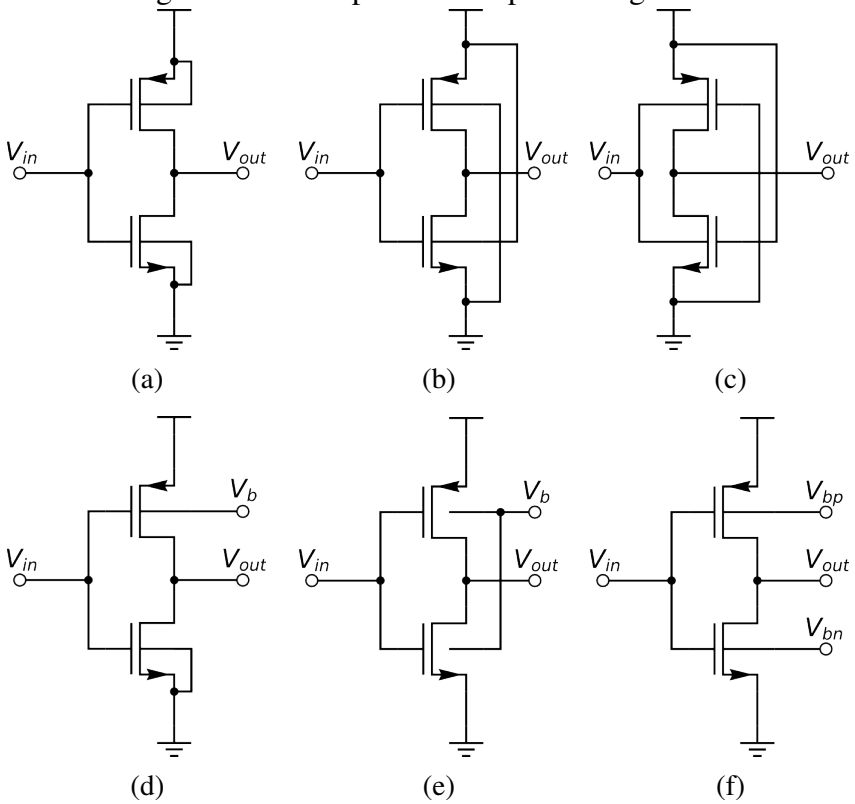
$$I_Q \approx kI_0 \tag{3.2a}$$

$$k = \left(\frac{V_{DD} + V_{T_P} - V_{T_N}}{\phi_t}\right)^2 \tag{3.2b}$$

$$I_0 = \left(\frac{1}{n_P/\sqrt{I_{S_P}} + n_N/\sqrt{I_{S_N}}}\right)^2 \tag{3.2c}$$

Still considering operation in weak inversion and $n = n_P \approx n_N$, the small-signal voltage gain A_V of the push-pull pair, defined in the equation 3.3, is independent of I_Q, and is mostly function of the Early voltage of the transistors. Yet, its gain bandwidth

Figure 3.1: Push-pull CMOS pair configurations



product is dependent of its input transconductance G_m, which is dependent of I_Q.

$$G_m = g_{m_P} + g_{m_N} = I_Q \left(\frac{1}{n_P \phi_t} + \frac{1}{n_N \phi_t} \right) \approx \frac{2I_Q}{n\phi_t} \tag{3.3a}$$

$$G_o = g_{DS_P} + g_{DS_N} = I_Q \left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}} \right) \tag{3.3b}$$

$$A_V = \frac{G_m}{G_o} \approx \frac{2}{n\phi_t \left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}} \right)} \tag{3.3c}$$

With ultra low voltages supplies, it is safe to use positive V_{BS} voltages to decrease the transistors $|V_T|$ as consequence of body effect, as shown in the equation 3.4. A decrease in $|V_T|$ increases I_Q, resulting in greater G_m. Without a bias circuit, the easiest way to decrease $|V_T|$ is to swap the transistor bulk terminals(NARENDRA et al., 2004), as depicted in figure 3.1b.

$$V_T = V_{T0} + \Delta V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \tag{3.4}$$

The push-pull pair with the bulk terminals as signal input, depicted in figure 3.1c,

has an increased I_Q due to body effect, however, accordingly to equation 3.5, the bulk-drain transconductance g_{mb} is a fraction of g_{mg}, since n is tipically within the range of 1.2 to 1.4 (SCHNEIDER; GALUP-MONTORO, 2010). The lower G_m turns this configuration impractical, due to a reduced lower gain compared to the common push-pull pair.

$$g_{mb} = (n-1)g_{mg} \tag{3.5}$$

The push-pull threshold voltage V_Q operating in weak inversion are functions of process parameters V_T and I_S and is consequently highly dependent of process variability and requires some kind of compensation. The transistor body effect can be used by to control V_Q by biasing the bulk terminal with a voltage V_b, as shown in equations 3.6. In standard CMOS processes, NMOS transistors are not build in isolated wells and shares the substrate with the entire die, so only the PMOS transistor can be biased, as shown in figure 3.1d. In processes featuring triple wells, V_b can be connected to both bulk terminals, resulting in a greater range of calibration as result of both V_T being controlled, as shown in figure 3.1e.

$$V_Q = V_{Q0} + \Delta V_Q \tag{3.6a}$$

$$V_{Q0} = \frac{V_{DD} + V_{T0_P} + V_{T0_N}}{2} - \frac{n\phi_t}{2} ln\left(\frac{I_{SP}}{I_{SN}}\right) \tag{3.6b}$$

$$\Delta V_Q = \frac{\Delta V_{T_P} + \Delta V_{T_N}}{2} \tag{3.6c}$$

$$\Delta V_{T_P}(V_b) = \gamma_P \left(\sqrt{2\phi_F + (V_{DD} - V_b)} - \sqrt{2\phi_F}\right) \tag{3.6d}$$

$$\Delta V_{T_N}(V_b) = \gamma_N \left(\sqrt{2\phi_F + V_b} - \sqrt{2\phi_F}\right) \tag{3.6e}$$

Finally, the push-pull pair can be used as transconductor and, in most transconductor applications, it's desired to tune its transconductance. Tuning can be achieved by biasing independently each bulk terminal, as shown in the figure 3.1f, where the voltage V_{bp} controls V_Q and the other voltage, V_{bn}, defines I_Q and consequently G_m. If $\Delta V_{T_P} = -\Delta V_{T_N}$, then there is no change in V_Q and there is a change in I_Q, as noted

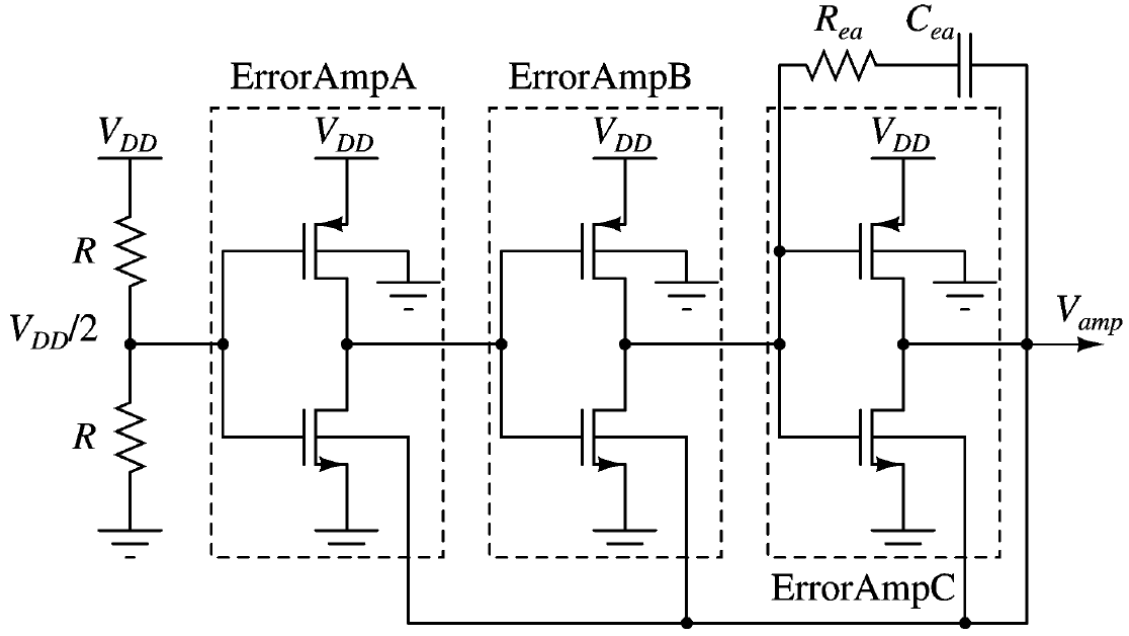
in equations 3.6c and 3.7, which derives from equation 3.2,.

$$k = \left(\frac{V_{DD} + V_{T0_P} + \Delta V_{T_P} - V_{T0_N} - \Delta V_{T_N}}{\phi_t} \right)^2 \tag{3.7}$$

Push-Pull Pair Biasing

As previously mentioned, transistor body effect can be used to define the quiescent output voltage of the push-pull pair. In order to make V_Q independent of process variability, V_Q should be defined by a reference voltage V_{REF} adequate for output signal excursion. In (NARENDRA et al., 2004) (KAENEL et al., 1994) (KOBAYASHI; SAKURAI, 1994) (KAO; MIYAZAKI; CHANDRAKASAN, 2002), adaptive body bias techniques have been used to optimize the delay through critical paths in digital circuits. A bias circuit has been proposed in (CHATTERJEE; TSIVIDIS; KINGET, 2005) which implements a feedback control system that compares V_Q with a reference voltage and corrects the quiescent output voltage of the push-pull pair through biasing the bulk of the NMOS transistor with a biasing voltage. This circuit. shown in figure 3.2, looks like a ring oscillator and has a very high loop gain, so, to keep this circuit stable, the feedback loop is established through a compensation capacitor with a zero-canceling series resistor.

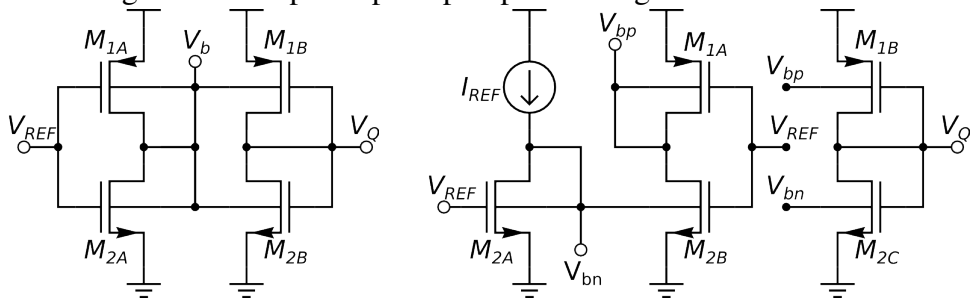
Figure 3.2: Biased error amplifier



Source: (CHATTERJEE; TSIVIDIS; KINGET, 2005)

To avoid extra area and power usage, the bias circuit proposed in (CHATTERJEE;

Figure 3.3: Proposed push-pull pair biasing circuits



TSIVIDIS; KINGET, 2005), shown in figure 2.4a, can be reduced to a single push-pull pair, as shown in figure 3.3a. The loop gain is reduced, however the circuit stability is guaranteed, since there is only one phase inversion. For process variability effects correction, the small loop gain still reduces V_Q variability to acceptable levels, since it is not the accuracy, but the range of voltage deviation ΔV_Q that can be corrected. V_b values range from $4\phi_t$ to $V_{DD} - 4\phi_t$, and any ΔV_Q deviation would require $\Delta V_b/(n-1)$, as deduced from equation 3.8 and previous push-pull pair definitions of G_m and G_o. The same circuit can be applied for standard CMOS processes without isolated NMOS transistors by only biasing the PMOS transistors N-well, at cost of reduced correction range.

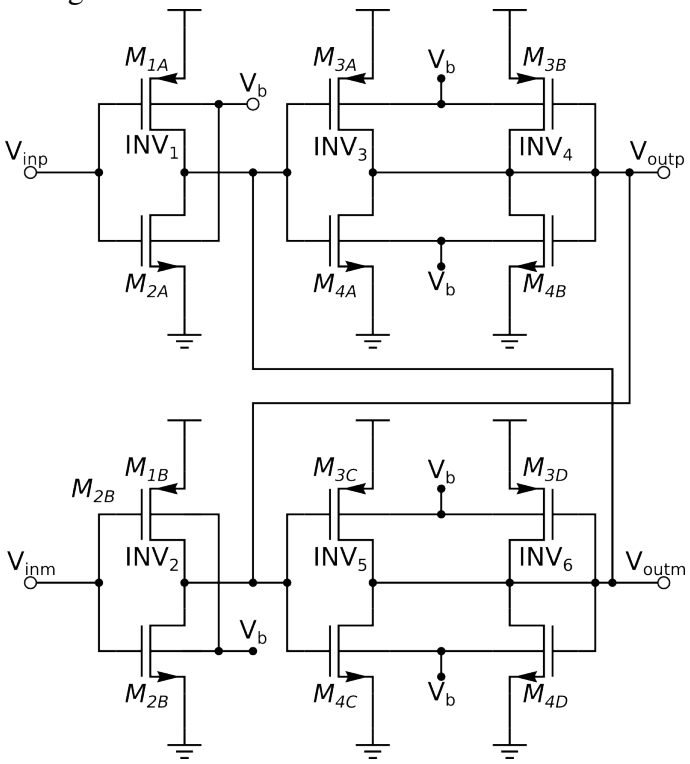
$$V_b = -V_{REF}\frac{G_m}{G_o + (n-1)G_m} \approx \frac{-V_{REF}}{(n-1)} \tag{3.8a}$$

$$V_Q = -V_b(n-1)\frac{G_m}{G_o + G_m} \approx V_{REF} \tag{3.8b}$$

The circuit shown in figure 3.3a defines V_Q at the expense of I_Q variation, since both V_{bp} and V_{bn} are shorted. To correct V_Q deviation without varying I_Q, V_{bp} and V_{bn} must be independently biased, as shown in figure 3.3b. In this circuit, the NMOS transistors mirrors the current reference I_{REF}, while the PMOS transistors mirror the curent from the NMOS. This biasing scheme results in a lower correction range potential as it aims to correct two parameters at the same time.

$$I_Q \approx I_{REF} \tag{3.9a}$$

Figure 3.4: Bulk-biased Nauta's transconductor



$$V_{bn(p)} = -V_{REF}\frac{G_m}{G_o + \frac{(n-1)G_m}{2}} \approx \frac{-2V_{REF}}{(n-1)} \tag{3.9b}$$

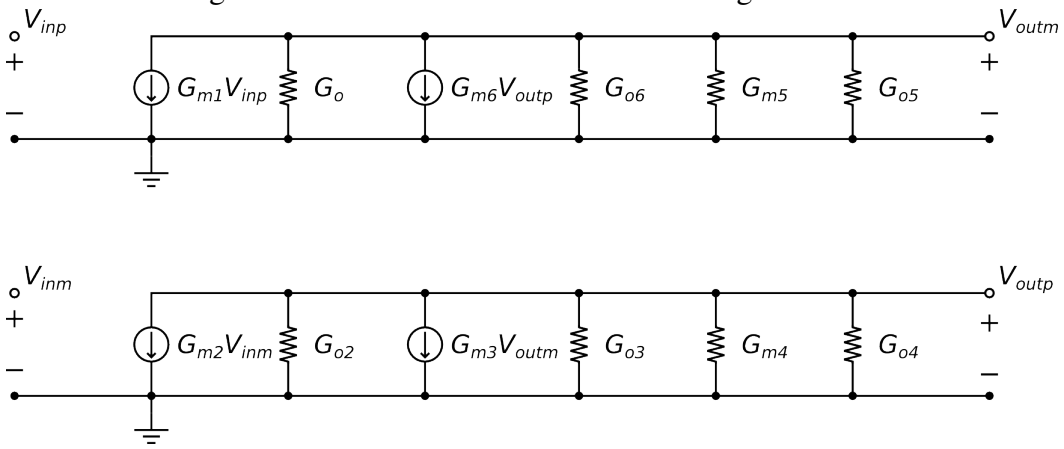
$$V_Q = -V_{bp}(n-1)\frac{G_m}{G_o + G_m} \approx V_{REF} \tag{3.9c}$$

Biased Nauta's Transconductor

The transconductor proposed in (NAUTA, 1992), shown in figure 3.4, is based on a push-pull pseudo differential pair and a circuit which rejects common-mode input signals. The common-mode output voltage is the quiescent voltage V_Q of the push-pull CMOS pair and it is a function of process parameters, so its is highly dependent of process variability. For nominal voltages, the output signal excursion reduction due to process variability isn't a concern as severe as for ultra low voltage, so, for ultra low voltage supplies, biasing is essential to make this topology feasible.

This transconductor achieves high gain by the use of push-pull pairs and a high operation speed by the lack of intermediary nodes between the input and output of the signal path. The pseudo-differential pair doesn't reject common mode input signals, therefore a circuit was devised to act as an large output resistance for differential signals and a small

Figure 3.5: Nauta's transconductor small-signal circuit



output resistance for common mode signals.

Equation 3.10 defines the small signal gains for differential and common-mode input signals, considering the small signal circuit from figure 3.5. Considering transistors with an infinite drain-source resistance, a perfectly simmetrical operation and no process variability, the output resistance of this circuit seen in the node V_{outm} is $1/(G_{m_6} + G_{m_5})$ for common-mode output voltages and $1/(G_{m_6} - G_{m_5})$ for differential output voltages. If Inv5 and Inv6 have the same dimensions and, consequently, the same G_m, output resistance is infinite, consequently voltage gain is also infinite. However, the process variability introduces a mismatch between those G_m, which results in a large but finite output resistance. Even neglecting the process variability, the drain-source impedance of all push-pull pairs is finite and in paralell to that infinite resistance, which results in a finite DC gain.

$$A_{V_{diff}} = \frac{G_{m_1}}{G_{o_1} + G_{o_5} + G_{o_6} + G_{m_5} - G_{m_6}} \tag{3.10a}$$

$$A_{V_{cm}} = \frac{G_{m_1}}{G_{o_1} + G_{o_5} + G_{o_6} + G_{m_5} + G_{m_6}} \tag{3.10b}$$

As seen in equations 3.3a and 3.3b, G_o and G_m of the push-pull pairs are both directly proportional to I_Q, therefore increasing equally I_Q of all push-pull pairs doesn't result in any change of $A_{V_{diff}}$ and $A_{V_{cm}}$, and consequently of CMRR. To properly control differential gain and common-mode gain, I_Q of the push-pull pseudo differential pair must be made different from the push-pull pairs of the common-mode rejection circuit, resulting in a trade-off between $A_{V_{diff}}$ and CMRR.

In order to properly bias the transconductor, the bias circuit must be designed according to the following constraints. The first constraint imposed by the push-pull biasing

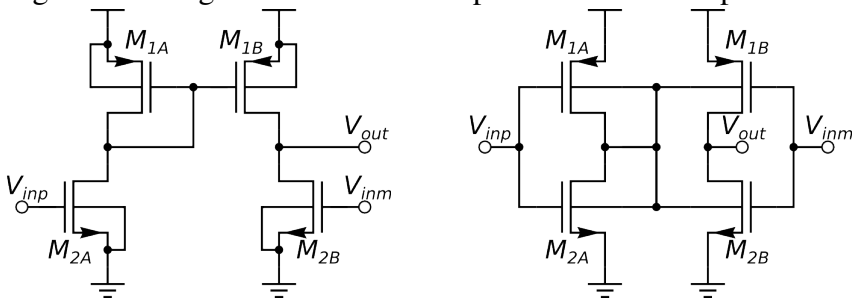
scheme is that every push-pull pair must have the same proportion $W_P L_N / W_N L_P$, since the biasing is achieved by using a replica of the push-pull pairs found in the transconductor. The second constraint is brought by device mismatch, consequently the transistor dimensions must be chosen in order to minimize mismatch between the push-pull pairs, otherwise the quiescent output voltage will be mainly defined by mismatch instead of process variability, defeating the purpose of the biasing scheme.

The viability of this scheme is limited by how much the biasing of the bulk terminals can correct the output quiescent voltages, which is limited by the transistor body effect parameters which are not available for circuit designers. The range of ΔV_Q is established by maximum and minimum V_b achievable by the biasing circuit, which are limited by transistor saturation voltage V_{SAT}, then $V_{SAT_N} < \Delta V_b < V_{DD} - V_{SAT_P}$. For typical operation conditions, the base push-pull pair must be sized in such a way that V_Q and V_b is $V_{DD}/2$, for optimal operation range.

Operational Transconductance Amplifiers Based in Pseudo Differential Pairs

Proposed self biased amplifiers

Figure 3.6: Single ended self biased pseudo differential pair OTAs

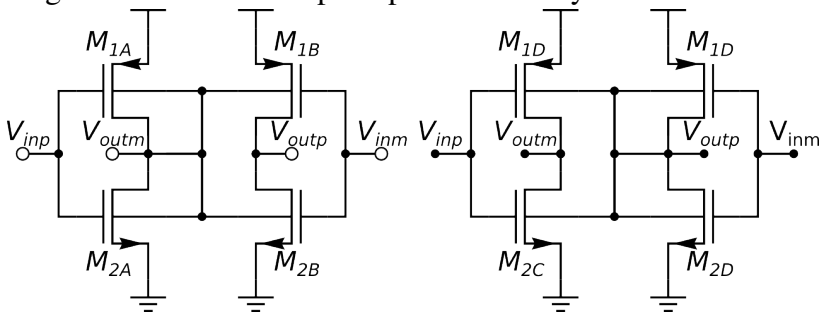


(a) Mirrored load pseudo differential pair

(b) Proposed push-pull based self biased pseudo differential pair

A pseudo differential pair can be implemented by two CMOS push-pull pairs, however, without any extra circuit, this topology doesn't offer any common mode rejection. For ultra low voltage supplies, the simplest topology to offer common mode rejection is the pseudo differential pair with an active mirrored load, as shown in figure 3.6a. In order to employ the push-pull pair in a pseudo differential amplifier, the common mode rejection of the mirrored active load and no extra stacked transistors, the bulk terminals must be used. Figure 3.6b shows a proposed push-pull based self-biased pseudo

Figure 3.7: Self biased push-pull based fully differential OTA



differential pair with mirrored loads implemented by forward body biasing with a process which enables NMOS bulk biasing. As can be deducted from equation 3.11 and previous definitions of G_m and G_o for the push-pull pair, the differential gain is approximately the gain of the push-pull pair and the common mode gain is tend to null as $(n-1)G_m >> G_o$.

$$V_{out} = \left[V_{inp} \frac{(n-1)G_m}{G_o + (n-1)G_m} - V_{inm} \right] \frac{G_m}{G_o} \approx (V_{inp} - V_{inm}) \frac{G_m}{G_o} \tag{3.11}$$

For a fully differential OTA, an approach similar to the previous single ended OTA can be used, by using two simmetrical single ended OTAs with shorted outputs, as the proposed amplifier shown in figure 3.7. For perfectly matched OTAs, the differential gain is approximately the gain of the push-pull pair and the common mode gain inversely proportional to $(n-1)$, as deduced from equations 3.12.

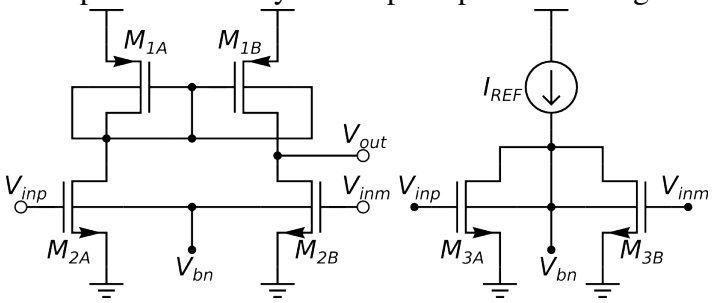
$$V_{outm(p)} = [2V_{inp(m)} + (n-1)V_{outp(m)}] \frac{G_m}{2G_o + (n-1)G_m} \tag{3.12a}$$

$$A_{V_{diff}} = \frac{2G_m}{2G_o + (n-1)(G_m - G_m)} \approx \frac{G_m}{G_o} \tag{3.12b}$$

$$A_{V_{cm}} = \frac{2G_m}{2G_o + (n-1)(G_m + G_m)} \approx \frac{1}{n-1} \tag{3.12c}$$

$$CMMR = \frac{A_{V_{diff}}}{A_{V_{cm}}} \approx (n-1)A_{V_{diff}} \tag{3.12d}$$

Figure 3.8: Proposed externally biased push-pull based single ended OTA



Proposed externally biased amplifiers

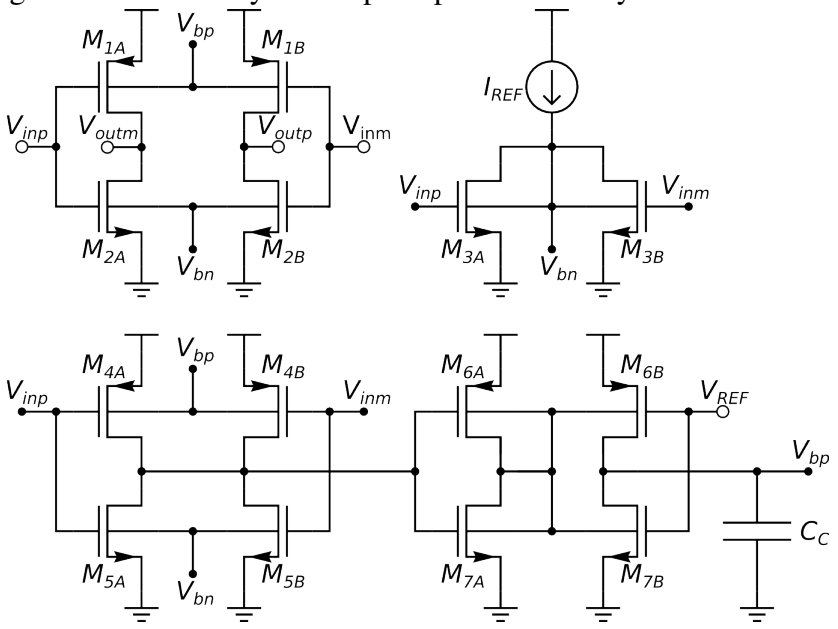
The previous OTAs, however, are not tolerant to process variability, since the push-pull pair quiescent voltage and current is dependent of process parameters. For single ended OTAs, the quiescent voltage is not important since their applications usually use feedback, but the quiescent current is highly dependent of the common mode input signal and process parameters, and, consequently, their transconductance varies accordingly. Figure 3.8 depicts an externally biased pseudo differential pair with mirrored load. The common mode input signal is compared to a current reference and defines the bulk terminal voltage of the pseudo differential pair NMOS transistors, which attenuates the output common mode signal while keeping the quiescent current constant.

$$V_{out} = [V_{inp} + (n-1)V_{bn}]\frac{g_{m_N}}{G_o + ng_{m_P}}\frac{ng_{m_P}}{G_o} - [V_{inm} + (n-1)V_{bn}]\frac{g_{m_N}}{G_o} \tag{3.13a}$$

$$V_{bn} = V_{cm}\frac{g_{m_N}}{g_{DS_N} + (n-1)g_{m_N}} \approx \frac{V_{cm}}{n-1} \tag{3.13b}$$

For fully differential OTAs, the quiescent voltage of the pseudo differential pair is relevant, as it defines the common mode output voltage. Figure 3.9 shown the proposed fully differential amplifier which additional circuits to bias the bulk terminals of the pseudo differential pair to achieve quiescent current and voltage stability while rejecting common mode signals. The reference current I_{REF} defines the current and transconductance of the pseudo differential pair and its replicas, while the voltage reference V_{REF} defines the quiescent voltage, as long as the feedback loop gain β is large, as shown in equations 3.14. The feedback loop can be unstable and can oscillate, since it has three phase inversions, therefore it requires some kind of stability compensation, which

Figure 3.9: Externally biased push-pull based fully differential OTA



is achieved by increasing the impedance of one of its nodes with a stability compensation capacitor C_C.

$$V_{outm(p)} = -\frac{V_{inp(m)}G_m + (n-1)(V_{bp}g_{m_P} + V_{bn}g_{m_N})}{G_o} \tag{3.14a}$$

$$V_{bn} = V_{cm}\frac{2g_{m_N}}{2g_{DS_N} + (n-1)2g_{m_N}} \approx -\frac{V_{cm}}{n-1} \tag{3.14b}$$

$$V_{bp} = -\frac{V_{cm}G_m + V_{bn}(n-1)g_{m_N} + V_{bp}(n-1)g_{m_P}}{G_o}\frac{G_m}{G_o} \tag{3.14c}$$

$$V_{bp} \approx -\frac{V_{cm}}{(n-1)}\frac{\beta}{(1+\beta)} \tag{3.14d}$$

$$\beta = \frac{1}{2(n-1)}\left(\frac{{G_m}^2}{G_o}\right) \tag{3.14e}$$

Section Summary

Nauta and Vieru topologies are push-pull based transconductors which use parallel inverters to the main pseudo differential pair to implement common mode rejection with the penalty of reduction of output resistance and DC voltage gain. Forward body biasing

can be used for both V_Q and I_Q external biasing, which reduces process variability effects. The proposed push-pull transconductors use the body terminals not just for V_Q and I_Q external biasing, but also or exclusively for common-mode rejection, which results in a DC voltage gain boost, since there is no output resistance reduction. The next chapter will present simulation results for the proposed topologies and compare with state-of-art topologies.

4 SIMULATION RESULTS - AMPLIFIERS

In this chapter, the proposed amplifiers will be designed and tested for a 250 mV supply voltage and the same process, in this case the IBM RF CMOS 130 nm. Later, their performances will be compared to state of art counterparts.

Amplifiers

In chapter 2, pseudo differential based amplifiers were discussed and analysed. In chapter 3, novel amplifier topologies were proposed. Those proposed topologies have two variants, single ended and fully differential, and each has its own peculiarities in regard to the expected performance. Common mode and power supply rejection are important single ended amplifier performance characteristics, however its not as important for fully differential topologies, which are intrinsically tolerant to common mode signals. Fully differential topologies still are affected by common mode and power supply interference, since those interferences can reduce output signal excursion. The performance of fully differential topologies, however, is highly dependent of the output common mode voltage, as it limits the output range swing for low distortion requirements. The single ended DC output voltage is usually defined by transistor biasing and input offset is often resulted from mismatch. In the following subsections, the proposed topologies will be designed with similar specifications and then compared with each other.

Single Ended

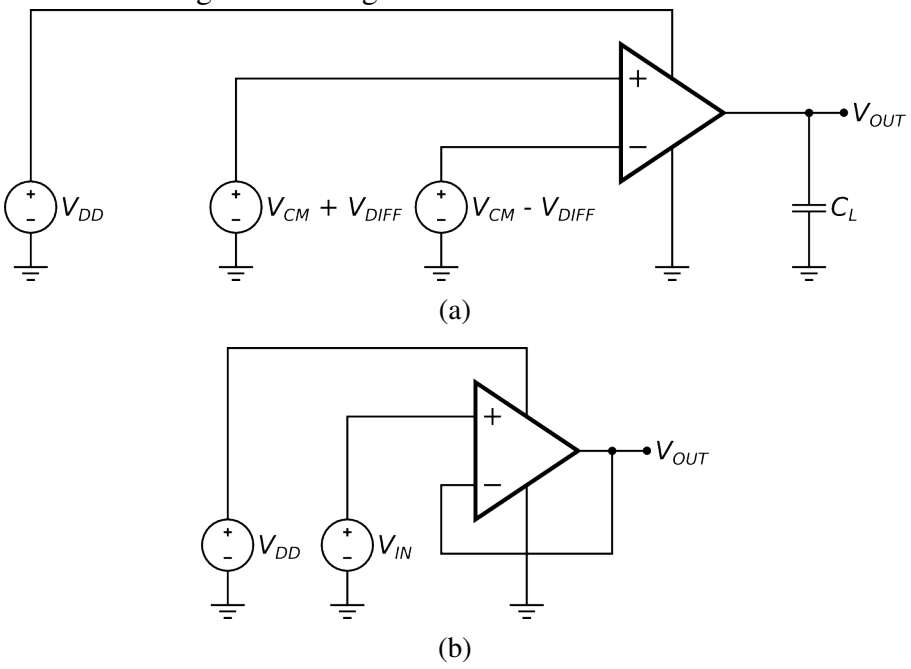
Two novel single ended amplifier topologies were proposed. The first one, shown in figure 3.6b, is based in self biased pseudo differential pairs and uses the bulk terminals for mirroring the currents of each pair for common mode signals. The second one, shown in figure 3.8, uses a feedforward common mode rejection and forward body biasing of the transistors to define the pseudo differential pair DC current. Those topologies may require special processes with isolated NMOS devices to access the bulk terminal. For comparison purposes, a common pseudo differential single ended amplifier with mirrored load, shown in figure 3.6a, was also designed.

The designed amplifiers performance characteristcs were extracted from simula-

tions done in the testbenchs depicted in figure 4.1. The testbenchs differ on their purposes: testbench (a) was designed for differential and common mode signal measurements whereas testbench (b) was designed to measure input offset voltage resulted from mismatch. The tests consisted of 1000 DC and AC process and mismatch Monte Carlo simulations at 27 °C, a supply voltage of 250 mV and a 15 pF capacitive load C_L for each design.

The simulation results are sumarized in table 4.1. Figures 4.2, 4.3 and 4.4 show graphs depicting the (a) DC and (b) AC transfer function responses (differential, common mode and power supply) and (c) open loop gain and (d) gain bandwidth product Monte Carlo simulation results for each designed topology.

Figure 4.1: Single Ended OTAs - Testbenchs



The small signal transconductance of the pseudo differential mirrored load OTA and the proposed self biased pseudo differential pair are function of the input DC voltage. In regard to the externally biased pseudo differential pair, the small signal transconductance is function of the pair DC current, which follows the reference current. The amplifier transconductance is a key aspect and defines many amplifier performance characteristics, as bandwidth, noise, power consumption and gain. For comparison purposes, however, all amplifiers were designed to have the same transistor length and pseudo differential pair area and the same DC input and output voltages, as detailed in table 4.2. Those topologies did not have a clear design goal on purpose, as they were designed for comparison only.

Table 4.1: Single Ended OTAs - Simulation Results Summary

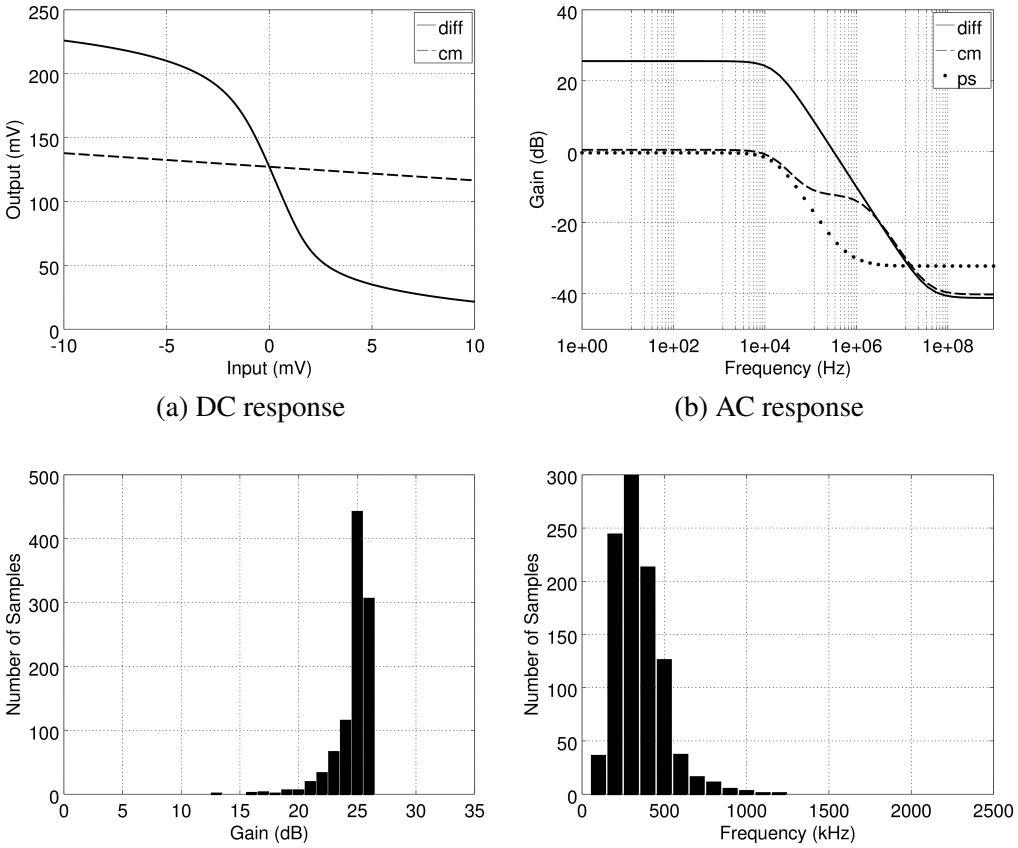
	$Gain\,(dB)$			$CMRR\,(dB)$			$PSRR\,(dB)$		
	μ	σ	σ/μ	μ	σ	σ/μ	μ	σ	σ/μ
Mirrored load	24.73	1.40	5.66%	24.60	1.87	7.60%	25.19	1.64	6.51%
Self biased	28.05	5.00	17.8%	15.49	4.32	27.9%	20.13	4.40	21.9%
Externally biased	25.19	1.02	4.05%	42.86	7.64	17.8%	25.63	1.26	4.92%
	$I\,(\mu A)$			GBW (kHz)			*Input Offset* (mV)		
	μ	σ	σ/μ	μ	σ	σ/μ	μ	σ	σ/μ
Mirrored load	1.455	0.676	46.5%	345	146	42.3%	-	1.327	-
Self biased	2.644	0.822	31.1%	1114	321	28.8%	-	1.868	-
Externally biased	3.275	0.320	9.77%	576	67	11.6%	-	1.087	-
	$FoM\,(\mu A)$			$P\,(\mu W)$					
	μ	σ	σ/μ	μ	σ	σ/μ			
Mirrored load	240.0	7.31	3.05%	0.364	0.169	46.5%			
Self biased	424.0	10.53	2.48%	0.661	0.206	31.1%			
Externally biased	175.6	3.26	1.86%	0.819	0.080	9.77%			

The pseudo differential pair with mirrored load does not use forward body biasing, then the PMOS transistors bulk terminals are connected to V_{DD} and the NMOS transistors bulk terminals are connected to ground. For the self and externally biased pseudo differential pairs, both PMOS and NMOS bulk terminals are biased at half supply voltage, for respectively better output range and biasing range. Forward body biasing reduces the transistors threshold voltage, which results in a greater inversion level for the same DC input voltage. As expected, forward body biasing increases the bandwidth but also increases the power consumption for similar sized topologies.

The most common figure of merit for amplifier efficiency, shown in equation 4.1, relates bandwidth and current consumption. That figure of merit does not take into account other desirable performance characteristics, which actually come from the tradeoffs of bandwidth and current consumption, since they require additional circuits, such as biasing feedback circuits. In the simulations results, the self biased pseudo differential pair has a high FoM, since the push-pull pair has an intrinsically greater transconductance and gain than a similar common source amplifier with active load, however its CMRR is poor. The biased pseudo differential pair with feedfoward common rejection is less efficient than the other topologies, however, since its DC current is externally biased, its transconductance is more tolerant to process variability and its CMRR is considerably larger.

$$FoM = 100 \times \frac{GBW \times C_L}{I} \tag{4.1}$$

Figure 4.2: Single Ended OTA - Mirrored - Simulation Results



(a) DC response

(b) AC response

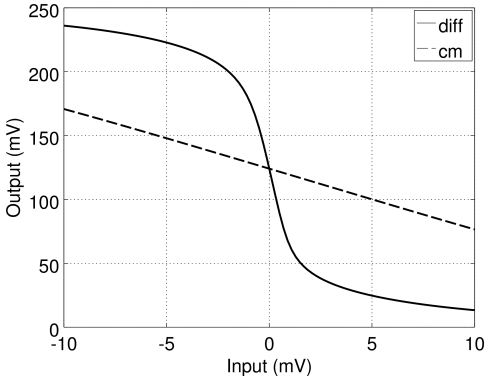
(c) Monte Carlo - Open loop gain

(d) Monte Carlo - GBW

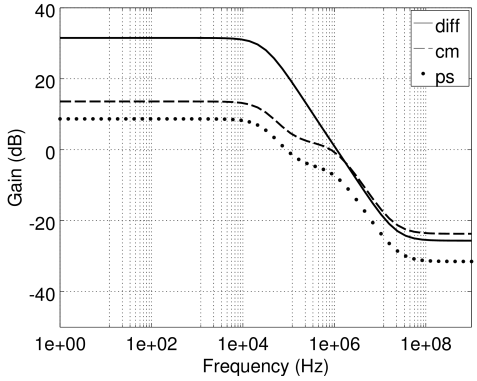
Table 4.2: Single Ended OTAs - Device Geometry

	$M_{1A,B}$	$M_{2A,B}$	$M_{3A,B}$
Mirrored load	$4 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	–
Self biased	$4 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	–
Externally biased	$4 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	$1 \times 5\mu m/2\mu m$

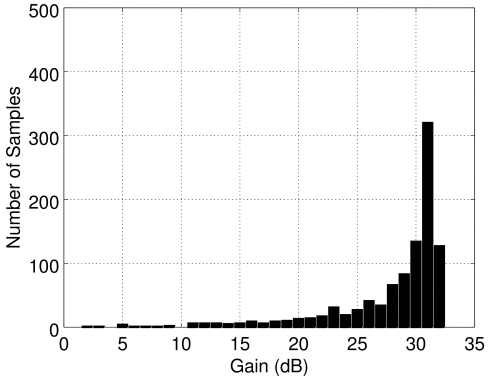
Figure 4.3: Single Ended OTA - Self biased - Simulation Results



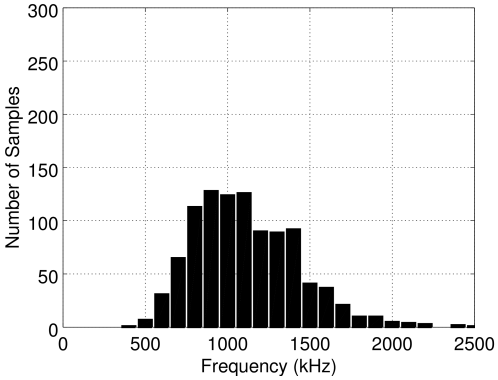
(a) DC response



(b) AC response

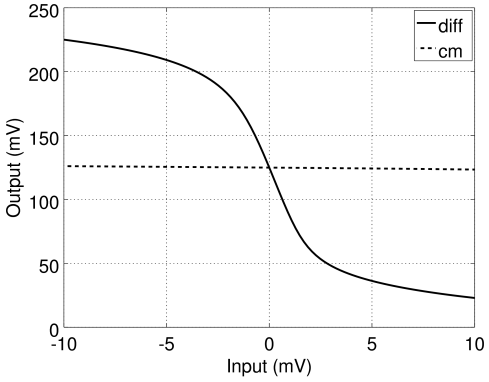


(c) Monte Carlo - Open loop gain

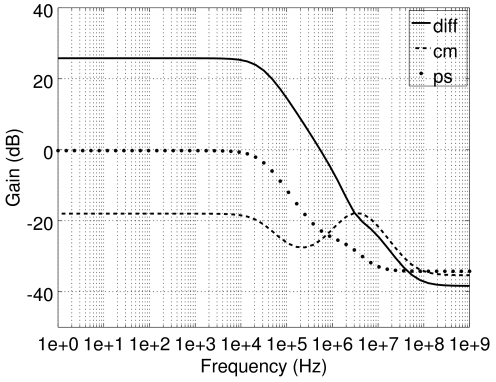


(d) Monte Carlo - GBW

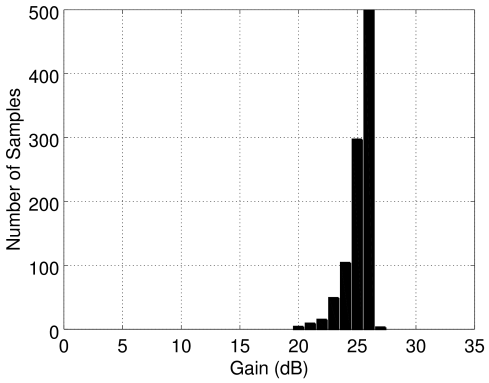
Figure 4.4: Single Ended OTA - Externally biased - Simulation Results



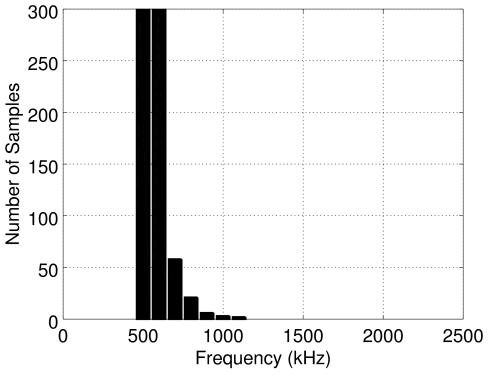
(a) DC response



(b) AC response



(c) Monte Carlo - Open loop gain



(d) Monte Carlo - GBW

Table 4.3: Fully Differential OTAs - Device Geometry

	M_{1A-D}	M_{2A-D}	$M_{3A,B}$	$M_{4A,B}$
Self biased Nauta	$4 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	$-$	
Externally biased Nauta	$4 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	$-$	
Self biased pseudo	$2 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	$1 \times 5\mu m/2\mu m$	
Externally biased pseudo	$4 \times 50\mu m/2\mu m$	$4 \times 5\mu m/2\mu m$	$1 \times 5\mu m/2\mu m$	$1 \times 50\mu m/2\mu m$
	M_{5A-B}	M_{6A-B}	$M_{7A,B}$	
Externally biased pseudo	$1 \times 5\mu m/2\mu m$	$1 \times 50\mu m/2\mu m$	$1 \times 5\mu m/2\mu m$	

Fully Differential

In addition to the single ended amplifiers, two novel fully differential amplifier topologies were proposed. The first one, shown in figure 3.7, is based in the self biased pseudo differential pairs and uses the bulk terminals to implement a common mode rejection circuit. The second one, shown in figure 3.9, uses a feedforward common mode rejection and forward body biasing of the transistors to define the pseudo differential pair DC current and common mode output voltage. Also, two versions of the Nauta's transconductor were designed, one self biased and another with external current and common mode output biasing, as shown in figures 3.3b and 3.4.

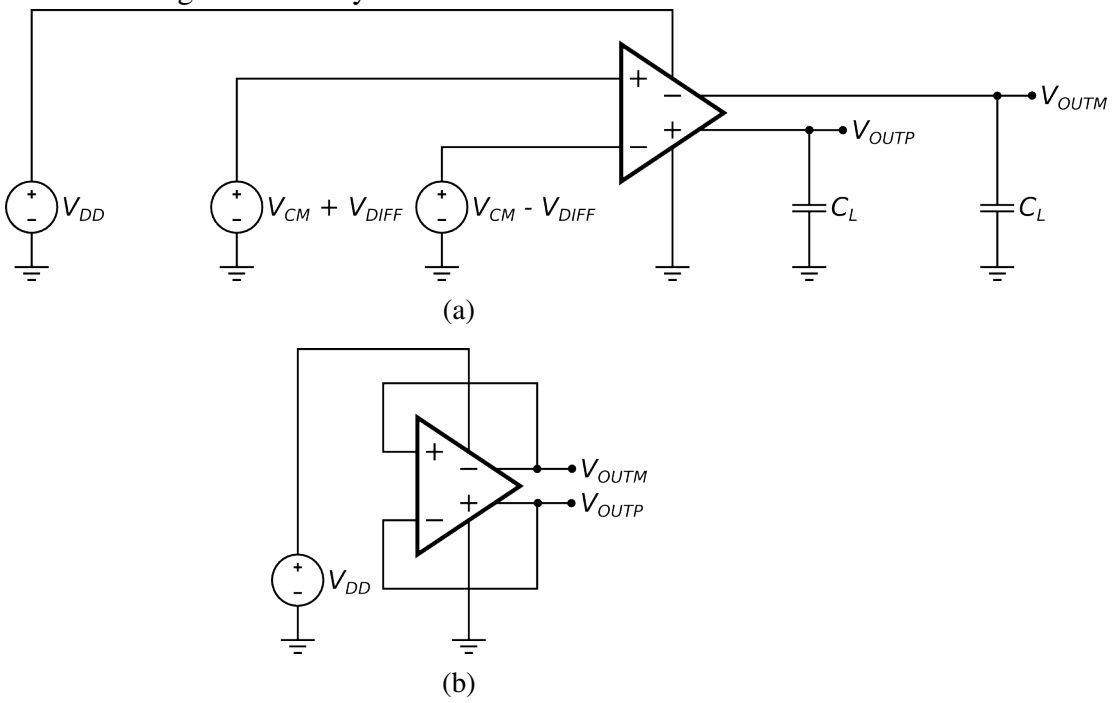
All topologies were designed with the same transistor size for the pseudo differential pair, which are based in the CMOS push-pull pair. The transistor sizes are detailed in table 4.3.

The designed amplifiers performance characteristcs were extracted from simulations done in the testbenchs depicted in figure 4.5. Those testbench and simulation parameters are similar to previous single ended OTA simulations, with minor adaptations for fully differential designs, as the output common mode voltage measurement in testbench (b). The unbiased Nauta transconductor transistor bulk terminals are connected to ground and V_{DD}, for NMOS and PMOS devices respectively, while, for the other topologies, all the bulk terminals were biased at half supply voltage. As expected, forward body biasing increases current consumption and transconductance.

The simulation results are sumarized in table 4.4. Figures 4.6, 4.7, 4.8 and 4.9 show graphs depicting the (a) DC transfer function responses (differential and common mode) (b) AC open loop gain, (c) gain bandwidth product and (d) output common mode voltage Monte Carlo simulation results for each designed differential topology.

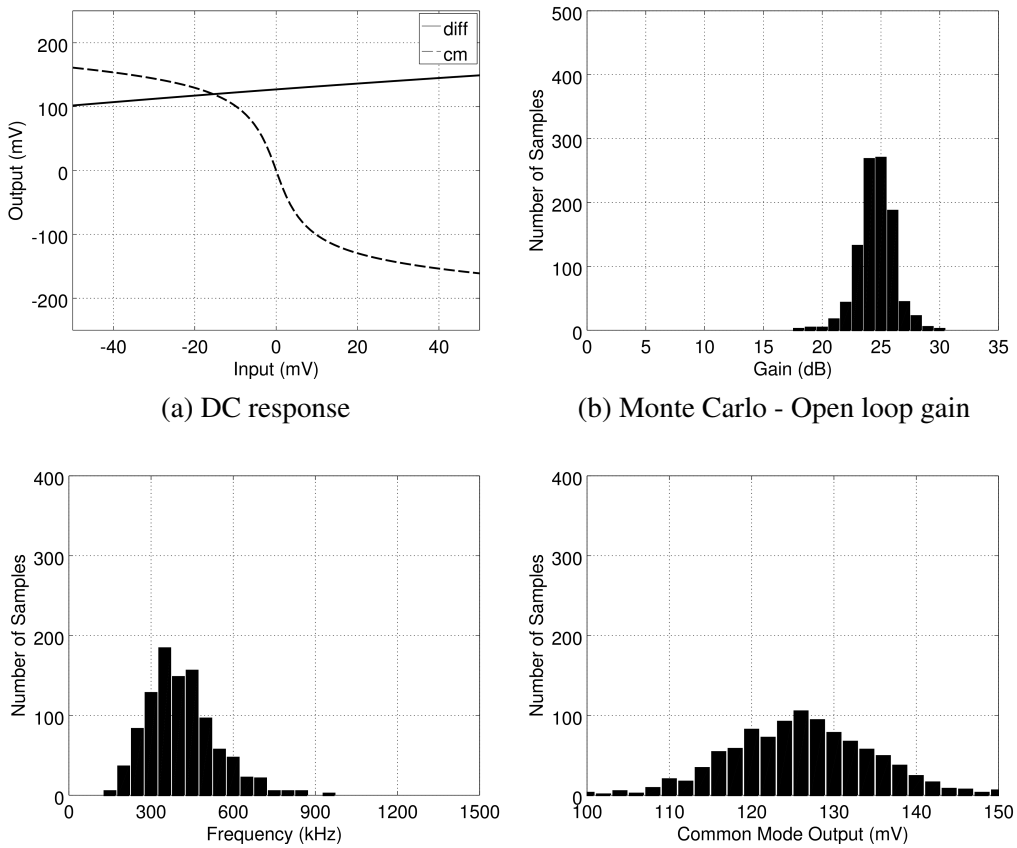
Nauta's transconductor topology has additional push-pull pairs to add common mode rejection to the pseudo differential pair and the externally biased one also has

Figure 4.5: Fully differential OTAs - Testbenchs



an additional biasing circuit. Both have a very good figure of merit and are very efficient. Obviously, the externally biased Nauta's amplifier has an additional biasing circuit, which increases current consumption to achieve better tolerance to process variability at the cost of efficiency. The novel topologies presented in this thesis have higher voltage gain and efficiency, however, their common mode output voltage tolerance is worse than those achieved by the Nauta's topologies. The externally biased pseudo differential pair transconductance is relatively tolerant to process variability and has a high CMRR.

Figure 4.6: Fully Differential Ended OTA - Self biased Nauta - Simulation Results



(a) DC response

(b) Monte Carlo - Open loop gain

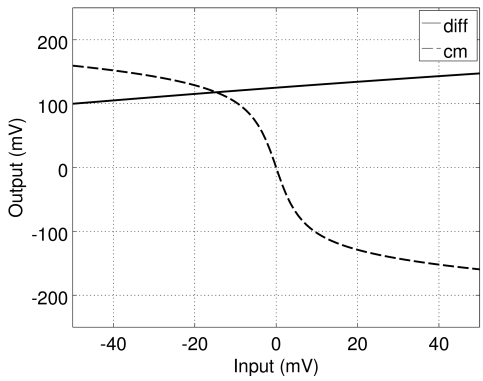
(c) Monte Carlo - GBW

(d) Monte Carlo - Common mode output

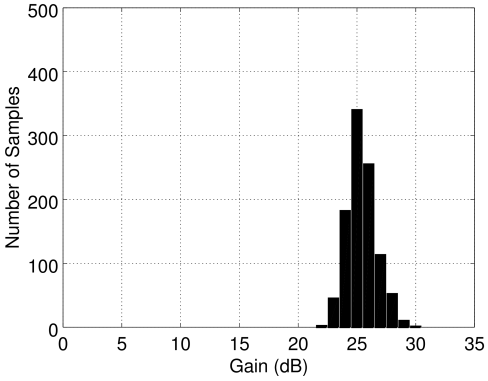
Table 4.4: Fully Differential OTAs - Simulation Results Summary

	$Gain\ (dB)$			$CMRR\ (dB)$			$I\ (\mu A)$		
	μ	σ	σ/μ	μ	σ	σ/μ	μ	σ	σ/μ
Unbiased Nauta	24.61	1.48	6.01%	25.05	1.33	5.31%	2.910	1.005	34.5%
Biased Nauta	25.33	1.22	4.82%	25.63	1.20	4.68%	5.871	0.766	13.0%
Unbiased Pseudo	30.24	4.86	16.1%	16.42	3.37	20.5%	2.506	0.763	30.4%
Biased Pseudo	31.02	3.67	11.8%	40.01	12.93	32.3%	4.454	0.587	13.2%
	GBW (kHz)			*C. M. Output* (mV)			*Input Offset* (mV)		
	μ	σ	σ/μ	μ	σ	σ/μ	μ	σ	σ/μ
Unbiased Nauta	395	126	31.9%	126	8.52	6.76%	-	0.374	-
Biased Nauta	670	84	12.5%	125	2.36	1.89%	-	0.364	-
Unbiased Pseudo	676	190	28.1%	125	11.5	9.20%	-	0.268	-
Biased Pseudo	745	95	12.8%	125	7.48	5.98%	-	0.264	-
	$FoM\ (\mu A)$			$P\ (\mu W)$					
	μ	σ	σ/μ	μ	σ	σ/μ			
Unbiased Nauta	204	6.94	3.40%	0.726	0.251	34.5%			
Biased Nauta	172	2.80	1.63%	1.468	0.192	13.0%			
Unbiased Pseudo	405	8.81	2.18%	0.627	0.627	30.4%			
Biased Pseudo	251	7.46	2.97%	1.136	0.147	13.2%			

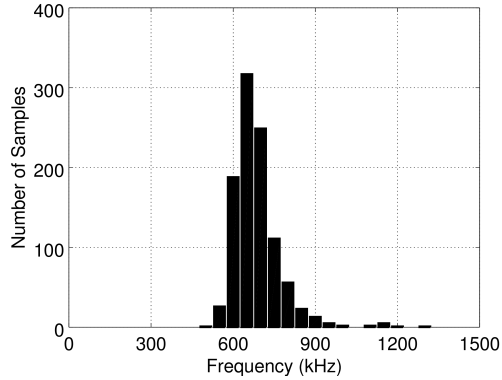
Figure 4.7: Fully Differential Ended OTA - Externally biased Nauta - Simulation Results



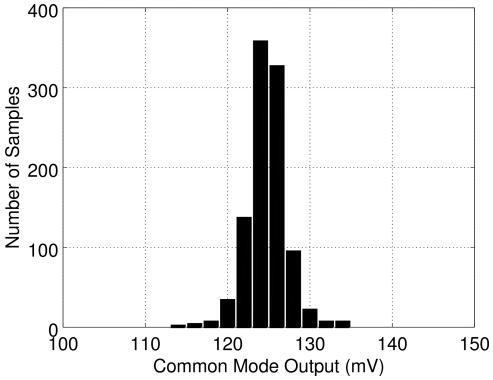
(a) DC response



(b) Monte Carlo - Open loop gain

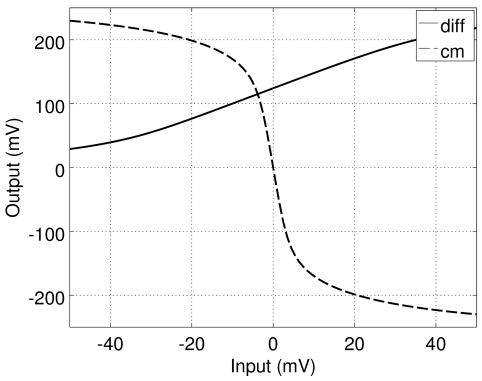


(c) Monte Carlo - GBW

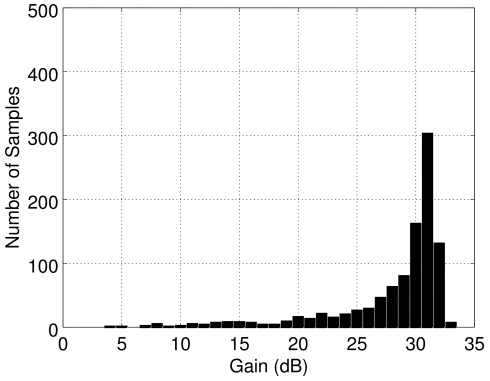


(d) Monte Carlo - Common mode output

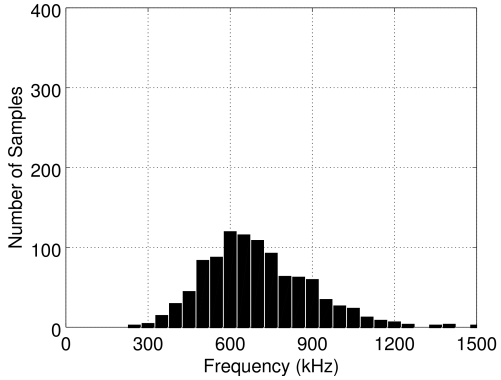
Figure 4.8: Fully Differential Ended OTA - Unbiased - Simulation Results



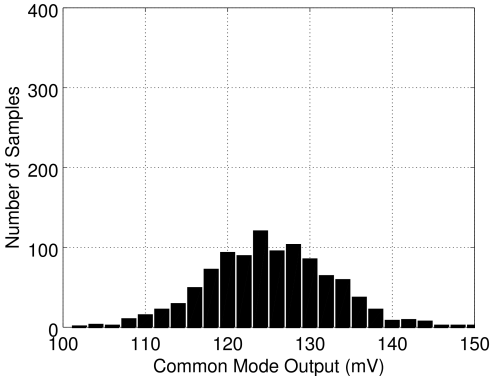
(a) DC response



(b) Monte Carlo - Open loop gain

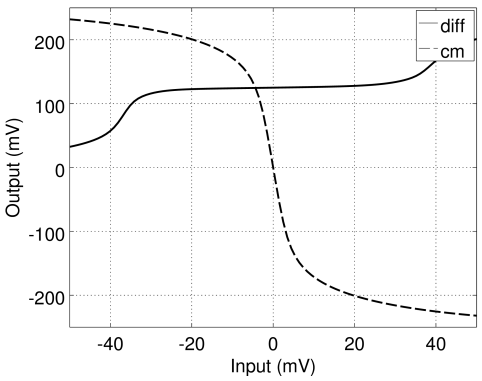


(c) Monte Carlo - GBW

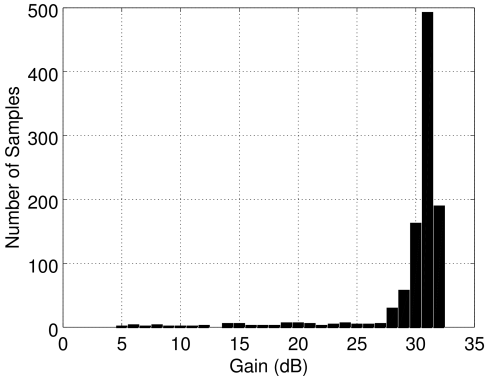


(d) Monte Carlo - Common Mode Output

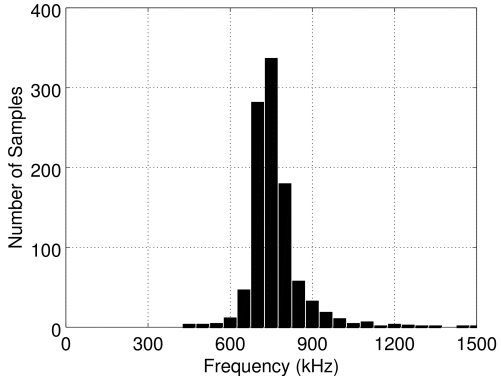
Figure 4.9: Fully Differential Ended OTA - Biased - Simulation Results



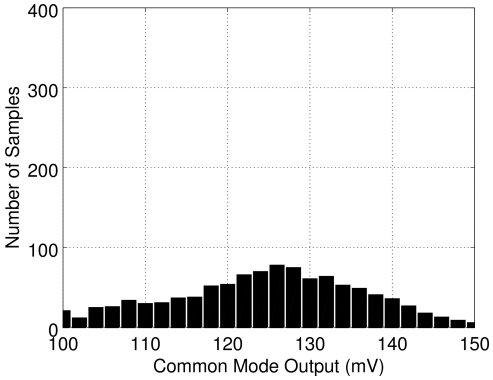
(a) DC Response



(b) Monte Carlo - Open loop gain



(c) Monte Carlo - GBW



(d) Monte Carlo - Common mode output

Two stage amplifier

Most of amplifier topologies researched for ultra low voltage employ two or more stages in order to achieve a greater DC gain. The use of multiple stages can make the amplifier unstable when negative feedback is used due to phase inversion, so a stability compensation scheme is necessary to define a minimum phase margin for a specified load. Stability compensation requires a tolerance margin to overcome process variability, which decreases the efficiency of multiple stage amplifiers in comparison to single stage amplifiers with the same load. Also, due to mismatch between cascading stages, multiple stage amplifiers do npt show the expected results from simulations with perfectly matched devices, which are optimized for maximum gain, therefore the average gain is lower.

For comparison purposes, a two stage non externaly biased fully differential amplifier was designed based on a single stage self biased amplifier depicted in figure. Each stage could be based in the several single stage amplifiers proposed in this work for general purposes, which could be area, power efficiency, process variability tolerance or performance. Most state of art referenced topologies aim to achieve energy efficiency and rarely show results in regards to process variability tolerance, which is crucial for ultra low voltages. Process variability could be further eliminated by calibration, however it requires additional circuits and challenges of its own that are outside the scope of this work.

Figure 4.10 shows graphs depicting the (a) DC and (b) AC transfer function responses and (c) open loop gain, (d) gain bandwidth product, (e) output common mode voltage and (f) input offset voltage Monte Carlo simulation results for the two stage voltage amplifier. Table 4.5 summarizes a performance comparison of several state-of-the-art amplifier topologies.

The two stage amplifier was based in self biased differential OTA, which shows the higher FoM among the proposed topologies, which should result in a high voltage gain. However, the DC voltage gain is relatively small compared to the other topologies. Despite the transistor length being very large, $2\mu m$ for a $0.13\mu m$ process node, the newer process has a very small transistor drain-source resistance r_{DS} for similar sized transistor in older technologies, which is the cause of the relatively small DC gain. The transistor large sizes results in very large parasitic capacitances, which decreases the GBW and, consequently, the power efficiency. This work provides Monte Carlo simulations and uses average DC gain instead of a optimal result, while the other results do not specify

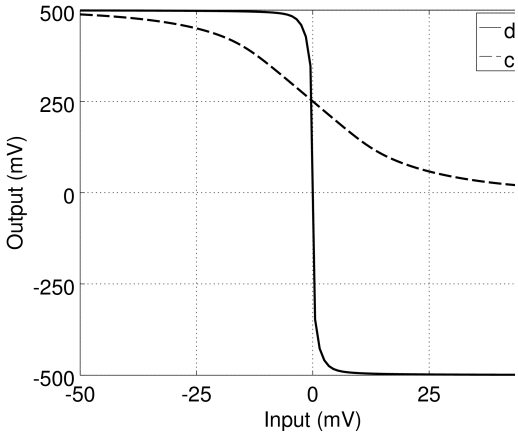
Table 4.5: OTA Performance Comparison

	[1]	[2]	[3]	[4]	[5]	[6]	This work
Technology node (nm)	180	180	180	180	180	180	130
Supply Voltage (V)	0.5	0.7	0.8	0.9	0.7	0.6	0.5
DC Gain (dB)	62	50	68	81	74	80	48
GBW (MHz)	10	10	8.1	11.5	25.3	6	13.9
PM (deg)	60	80	89	78	76	50	70
Power (μW)	75	55	94	110	82	13	73.2
Load (pF)	20	4	1	6.5	3	10	10
FoM	133	51	7	61	65	286	95

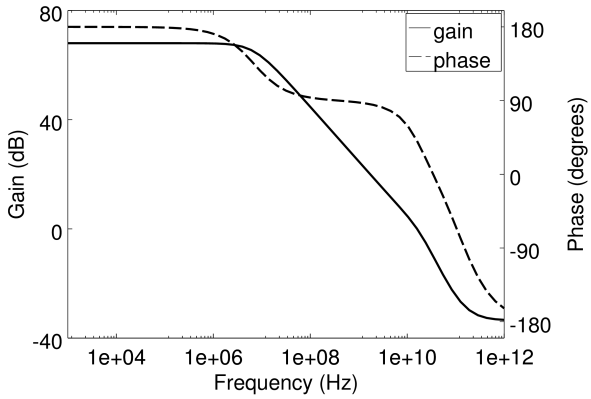
[1] (CHATTERJEE; TSIVIDIS; KINGET, 2005)
[2] (SAUERBREY et al., 2002)
[3] (ROSENFELD; KOZAK; FRIEDMAN, 2004)
[4] (ZABIHIAN; LOTFI, 2007)
[5] (ZABIHIAN; LOTFI, 2007)
[6] (VIERU; GHINEA, 2011)

statistical data for those metrics.

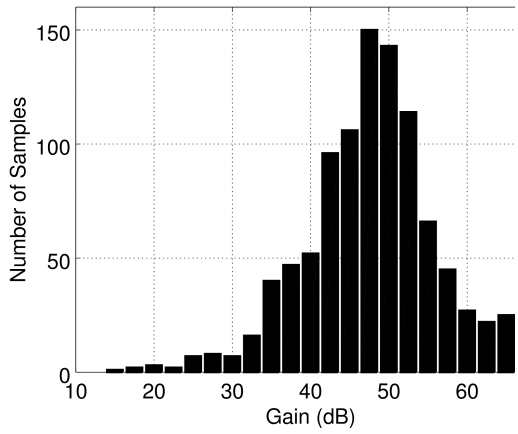
Figure 4.10: Fully Differential Ended 2 Stage Unbiased OTA - Simulation Results



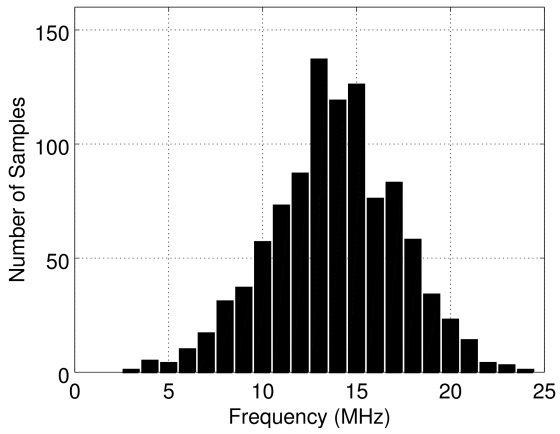
(a) DC response



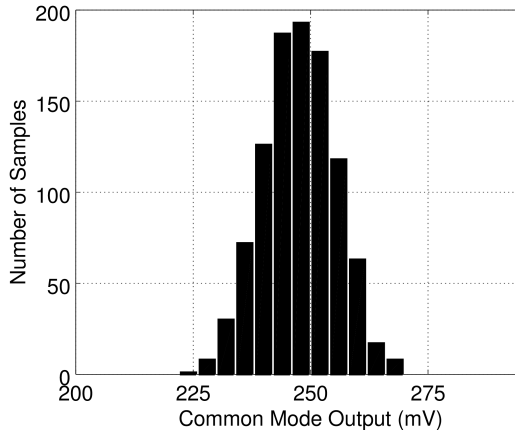
(b) AC response



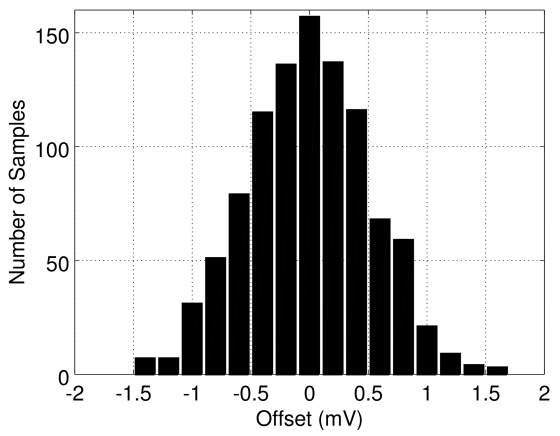
(c) Monte Carlo - Open loop gain



(d) Monte Carlo - GBW



(e) Monte Carlo - Common mode output



(f) Monte Carlo - Input offset

5 APPLICATIONS FOR THE PROPOSED BIASING STRATEGY

Amplifiers are basic components of several applications, including analog signal processing, data converters and oscillators. This chapter will discuss the usage of amplifiers as the building blocks of ring oscillators, specially about how the previously described push pull pair biasing strategies apply to reference oscillators and voltage controlled oscillators with improved linearity.

Ring Oscillator Analysis

The simplest ring oscillator topology is composed of a ring loop of an odd number of single ended amplifiers based in the CMOS push-pull inverter, as shown in figure 5.1. Ring oscillators with an even number of stages could also be implemented with fully differential amplifiers, which have common mode and power supply rejection, but are not as power efficient as the single-ended counterparts. In order to a ring oscillator properly operate, the feedback loop must be negative with a gain greater than one. The oscillation occurs in the frequency whose phase is 180° in the loop gain. A simple way to calculate this frequency f is by defining the number of stages N and respective delays t_d, as shown in the equation 5.1.

$$f = \frac{1}{2Nt_d} \tag{5.1}$$

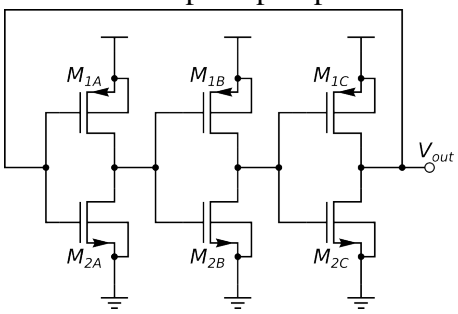
The delay in single ended amplifiers as the CMOS push-pull pair is proportional to the ratio of the capacitive C_L load, usually the input of the next stage, and the inverter transconductance G_m, as shown in the equation 5.2a. For weak inversion operation, which is common for ultra low supply voltages, G_m is proportional to the quiescent current I_Q of the inverter, as shown in the equation 5.2b.

$$t_d \propto \frac{C_L}{G_m} \tag{5.2a}$$

$$G_m \approx 2\frac{I_Q}{n\phi_t} \tag{5.2b}$$

The current I_Q of a non-biased CMOS push-pull pair is very sensitive to the supply voltage and process parameters, as seen in the equation 3.2, derived from the UICM model

Figure 5.1: Self biased push-pull pair based oscillator



in (SCHNEIDER; GALUP-MONTORO, 2010).

Additionally, both G_m and I_Q are dependent of the thermal potential ϕ_t, charge mobility μ and n, as shown in the equations 5.3a and 5.3b, which are highly dependent of temperature T. To design a ring oscillator with frequency stability tolerant to PVT, the oscillator must be biased by a reference current that is simultaneously independent of supply voltage variations and the effects of the temperature in the inverter delay.

$$\phi_t = \frac{kT}{q} \tag{5.3a}$$

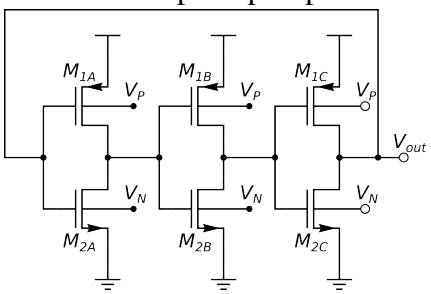
$$\mu \propto T^{-\alpha} \tag{5.3b}$$

Current biasing scheme for a CMOS Based Reference Oscillator

Electronic applications which relies in energy harvesting or very small batteries, requires low power, low voltage and integrated oscillators to achieve a small size, low cost and high autonomy. Crystal based oscillators are accurate and stable, but require a large discrete component (the crystal itself), which increases cost and size. Integrated oscillators, in special ring oscillators, relatively to crystal based oscillators, can be very inaccurate due to being dependent of process variability, supply voltage and temperature (PVT) (AITA; CRUZ; BASHIRULLAH, 2015), consequently, their application is limited by larger tolerance margins. In order to improve an integrated oscillator frequency stability and accuracy, some kind of stable reference is needed to counter back supply voltage and temperature fluctuations and further calibration to counter back process variability.

To compensate the impact of supply voltage fluctuations in a ring oscillator operation, the inverter quiescent current I_Q must be tolerant to those changes, so, this current must be referenced to another one with a biasing circuit. One possible solution is the use

Figure 5.2: Bulk biased push-pull pair based oscillator

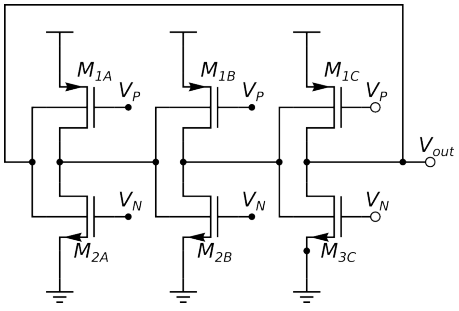


Source: (DEEN; KAZEMEINI; NASEH, 2003)

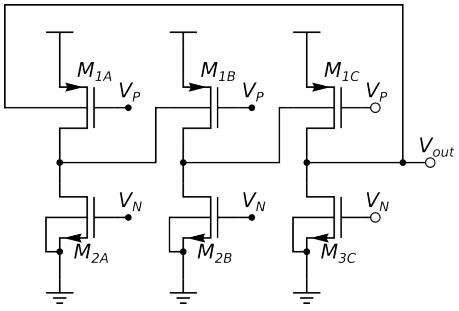
of the current starved ring oscillator. However, this topology is limited to greater supply voltages due to the use of stacked transistors. For supply voltages under 0.5 V, it is safe to use forward body biasing, which enable biasing using the bulk terminals of the transistor safely, as proposed in (DEEN; KAZEMEINI; NASEH, 2003) and depicted in figure 5.2. Bulk biasing uses the body effect to control the threshold voltage V_T to control I_Q.

The approach using the gate terminals for the loop signal and the bulk terminals for biasing offers a very limited tolerance to process variability and a short range for supply voltage operation, since the bulk terminal voltage has a fraction of the ability of the gate terminal to control the transistor current. For a better frequency stability, it is more suitable to bias the current of the inverters using the gate terminals and use the bulk terminals as the inverter input signal, with a tradeoff of a lesser nominal frequency.

Figure 5.3: Proposed biased oscillators



(a)



(b)

Figure 5.4: Proposed biasing circuit

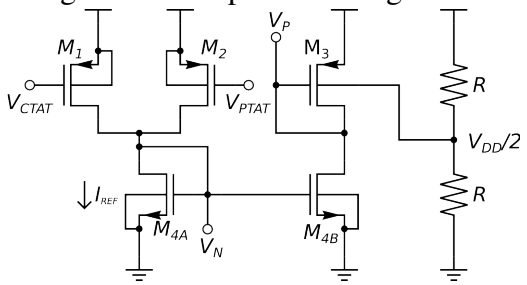
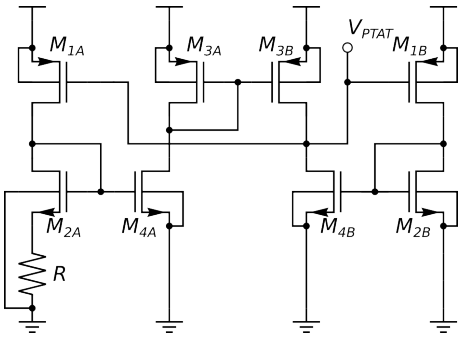
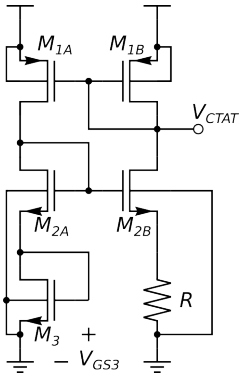


Figure 5.5: PTAT self biased current reference



Source: (RAZAVI, 2006)

Figure 5.6: CTAT self biased current reference



Source: (POPA, 2009)

Figures 5.3a and 5.3b show two variations proposed bulk driven ring oscillator. The biasing comes from mirroring the currents of replicas of the PMOS and NMOS transistors of the oscillator CMOS inverters, as shown in the figure 5.4. As long as all transistors are operating in saturation ($V_{DS} > 4\phi_t$), all currents follow the reference current I_{REF}. Once the biasing scheme is operational, the transconductance G_m of all inverters is proportional to I_{REF}. However, G_m is reduced by a factor of $1/(n-1)$, due to body effect.

In addition to the current biasing, the bulk terminal voltage of the PMOS defines the DC output voltage of all inverters. Without biasing the DC output voltage, since the oscillating wave may not reach the maximum amplitude provided by the supply voltage

for some operation conditions, the signal could not achieve voltage levels required by digital logic or result in variations of the square wave duty cycle after buffering.

A constant reference current, despite of improving the oscillator frequency stability to supply voltage fluctuations, does not improve the frequency stability to temperature variations, since G_m is function of n and ϕ_t, which are temperature dependent. To overcome the transconductance temperature dependence, the reference current must change with temperature to make G_m constant. ϕ_t is proportional to temperature, which suggests that I_{REF} must be a PTAT current.

In order to produce a reference current with the proper temperature coefficient, both PTAT reference and CTAT reference are needed. Any coefficient between the PTAT and CTAT coefficients can be achieved by summing multiples of both currents. The PTAT reference current is produced by a self biased constant-gm circuit with gain boosting for improving supply voltage stability, as depicted in figure 5.5. The CTAT reference current is a variation of a common current reference circuit based in the gate-source voltage of a weakly inverted MOSFET (POPA, 2009), as depicted in figure 5.6. The implementation of a specific PTAT reference by summing PTAT and CTAT current references is more practical than using only a specific PTAT reference for the oscillator since they can be used for another purposes with different requirements. The CTAT current reference employs three stacked transistors, but one of them operates in the triode region and, consequently, does not adds a higher supply voltage requirement as a transistor operating in saturation.

Biasing scheme for CMOS Ring Voltage Controlled Oscillator

VCOs are used in a wide range of applications. One of those applications is analog-digital data conversion, in the form of Frequency Sigma Delta Modulation in oversampling data converters. The main limitation of VCO use in ADCs is its own linearity, as it defines the maximum achievable bit resolution. (NARASIMMAN; KIM, 2013) discusses many strategies to address non-linearity in ring voltage controlled oscillators for ultra low power, both in the analog and digital domains. Digital non-linearity correction relies on look-up tables and calibration algorithms and trade off area and conversion speed for linearity, which degrades performance.

The RVCO proposed in (WISMAR; WISLAND; ANDREANI, 2006), uses forward body biasing to control the output frequency and includes a soft-rail transistor to improve linearity in the analog domain. Although this approach uses three stacked tran-

sistors, it is still feasible for ultra low voltages, as it may operate at supply voltages as low as 180 mV.

For further improvement in the performance of the FSDM, (WISMAR; WISLAND; ANDREANI, 2007) uses two VCOs for a differential frequency output, which increases linearity by canceling second order harmonics. Additionally, it uses all phases provided by the VCO to achieve multi-bit modulation.

The previously proposed ring oscillator can be used as a current controlled oscillator by replacing the current reference with a variable input current, achieving a very good linearity, since the output oscillation frequency is proportional to G_m and I_Q. To use the same ring oscillator as a VCO, the reference current must derived from a transconductor input voltage, which must be as linear as possible.

The main idea behind the biasing scheme is centered at the transconductor depicted in figure 5.7a, whose linearity is improved by referencing it to a resistor. The first step is to define the gate voltage of the PMOS transistors, which is achieved by defining the voltage V_R, which is the voltage across the reference resistor R_{REF}. As long as the loop gain is high, V_R is approximately the input voltage V_{in}, as shown in the equation 5.4a. The loop gain is the result of two cascading gain stages, A_1 and A_2, respectively the pseudo-differential voltage amplifier, depicted in figure 5.7b, and the common source amplifier with resistive load. The current I_R, which flows over the resistor, is proportional to V_{in}, accordingly to equation 5.5, and defines the current of all PMOS transistors, since they have the same gate voltage V_P and aspect ratio W/L. The gate and the drain terminals of the NMOS transistor are shorted, so every NMOS has a gate voltage V_N resulting in a drain current equal to I_{REF}.

$$V_R = V_{in}\frac{A_1 A_2}{1 + A_1 A_2} \tag{5.4a}$$

$$A_1 = \frac{g_{m_N}}{g_{DS_N} + g_{DS_P}} \tag{5.4b}$$

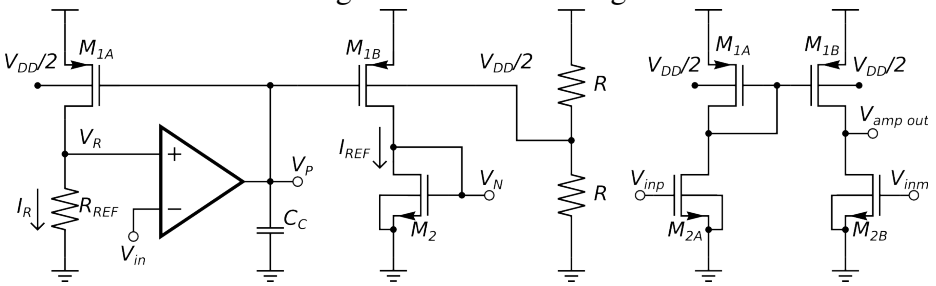
$$A_2 = \frac{g_{m_P}}{\frac{1}{R_{REF}} + g_{DS_P}} \tag{5.4c}$$

$$I_{REF} = I_R = \frac{V_R}{R_{REF}} \approx \frac{V_{in}}{R_{REF}} \tag{5.5}$$

The feedback loop has three inverter stages and can be unstable. The output node

of the voltage amplifier is responsible for the dominant pole, as its connected to the gates of all PMOS transistors but those from the differential voltage amplifier. For better stability, it is recommended to increase the node impedance with a stability compesation capacitor C_C. This dominant pole defines the dynamic limits of the VCO, since there is a delay between a change in V_{in} and V_R and, consequently, a change of output frequency.

Figure 5.7: VCO biasing scheme



(a) Transconductor (b) Pseudo differential amplifier

6 SIMULATION RESULTS - OSCILLATORS

In this chapter, the proposed oscillators will be designed and tested for a 250 mV supply voltage and the same process, in this case the IBM RF CMOS 130 nm. Later, their performances will be compared to state of art counterparts.

Reference Oscillator

For proof of concept, the four ring oscillator topologies presented in this work, (non compensated, the gate driven bulk biased, PMOS-NMOS bulk driven (a) and PMOS only bulk driven (b) gate biased), were designed in the 130 nm IBM RF CMOS process to operate with a nominal voltage of 400 mV at nominal temperature of 27 °C. The range for supply voltages were 300 mV to 500 mV and temperatures were -40 to 125 °C. Transistor dimensions and performance specifications are summarized in tables 6.1 and 6.2.

The proposed gate biased oscillators frequency are immune to voltage variation, as shown in the figure 6.1, while the bulk biased oscillator is considerably unstable, with a small improvement over the non-biased oscillator. The PTAT current reference has a minimum supply voltage requirement of 250 mV, while the CTAT reference has a minimum of 300 mV and is more unstable, as can be noticed in figure 6.2. The PMOS-only bulk driven oscillator shows second order effects which results in more stability than the oscillator driven by both transistor bulks, while both suffer from the instability caused by the CTAT reference.

All externally biased oscillators were biased with PTAT currents, which are a sum of the PTAT and CTAT current references to achieve the required temperature coeffient. The CTAT current reference is not linear, as shown in figure 6.3, which decreases the flat frequency range of the gate biased oscillator. The PTAT current reference does not have a temperature coefficient large enough to correct the output frequency of the bulk biased oscillator. Despite of all the reference imperfections, all externally biased oscillators are more stable than the self-biased one, as shown in figure 6.4

Table 6.1: Transistor dimensions

	Gate Biased (b)		Others	
	L (μm)	W (μm)	L (μm)	W (μm)
P_{1-3}	2	50	2	50
N_{1-3}	2	9	2	4.5

Figure 6.1: Supply voltage frequency stability

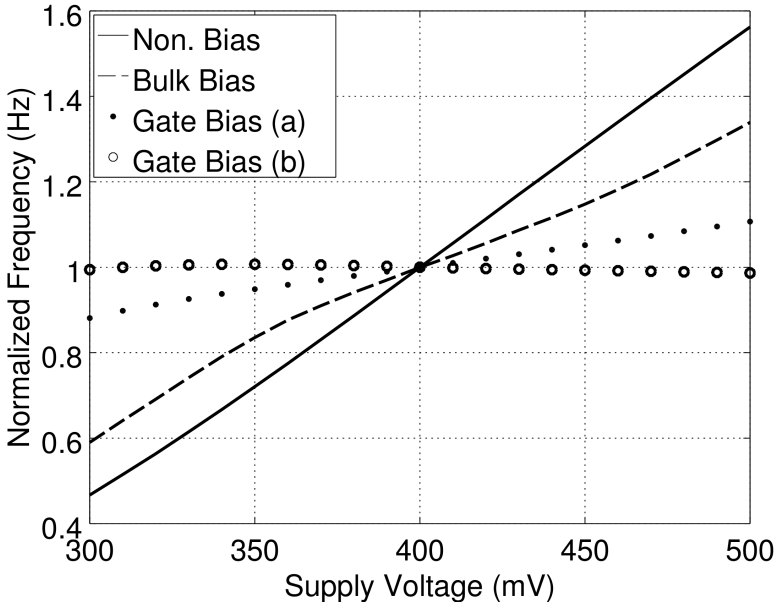


Figure 6.2: Current reference supply voltage stability

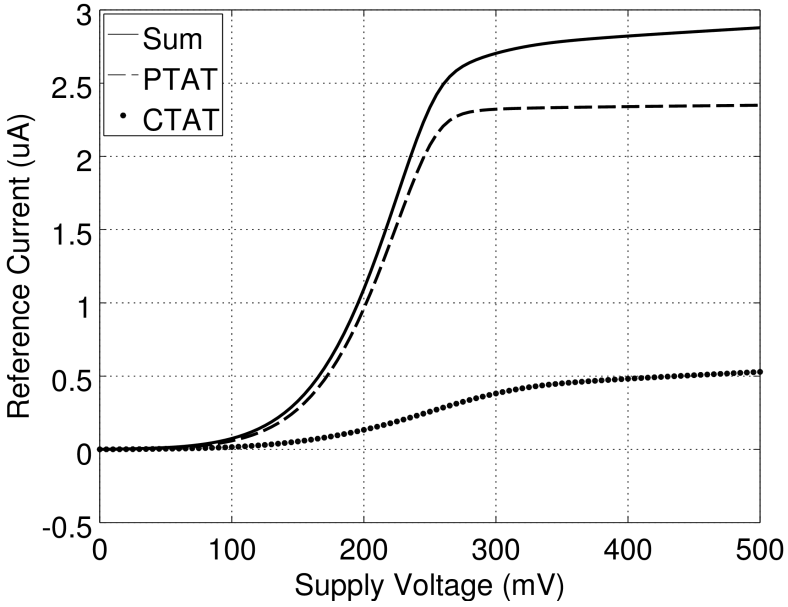


Figure 6.3: Current reference temperature frequency stability

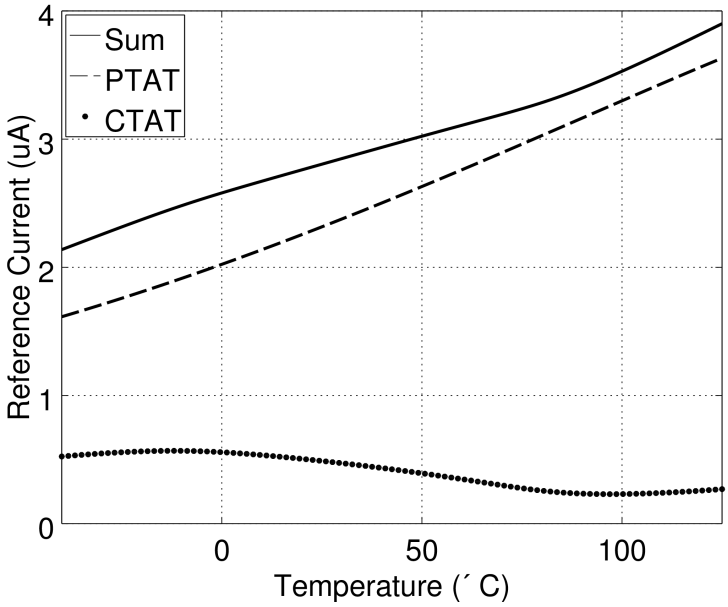


Figure 6.4: Temperature frequency stability

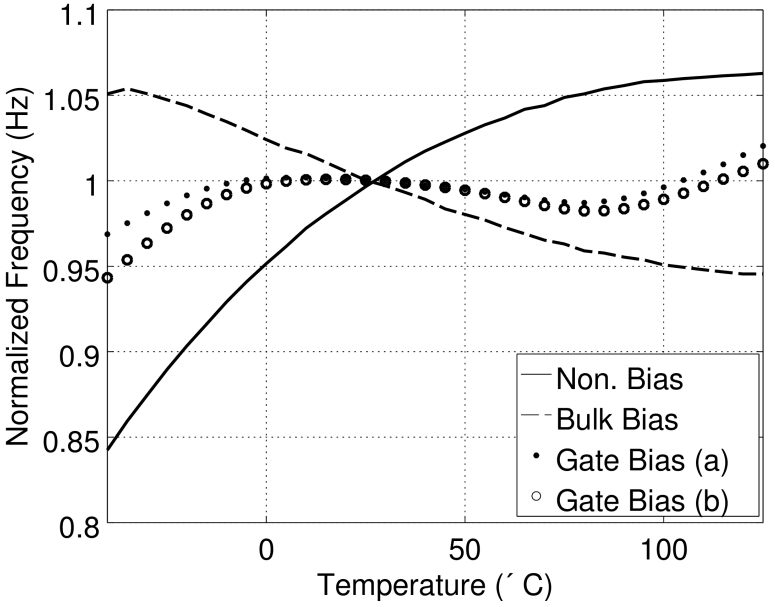
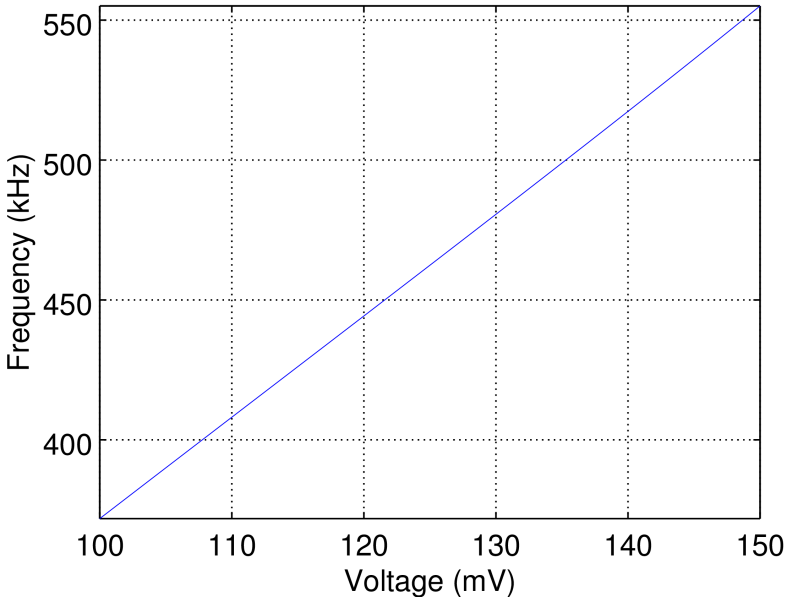


Table 6.2: Design Specifications

	Bulk Biased	Gate Biased (b)	[1]
Nominal supply (mV)	400	400	450
Supply range (mV)	300 / 500	300 / 500	400 / 1200
Nominal temperature (°C)	27	27	27
Temperature range (°C)	-40 / 125	-40 / 125	-55 / 125
Power consumption (μW)	8.66	9.13	0.08
Nominal frequency f_N (MHz)	19.67	2.354	0.087
Power efficiency (MHz/μW)	2.27	0.26	1.09
Supply stability (ppm/mV)	1025	103	1333
Temperature stability (ppm/°C)	657	404	277
Technology	IBM 130	IBM 130	UCM 130

[1] (AITA; CRUZ; BASHIRULLAH, 2015)

Figure 6.5: Voltage-to-frequency response



VCO

For proof of concept, the VCO proposed in this work was designed for a 130 nm IBM RF CMOS process. The circuit, operating with a supply voltage of 250 mV and a reference current I_{REF} of 320 nA, achieved a central frequency of 462.4 kHz and a total power consumption of 590 nW at typical process parameters and temperature of 27 ° C. Figure 6.5 shows the VCO voltage-to-frequency response, which demonstrate a frequency range from 370 to 555 kHz from an input range from 100 mV to 150 mV, which results in a voltage-to-frequency gain of 3.7 kHz/mV. Figure 6.6 shows the non linearity error of the normalized frequency-to-voltage function, which has a maximum absolute integral non linearity of 0.33%.

Figure 6.6: Integral Non Linearity Error

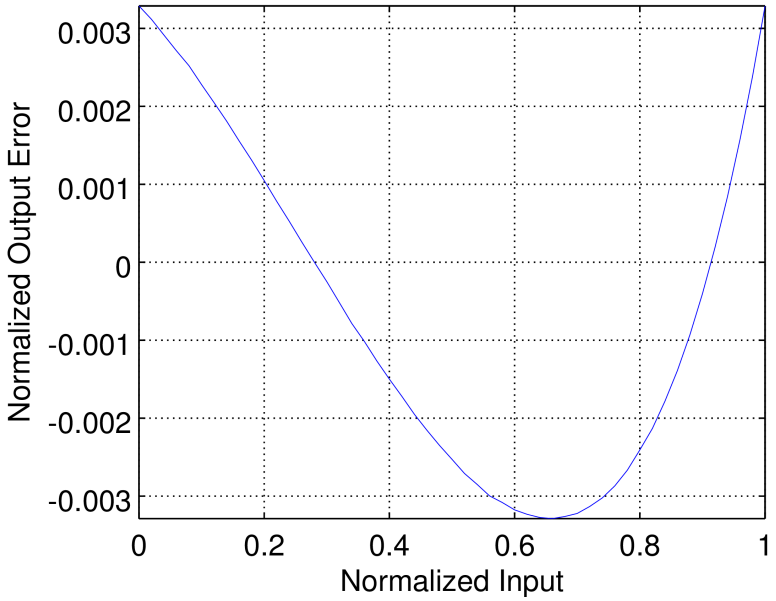
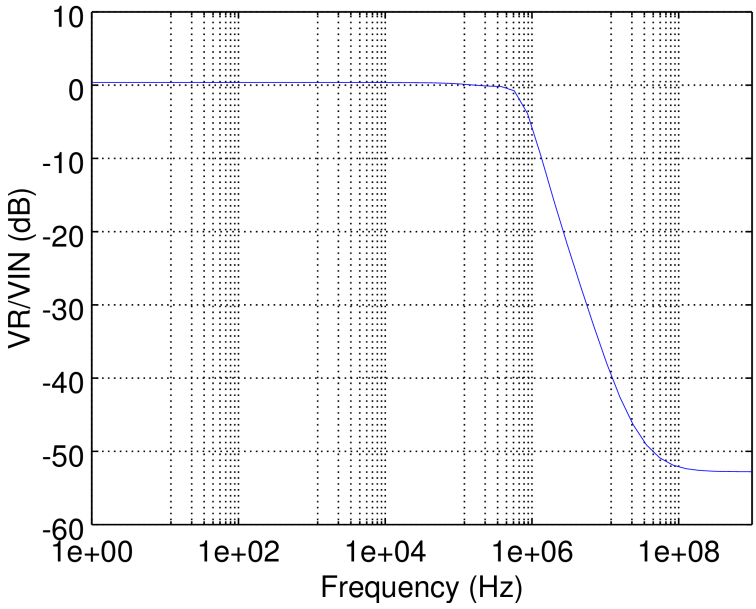


Figure 6.7: Loop AC response



The transconductor performance is limited by the ability of the feedback loop to make $V_R = V_{REF}$, which is limited by the loop gain and dynamic response. Figure 6.7 shows the dynamic response of the transconductor, which shows a dominant 3dB attenuation at the frequency of 825 kHz, which is higher than the maximum frequency in the input range of the VCO.

Figure 6.8 shows the results of a monte carlo simulation of the linearity of the transconductor, which suggests a 94% yield for a limit of 1% integral non linearity of the output current of the ring oscillator oscillator inverters.

Figure 6.8: DC response

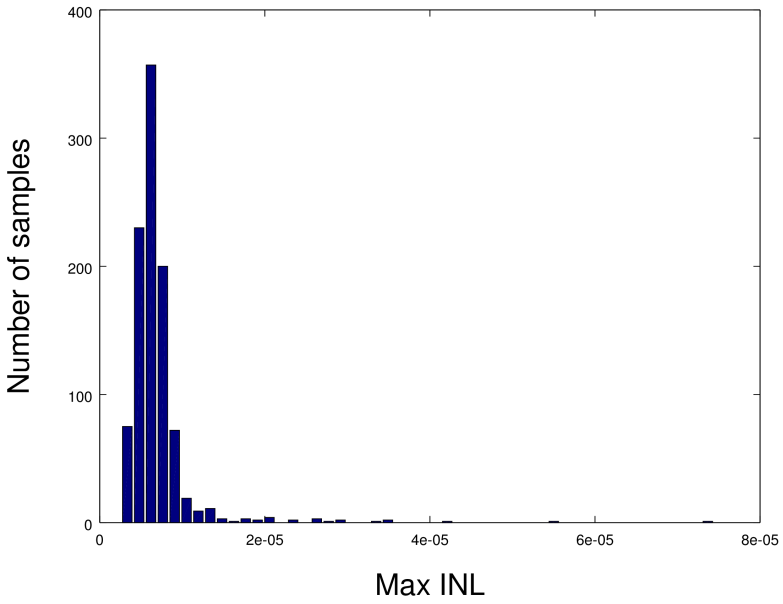


Figure 6.9: Frequency temperature stability

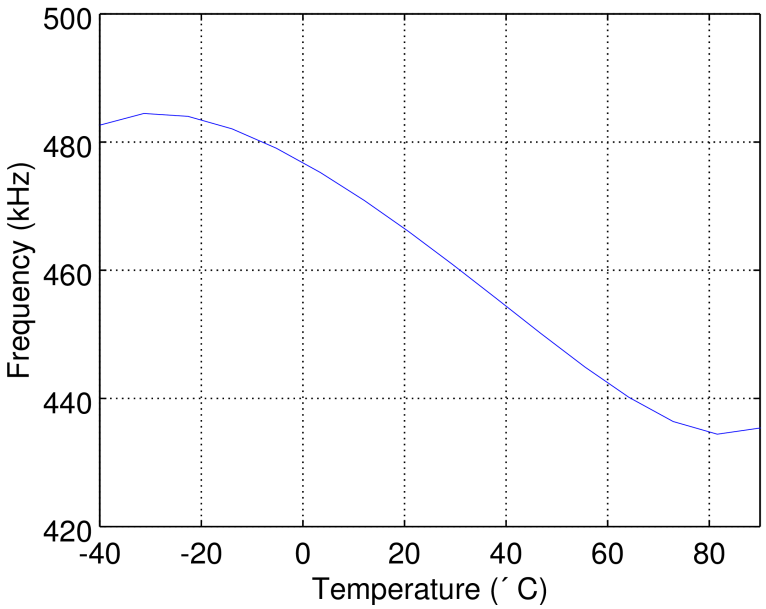


Figure 6.10 shows the results of a monte carlo simulation, which has a mean frequency of 462 kHz and a standard deviation of 20.7 kHz.

Sigma delta ADCs implemented with frequency-to-digital modulators, such as those proposed in (WISMAR; WISLAND; ANDREANI, 2006), shown in figure 6.11, when used in a open loop configuration, are strongly limited by the frequency range and maximum linearity. Using the simulated VCO specifications as parameters, a time-based ADC could achieve a 44 dB SNR for a 1.5 kHz signal bandwidth, which is equivalent to 7 ENOB after digital filtering. Figure 6.12 shows the designed FDSM output spectrum,

Figure 6.10: Central frequency - Monte carlo simulation

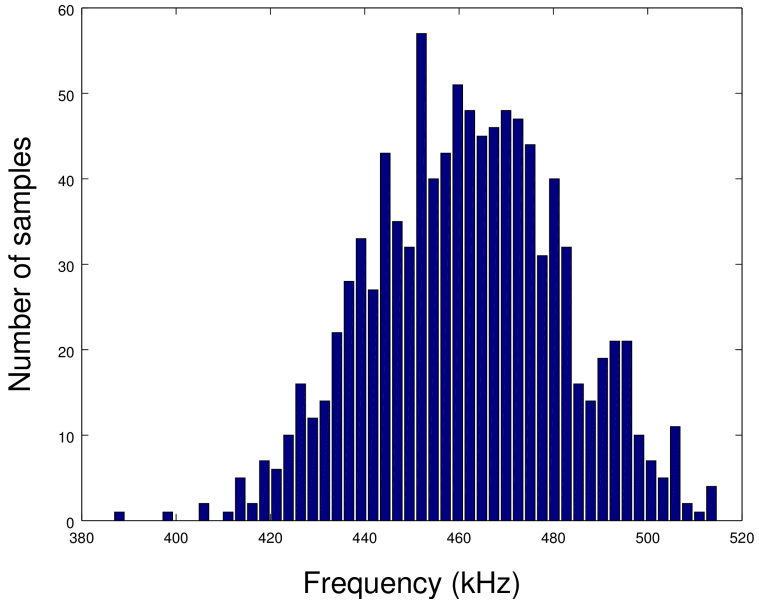
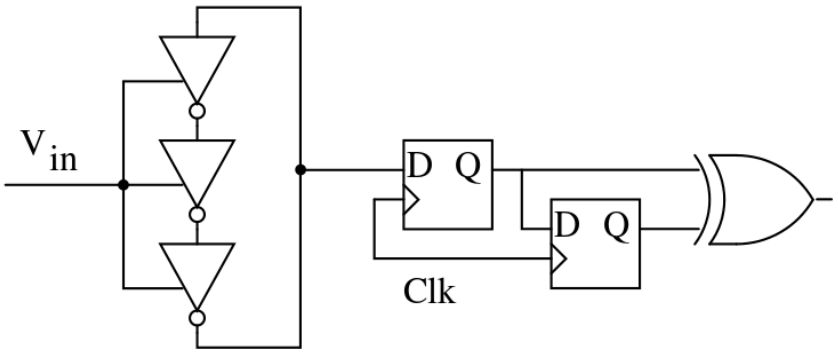


Figure 6.11: Frequency-to-Digital Sigma Delta Modulator



Source: (WISMAR; WISLAND; ANDREANI, 2006)

which clearly shows the second and third harmonics resulted from the VCO nonlinearity. Another limitation is the VCO temperature frequency stability, as shown in the figure 6.9, which can be avoided by having a reference frequency produced by a replica of the signal VCO with a constant voltage reference input.

Figure 6.12: FSDM output spectrum

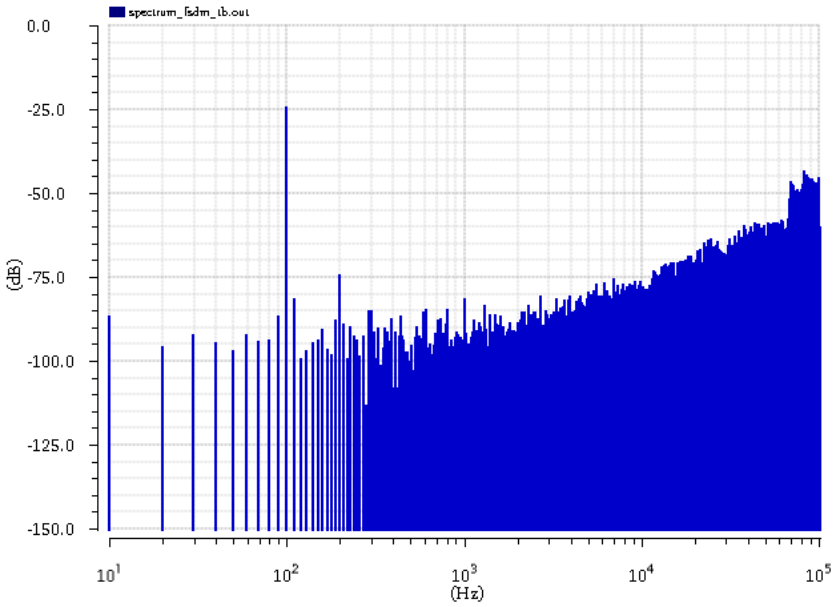


Table 6.3: VCO - Summary of simulated performance

Clock frequency (kHz)	370
Signal bandwidth (kHz)	1.5
SNR	44 dB
Supply voltage (mV)	250
Power consumption (uW)	590
Input range (mV)	100-150
Frequency range (kHz)	370-555
Maximum Non-linearity (%)	0.33
Technology	130 nm CMOS

7 CONCLUSION

As this work presents, forward body biasing is an oportunity for amplifier topologies with ultra low voltage supplies, as it enables the transistor bulk terminal for many additional functions. Pseudo differential pairs with only two stacked transistor are necessary to achieve better signal excursion for lower supply voltages, but the lack of current sources, as those found in common differential pairs, results in poor common mode rejection and no DC current biasing, a problem which must be addressed with additional circuits.

The amplifier topologies proposed in this work were intended to address the problems coming from the lack of a tail current source in pseudo differential pair. To address those problems were proposed additional circuits which employ forward body biasing. The externally biased topologies presented in this work use the bulk terminals for common mode rejection, output common mode definition and DC current biasing additionally bring robustness to process variability. The self biased topologies use the bulk terminals solely for common mode rejection without any additional circuits, therefore they are very power efficient.

Both self and externally biased amplifier topologies have their design uses. Unbiased topologies are better suited for signal processing applications where the filter cutoff frequency is defined by the feedback circuit, consequently, the operational amplifier voltage gain must be priorized in the design to reduce nonlinearity. For Gm-C based filters, externally biased topologies are better suited, since the transconductor, which defines the cutoff frequency with the capacitance, must be PVT tolerant and have calibration capabilities.

A ring oscillator which relies in forward body biasing was proposed in this work as an approach to increase robustness to PVT variations. To further decrease supply voltage, it was proposed a ring oscillator based in inverters with only two stacked transistors. The key inovation was to use the bulk terminals for the signal loop and the gate terminals for biasing, which results in a tradeoff between biasing range and power efficiency. The extra biasing range is useful for the design of reference oscillators, as stability is priorized at the expense of efficiency. For VCO designs, the extra biasing range increases the voltage input range, which is very important for the linearization technique that was also proposed in this work.

Ultra low voltage is a vanguard area of microelectronics and most commercialized

integrated circuits uses nominal supply voltages. In future works, we expect to use these novel amplifier and oscillator topologies in a wide range of integrated systems, which are more complex and closer to real world uses. Energy savings and process reliability made possible by ultra low voltage techniques could further enable promissing applications for several fields such energy harvesting, biomedical sensors and the Internet of Things.

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- RODOVALHO, FABRIS, KLIMACH. “Stable Ring Oscillator for Ultra Low Supply Voltages”. VII IEEE Latin American Symposium on Circuits and Systems.
- RODOVALHO, FABRIS, KLIMACH. “Ultra Low Voltage Supply VCO with Improved Linearity”. 2016 IEEE International Symposium on Circuits and Systems.

APPENDIX A — SUMMARY IN PORTUGUESE

Introdução

Com a invenção e popularização do transistor e circuitos integrados, uma nova era emergiu e desde então a Eletrônica seguiu uma tendência de miniaturização e produção em massa que trouxe processamento computacional uma vez exclusivo a grandes corporações para o bolso do cidadão ordinário. Os primeiros dispositivos eletrônicos móveis eram versões portáteis de equipamentos eletrônicos comuns. Exemplos comuns bem conhecidos são rádios e relógios portáteis. Com a evolução da tecnologia de circuitos integrados, a densidade de transistores cresceu exponencialmente e possibilitou a invenção de aplicações cada vez menores e mais complexas. Um dos pontos históricos mais recentes dessa evolução foi a popularização de comunicações sem fio, que começou com funcionalidades básicas como chamadas de voz e progressivamente adicionou mais funções como reprodução e gravação de áudio e vídeo e conectividade com a internet.

Um ponto negativo da rápida evolução de equipamentos eletrônicos em complexidade e miniaturização foi a lenta evolução de tecnologias de armazenamento de energia, um ponto crucial na eletrônica móvel, e é recentemente uma das maiores preocupações em projetos eletrônicos. Para solucionar a falta de energia armazenada disponível requerida por aplicações complexas e o desejo crescente por mais autonomia pelos consumidores, é altamente necessário projetar circuitos eletrônicos mais eficientes visando menos consumo de energia sem penalidades de performance consideráveis. Uma solução para esse problema é a diminuição da tensão de alimentação dos circuitos elétricos, que reduz a densidade de potência em resultado da crescente densidade de transistores nos circuitos integrados. Enquanto a tecnologia de semicondutores evolui, a tensão de alimentação tende a diminuir.

Algumas aplicações, como sensores biomédicos ou remotos, apesar de serem relevantes, não são tão comuns como comunicações sem fio, um dos principais alvos da maior parte da indústria eletrônica. Essas aplicações devem ser adaptadas para processos industriais não visadas por suas especificações, já que processos especiais são mais caros e, na maioria dos casos, não justificam a demanda, portanto não são práticas numa perspectiva comercial. Uma dessas adaptações para economizar energia em processos industriais comuns é a utilização de tensões de alimentação muito abaixo da tensão nominal.

A energia de dispositivos móveis pode ser provida por várias fontes como bate-

rias químicas portáteis ou pelo ambiente. Baterias tem capacidade de armazenamento limitada e devem ser substituídas ou recarregadas uma vez completamente descarregadas, enquanto *energy harvesting* converte energia do ambiente em energia elétrica desde que disponível, o que pode aumentar a autonomia do dispositivo. *Energy harvesting* geralmente disponibiliza uma tensão muito baixa que deve ser regulada para alimentar circuitos eletrônicos propriamente. Mesmo sendo possível disponibilizar tensões nominais de alimentação através da conversão DC-DC a partir de tensões de alimentação mais baixas, esta conversão perde eficiência de energia proporcionalmente ao fator de conversão de tensão, então, circuitos elétricos devem continuar funcionais com uma tensão de alimentação menor possível para economizar energia. Adicionalmente, a conversão de tensão é feita por circuitos elétricos e chaves que devem operar com as tensões de alimentação baixas originais nos primeiros estágios, o que é um desafio em si.

Circuitos integrados podem ser sistemas muito complexos, como processadores digitais com bilhões de transistores, or podem ser simples e ainda assim operar em condições extremas, como CIs militares, e a utilização de tensões de alimentação abaixo da nominal tem efeitos degradantes em muitas de suas características. Sistemas completos em um único CI contêm vários módulos, em ambos domínios digital e analógico, e cada um tem seus próprios desafios de projeto em relação ao uso de tensões de alimentação ultra baixa. O escopo dessa tesa foca no projeto de amplificadores, um bloco essencial no processamento de sinais analógicos e conversores analógicos-digitais.

Topologias de Amplificadores Pseudo Diferenciais e Polarização para ULV

Em razão de tensões de alimentação ultra baixas reduzirem a excursão de sinal de amplicadores, é necessário reduzir o número de transistores empilhados ao máximo. O par diferencial com carga ativa necessita de ao menos três transistores empilhados, por isso tensões ultra baixa utilizam pares pseudo diferenciais, que são semelhantes ao par diferencial, no entanto não possuem fonte de corrente e apresentam uma rejeição de modo comum pior.

Pares pseudo diferenciais geralmente são feitos a partir de amplificadores de fonte comum com carga ativa (figura 3.6a) . Uma alternativa ao uso de amplicadores de fonte comum e carga ativa é o uso do par *push-pull*, que apresenta maior ganho de tensão e transcondutância, no entanto necessita de circuitos adicionais para rejeição de modo comum e definição de tensão modo comum de saída.

Foi proposta uma alternativa ao par pseudo diferencial com carga espelhada que utiliza alimentação em avanço para aumentar a rejeição de modo comum e polarização externa da corrente DC do transcondutor (figura 3.8). Adicionalmente, foi proposto um par pseudo diferencial baseado no par *push-pull* que utiliza os terminais de corpo para espelhar a corrente do par pseudo diferencial (figura 3.6b).

O transcondutor proposto por Nauta baseado em pares *push-pull* utiliza realimentação negativa para rejeição de comum, no entanto não possui um sistema para polarizar externamente o modo comum de saída, uma vez que é auto-polarizado, portanto é intolerante à variações de processo. Para solucionar este problema, foram propostos circuitos de polarização de corrente e modo comum de saída utilizado o efeito de corpo dos transistores (figura 3.3).

Uma desvantagem do amplicador proposto por Nauta é a diminuição da resistência de saída e, consequentemente, de ganho de tensão acarretada pelo uso de pares *push-pull* em paralelo aos transcondutores do sinal de entrada. Para solucionar esse problema, foi proposta uma variante deste amplificador que utiliza os terminais de corpo para rejeição de modo comum (figura 3.7). Esta variante é mais eficiente e tem um ganho de tensão maior, no entanto apresenta uma rejeição de modo comum menor e é auto polarizada, sendo sujeita a variações de processo e temperatura. Outra topologia baseada nos pares *push-pull* foi proposta que emprega um circuito de alimentação em avanço para rejeição de modo comum e um circuito de polarização externo de corrente e modo comum de saída (figura 3.9).

Aplicações para a Estratégia de Polarização Proposta

O par *push-pull* pode ser utilizado na composição de um oscilador em anel. Osciladores em anel baseados no par *push-pull* podem ser externamente polarizados variando as tensões no terminal de fonte dos transistores, como na topologia *current starved* , no entanto isso exige o empilhamento de quatro transistores, que limita o uso de tensões ultra-baixas.

Uma alternativa para a polarização externa do oscilador em anel é a utilização do terminais de corpo dos transistores com polarização direta do substrato (DEEN; KAZEMEINI; NASEH, 2003). No entanto, o terminal de corpo tem um efeito pequeno no controle da frequência de oscilação em comparação com o terminal de porta. Portanto, foi proposto a utilização do terminal de porta para a polarização do oscilador e os terminais

de corpo para o circuito de realimentação (figura 5.3).

Para utilização do oscilador em anel proposto como oscilador de referência, foram utilizados os circuitos de polarização de corrente e modo comum de saída propostos anteriormente para as topologias de amplificadores (figura 5.4). A corrente de referência utiliza circuitos autopolarizados comuns (figuras 5.5 e 5.6) adaptados para o uso sob tensões de alimentação ultra baixas de forma que a corrente varie minimamente com a variação da tensão de alimentação. Adicionalmente, o coeficiente de temperatura da corrente de referência foi escolhido de forma que compense os efeitos da variação de temperatura na frequência de oscilação.

Para a utilização do oscilador em anel como oscilador controlado por tensão (VCO), foram utilizados os mesmos circuitos de polarização de corrente com a adição de um transcondutor para transformar a tensão de entrada numa corrente de polarização. O transcondutor proposto (figura 5.7a) utiliza uma técnica de linearização que se aproveita da linearidade intrínsica de um resistor como referência em um circuito de realimentação. A linearidade do VCO e a excursão de sinal de entrada são essenciais para se conseguir mais resolução em conversores analógico-digitais baseados em VCOs.

Conclusão

Como foi apresentado neste trabalho, polarização direta de substrato é uma oportunidade para topologias de amplificadores com tensões de alimentação ultra baixas. Pares pseudo diferenciais com apenas dois transistores empilhados são necessários para conseguir melhor excursão de sinal para tensões de alimentação mais baixas, entretanto a falta de fontes de corrente, como as encontradas em pares diferenciais, resulta em uma rejeição de modo comum baixa e falta de polarização de corrente DC, um problema que deve ser resolvido com circuitos adicionais.

As topologias de amplificadores propostas neste trabalho pretendem solucionar os problemas originados pela falta de fontes de corrente no par diferencial e para foram propostos circuitos adicionais que empregam polarização direta de corpo. As topologias externamente polarizadas propostas neste trabalho usam os terminais de corpo para rejeição de modo comum, definição de tensão de modo comum de saída e a polarização de corrente DC adicionalmente traz mais imunidade à variações de processo. As topologias auto-polarizadas usam os terminais de corpo apenas para rejeição de modo comum sem circuitos adicionais, portanto são muito eficientes no consumo de energia.

Ambas topologias de amplificadores auto e externamente polarizadas ten seus próprios casos de projeto. Topologias autopolarizadas são mais adequadas para aplicações de processamento de sinais onde a frequência de corte dos filtros são definidas pelo circuito de realimentação, consequentemente, o ganho de tensão do amplificador operacional deve ser priorizado no projeto para reduzir não linearidade. Para filtros do tipo Gm-C, topologias polarizadas externamente são mais adequadas, uma vez que o transcondutor, que define a frequência de corte juntamente com o capacitor, deve ser tolerante à variações de PVT (processo, tensão de alimentação e temperatura) e ter capacidade de calibração.

Um oscilador em anel que depende da polarização direta do corpo foi proposta neste trabalho como uma abordagem para aumentar a estabilidade em relação a variações PVT. Para diminuir a tensão de alimentação ainda mais, foi proposto um oscilador em anel com apenas dois transistores empilhados. A inovação principal foi usar os terminais de corpo para o laço de realimentação e os terminais de porta para polarização, o que resulta numa troca entre intervalo de polarização e eficiência energética. O alcance maior de polarização é útil para o projeto de osciladores de referência, já que a estabilidade é priorizada em detrimento da eficiência. Para projetos de osciladores controlados por tensão, o alcance maior de polarização aumenta a excusão de sinal de entrada, o que é muito importante para a técnica de linearização que também foi proposta neste trabalho.

Tensões de alimentações ultra baixa é uma área de pesquisa que se situa na vanguarda da microeletrônica e a maioria dos circuitos integrados usam tensões de alimentação nominais. Em trabalhos futuros, esperamos utilizar essas topologias inéditas de amplificadores e osciladores em uma vasta quantidade de sistemas integrados, que são mais complexos e mais próximos de casos de uso reais. A economia de energia e imunidade de processo possibilitadas por técnicas de tensão de alimentação ultra baixas podem tornar possíveis aplicações promissoras em áreas como *energy harvesting*, sensores biomédicas e Internet das Coisas.