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Bandgap Voltage References in submicrometer CMOS technology

Thesis presented in partial fulfillment of the requirements for the degree of Master in Microelectronics

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LIST OF SYMBOLS

V_{REF}	Voltage Reference
V_{G0}	Bandgap energy of silicon extrapolated for zero Kelvin
V_{BE}	Base-emitter voltage
ΔV_{BE}	The difference between the emitter-base voltages of two BJT´s
ΔV_{REF_TEMP}	Variation of the V_{REF} over the operation temperature range
V_{LSB}	Voltage that corresponds to 1 bit variation in Data Converter
V_{TH}	Thermal voltage
J_C	Collector current density
A	Geometric and fabrication process parameter
γ	Temperature coefficient
α	Temperature coefficient of the current source supplying the diodes
k	Boltzmann´s constant
q	Charge of electron
T	Absolute temperature
T_0	Room Temperature
β_F	Common-emitter current gain
I_C	Collector Current
I_B	Base Current
I_S	Saturation Current
n	Ratio of emitter areas
C	Temperature-independent constant
D	Temperature-independent constant
N	Temperature-independent constant
x	Arbitrary number defined by the temperature dependence of the current forced through the collector

V_{GS}	Gate-source voltage
I_{D0}	Process constant
n´	Subthreshold slope factor
W	Channel Width
L	Channel Length
V_{OV}	Overdrive Voltage
V_{OS}	Offset Voltage
V_T	Threshold Voltage
β_N	Negative feedback factor
β_P	Positive feedback factor
V_{PTAT}^2	Square proportional to the temperature voltage
I_{Supply}	Supply Current
VDD_{MIN}	Minimum supply voltage for one traditional BGR
ΔV_{REF}	Variation in V_{REF}
ΔV_{REF_TOTAL}	Total Variation in V_{REF}
ΔV_{REF_i}	Variation in V_{REF} due to each error source
$V_{REF\_MONTE\_CARLO}$	Output voltage from Monte Carlo Analysis
$\Delta V_{REF\_TEMP\_MONTE\_CARLO}$	Variation in V_{REF} over TEMP range from Monte Carlo Analysis
$V_{OS\_MONTE\_CARLO}$	Offset voltage from Monte Carlo Analysis
V_{REF_UPPER}	3σ behavior for the damaged output voltage
V_{REF_DOWN}	3σ behavior for the damaged output voltage
ΔV_{REF_NOISE}	Variation of output voltage due the noise
$V_{PEAK\text{-}TO\text{-}PEAK}$	3σ value of noise behavior
V_{RMS}	RMS noise
gm	Transconductance
N_{BITS}	Number of bits needed to trim the circuit
V_{FS}	Initial full-scale tolerance expected
V_{LSB}	Value of the least significant bit
$V_{Accuracy}$	The target accuracy (after trimming)
K_C	“Safety Factor” used to reduce the value of V_{LSB}
K_F	Device-specific noise constant

LIST OF ABREVIATIONS AND ACRONYMS

BGR	Bandgap voltage reference
BiCMOS	Bipolar Junction Transistor and CMOS technology
TC	Temperature coefficient
DTMOST	Dynamic-threshold voltage MOS transistor
PTAT	Proportional to absolute Temperature
$PTAT^2$	Square PTAT
CTAT	Complementary to Absolute Temperature
OA	Operational amplifier
VLSI	Very Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar junction transistor
IC	Integrated Circuit
PSR	Power Supply Rejection
PSRR	Power Supply Rejection Ratio
BW	Bandwidth
DRAM	Dynamic Random Access Memory
PLL	Phase Locked Loop
TSMC	Taiwan Semiconductor Manufacturing Company
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
VLSB	Least Significant Bit
VR	Voltage Reference
PLL	Phase Look Loop
TC	Temperature Coefficient
SNR	Signal-to-noise ratio
RMS	Root-mean-square
TEMP	Temperature

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ABSTRACT

A Voltage Reference is a pivotal block in several mixed-signal and radio-frequency applications, for instance, data converters, PLL´s and power converters. The most used CMOS implementation for voltage references is the Bandgap circuit due to its high-predictability, and low dependence of the supply voltage and temperature of operation.

This work studies the Bandgap Voltage References (BGR). The most relevant and the traditional topologies usually employed to implement Bandgap Voltage References are investigated, and the limitations of these architectures are discussed. A survey is also presented, discussing the most relevant issues and performance metrics for BGR, including, high-accuracy, low-voltage and low-power operation, as well as the output noise of Bandgap References fabricated in submicrometer technologies.

Moreover, a comprehensive investigation on the impact of fabrication process effects and noise on the reference voltage is presented. It is shown that output noise can limit the accuracy of the BGR and trim circuits.

To support and develop our work, three BGR´s were designed using the IBM 0.18 Micron 7RF process with a supply voltage of 1.8 V. The layouts of these circuits were also designed to provide post-extracted layout information and electrical simulation results. This work provides a comprehensive discussion on the structure and design practices for Bandgap References.

Keyworkds: Analog Design, CMOS, Voltage References, Bandgap References.

Referências de Tensão Bandgap em Tecnologias CMOS Submicrométricas

RESUMO

Referências de tensão são blocos fundamentais em uma série de aplicações de sinais mistos e de rádio frequência, como por exemplo, conversores de dados, PLL´s e conversores de potência. A implementação CMOS mais usada para referências de tensão é o circuito Bandgap devido sua alta previbilidade, e baixa dependência em relação à temperatura e tensão de alimentação.

Este trabalho estuda aplicação de Referência de Tensão Bandgap. O princípio, as topologias tradicionalmente usadas para implementar este método e as limitações que essas arquiteturas sofrem são investigadas. Será também apresentada uma pesquisa das questões recentes envolvendo alta precisão, operação com baixa tensão de alimentação e baixa potência, e ruído de saída para as referências Bandgap fabricadas em tecnologias submicrométricas.

Além disso, uma investigação abrangente do impacto causado pelo o processo da fabricação e do ruído no desempenho da referência é apresentada. Será mostrado que o ruído de saída pode limitar a precisão dos circuitos Bandgap e seus circuitos de ajuste.

Para desenvolver nosso trabalho, três Referências Bandgap foram projetadas utilizando o processo IBM 7RF 0.18 micra com uma tensão de alimentação de 1.8V. Também foram projetados os leiautes desses circuitos para prover informações pós-leiaute extraídos e resultados de simulação elétrica. Este trabalho provê uma discussão de algumas topologias e das práticas de projeto para referências Bandgap.

Palavras Chave: Projeto Analógico, CMOS, Referência de Tensão, Referência Bandgap

1 INTRODUCTION

A Voltage Reference (VR) is a circuit that provides stable and accurate output voltage. The term “Reference” is used to distinguish from “source”, since a source has less stability and accuracy. The stable voltage provided is used to bias others subcircuits to generate predictable and repeatable results. References are therefore an essential building block in the design of several applications; for example, voltage regulators, analog to digital (ADC), digital to analog converters (DAC), AC-DC converters, phase-locked Loop (PLL) and power converters. Figure 1 shows a typical example of one voltage-scaling DAC. Depending on the value of digital input word, the switches are configured in such way that a proper fraction of the voltage reference is connected to the output (Allen, 2004).

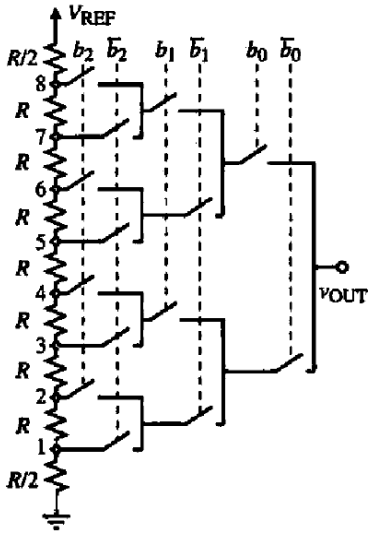

Figure 1.1: Voltage-Scale 3-bit DAC (Allen, 2004).

To illustrate the importance of a good voltage reference, consider the following example. A 10-bit ADC has a voltage reference (V_{REF}) tuned to 3.072 V at 25 °C. Once this reference is allowed to cause a maximum error of ± ½ V_{LSB} (voltage that corresponds to 1 least-significant-bit variation) over the temperature range of 0 to 50 °C, which is the maximum allowable temperature coefficient (TC) for the VR?

$$V_{LSB} \equiv \frac{V_{ref}}{2^N} = \frac{3.072}{2^{10}} = 0.003\,V$$

$$\frac{\Delta V_{REF}}{\Delta T} = \frac{V_{LSB}/2}{25°} = \frac{0.0015}{25°} = 60\mu V/°C$$

Accordingly, the VR for this application should vary at maximum 60μV/°C, otherwise the target DAC accuracy can not be met. A reference voltage variation of only 60μV/°C frequently can not be achieved by circuits without techniques of temperature compensation.

A reference circuit is designed to be independent of: supply voltage (VDD), temperature range of operation and fabrication process effects. Moreover, this circuit should have high accuracy, low output noise and present a long-term stability. The long-term stability is the capacity of the reference to present the same output voltage and performance over a long period of time. Finally, since today there is a large demand for battery-powered products and embedded systems, the recent voltage references also are required to present low-voltage and low-power operation (Ker, 2005).

In respect of the connected load, the voltage references usually are able to drive up to 100 μA (Rincon-Mora, 2002), more often less than this value. In case the load demands a higher current, it is necessary to use a buffer amplifier to isolate the reference from the load, and in this way, the high performance is guaranteed even if larger loads have to be driven.

In the past, many voltage references were designed to be off-chip. However, external circuits influence the signal integrity and increase the pin count of the system, what is a large disadvantage in the current scenario requiring high integration and low cost, where many times whole systems are fully integrated inside a single chip (Freitas, 2007). Thus, voltage references should present the features listed above and be compatible with integrated CMOS technology.

As some desired characteristics impose design decisions that are conflicting with other features, usually two important system trends can be distinguished when designing a voltage reference: i) targeting at low-power, or ii) targeting at high-performance (Annema, 1999).

Bandgap references (BGR) are one of the most popular implementation for voltage references. The origin of this technique was the work by Hilbiber (Hilbiber, 1964) and seven years later, Robert Widlar (Widlar, 1971) proposed the first integrated circuit implementation of the Bandgap concept.

This work presents a study of BGR design in CMOS technology. The Bandgap principle, the traditional topologies usually employed to implement this idea and the limitations of such architectures, especially if new fabrication processes are used, are addressed herein. The state of the art of the research underway in this area is also presented. Constraints and performance metrics including high-accuracy, low-voltage and low-power operation are discussed, and noise issues related to the Bandgap performance are also treated.

Special investigation on the impact of fabrication process effects on the Bandgap performance is presented. In addition, it is shown that the output noise can limit the performance of the BGR and the trim circuits.

To support and to develop our work, three BGR´s were designed using a submicrometer technology. The layouts of these circuits were also designed to provide post-extracted information. The fabrication process to be used is the IBM 0.18 Micron 7RF (accessible through the MOSIS service). This technology was chosen because it is

a standard CMOS fabrication process which has also capabilities for RF and mixed signal applications, and, moreover, the design kit for it was licensed by UFRGS University through the MOSIS silicon brokerage service. It has 6 metal layers and supports a nominal supply voltage of 1.8 volts. The Cadence CAD tools, including the SPECTRE simulator were used to design and simulate all circuits.

The text is organized as follows. Chapter 2 presents the BGR principle, an historical view of this voltage reference method and some usual definitions related to it.

In the Chapter 3, the three Bandgap voltage references designed are described in detail. The layout techniques applied to reduce the impact of fabrication process variations is also presented.

Chapter 4 presents some limitations inherent to the traditional topologies, mainly in designs requiring low-voltage and low-power operation. The state-of-art design techniques presented in the literature to overcome these restrictions are also presented. Moreover, variability caused by the fabrication process and the output noise are investigated.

The conclusions are presented in chapter 6. Appendix A presents the summary of this Master thesis in Portuguese. Appendix B and C show figures and the deduction of output voltage for the designed BGR3 circuit, respectively. In Annex A, examples of commercial Bandgap reference voltages and their performance parameters are presented. Annex B shows the model parameters of the technology used to design the circuits.

2 BANDGAP VOLTAGE REFERENCES

The Bandgap voltage reference is a technique that allows the generation of an output voltage with little dependence upon temperature and power supply. This reference was named “Bandgap” because its output voltage is close to 1.166 volts, which is the Bandgap energy per elementary electron charge in silicon, extrapolated to zero Kelvin (V_{G0}) (Allen, 2004).

Before to start explaining how this reference works, it is important to define the usual metrics used to characterize the performance of voltage references.

- Temperature drift: it is the variation of the reference voltage over the operation temperature range of the application. The typical metric used for these variations is the temperature coefficient (TC), and it is frequently expressed in parts-per-million per degree Celsius (ppm/°C). The TC is calculated by means of equation 2.1 (Rincon-Mora, 2002).

$$TC_{REF} = \frac{1}{V_{REF}} \cdot \frac{\partial V_{REF}}{\partial Temperature} \tag{2.1}$$

- Line regulation: it is the variation in V_{REF} caused by power supply variations. It is usually expressed in percentage.

- Load regulation: it is the variation in V_{REF} caused by the effects of loading the reference supply.

BGRs with different temperature coefficients can be implemented. Very different TC values are reported in the literature, as for instance 70 ppm/°C (Tzanateas, 1979) down to 3 ppm/°C (Yao, 2005) over a wide temperature range. There are many possible implementations for the BGR concept, where each one achieves a different accuracy. Often trade offs have to be met, as for instance, more accurate BGR’s often demand larger silicon area. Thus, it is the application who defines which BGR architecture should be used in each design. For many applications, such as an operational amplifier, a simple low-precision reference is fully adequated.

The small dependence of V_{REF} upon temperature is achieved through a balanced adding of two voltages with opposite temperature coefficient, as described by equation (2.2). If the constants $\alpha 1$ and $\alpha 2$ – both temperature-independent – are chosen in such way that equation (2.3) is satisfied, V_{REF} with zero TC at room temperature is achieved at some given temperature T where the equation 2.3 below applies.

$$V_{REF} = \alpha 1 \cdot V_1 + \alpha 2 \cdot V_2 \tag{2.2}$$

$$0 = \alpha 1 \cdot \frac{\partial V_1}{\partial T} + \alpha 2. \frac{\partial V_2}{\partial T} \tag{2.3}$$

Considering that V_1 increases with temperature, it is usually called Proportional to Absolute Temperature (PTAT) voltage. Then, V_2 decreases with temperature and is frequently called Complementary to Absolute Temperature (CTAT) voltage (Razavi, 2001). There are different ways to generate V_1 and V_2, and in the section 2.1 one of the most widespread methods is presented.

2.1 Generation of V_1 and V_2

The most prevalent technique in the literature to provide V_1 and V_2 is through the built-in voltage of a diode or the base-emitter voltage (V_{BE}) of a bipolar junction transistor (BJT). The widespread use of this technique is due to:

- High-stability against fabrication process effects (Widlar, 1971) with a predictability of about ± 2 to 5% (Rincon-Mora, 2002).
- Well characterized temperature dependence.

Equation 2.4 describes V_{BE} voltage and equation 2.5 describes its temperature drift. Table 2.1 presents all the parameters of equations 2.4 and 2.5. Assuming room temperature T_0 = 300 K and typical values for other parameters, TC calculated by equation 2.5 is about –1.5 mV/ºC. Since V_{BE} voltage decreases with temperature, it is a CTAT voltage.

$$V_{BE} = V_{TH} \cdot \ln\left(\frac{J_C}{A \cdot T^{\gamma}}\right) + V_{G0} \tag{2.4}$$

$$\frac{\partial V_{BE}}{\partial T}\Big|_{T=T0} = \frac{V_{BE} - V_{G0}}{T_0} + (\alpha - \gamma) \cdot \left(\frac{k}{q}\right) \tag{2.5}$$

The thermal voltage (V_{TH}), in table 2.1, is described by equation 2.6 (Razavi, 2001).

$$V_{TH} = \frac{k \cdot T}{q} \tag{2.6}$$

Table 2.1: Parameters of equations 2.4 and 2.5 (Allen, 2004)

Parameter	Description	Typical value	Unit
V_{BE}	Base-emitter voltage	0.7	V
V_{G0}	Bandgap energy of silicon extrapolated to zero Kelvin	1.166	V
V_{TH}	Thermal voltage	-	V
J_C	Collector current density	-	A/m^2
A	Geometric and fabrication process parameter		
γ	Temperature coefficient	3.2	-
α	Temperature coefficient of the current source supplying the diodes	1	-
k	Boltzmann´s constant	$1.38x10^{-23}$	J/K
q	Charge of electron	$1.6x10^{-19}$	C
T	Absolute temperature	-	K
T_0	Room temperature	-	K

Unfortunately typical BJTs with optimized device structure are not available in standard CMOS processes and therefore these transistors must be built through parasitic devices. In general, there are two parasitic BJTs in CMOS process: vertical and lateral BJTs. The cross-section of (a) vertical PNP transistor and (b) lateral PNP transistor in CMOS p-substrate process can be seen in figure 2.1. The shaded area in the figure represents the flow of charge carriers, hence the electrical current lines.

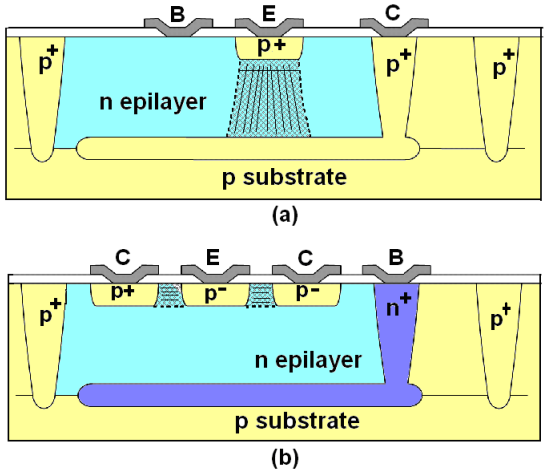

Figure 2.1: Cross-section of (a) vertical (b) lateral PNP BJT in CMOS technology

As can be seen in figure 2.1 (a), the vertical BJT is built with a drain diffusion, n-well and p-substrate, that act respectively as emitter, base and collector. Once the substrate (collector) is always connected to the most negative supply voltage, the use of vertical devices is limited for certain applications where the grounded collector is

admissible. For circuits where it is necessary to control the voltage at the collector terminal, lateral PNP BJT is recommended.

However, parasitic devices present some disadvantages if compared to standard transistors. Due to the large base size, parasitic BJTs present a large base resistance and a high rate of recombination – which leads to a small value for the common-emitter current gain (β_F). Such effects lead to a more difficult matching and a large possibility of latchup. But, if good layout techniques are applied in the design, these disadvantages can be significally reduced - what explains the large use of parasitic BJTs in BGR designs (Vermaas, 1998), (Cajueiro, 2002) and (Leung, 2004). Equation 2.7 describes beta gain and table 2.2 shows its parameters.

$$\beta_F = \frac{I_C}{I_B} \tag{2.7}$$

Table 2.2: Parameters of equations 2.7 and 2.8

Parameter	Description	Unit
β_F	Common-emitter current gain	-
I_C	Collector Current	A
I_B	Base Current	A
I_S	Saturation current	A
J_C	Collector current density	A/m^2
n	Ratio of emitter areas	-

Up to this point, the reasons why the V_{BE} voltage has been vastly used as CTAT voltage have been discussed. But, how will the PTAT voltage needed to achieve the compensation proposed by equation 2.3 be generated?

The PTAT voltage can be obtained through the Thermal voltage. Equation 2.8 describes the temperature dependence of V_{TH} voltage, and its value is +0.087 mV/ºC. (Razavi, 2001).

$$\frac{\partial V_{TH}}{\partial T} = \frac{V_{TH}}{T} \tag{2.8}$$

One way to generate the thermal voltage is from the difference between the emitter-base voltages (ΔV_{BE}) of two bipolar transistors. If these two devices differ only by their emitter area and are operated at the same I_C and temperature, the ΔV_{BE} is given by equation 2.9 (Razavi, 2001).The parameters of 2.9 are also given by table 2.2.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_{TH} \cdot \ln\frac{J_{C1}}{J_{C2}} = V_{TH} \cdot \ln\left(\frac{I_{C1} \cdot I_{S2}}{I_{S1} \cdot I_{C2}}\right) = V_{TH} \cdot \ln(n) \tag{2.9}$$

Figure 2.2 shows one possible scheme to generate the ΔV_{BE} voltage. If the voltages V_{O1} and V_{O2} are forced to be equal, using for example cascode devices, ΔV_{BE} voltage appears across the resistor R.

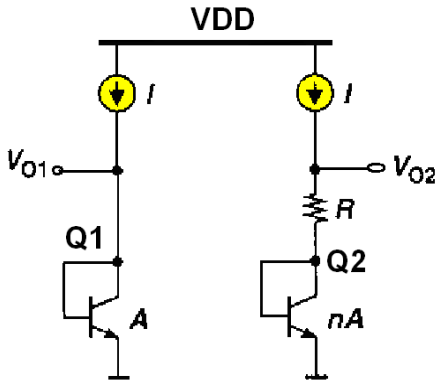

Figure 2.2: Generation of V_{TH} using two BJT´s with different areas

In summary, following the concept expressed by equation 2.2, it is possible to generate a PTAT voltage (V_1) and a CTAT voltage (V_2) by means of V_{TH} and V_{BE} voltage using standard CMOS processes with parasitic BJTs. Section 2.2 presents the achieved output voltage when V_1 and V_2 are summed to produce the reference.

2.2 Output voltage

Substituting V_{BE} and V_{TH} voltages in equation 2.2 and making $\alpha 2$ equal to 1, the output voltage obtained is described by equation 2.10. Then, it is possible to design $\alpha 1$ in such way that the output voltage shows zero temperature drift at room temperature.

$$V_{REF} = V_{BE} + \alpha 1 \cdot V_{TH} \tag{2.10}$$

After choosing a proper value for $\alpha 1$, one can prove that the value of V_{REF} at room temperature is given by 2.11, where V_{T0} is the thermal voltage at room temperature and the parameters α and γ are given by table 2.1. Details of this deduction are presented in (Allen, 2004). Considering T_0 = 300 K and typical values for other constants, V_{REF} has a value around 1.262 V, what is few milivolts higher than V_{G0} - explaining the reason for the name “Bandgap voltage reference”.

$$V_{REF}\big|_{T=T0} = V_{GO} + V_{T0}(\gamma - \alpha) \tag{2.11}$$

Althought the negative TC of V_{BE} is cancelled by the positive TC of V_{TH} near the room temperature; the obtained V_{REF} still has temperature dependence of the order of 20 to 100 ppm/ºC. One of the major reasons for this behavior is better explained through equations 2.12 and 2.13, which describe the temperature dependence of V_{BE} voltage (Tsividis, 1980). Equation 2.13 is the Taylor series expansion of equation 2.12. Table 2.3 explains all parameters of these equations.

$$V_{BE} = V_{G0} + V_{TH} \cdot \ln\left(\frac{D}{C}\right) - \left[(4 - N) - x\right] \cdot V_{TH} \cdot \ln T \tag{2.12}$$

$$V_{BE} = a_0 + a_1 T + a_2 T^2 + \ldots + a_n T^n \tag{2.13}$$

Table 2.3: Parameters of equations 2.12 and 2.13

Parameter	Description	Unit
V_{BE}	Base-emitter voltage	V
V_{G0}	Bandgap energy of silicon extrapolated to zero Kelvin	V
V_{TH}	Thermal voltage	V
C	Temperature-independent constant – comes from the saturation current.	-
D	Temperature-independent constant – comes from the collector current.	-
N	Temperature-independent constant – comes from average mobility for minority carriers in the base	-
x	Arbitrary number defined by the temperature dependence of the current forced through the collector, i.e., x is 1 to a PTAT current.	-
T	Absolute Temperature	K
a_0, a_1, .. a_n	Constants of theTaylor series expansion	-

As can be verified through equation 2.12, the V_{BE} voltage is not exactly complementary to the absolute temperature; it has a non-linearity described by the multiplication of the temperature by the logarithm of temperature. Equation 2.13 provides another way to see this non-linearity through the Taylor expansion of 2.12.

When the sum of V_{BE} and V_{TH} (Linear term) is evaluated, only the linear part of V_{BE} voltage is offset. The term T*ln(T) is not compensated, what explains the remaining temperature-dependence of the output voltage even after the sum. Figure 2.3 represents graphically the topics discussed in the last two paragraphs.

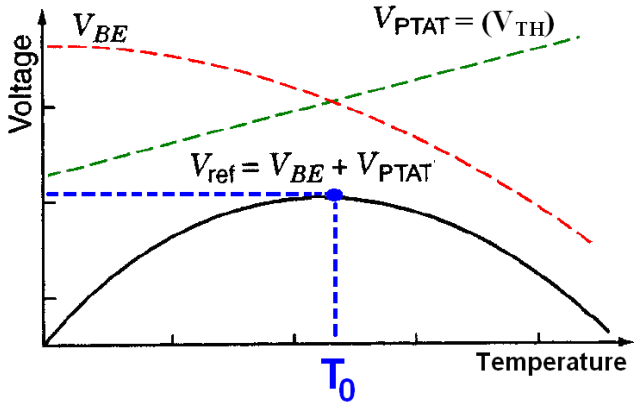

Figure 2.3: Typical Curvature of first-order V_{REF} over temperature range

From figure 2.3, it is possible to add some observations:

• The maximum value of V_{REF} is at room temperature, that is, the point where the derivation of the output voltage in relation to temperature assumes the value described by equation 2.11. At room temperature, the term V_{BE} is exactly equal to the V_{TH}.

• For temperatures below T_0, the non-linear term of V_{BE} is small and therefore, it is the V_{TH} term that dominates the behavior – V_{REF} increases with temperature.

• For temperatures above T_0, the non-linear term of V_{BE} increases faster, in such a way that it dominates the behavior - V_{REF} decreases with temperature.

In this section, the output voltage generated through the Bandgap concept and the performance achieved were discussed. For many applications the achieved performance of 20 to 100 ppm/ºC is fully enough, and because of this reason, BGR circuits became maybe the most widespread technique to provide voltage references. Section 2.3 shows a historical view about this technique.

2.3 Historical View

In the 60´s, one of the most used voltage references was the Zener diode. The extensive use of this technique was due to its good performance, such as 10 to 50 ppm/°C over moderate temperature ranges. However, the high value of the breakdown voltage, the noise performance, the poor long-term stability and its variability due the fabrication process of this device, lead to a search for alternative solutions for voltage references.

The Bandgap principle was proposed by Hilbeber (1964), but was only in Widlar (1971) that the first integrated regulator using a Bandgap Voltage Reference was presented. Figure 2.4 presents the simple form of this reference.

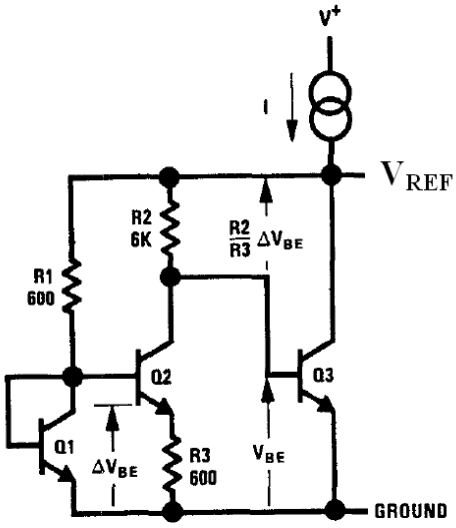

Figure 2.4: Integrated voltage reference proposed by (Widlar, 1971)

The proposed Bandgap reference using bipolar technology works as explained in sections 2.1 and 2.2, generating an output voltage of 1.205 V. In this circuit, Q1 is operated with a current density 10 times larger than Q2 and consequently, the ΔV_{BE} voltage appears across R3. Using transistors with high-gain, the voltage across R2 will also be proportional to the ΔV_{BE} voltage. Thus, using transistor Q3, the output voltage is forced to be equal to V_{BE3} plus a constant multiplied by the ΔV_{BE} voltage, as suggested by equation 2.10. More specifically, the output voltage is given by 2.14, where the aspect ratio of resistors R2 and R3 will define the temperature compensation.

$$V_{REF} = V_{BE\_Q3} + \frac{R2}{R3} \cdot V_{TH} \cdot \ln(10) \quad (2.14)$$

The good performance and the viability offered by the BGR technique resulted in a large use of this method and the emergence of different implementations, each one suitable for a different application.

In Tzanateas (1979) one of first implementations of CMOS Bandgap reference is proposed. Using a standard process with MOS transistors operating in the weak inversion region and one parasitic BJT, a BGR that achieved 70 ppm/°C of temperature performance was designed. The MOS transistors operating in weak inversion were used to build the thermal voltage, instead of using the ΔV_{BE} of two BJTs. Please note that the behavior of MOS transistors operating in weak inversion (subthreshold) is similar to the behavior of BJT´s, where the current has an exponential relationship with the control voltage. The drain current of the MOSFET in subthreshold operation is roughly described by equation 2.15 (Allen, 2004). Table 2.4 explains the parameters of this equation.

$$I_D \cong \frac{W}{L} \cdot I_{D0} \cdot \exp\left(\frac{V_{GS}}{n' V_{TH}}\right) \quad (2.15)$$

Table 2.4: Parameters of equation 2.15

Parameter	Description	Unit
V_{GS}	Gate-source voltage	V
I_{D0}	Process Constant. It also depends of V_{SB} (Source-Bulk voltage) and V_T (threshold voltage)	A
n´	Subthreshold slope factor	-
W	Channel Width	μm
L	Channel Length	μm

Due to the need of more precise voltage references, in the years 1980´s works emerged that investigated techniques to reduce the non-linearity of Bandgap reference and thus, achieve greater temperature-performance.

In Tsividis (1980) a carefully investigation about the temperature effects in I_C-V_{BE} characteristics with application to BGR´s was presented. It was shown that the main cause of disagreement between the theoretical equation for $V_{BE}(T)$ (base-emitter voltage in function of temperature) and the measured data, is due to the wrong assumption that the silicon Bandgap voltage varies linearly with the temperature. This wrong supposition led to errors in predicting the output voltage of BGRs. The temperature-dependence of V_{BE} was discussed in detail, and some suggestions to improve the accuracy achieved by the Bandgap references were presented. The equation for $V_{BE}(T)$ presented in that work is equation 2.13, presented in section 2.2.

As already discussed in section 2.2, Tsividis clarified the need to thermally cancel not only the first term, but also the high-order terms of equation 2.13 to allow a better temperature performance. This work was the base for high-accuracy Bandgap designs.

One of the suggestions of Tsividis was implemented by (PALMER, 1981). This work proposed a Curvature-Corrected Bandgap reference that implements the thermal compensation of the nonlinearity of V_{BE} by means of the inclusion of another non-linear with opposite temperature coefficient. For one output voltage of 5 V, it was possible to achieve only ±0.02% of variation over temperature range from -55 to 125°C.

Nicollini (1991) proposed a switched-capacitor fully differential Bandgap reference suitable for applications that require good PSRR, for instance, telephony and audio processing systems. Making use of standard CMOS process, a fully differential approach and without the need of any trimming in mass production, it was possible to achieve a typical performance of 15.2 ppm/°C and about 90 dB up to 500 kHz of power supply rejection.

Nowadays, the traditional high-accuracy BGR´s is not enough anymore to satisfy the requirement of the current electronic applications. Due the increasing demand for low-power portable equipments, low-voltage and low-power operation becomes essential for any analog block. In Malcovati (2001), a Curvature-Compensated BiCMOS Bandgap with 1-V Supply voltage was proposed. This circuit has an output voltage of 0.54 V, 7.5 ppm/°C of temperature performance and only 92μW of power consumption at room temperature. One disadvantage of this technique is the need of a 0.8-μm BiCMOS process to permit low-voltage operation of the operational amplifier used in this design – what increases the cost of fabrication.

Another method to reduce the supply voltage was present in Kim (2008). With a hybrid design, discrete Ge (Germanium) diodes - whose Bandgap voltage is only 0.6 V - and a silicon chip connected through one printed circuit board, it was possible to achieve an output voltage reference of 310 mV with a 302 ppm/°C TC at 1V of supply voltage. Nevertheless the use of discrete diodes is not compatible with the need for fully integration demanded by recent applications.

In summary, more than forty years have passed since the Bandgap technique was first proposed, and today it is a commercial reference used in the design of a large number of applications. Moreover, this technique is still the subject of many research works, where the current focus is to adapt the BGR method to design in submicrometer technologies. We finish this section with table 2.5 showing a comparison of the BGRs discussed. In Colombo (2008) is also presented a wide comparison between different Bandgap Circuits. Annex A presents a table with a few examples of commercial BGR chips and its performance parameters.

Table 2.5: Summary of the BGR´s discussed in this section

Work	Temp. Performance (ppm/°C)	VDD (V)	Power Consumption (μW)	Process
WIDLAR, 1971	≈ 30	5	-	Bipolar
TZANATEAS, 1979	70	3.5	10	CMOS
PALMER, 1981	≈ 3	10	2000	Bipolar
NICOLLINI, 1991	15.2	± 5	4800	CMOS
MALCOVATI, 2001	7.5	1	92	BiCMOS
KIM, 2008	302	1	-	Hybrid

3 BANDGAP VOLTAGE REFERENCES DESIGNED

After understanding the Bandgap idea and its origins, this chapter supports and develops our study presenting three BGR´s designed using IBM 0.18 Micron 7RF technology. The IBM technology is a standard CMOS process that presents a vertical BJT´s and its parameters are shown in Annex B

The types of the implemented BGRs were chosen because their topologies are the basis for the more complex Bandgap architectures, and then, comprehending its principles it is possible to understand the issues involving any BGR. Furthermore, to have a more comprehensive study of the impact of noise and the variability, we have opted to choose three circuits with different performance.

All Voltage References were designed to operate in the temperature range of -55 to 125°C, and with a supply voltage variation of 1.7 to 1.9 V. The order which these circuits are here presented is related to their achieved performance.

3.1 BGR1

Every BGR presents a balanced sum of two voltages with opposite temperature coefficient to achieve a good temperature performance. As already explained, the most common voltages used in this addition are the V_{BE} and V_{TH} produced by means of parasitic BJT´s. The first Bandgap Reference (BGR1) implements this concept through the architecture depicted in figure 3.1.

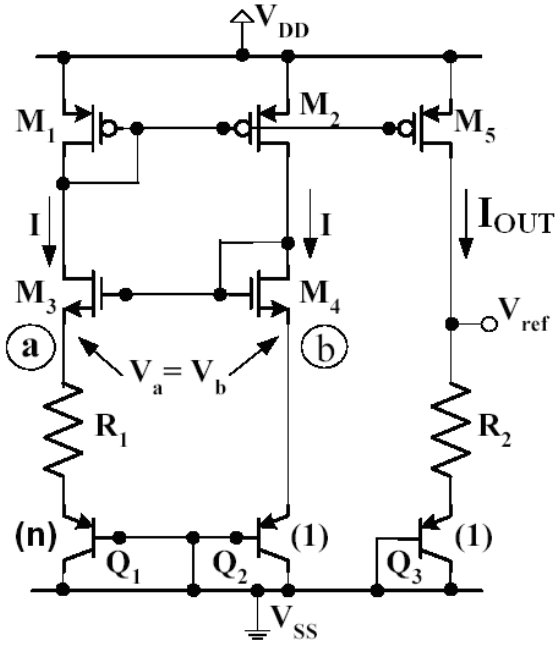

Figure 3.1: BGR1

This circuit is a well-know BGR topology (Gray, 2001) that achieves good performance with a very simple structure. The reference uses a "bootstrapped" current mirror to reduce the power supply dependency. The transistors M_3 and M_4 force nodes A and B to be of equal voltage, and once the Q_1 area is n times bigger than Q_2, a PTAT voltage appears across R_1. Equation 3.1 describes the current flowing through R_1.

$$I = \frac{\Delta V_{BE}}{R_1} = \frac{V_{TH} \cdot \ln(n)}{R_1} \tag{3.1}$$

The bulk of the NMOS and PMOS devices are respectively connected to VSS and VDD. Transistors M_1 and M_2 have the same dimensions and the output current I_{OUT} is given by equation (3.2).

$$I_{OUT} = \left(\frac{(W/L)_5}{(W/L)_1} \right) \cdot I \tag{3.2}$$

Thus, the output voltage is described by equation (3.3). Observe that 3.3 has the same form of equation 2.10, where $\alpha 1$ (adjust factor) is given by (3.4). Remember now that the TC of V_{BE} voltage and the V_{TH} are respectively, roughly -1.5 mV/°C and exactly +0.087 mV/ºC. Accordingly, the adequate value for $\alpha 1$ is about 17, for the voltage reference to achieve the temperature compensation. The exact value of $\alpha 1$ depends on several variables, but mainly on the bias point, the type of the BJT (typical, vertical or lateral), the TC of the resistors and the room temperature T_0.

$$V_{REF} = V_{BE3} + \left(\frac{(W/L)_5}{(W/L)_2} \right) \cdot \frac{R2}{R1} \cdot \ln(n) \cdot V_T \tag{3.3}$$

$$\alpha 1 = \left(\frac{(W/L)_5}{(W/L)_2} \right) \cdot \frac{R2}{R1} \cdot \ln(n) \tag{3.4}$$

In general, the curve of V_{REF} is designed to flatten to a zero-derivative at the room temperature, but this is not a requirement. However, considering that this assumption is true, there will be different values of $\alpha 1$ for each specific T_0. Figure 3.2 shows each curve (for different $\alpha 1$ values) for three different room temperatures. Note that the point where each curve flattens to zero is labeled as T_0.

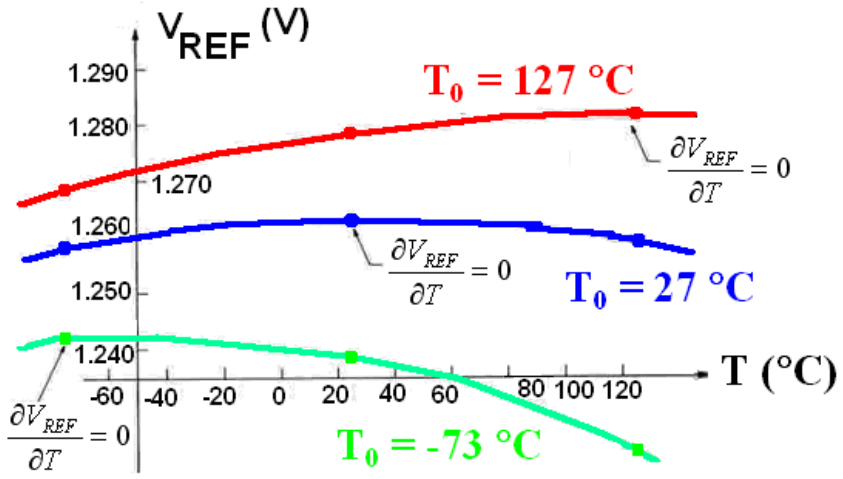

Figure 3.2: V_{REF} as a function of temperature and different value of T_0

Section 3.1.1 presents details about the implementation, such as transistors size and design decisions focusing on good performance. Section 3.1.2 shows the startup circuit. The layout of this circuit is presented in section 3.1.3 and we finish with the post-layout simulation results in section 3.1.4.

3.1.1 Implementation Details

Here a series of decisions taken into account in our design are presented:

(a) The channel length modulation negatively impacts the output performance, and hence should be reduced. Thus large transistor channel lengths were used in the design.

(b) The overdrive voltage (V_{OV}) was assumed to be between 150 and 200 mV, and consequently, the weak inversion operation was avoided and more voltage headroom was provided.

(c) Current I described by equation 3.1 was defined based on the tradeoff between minimization of resistors area, minimization of consumed power and the matching between the bipolar transistors. Figure C.1, in Appendix C, shows that the β_F of the vertical BJT is very small and depends on the bias collector current – which is not good for matching. However, it is reported in Vermaas (1998) that the best choice for matching is to bias the bipolar device in such way that the β_F is large and constant. Hence, in our design, the emitter current was chosen to achieve a large and constant value for β_F.

(d) The room temperature was defined to be in the middle of the temperature range (35°C). This helps to reduce the output variation over the whole temperature range.

(e) To reduce the mismatching due the fabrication process and the flicker noise generated by MOSFET´s, these devices were designed to have a large area. Chapter 4 discusses the variability and the output noise of BGR´s.

(f) To allow a good layout matching between the bipolar transistors, Q_1 was designed to be 8 times larger than Q_2. Values larger that 8 are not adequate, as the separation of the devices increases and more errors are introduced. Moreover, a large area will be spend with a little increment in the ln(n) function – equation 3.1

(g) To allow a good layout matching between the resistors, they were designed to have the same size, then enabling a common centroid configuration.

(h) The type of resistors was chosen based on their TC´s, resistivity and the matching properties. The temperature dependence of the resistor influences the reference performance. More specifically, it was shown in Falconi (2005) that appropriate choice of the resistor material can significally reduces the non-linearity of the output reference and then, achieves a better temperature performance. For the task of choosing the resistor material, analog simulation is fundamental. Figure C.2, in Appendix C, shows an illustration of the output curvature for different resistors with different TC´s. In our case, P^+ Poly silicon resistor presents the best tradeoff between resistivity, matching properties and non-linearity reduction. This resistor presents a TC equal to 160 ppm/°C (IBM, 2005).

Following all decisions listed above, the transistors in the circuit were sized. Table 3.1 shows the final size of transistors, the value of the resistors and the aspect area ratio of the BJT´s. The dimensions used in the layout are also shown.

Table 3.1: Size of transistors and value of the resistor of BGR1

Device	Design Dimensions	Layout Dimensions	Units
$M_{1,2}$	$\frac{W}{L}=\frac{97.52}{5}$	$8\times\left(\frac{12.19}{5}\right)$	$\frac{\mu m}{\mu m}$
$M_{3,4}$	$\frac{W}{L}=\frac{70}{7}$	$4\times\left(\frac{17.5}{7}\right)$	$\frac{\mu m}{\mu m}$
M_5	$\frac{W}{L}=\frac{354}{3}$	$40\times\left(\frac{8.85}{3}\right)$	$\frac{\mu m}{\mu m}$
$R_{1,2}$	3	3×1	$K\Omega$
Q_1	$8\times A2$	$8\times A2$	-
Q_2	A2	A2	-

3.1.2 Startup-Circuit

One point that should be carefully analyzed in the BGR design is the operation point stability. The BGR1 circuit presents two possible points of operation: the first one

showing the biasing current equal to zero, and the second one showing the current equal to the value described by equation 3.1. Therefore, it is necessary to use a start-up circuit to force the correct operation point. Figure 3.3 shows the start-up circuit inserted in the BGR circuit – this circuit is very similar to the one present in Brito (2007).

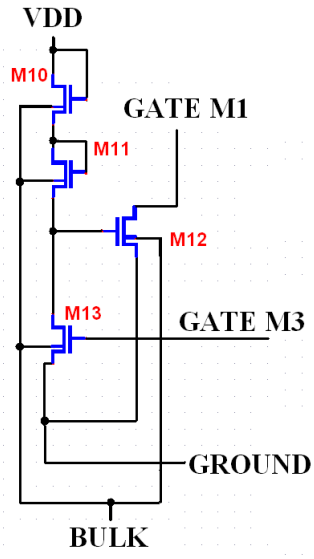

Figure 3.3: Start-up Circuit of BGR1

The Start-up circuit works as follows. Suppose the circuit with the biasing current equal to zero even if the VDD voltage is applied – the wrong operation point. Thus, it is possible that the gate of transistor M_1 is at a high voltage that causes a V_{SG_M1} less than V_T (Threshold Voltage), making current conduction impossible. Without current, the BJT´s are not in forward operation and probably the gate of M_3 has low value in such way that V_{GS_M3} is less than V_T. In such a situation, device M_{13} of the start-up circuit is cut-off and M_{12} enters in conduction, since its gate is connected to VDD – Devices M_{10} and M_{11} are always in conduction. Thus, the gate of M_1 is connected to ground, forcing V_{SG_M1} to be greater than V_T and putting the BGR circuit to its corrected operating point.

With the reference in operation, the gate M_3 is above threshold, which makes M_{13} to enter in conduction. Accordingly, the gate of M_{12} is connected to ground, which leads to its cut-off – disconnecting the start-up circuit from the Bandgap Reference. This disconnection is important to avoid that the start-up circuit affects the performance of the voltage reference.

Two observations about the size of start-up devices are done here. Since the transistors M_{10} and M_{11} are always conducting, they were design with larger channel lengths to increase the resistance – what leads to less power consumption of this auxiliary circuit. Devices M_{12} and M_{12} were designed with the minimum channel length to provide a low-resistance path to the ground and make the start-up procedure faster. Table 3.2 shows the devices sizes and start-up time of this auxiliary circuit.

Table 3.2: Size of devices in Start-up circuit of BGR1

Devices	Design Dimensions	Layout Dimensions	Units
M10, 11	$\frac{W}{L}=\frac{1}{15}$	$\frac{W}{L}=\frac{1}{15}$	$\frac{\mu m}{\mu m}$
M12, 13	$\frac{W}{L}=\frac{0.40}{0.18}$	$\frac{W}{L}=\frac{0.40}{0.18}$	$\frac{\mu m}{\mu m}$

Figure 3.4 shows the importance of this auxiliary circuit in case of operation at the wrong point. Two BGR´s circuits were simulated, one with and another one without the startup circuit in a forced wrong operation point. The circuit with start-up enters in stable conduction after about 2.7 µs while the other circuit remains in cut-off. In fact, it is well known that fabricated circuits will hardly remain in the wrong operation point, due the noise and the existing fabrication mismatches. However, the time of the start-up procedure can be large for many applications and then, the auxiliary circuit provides a faster operation.

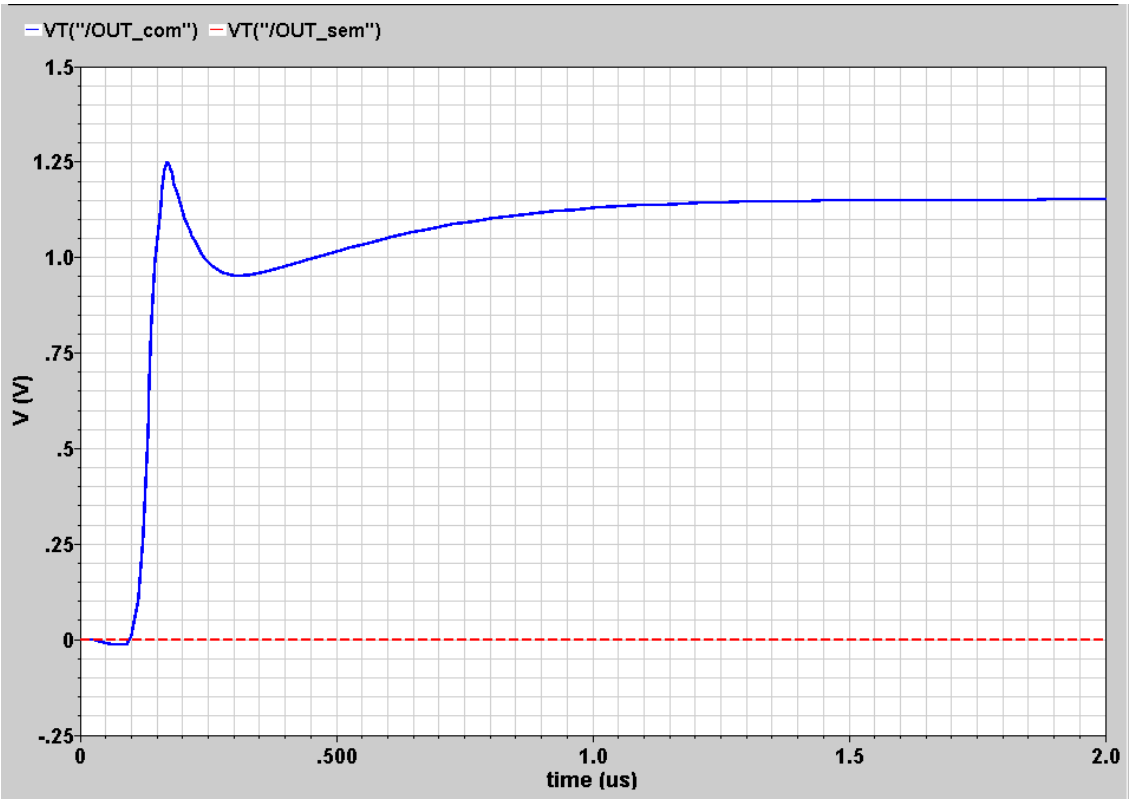

Figure 3.4: Start-up Time of BGR1 with and without (Dotted Line) start circuit

3.1.3 Layout of BGR1

Figure 3.5 shows the layout of the BGR1. The total used area is less than 123 x 89 μm^2. The layout of the PNP vertical BJT is provided by the foundry and it can not be changed. Good layout techniques such as common centroid configuration and dummy

devices were used to allow a good matching between the MOSFET´s, BJT´s and resistors. Appendix B shows more details about the applied layout techniques.

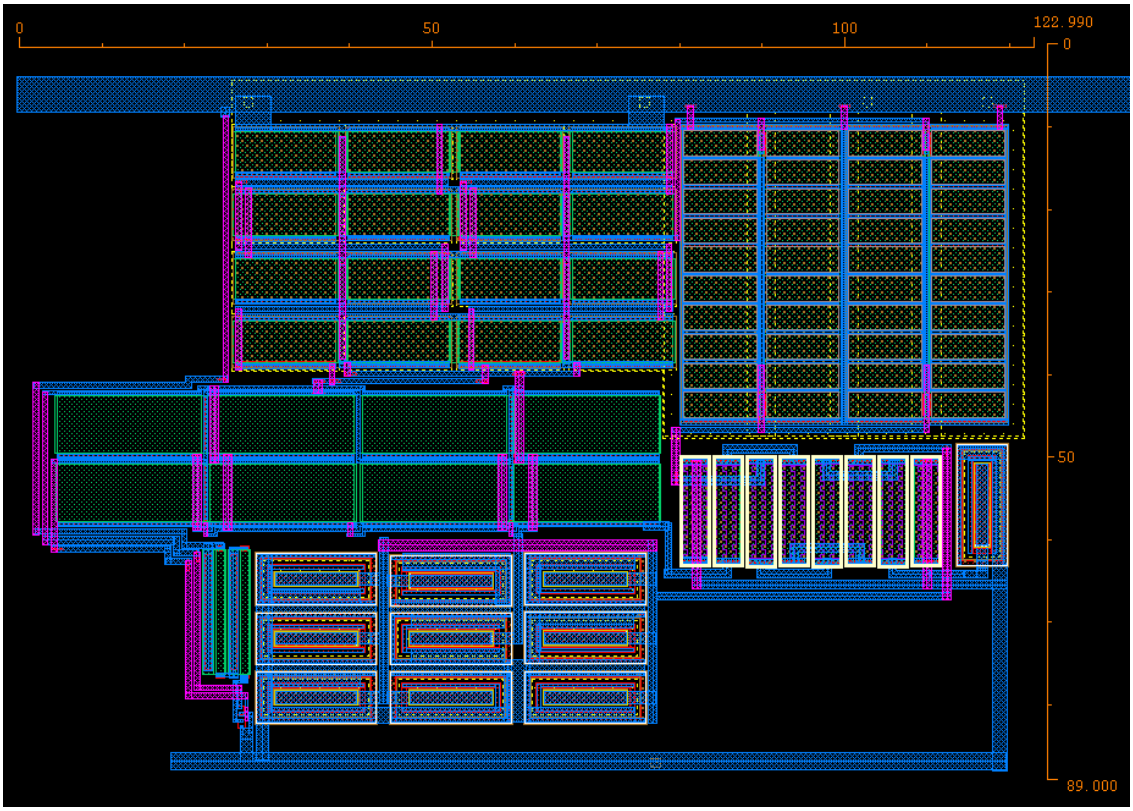

Figure 3.5: Layout of BGR1

3.1.4 Post-Layout Simulation results

After concluding the layout, the extraction of the circuit parasitics was performed. Afterwards, the circuits were simulated to verify the temperature performance, line regulation, power consumption and the power supply rejection. Table 3.3 shows the results obtained.

Table 3.3: Post-Layout Simulation Results of BGR1

Parameter	Value	Unit
V_{REF} @ 27 °C	1.152	V
ΔV_{REF_TEMP}	3 (26 ppm/ °C)	mV
Temp. Range	-55 to 125	°C
Line Regulation (VDD: 1.7 – 1.9)	7 (35 mV/V)	mV
VDD	1.8	V
I_{Supply}	147.4	µA
PSR @ 1 kHz	29	dB

Figures 3.6-3.8 show respectively, the V_{REF} as a function of temperature, the line regulation performance and the power supply rejection.

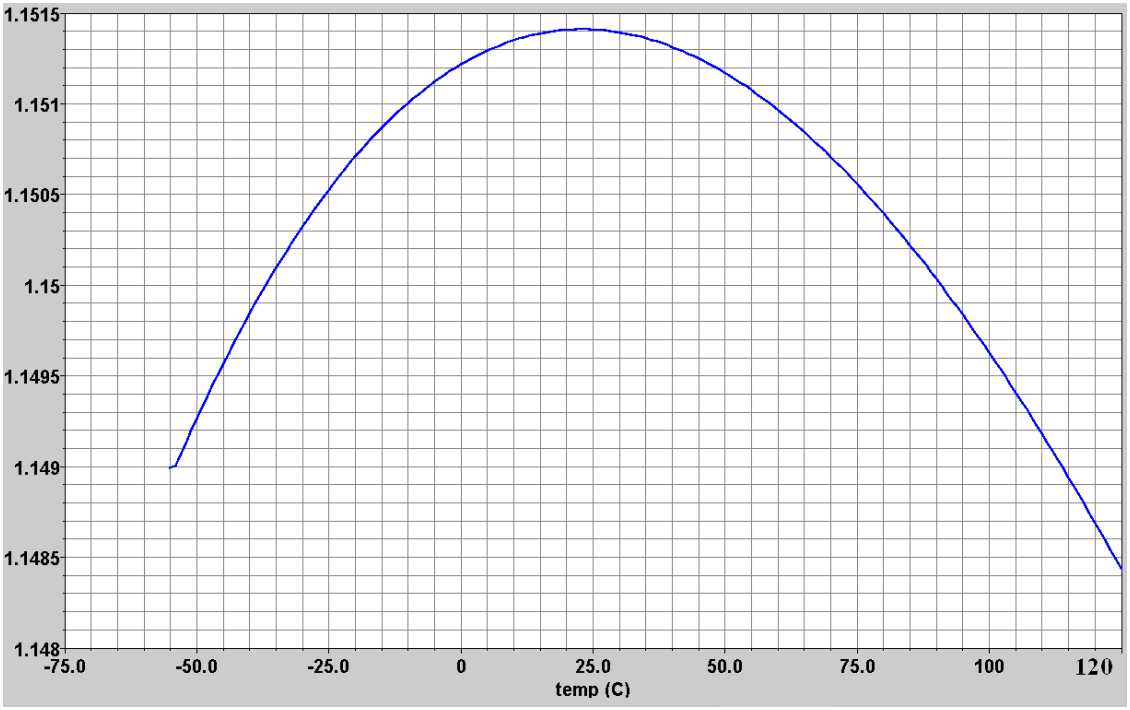

Figure 3.6: V_{REF} as a function of temperature of BGR1

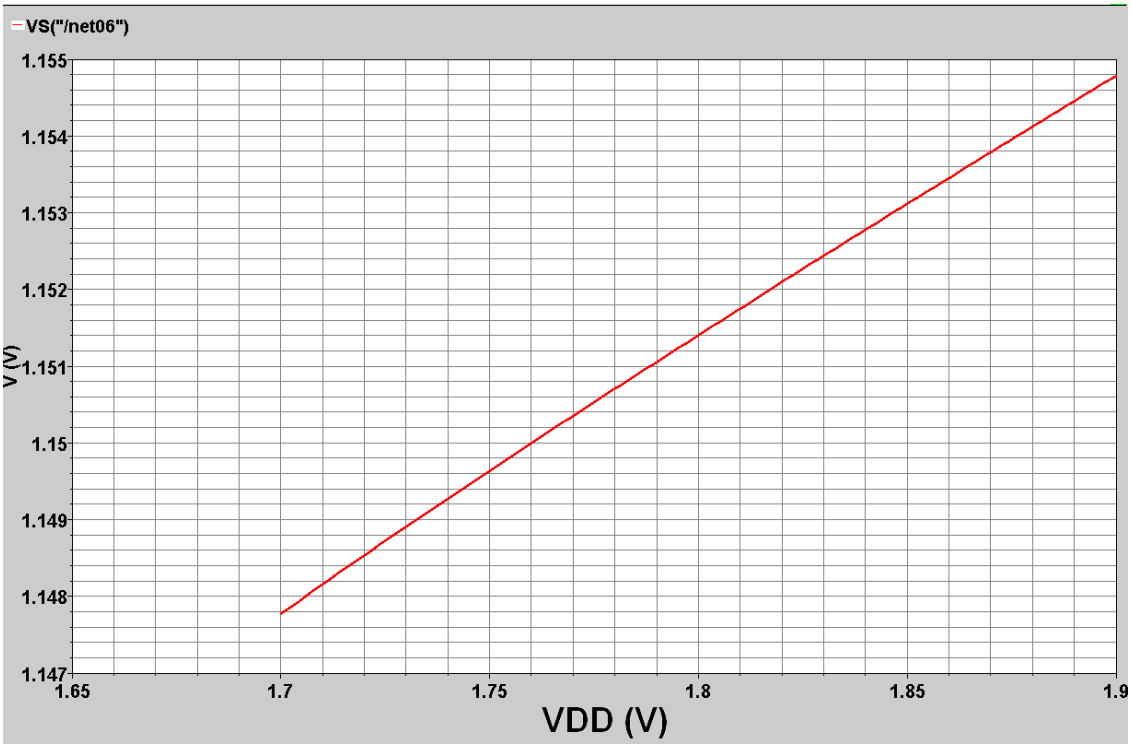

Figure 3.7: Line Regulation for BGR1 (1.7 – 1.9V)

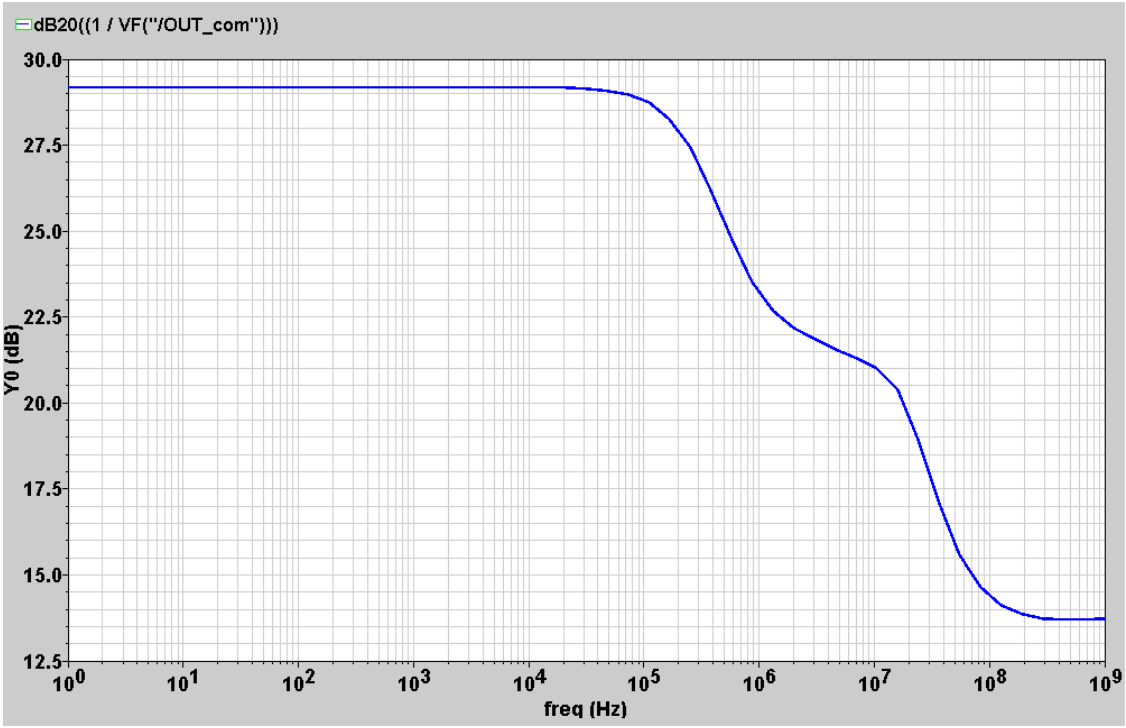

Figure 3.8: PSR of BGR1

The obtained TC of 25 ppm/ºC is in close agreement to the first order Bandgap voltage references; in Annema (1999) it is reported that output voltage variation in the temperature range of - 40 to 120 ºC is around 4 mV.

As can be seen in table 3.3 the worst performance parameter is the line regulation, with a value equal to 7 mV for a variation of the supply voltage equal to ± 100mV. This data shows that the current mirror and the voltage-clamping composed by M1-M5 are not effective at different supply voltages. One reason for the large output variation is the channel length modulation. The values of channel length used in the current source transistors are already big, and then increasing these values will not contribute in a significant way to reduce the channel length modulation. One way to reduce the supply voltage dependence would be the insertion of cascode devices in the current mirror, increasing the output resistance. However, the low-supply voltage of 1.8 V makes device cascoding impossible. One alternative to favour the insertion of cascode devices is to use triple-well NMOS devices (IBM, 2005). Through these devices, it is possible to reduce the bulk-effects and provide a better use of the voltage headroom. This solution frequently requires extra-fabrication steps, which would lead to increased cost.

Besides the high-VDD dependence, this architecture achieves a poor power supply rejection rate of 29 dB at low-frequency. The next topology to be studied, BGR2, is less sensitive to VDD and presents a better PSR.

3.2 BGR2

The second implemented Bandgap Voltage Reference (BGR2) was proposed initially in Gregorian (1981). This popular topology achieves the same temperature coefficient as BGR1, however, using an error-amplifier-based current mirror it is possible to obtain a better line regulation performance. Figure 3.9 shows the BGR2 architecture.

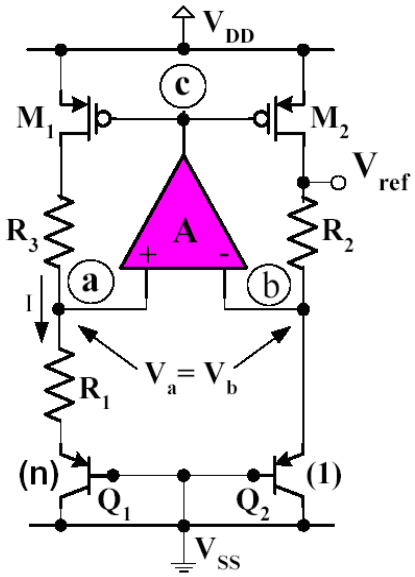

Figure 3.9: BGR2 using error-amplifier-base current mirror

Using an error-amplifier with a high voltage gain A, it is possible to get equal voltages at the nodes A and B, since the negative feedback is provided. The negative feedback is guaranteed because the negative feedback factor β_N is greater than the positive feed factor β_P.

The resistors R_2 and R_3 are designed to be matched, what leads to $V_{DS1} = V_{DS2}$ for the matched devices M_1 and M_2. As a consequence, the BJT´s are supplied by equal currents given by equation 3.5

$$I = \frac{\Delta V_{BE}}{R_1} = \frac{V_{TH} \cdot \ln(n)}{R_1} \tag{3.5}$$

If we consider that the Offset voltage (V_{OS}) of the amplifier is zero, V_{REF} is described by equation (3.6). Observe again that 3.6 also has the form of equation 2.10, where the adjust factor ($\alpha 1$) is given by (3.7). Therefore, the resistor aspect ratio and the bipolar areas should be designed to achieve $\alpha 1$ roughly equal to 17.

$$V_{REF} = V_{BE2} + \left(\frac{R_2}{R_1}\right) \cdot \ln(n) \cdot V_T \tag{3.6}$$

$$\alpha 1 = \left(\frac{R2}{R1}\right) \cdot \ln(n) \tag{3.7}$$

Section 3.2.1 shows details about the implementation such as, transistors size and design decisions focusing in good performance. Section 3.2.2 shows the startup circuit. The layout of this circuit is presented in section 3.2.3 and we finish with the post-layout simulation results in section 3.2.4.

3.2.1 Implementation Details

Alls decisions taken into account in the design of BGR1 were also considered in the design of BGR2. Moreover, other issues were investigated, for instance, the architecture of the error-amplifiers.

In the literature, several types of topologies are used to implement the “error amplifier”. In Kourdounas (2007) and Xing (2007) Operational Transconductance Amplifier (OTA) with 2-stages were used. In Leung (2004) and Tom (2004) a simple differential pair is used to implement this function. In addition, Mok (2004) defends the use of the simplest architecture due to its reduced offset and the easy matching that this topology achieves. In summary, the architecture choice depends on the constrains of the system for which the reference is intended, such as area occupied, accuracy, low-voltage and low-power operation. However, regardless of the architecture used, it must provide high gain. The errors in the PTAT voltage generation are inversely proportional to the gain. Frequently, open loop gains higher than 60 dB are used in this design. Another issue that must be carefully analyzed is the stability of the error-amplifier, and in this case, it is often necessary to use compensation to avoid instability.

In our case, considering that the gain can be reduced after fabrication, we decided to design an amplifier with more than 70 dB of gain and a phase margin greater than 45°. A Compensated OTA with two stages was chosen to implement the error amplifier. Figure 3.10 illustrates the op-amp circuit and the supply independent current source used to bias it. Figure C.3, in appendix C, shows the Bode diagram of the OP-AMP. To ensure that the bias circuit does not become instable, transistor M_{21} is designed with a width 3 times larger than that of M_{20} (Sedra, 1997).

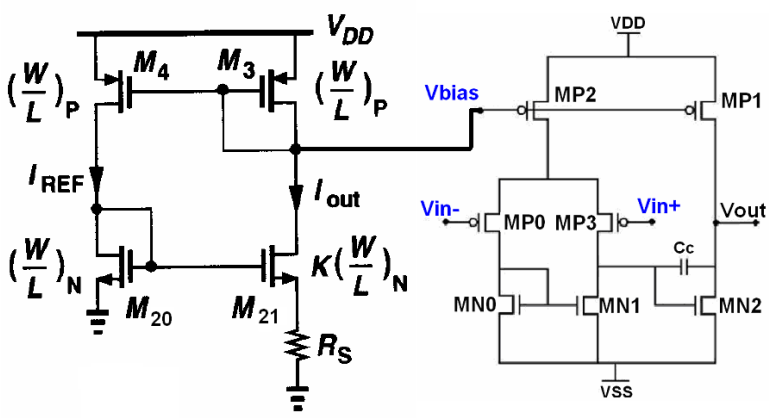

Figure 3.10: OTA with 2-stages and its bias circuit

Table 3.4 shows the simulation results for the amplifier and table 3.5 shows the final size of transistors, the value of the resistors and the aspect area ratio of the BJT´s. The dimensions used in the layout are also shown.

Table 3.4: Simulated results for the error-amplifier

	Value	Unit
Open-loop gain	74	dB
Phase Margin	50	°
Bandwidth	13	MHz

Table 3.5: Size of transistors and value of the resistor of BGR2

Device	Design Dimensions	Layout Dimensions	Units
OP-AMP			
M_{P2}	$\frac{W}{L}=\frac{11.25}{1.5}$	$5\times\left(\frac{2.25}{1.5}\right)$	$\frac{\mu m}{\mu m}$
M_{P1}	$\frac{W}{L}=\frac{174.2}{2}$	$20\times\left(\frac{8.71}{2}\right)$	$\frac{\mu m}{\mu m}$
$M_{P0,\ P3}$	$\frac{W}{L}=\frac{11.6}{1.5}$	$8\times\left(\frac{1.45}{1.5}\right)$	$\frac{\mu m}{\mu m}$
$M_{NO,N1}$	$\frac{W}{L}=\frac{1.6}{4}$	$4\times\left(\frac{0.4}{1.5}\right)$	$\frac{\mu m}{\mu m}$
M_{N2}	$\frac{W}{L}=\frac{37.4}{4}$	$\frac{37.4}{4}$	$\frac{\mu m}{\mu m}$
C_C	500f	500f	F
Independent-Supply Voltage Current Source			
$M_{3,4}$	$\frac{W}{L}=\frac{30}{2}$	$4\times\left(\frac{7.5}{2}\right)$	$\frac{\mu m}{\mu m}$
M_{20}	$\frac{W}{L}=\frac{5}{5}$	$\frac{5}{5}$	$\frac{\mu m}{\mu m}$
M_{21}	$\frac{W}{L}=\frac{15}{5}$	$\frac{15}{5}$	$\frac{\mu m}{\mu m}$
R_S	7.4	6×1.2332	$K\Omega$
Other Devices			
Q1	$8\times A2$	$8\times A2$	-
Q2	A2	A2	-
$R_{2,3}$	7.5	4×1.875	$K\Omega$
R_1	1.1	2×0.550	$K\Omega$
$M_{1,2}$	$\frac{W}{L}=\frac{38}{2}$	$4\times\left(\frac{9.5}{2}\right)$	$\frac{\mu m}{\mu m}$

3.2.2 Start-up Circuit

The BGR2 also requires a start-up circuit to avoid the wrong operation point. This auxiliary circuit is the same used in BGR2 and the connections are shown in figure 3.11.

The analysis is similar to that presented for BGR1 and the start-up procedure was simulated, as shown in figure 3.12, The reference with the start-up circuit entered in operation after 5 miliseconds, while the circuit without start-up started conduction after 15 milisenconds. The large time of start-up indicates that the size of M_{12} transistor should be increased to permit a greater driving current.

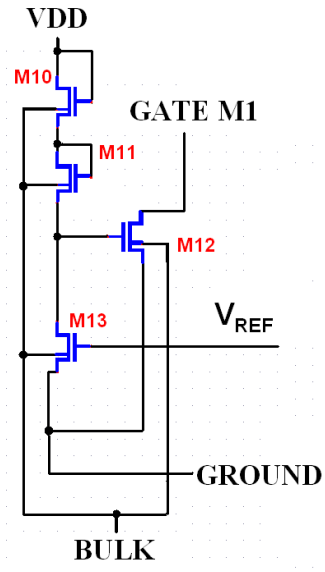

Figure 3.11: Start-up circuit used in BGR2

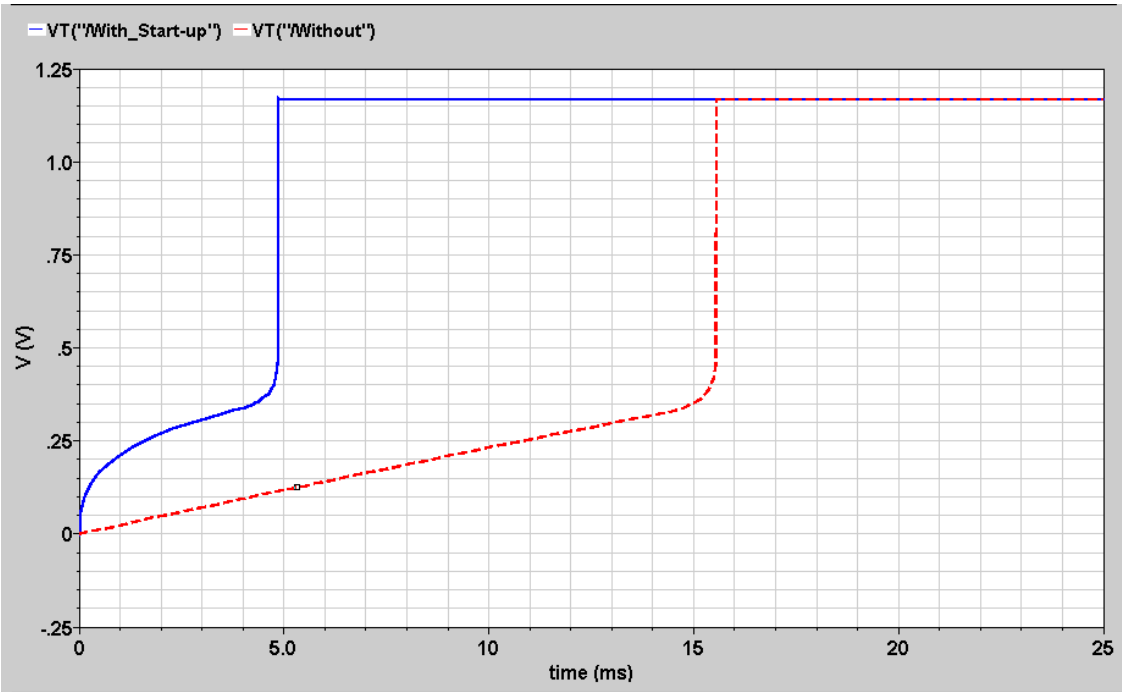

Figure 3.12: Start-up time of BGR2 with and without (dot line) start-circuit

3.2.3 Layout of BGR2

Figure 3.13 shows the layout of BGR2. The layout was done manually and the total area used is less than 63 x 150 μm^2, which is almost the same size of BGR1. Good layout techniques were also applied in this design. Figure 3.14 shows the layout of the

operational amplifier and its current source in detail. One can see that the bias circuit has approximately the same size of the error-amplifier due to the large size of the resistors. The compensation capacitor is implemented with Metal-Insulator-Metal (MIM) material.

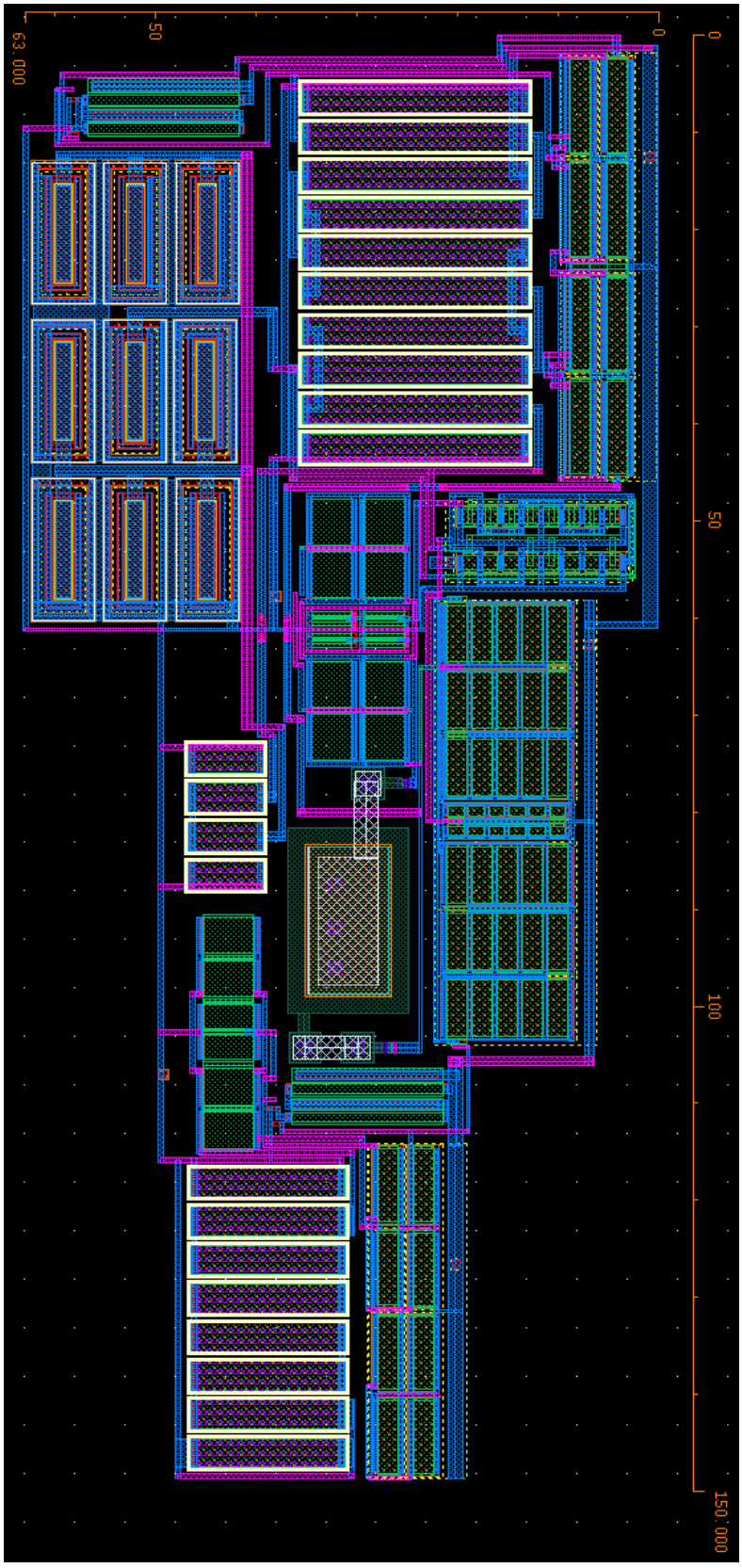

Figure 3.13: BGR2 layout

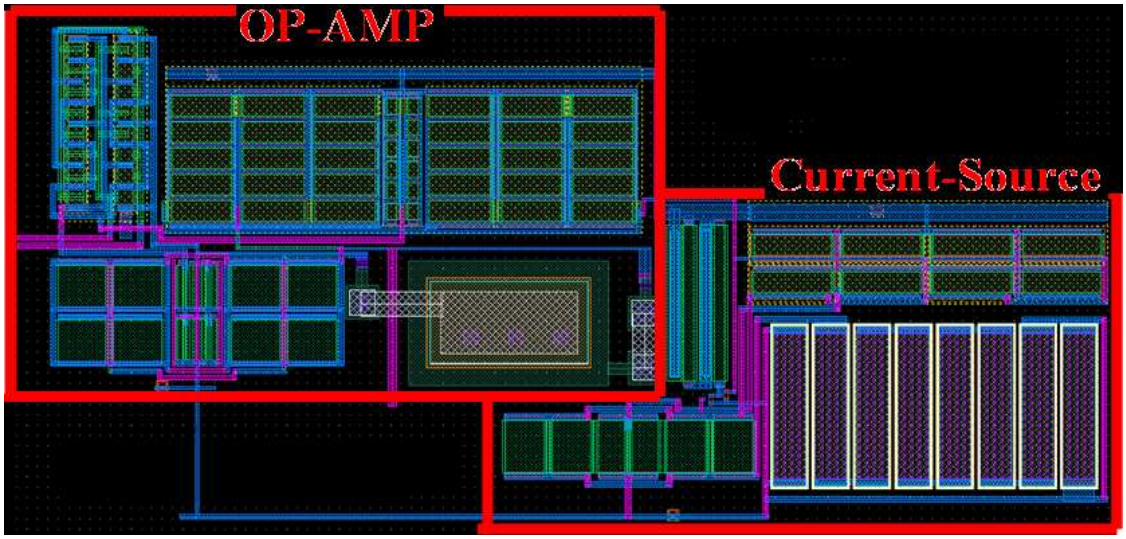

Figure 3.14: Layout of error-amplifier and its bias circuit

3.2.4 Post-Layout Simulation Results

In a similar way as for BGR1, post layout simulation, after parasitics extraction, as run to verify the temperature performance, the line regulation and the PSR. Table 3.6 shows post-layout simulation results. Figures 3.15-3.17 show respectively, the V_{REF} as a function of temperature, the line regulation performance and the power supply rejection.

Table 3.6: Post-Layout Simulation Results of BGR2

Parameter	Value	Unit
V_{REF} @ 27 °C	1.166	V
ΔV_{REF_TEMP}	3.12 (24 ppm/ °C)	mV
Temp. Range	-55 to 125	°C
Line Regulation (VDD: 1.7 – 1.9)	170 (0.85 mV/V)	µV
VDD	1.8	V
I_{Supply}	262	µA
PSR @ 1 kHz	60	dB

As can be seen on table 3.6, BGR2 presents the same temperature performance as BGR1. However, it presents an improvement of 40 times in terms of line regulation. With almost the same area used, and 1.7 times more power consumption, it was possible to achieve an improvement of more than 15 dB in the power supply rejection. However, the temperature drift of 24 ppm/ °C may be not enough to achieve the performance requirements of many applications, for instance, for high-resolution data-converters. Hence, Bandgap architectures that correct the curvature of the output voltage should be used. Section 3.3 shows the design of a second-order BGR.

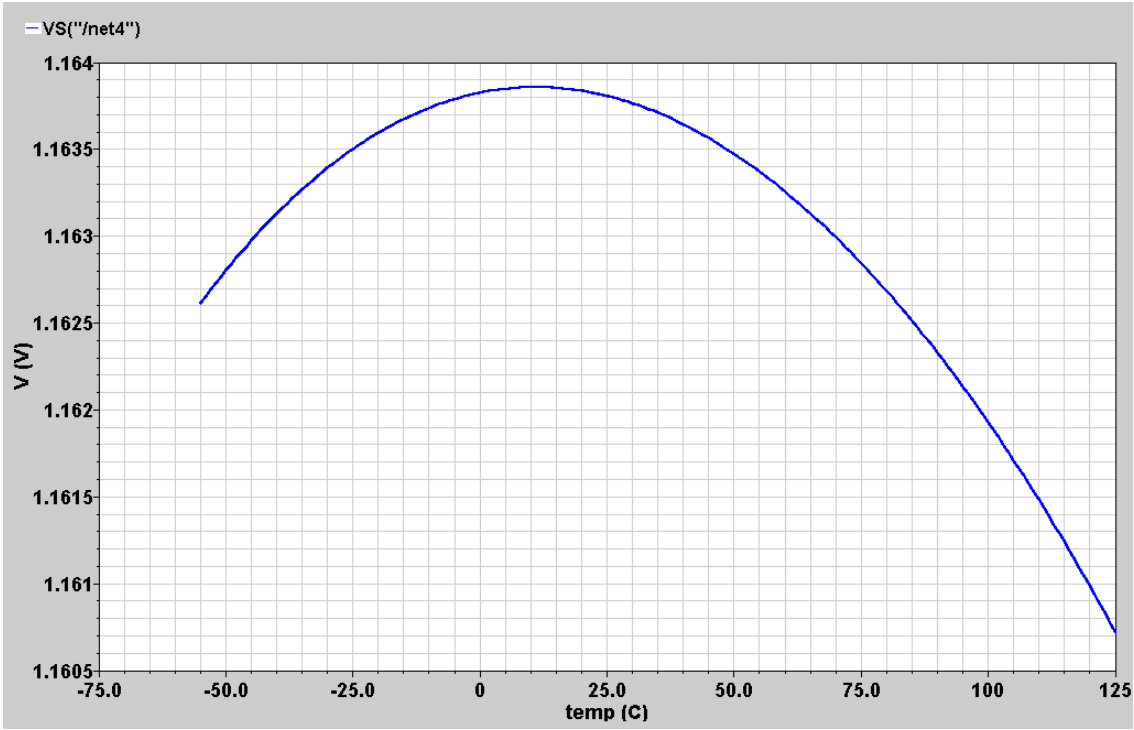

Figure 3.15: V_{REF} as a function of temperature for BGR2

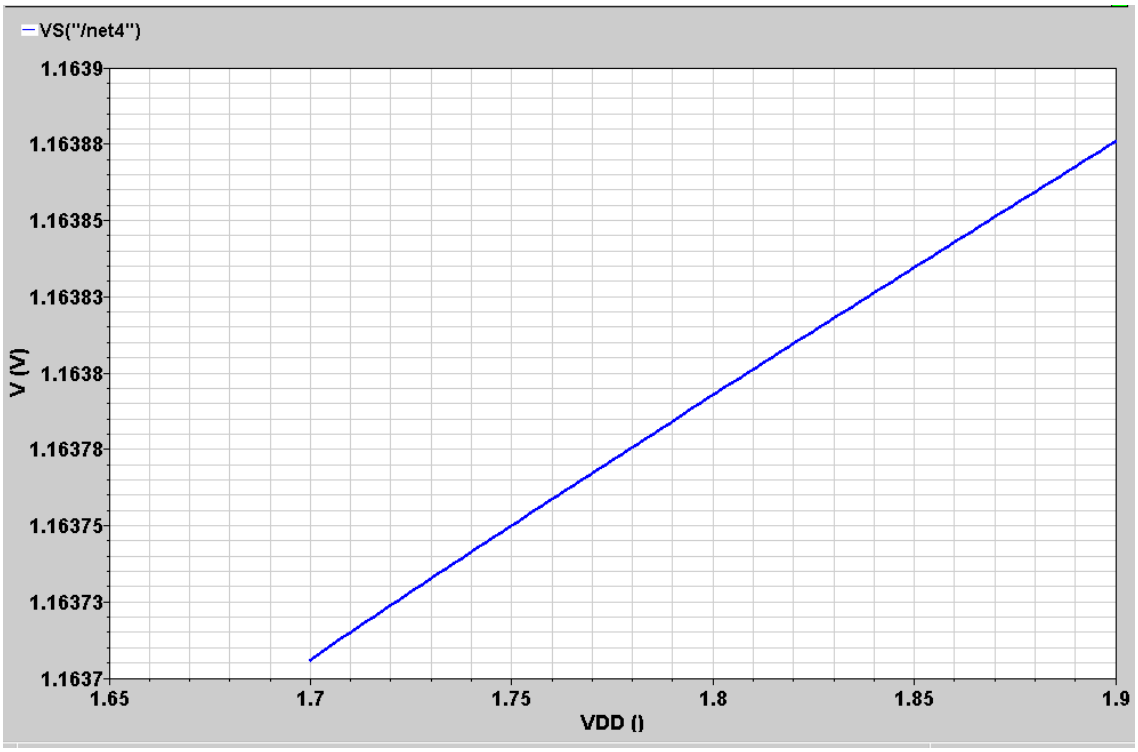

Figure 3.16: Line Regulation for BGR2 (1.7 – 1.9 V)

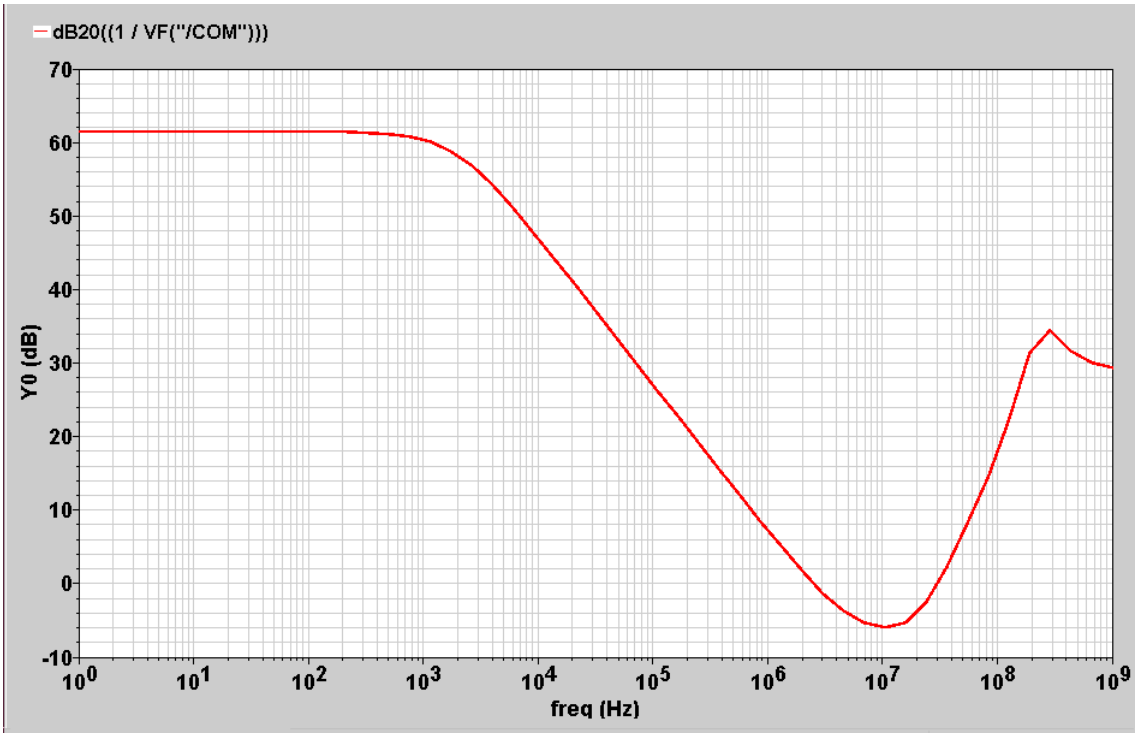

Figure 3.17: PSR for BGR2

3.3 BGR3

As already introduced in section 2.2, one of the main contributors for the output voltage curvature is the non-linear dependency of V_{BE} voltage – described by equation 2.12. Thus, to correct this temperature curvature and achieve an improved accuracy over the whole operation range, the non-linear terms of the CTAT voltage should be also temperature offseted. In fact, compensating the second term of equation 2.13 is enough to achieve the high-accuracy output voltage required by the most of applications. The non-linear terms of order higher than the second are important only for very high-accuracy application and/or for very large temperature ranges (Falconi, 2005).

The first BGR´s to use techniques to provide a high-order correction were proposed in Palmer (1981) and Meijer (1982). The first one implements the thermal compensation of the nonlinearity of V_{BE} by means of the inclusion of another non-linear term with opposite temperature coefficient; and achieves a temperature performance better than 3 ppm/°C. In the second work, a compensated BGR without introduction of extra non-linear terms was presented. By the control of the collector current it was possible to generate a V_{BE} voltage that is totally linear with temperature, and accordingly, a temperature coefficient of 0.5 ppm/°C is obtained.

Several methods are found in the literature to design second-order BGR´s (Rincon-mora, 2002). One of the most diffused techniques is to use the ratio of resistors of different materials to generate a squared PTAT voltage ($PTAT^2$). The widespread use of this technique is due to this simplicity and low-cost of implementation. Through only one extra-resistor it is possible to achieve second-order compensation. This parabolic term is added to equation 2.2 to compensate the non-linearity of the V_{BE} voltage, what leads to a temperature coefficient of 1 to 20 ppm/°C. Equation 3.8 describes the output voltage in this case and figure 3.18 shows temperature dependency graphically.

$$V_{REF} = V_{BE} + \alpha 1 \cdot V_{TH} + \alpha 2 \cdot V_{PTAT^2} \quad (3.8)$$

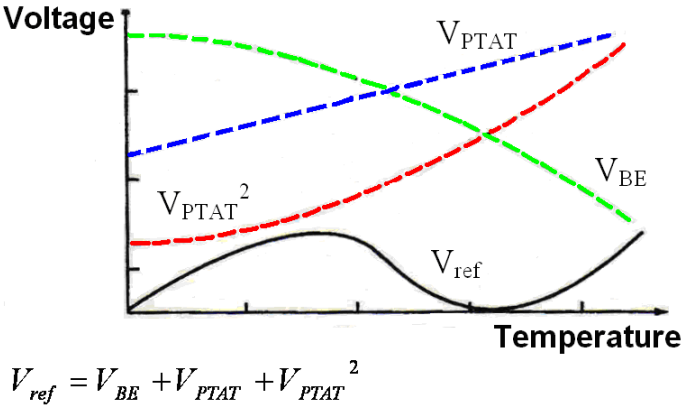

Figure 3.18: Typical Curvature of second-order compensated BGR

Through figure 3.18 it is possible to see that at low temperatures the term V_{PTAT}^2 is small and can not compensate the non-linearity of V_{BE} voltage – what leads to an output curvature similar to the one presented by the first-order BGR´s. In the middle of the temperature range, this term already compensates part of the non-linearity of the base-emitter voltage and consequently reduces the temperature dependency of the output voltage. At higher temperatures, due to the exponential relationship with temperature, V_{PTAT}^2 assumes large values and dominates the behavior of the reference voltage.

Figure 3.19 presents the designed BGR3 topology that uses the ratio of resistors made of polysilicon and P diffusion to generate the V_{PTAT}^2 voltage. This architecture was used in several works, such as (Leung, 2003), (Leung, 2004) and (Mok, 2005). The current I and the output voltage of this reference are given respectively by 3.8 and 3.9.

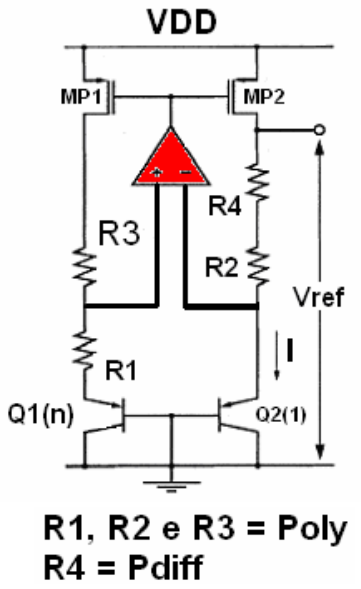

Figure 3.19: BGR3 topology

$$I_{REF} = \frac{\Delta V_{BE}}{R1} \tag{3.8}$$

$$V_{REF} = V_{TH} \cdot \ln(n) \cdot \frac{R_2}{R_1} + V_{TH} \cdot \ln(n) \cdot \frac{R_4}{R_1} + V_{BEQ2} \tag{3.9}$$

To evaluate the second-order temperature compensation of V_{REF} is necessary to write the temperature dependency of the ratio R_4/R_1in an explicit form. If one considers the temperature coefficient of the resistor, given by equation 3.10, it is possible to prove that the output voltage is described by equation 3.11. Appendix C shows the derivation of this equation. Table 3.7 explains the parameters of these equations and the values of TC_{Pdiff} and TC_{poly} for the IBM process technology used in this work.

$$TC = \frac{1}{R} \cdot \frac{\partial R}{\partial T} \tag{3.10}$$

$$\begin{aligned} V_{REF} = & \left(\frac{R_2}{R_1} + \frac{R_4(T_0)}{R_1(T_0)} \right) \cdot \ln(n) \cdot V_{TH} \\ & + \frac{R_4(T_0)}{R_1(T_0)} \cdot \left(TC_{Pdiff} - TC_{poly} \right) \cdot \ln(n) \cdot \Delta T \cdot V_{TH} + V_{BEQ2} \end{aligned} \tag{3.11}$$

Table 3.7: Parameters of equations 3.10 and 3.11

Parameter	Description	Typical value	Unit
TC	Temperature Coefficient	-	ppm/°C
TC_{Pdiff}	TC of P^+ S/D Diffusion Resistor	160	ppm/°C
TC_{poly}	TC of P^+ Poly-Silicon Resistor	1340	ppm/°C
ΔT	Temperature range	-	°C
$R(T_0)$	Value of Resistor at room temperature	-	Ω

As a final comment, one can see from table 3.7 and equation 3.11 that the $PTAT^2$ voltage is produced by the second term. Moreover, the ratio between R_2/R_1 ideally doesn't contribute to the temperature compensation because these resistors are of the same material.

3.3.1 Implementation Details

All design practices taken into account in the design of BGR2 were also considered in the design of BGR3, and even the error-amplifier is the same. Bellow there are important discussions:

(a) The choice of the resistors used in the design will depend on the availability in the fabrication process. Thus, this architecture is more dependent on the technology than BGR2 due to the need of resistors whose ratio generates a $PTAT^2$ relationship with temperature.

(b) In the IBM fabrication process, there are more than 2 resistors that satisfy condition (a). Therefore, other factors, such as Sheet Resistance and Tolerance/Matching behavior should be taken into account.

(c) Like for the BGR2, R_3 is used to improve the current mirror matching and the value of this resistor is $R_3(T@\ 27°C) = R_2(T@\ 27°C) + R_3(T@\ 27°C)$. It is true that a perfect matching of R_3 and $(R_2 + R_4)$ is not achieved at different temperatures. However, such an arrangement is sufficient to compensate the mismatch of the source-drain voltage of transistors MP1 and MP2 (Leung, 2003).

(d) There are several works, such as (Brokaw, 1981), (Lewis, 1989) and (Coady, 2007) that discuss practical aspects on how to find the value of the resistor ratio to achieve a good temperature performance. However, in high-accuracy designs, analog simulation and good process characterization are fundamental steps to find the optimal value for these devices.

(e) The high-accuracy of the BGR3 topology depends strongly on device matching and chapter 4 will focus on this issue.

We finish this section presenting in Table 3.8 the sizes of the transistors and the values of the resistors of BGR3. The sizes of transistors used in the op-amp were omitted, since they are already presented in table 3.5

Table 3.8: Sizes of transistors and values of the resistors in BGR3

Device	Design Dimensions	Layout Dimensions	Units
$M_{1,2}$	$\frac{W}{L} = \frac{38}{2}$	$4\times\left(\frac{9.5}{2}\right)$	$\frac{\mu m}{\mu m}$
Q1	$8\times A2$	$8\times A2$	-
Q2	A2	A2	-
R_4	1.38	3×0.460	$K\Omega$
R_3	7.110	6×1.18505	$K\Omega$
R_2	5.728	5×1.457	$K\Omega$
R_1	1.1	2×0.550	$K\Omega$

3.3.2 Start-up circuit

The Start-up circuit is the same as for BGR2 and provides the same start-time, equal to 5 ms.

3.3.3 Layout of BGR3

Figure 3.20 shows the layout of BGR3. The layout was done manually and the total area used is less than 60 x 160 μm^2, which is almost the same size of BGR1 and BGR2.

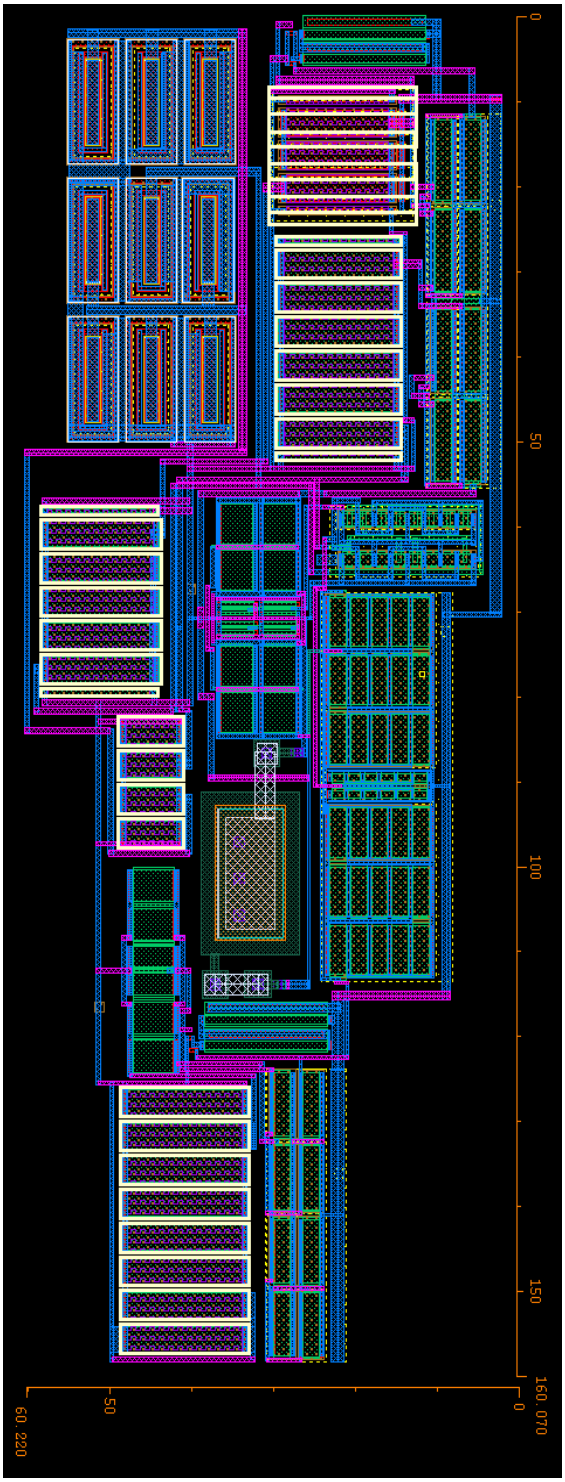

Figure 3.20: Layout of BGR3

3.3.4 Post-Layout Simulation Results

In a similar way as done for BGR1 and BGR2, after extracting the Spice net list with all parasitics from the layout, BGR3 was simulated to verify its performance. Table 3.9 presents the post-layout simulation results for BGR3. Figures 3.21 – 3.23 show the temperature performance, line regulation and PSR simulations. Please note that output voltages variations for two different temperature ranges are reported. This is done

because the BGR3 was optimized to achieve the best temperature performance in the range of 0 – 100 °C.

Table 3.9: Post-Layout Simulation Results of BGR3

Parameter	Value	Unit
V_{REF} @ 27 °C	1.144	V
ΔV_{REF_TEMP} in (a)	51 (0.5 ppm/ °C)	µV
ΔV_{REF_TEMP} in (b)	143 (3 ppm/ °C)	µV
(a) Temp. Range	0 to 100	°C
(b) Temp. Range	-55 to 125	°C
Line Regulation (VDD: 1.7 – 1.9)	186 (0.93 mV/V)	µV
VDD	1.8	V
I_{Supply}	260	µA
PSR @ 1 kHz	60	dB

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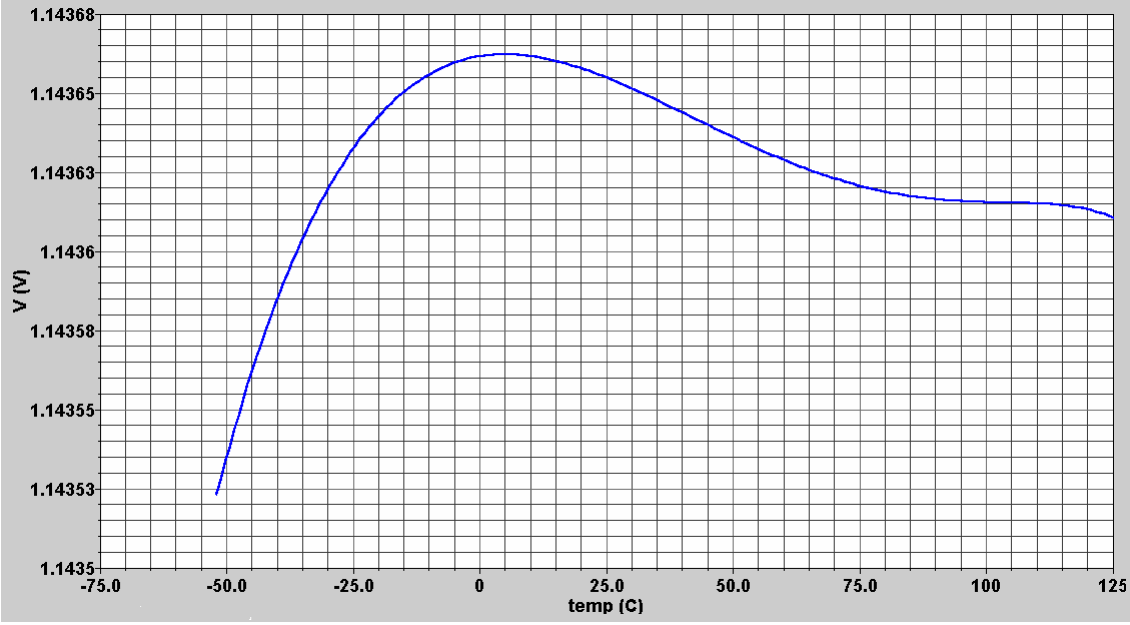

Figure 3.21: V_{REF} as a function of temperature for BGR3

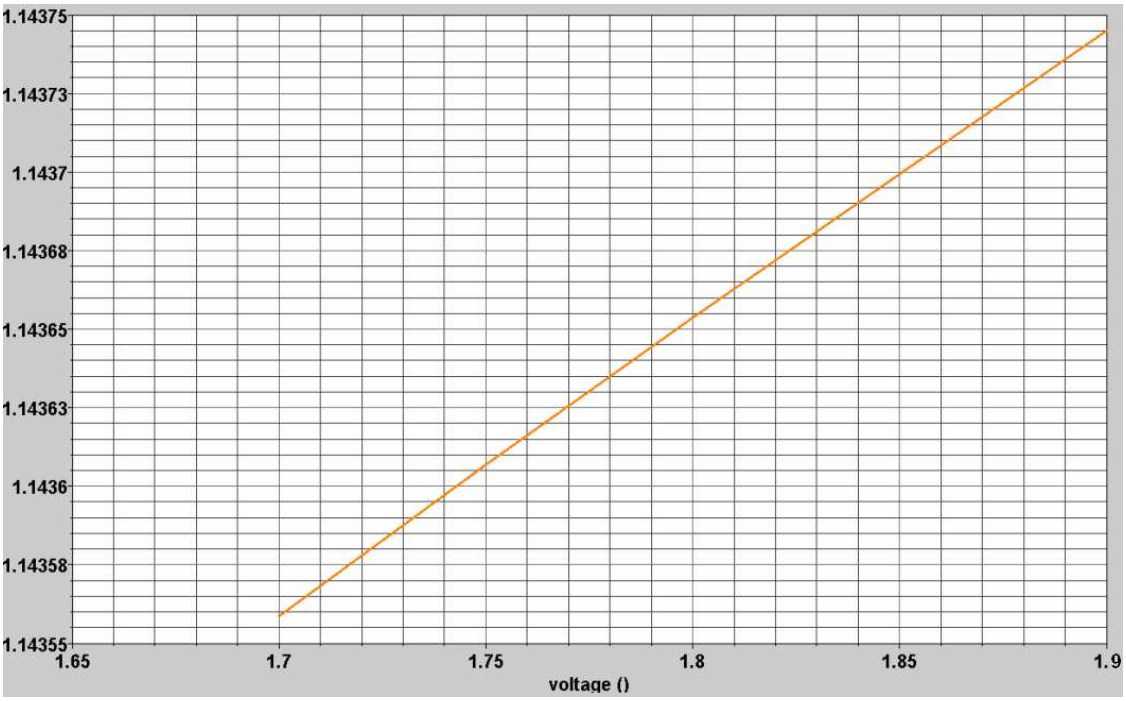

Figure 3.22: Line Regulation of BGR3 (1.7 – 1.9V)

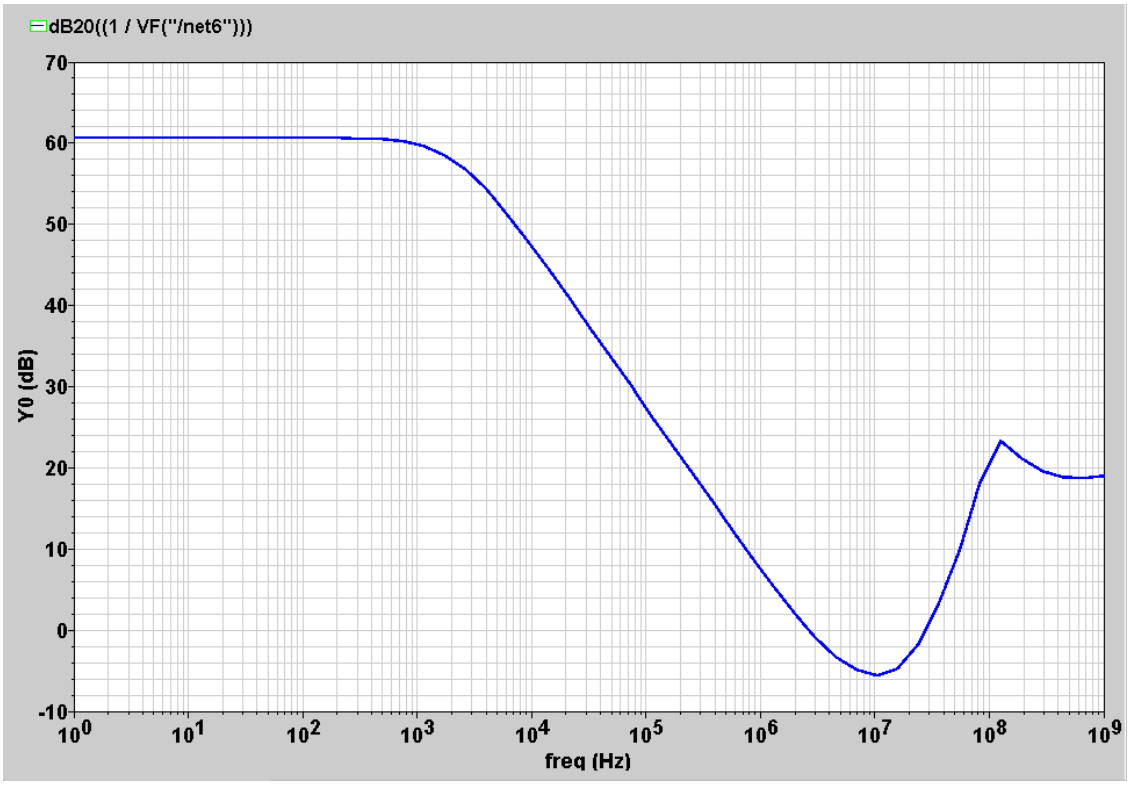

Figure 3.23: PSR for BGR3

As verified by simulations, this topology provides a significant improvement in temperature performance, achieved mainly through the insertion of extra resistors. The drawback is the increased V_{REF} dependency on fabrication process because two types of resistors whose ratio has positive TC must be available in the fabrication process.

Moreover, the possible large mismatch between these two resistors will lead a larger trim range. This will be discussed in detail in chapter 4.

All BGR´s designed in this work are largely used in several applications found in the literature, and are also the base architecture for most BGR´s recently proposed. However, the operation of these traditional topologies suffers a large negative impact if recent sub-micrometers fabrication processes, with low supply voltage, are used to implement the references. Chapter 4 focuses on this issue.

4 LOW-VOLTAGE LOW-POWER, NOISE AND VARABILITY ISSUES

This chapter discusses some limitations of the traditional topologies, mainly in designs requiring low-voltage and low-power operation, which is a realistic requirement in many current applications.

Moreover, it will be also discussed that the high-accuracy target at high-order BGR´s (for example BGR3) generally can not be achieve due to two hindrances: (a) fabrication process parameter variability and (b) the output noise generated by integrated devices and the noise that comes from the supply voltage or load.

The chapter is organized as follow. Section 4.1 analyses the limitations of the designed BGRS in the low-voltage and low-power scenario. The state-of-the-art techniques used to overcome these restrictions are also discussed. Section 4.2 presents the major error sources (due to the fabrication process) that degrade the performance of BGR circuits, and an estimation of its effects on the reference voltage is provided. Section 4.3 investigates the noise issue and the simulated output noise of BGR1, BGR2 and BGR3 used as cases of study. Finally, the proper treatment of the combined effect of variability and noise is discussed in section 4.4, and its impact on the design of the BGR´s and the trim circuit is analyzed.

4.1 Low-Voltage and Low-power

Nowadays, there is a wide demand for high-performance and low-power systems. The mass production of portable applications contributes to this wide demand. The portability of these products imposes limits on battery weigh and size, leading to a severe constraint on power dissipation. Besides the higher speed, density and size of recent CMOS systems also help to increase the need for power consumption reduction.

The design of low-power low-voltage systems relies on efficient design of low power and low voltage references. Thus, it is fundamental to design BGR´s with these features. To be more specific, BGR´s supplied with VDD below 1 V and a power consumption of a few tens of nW to a few mW is a realistic requirement (Fayomi, 2006).

Typical BGR´s have an output voltage of about 1.2 volts. This value is because the V_{REF} is composed by the sum of V_{G0} plus V_{TH} multiplied by one constant as describe by equation 2.11 in chapter 2. Besides V_{REF}, these BGRs need voltage headroom at least of 100-300 mV for proper operation. Therefore, the BGR circuit requires a supply voltage

of at least about 1.5 V, as described by 4.1 (Annema, 1999), which may not conform to low-power and low-voltage operation requirements.

$$VDD_{MIN} \geq V_{GO} + V_{T0}(\gamma - \alpha) + VoltageHeadroom \approx 1.5\,V \qquad (4.1)$$

It is also worthwhile to remember that the nominal supply voltage has been decreasing with each new fabrication process. Table 4.1 illustrates the relation between the channel size and the nominal supply voltage of TSMC fabrication processes (MOSIS).

Table 4.1: Value of Nominal Supply Voltage for different Technology Processes

L (µm)	0.35	0.25	0.18	0.13	0.09	0.065	0.045
VDD (V)	3.3	2.5	1.8	1.2	1.0 to 1.2	0.9 to 1.2	0.9 to 1.0

As can be seen, once the VDD voltage of the 0.13 µm process is less than VDD_{MIN}, it is not possible to design a BGR in this technology using the traditional topologies, such as BGR1, BGR2 or BGR3. To verify the minimum VDD necessary for the designed references, the output voltage as a function of VDD (0-1.8V) at room temperature was simulated. Figure 4.1 shows this curve for BGR2, and figures C.7 and C.8, in Appendix C, show for BGR1 and BGR3.

It is possible to see that if VDD is below 1.5 V, the current source transistors operate in the linear region and, with supply voltage below 1.2 V the output voltage decreases drastically.

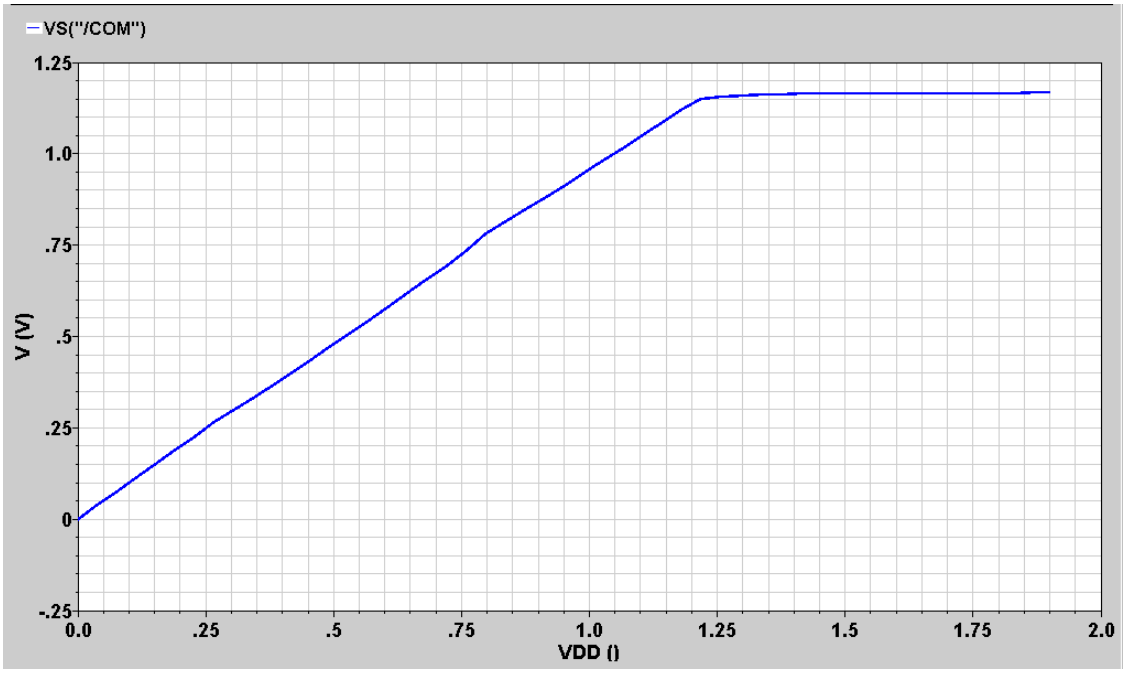

Figure 4.1: V_{REF} as a function of Supply Voltage for BGR2

To overcome the limitation of VDD_{MIN}, many techniques have been proposed in the literature, and these methods can be classified basically in three sets (Anemma, 1999):

(a) Resistive Subdivision

(b) Low-Bandgap material

(c) Virtual Low-Bandgap Device

Sections 4.1.1 – 4.1.3 describe examples of BGR´s employing these techniques to achieve low-voltage and low-power operation.

4.1.1 Resistive Subdivision

Once the output voltage of a BGR is the silicon Bandgap voltage plus a constant multiplied by the thermal voltage, if one multiplies V_{REF} by a constant less than 1 – as described by equation 4.2 – a V_{REF} voltage less than 1.2 V is obtained and the required supply voltage can be reduced. In equation 4.2, constant ω is less than unit.

$$V_{REF}\big|_{T=T0} = \omega\left(V_{GO} + V_{T0}(\gamma - \alpha)\right) \tag{4.2}$$

The first work to propose this idea was (Banba, 1998), and the BGR architecture is show in figure 4.2. In this circuit, transistors P1, P2 and P3 are equal and carry the same current. Resistors R1 and R2 are equal. Hence currents I2b and I1b are also equal, since Va = Vb is provided by the operational amplifier.

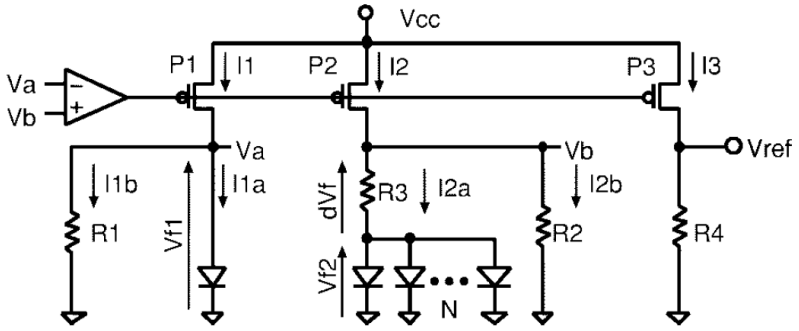

Figure 4.2: Bandgap with Sub-1V operation proposed by (Banba, 1998).

The currents I2a, I2b and I2 are given by equations 4.3 – 4.5 respectively (Banba, 1998). The output voltage is described by equation 4.6. As can be seen, the output voltage has the form of a traditional reference voltage but with an additional multiplicative constant, that can be chosen to have a desired value.

$$I1a = I2a = \frac{V_{TH} \cdot \ln(N)}{R3} \tag{4.3}$$

$$I1b = I2b = \frac{V_{BE1}}{R1} \tag{4.4}$$

$$I2 = I2a + I2b \tag{4.5}$$

$$V_{REF} = \frac{R4}{R2}\left(V_{BE1} + \frac{R2}{R3} \cdot V_{TH} \cdot \ln(N)\right) \tag{4.6}$$

Therefore, with the proposed topology it is possible to have a BGR operating at VDD less than VDD_{MIN}. In Lin, (2005) a low-voltage BGR using the technique explained above is implemented. With a supply voltage of 0.88 V and a power dissipation of 25 μW, an output voltage of 612 mV with 20 ppm/°C of temperature performance is produced. One disadvantage of this architecture is the vast resistors area used, which leads to a higher cost. More recently, Zhan (2007) suggests some

improvements, such as resistor area reduction and better matching capacity, for the circuit illustrated in figure 4.2.

4.1.2 Low-Bandgap Material

Other method to reduce the supply voltage requirements is also intuitive: if a lower-Bandgap material is used, the output voltage will be less than VDD_{MIN}.

One example of low-Bandgap material is the Ge (Germanium) with V_{G0} equal to about 660 mV. In Kim, (2008) two Hybrid Bandgap references using integrated devices and discrete Ge diodes were proposed. The first one presents the same topology of BGR2 and generates a voltage reference of 670 mV with 9.3 mV (287 ppm/°C) of variation in the temperature range. The second circuit implemented uses a resistive subdivision - such as discussed in section 4.1 - which produces a V_{REF} equal to 310 mV with a thermal variation of 4.6 mV (302 ppm/°C). Both circuits can operate with supply voltage as low as 1V.

One drawback of these circuits is the limited temperature range of operation. It was demonstrated that the lower limit of the Ge diode voltage is about three times the thermal voltage, and below this value, the temperature performance of the output voltage is degraded. Due to this issue, the highest temperature operation used in this work is 56°C. Besides this limitation, other feature of this circuit that does not comply with the current trend of ultra-integration is the use of discrete diodes. The discrete diodes can be replaced by integrated devices, but this option is expensive, and is not available in standard CMOS process.

4.1.3 Virtual Low-Bandgap Device

In Annema (1999) a low-power and low-voltage BGR using dynamic-threshold MOS transistors (DTMOST´s) is presented. The DTMOST is basically a MOS transistor with an interconnected well and gate; the P-type version of this device can be seen in figure 4.3. The operation of this device is similar to weak-inversion MOST and has similarities with bipolar operation. In fact, through the cross-section it is possible to see one lateral PNP device. Once the gate and well are tied, every change in V_{GS} causes a change in the threshold voltage. The details about operation will not be explained here, but for our understanding about the BGR proposed, it is enough to assume that the apparent Bandgap voltage generated by this device is a function of some parameters, such as V_{GS} and well doping, and a typical value of 0.6 V can be found.

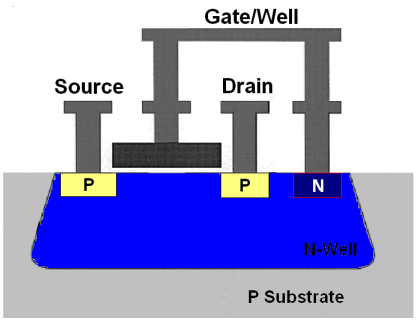

Figure 4.3: Cross Section of DTMOST (Annema, 1999)

The topology used in this work is the same of BGR2 with the only exception of bipolar transistors being replaced by DTMOST´s. Consequently due to the virtual reduced $V_{G0,}$ an output voltage of 0.65 V can be produced with a VDD of 0.85 volts.

4.2 Variability caused by Fabrication Process

Mismatch and Tolerance are results of several random processes which occur during every fabrication phase of the devices. This variability is a limiting factor of performance for any analog circuit, and specially, in multiplexed analog systems, data converters and references. Once the dimensions of the devices are decreasing, the impact of variability becomes critical in the recent technologies.

The most important sources of error are: resistor's tolerance and mismatch, resistor's temperature coefficient, transistor's tolerance and mismatch, and package shifts. Package shift refers to the changes in V_{REF} induced by package induced stress on the die surface. This problem occurs mainly due the difference in the thermal coefficient of expansion of the silicon die and the plastic mold (Fruett, 2003). All these errors lead to a reference voltage different from the nominal value, resulting in a non-accurate output voltage with degraded temperature performance (Gupta, 2005).

To illustrate the impact of fabrication process on the output voltage, an estimation of variability effects on the output voltage of BGR2 is presented in table 4.2 (Sengupta, 2005). In this work, the process induced errors are investigated through analytical equations and simulation in a 0.18 μm CMOS process using the BSIM3V3 models.

Table 4.2: Variation in V_{REF} caused by each error source (Sengupta, 2005)

Process Variation	ΔV_{REF}	Unit
Mismatch in BJT area (11%)	16	mV
Absolute variation in area of both BJTs (11%)	-3	mV
Variation in R1 (10%)	-45	mV
Mismatch in R3 (1%)	-5	mV
Mismatch in R1 (1%)	0.1	mV
Offset voltage (1 mV)	-7	mV
Current Mirror Mismatch (1%)	-6	mV

Through table 4.2 it is possible to verify how each error source generates variation in output voltage. Now, a reasonable assumption is to assume that these induced process-errors – listed in table 4.2 - are uncorrelated. In this case, the resulting error in the reference voltage (ΔV_{REF_TOTAL}) is given by equation 4.7, that is, the root sum squared (RSS) of these individual random errors (Gupta, 2005). Where Nu is the number of errors source and ΔV_{REF_i} is the variation of V_{REF} due to each error source.

$$\Delta V_{REF\_TOTAL} = \sqrt{\sum_{i}^{Nu} \Delta V_{REF\_i}^{2}} \tag{4.7}$$

Applying equation 4.7 to the data presented in table 4.2, it is found that the total variation of V_{REF} is about 50 mV. As can be seen, the impact of the variability in output voltage severely degrades the accuracy of BGR´s. Further, these errors also harm the temperature drift of V_{REF} – which is not shown in table 4.2.

Besides verifying how much each error source impacts on the output voltage, it is also important to analyze the temperature dependence of the generated errors and the possibility to correct them through trim techniques. In Gupta (2002) this data is presented and it is here reproduced in table 4.3. As can be seen, the errors caused by the resistor temperature coefficient can not be trimmed – what evidences again the importance of choosing an adequate resistor material when designing BGR´s.

Table 4.3: Temperature dependence of error sources (Gupta, 2002)

Error Source	Trimmable	Temp. Dependence of the errors caused by
Resistor Mismatch	Yes	PTAT
Resistor Tolerant	Yes	CTAT
Resistor TC	No	Non-Linear
Transistor Mismatch	Yes	PTAT
Current Mirror Mismatch	Yes	PTAT

Note that the error caused by mechanical stress (mainly due to packaging-induced inaccuracy) is not presented in table 4.3. Frequently, an error of about ±7 mV (Gupta, 2005) in output voltage can be generated by this process. This type of error is not easily corrected in the design phase, since its impact on V_{REF} is difficult to model and predict. Nevertheless, work (Fruett, 2003) discusses how the Mechanical-Stress-induced Inaccuracy can be minimized.

Another method to estimate the variability caused by fabrication is through the Monte Carlo Simulation. All design BGR´s were simulated over fabrication process and Mismatch variations using the Monte Carlo model provided by foundry (IBM, 2005). Figure 4.4 and 4.5 show the variations of V_{REF} and for ΔV_{REF_TEMP} for 1000 samples in respect of BGR1. Figures B.10-B.12, in Appendix B, show the same histogram for BGR2 and BGR3 respectively. Table 4.4 summarizes the results for BGR1, BGR2 and BGR3.

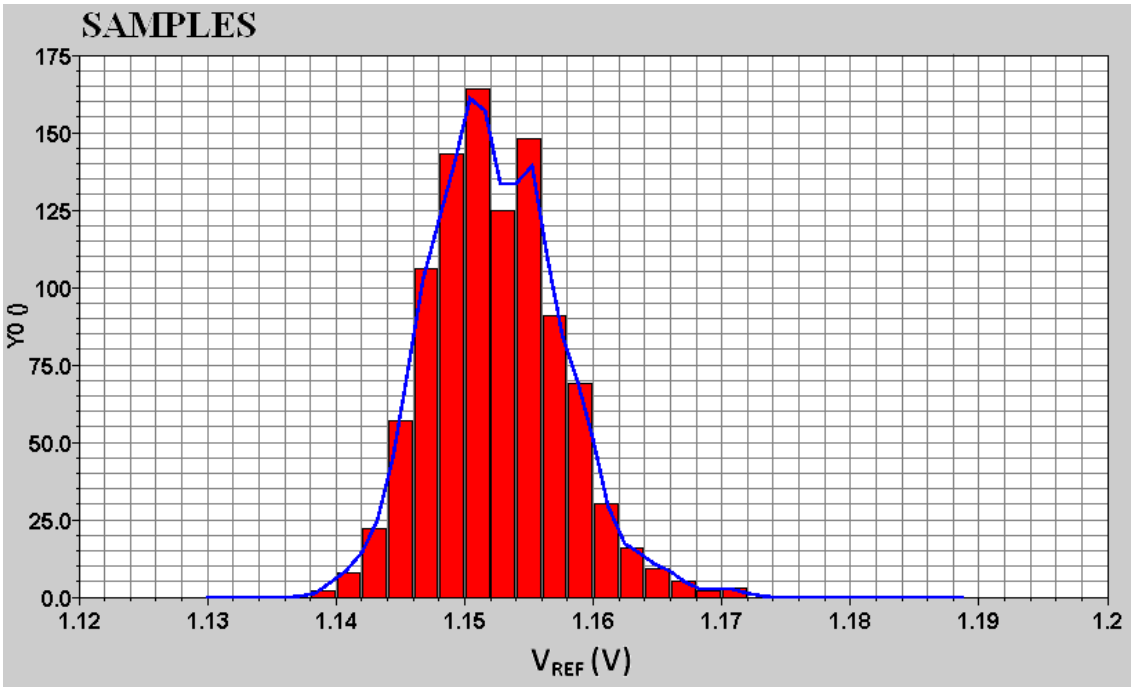

Figure 4.4: Monte Carlo Analysis of V_{REF} for BGR1

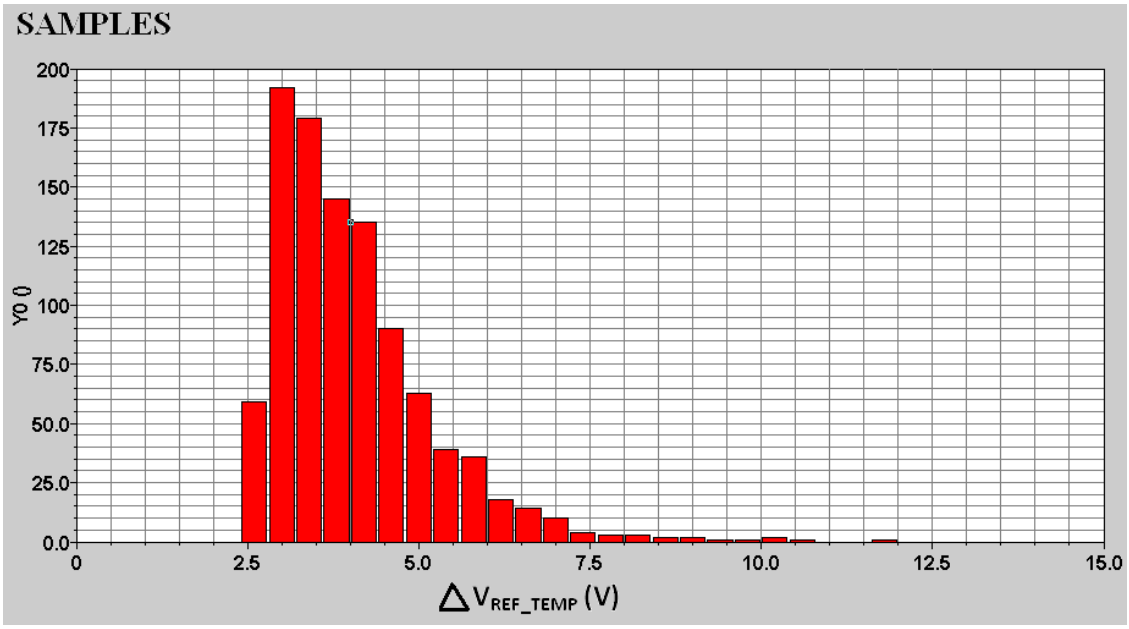

Figure 4.5: Monte Carlo Analysis of ΔV_{REF_TEMP} for BGR1

Table 4.4: Monte Carlo Analysis for BGR1, BGR2 and BGR3

Monte Carlo Analysis					
Parameters		BGR1	BGR2	BGR3	Units
$V_{REF\_MONTE\_CARLO}$	Mean	1.15241	1.16903	1.1523	V
	σ (Sigma)	5.053	11.253	12.420	mV
	Mean - 3σ (V_{REF_DOWN})	1.13725	1.13527	1.11504	V
	Mean +3σ (V_{REF_UPPER})	1.16757	1.20279	1.18956	V
	Full-Scale	30.32	67.52	74.52	mV
$\Delta V_{REF\_TEMP\_MONTE\_CARLO}$	Mean	4.063	4.842	6.802	mV
	σ	1.184	2.575	5.101	mV
$V_{OS\_MONTE\_CARLO}$	Mean	-	80		μV
	σ	-	1.3		mV
Nominal Values					
V_{REF}	-	1.152	1.166	1.144	V
ΔV_{REF_TEMP}	-	3	3.12	0.143	mV

Table 4.4 shows the impact of fabrication process variations on the output voltage ($V_{REF\_MONTE\_CARLO}$), the temperature performance ($\Delta V_{REF\_TEMP\_MONTE\_CARLO}$) and the Offset voltage ($V_{OS\_MONTE\_CARLO}$) respectively, as well as their nominal values V_{REF}, ΔV_{REF_TEMP}. It is shown the 3σ behavior for the degraded output voltage, V_{REF_UPPER}, V_{REF_DOWN} and the expected full scale of V_{REF} that is V_{REF_UPPER} - V_{REF_DOWN}.

Thus comparing the nominal values with the results of Monte Carlo Analysis, one can see that the fabrication process significantly degrades the accuracy and the temperature performance of the voltage reference. After fabrication, it is possible that the reference achieves a temperature performance worse than 100 ppm/°C.

As can be seen through the expected full scale of V_{REF} after fabrication, the impact of fabrication process on BGR1 is less than on BGR2 and BGR3. This happens because the offset voltage of BGR2 is amplified to the output, which leads to larger errors. In fact, the offset voltage is the major factor of performance degradation for BGR2 and BGR3 architecture, and consequently it should be reduced. Figure B.9, in appendix B, shows the Monte Carlo analysis of the offset voltage. Moreover, the number of devices of BGR1 is less than BGR2, and the transistors were designed with a very large area.

Comparing the impact on BGR2 and BGR3, it is possible to see that the impact is larger in the compensated Bandgap. This effect is also expected since BGR3 uses an extra resistor of different material, which adds another error source. Note that the full-

scale errors found by Monte Carlo Analysis for BGR2 are in agreement with those calculated by equation 4.7. The value of ΔV_{REF_TOTAL} (variation of reference voltage after fabrication process) calculated by equation 4.7 is about 50 mV; while the full scale variation of V_{REF} simulated by Monte Carlo Analysis (table 4.4) is about 67 mV.

It is important to note that frequently the results of Monte Carlo Simulation is an overestimated analysis, what means that the fabricated circuit probably will have better performance than presented in table 4.4 . One example of this is that all techniques applied into BGR´s layouts to achieve a better matching, such as, Centroid Common, dummy devices and guard rings, are not taken into account in the Monte Carlo simulation.

Besides layout techniques, other techniques are frequently used to mitigate the impact of fabrication process variations. For example:

(a) Pelgrom Model (Pelgrom, 1999): Mismatch model used to calculate the area of devices focusing on the desired accuracy.

(b) Trimming techniques (Rincon-Mora, 2002): There are several methods to trim the circuit, for example, Fusible links, Laser-Trimmable resistor, resistor trimming (several resistors connected in parallel), transistor trimming (several transistors connected in parallel) and so on.

(c) Good layout foorplanning such as: BGR far way from noisely circuits (ie. Oscillators and PLL´s) and thermal sources (regulators). If is also recommend to center the Bandgap circuit in the center of the die to mitigate the temperature variations across the die (Rincon-Mora, 2002).

As discussed in this section, the performance of BGR´s is directly dependent of good matching, what requires application of some of the methods listed above. As the impact of fabrication process tend to be more severe in nanometer process, new topologies or techniques should be developed to permit high-accuracy performance.

4.3 Output Noise

Other hindrance that limits the performance of Bandgap References is the noise. The output noise results from two components: (a) the intrinsic noise generated by integrated devices and (b) the noise that comes from the supply voltage, ground lines, substrate and load. A noisely voltage reference can limit, for example, the signal to noise ratio of biomedical applications or the full-scale signal swing of ADC converters (Mok, 2004).

As already discussed, the demand for battery-powered ICs requires low-voltage and low-power circuit design. Low-power designs lead to noisier circuits and lower accuracy. The noise does not scale down with decreasing supply voltages, and the signal-to-noise ratio (SNR) tends to get worse. The demand for high accuracy and low-power are major concerns in the development of low-noise circuits.

In the past, external components were employed, for instance capacitors and filter networks, as common solutions to reduce the output noise of voltage references. Nowadays, the need to place the voltage reference on the same substrate as the application requires design of circuits with intrinsically low noise. But which is the best way to measure the output noise of BGR or other analog circuit?

As the noise process is random, it is not possible to predict the amplitude of the noise voltage in a particular time. In fact, some types of noise, such as, thermal and shot noises, have Gaussian probability density functions (Texas, 1999). Hence, the best way to specify the noise of a circuit is through of statistical measures, as for instance, root-mean-square (RMS) or mean-square values.

Equation 5.2 is a coherent way to estimate the maximum impact of the noise in the output voltage (Holman, 1994). Where V_{RMS} is the RMS noise integrated in an appropriate bandwidth (BW), ΔV_{REF_NOISE} is the variation of output voltage due the noise and $V_{PEAK\text{-}TO\text{-}PEAK}$ corresponds to the 3σ value of noise behavior. Equation 4.8 assumes that the output noise in V_{REF} has a Gaussian distribution, and thus the use of 3σ value means that in 99.7% of the time the ΔV_{REF_NOISE} value contains the instantaneous value of the output noise voltage.

$$\Delta V_{REF\_NOISE} = V_{PEAK-TO-PEAK} = 3 \cdot V_{RMS} \tag{4.8}$$

To estimate the output noise generated by the integrated devices in the designed BGR´s, the noise spectrum simulation was performed. To obtain the V_{RMS}, the noise was integrated in a bandwidth of 500 kHz that is the corner frequency of the designed circuits – as can be seen in figure 4.6 that shows the noise spectrum of BGR2. The RMS noise and its impact on the reference voltage - calculated by means of equation 4.8 – for the designed BGR´s are presented in table 4.5. The noise Spectrum of BGR1 and BGR3 are presented in figures C.13 and C.14 of Appendix C.

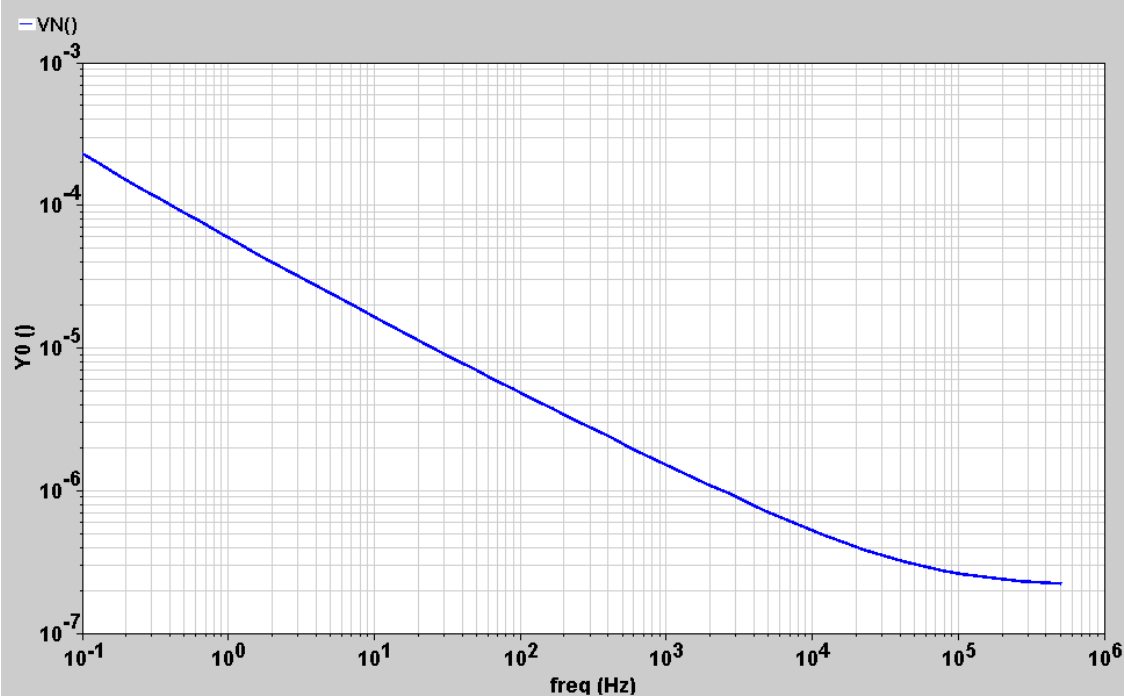

Figure 4.6: Output noise Spectrum of BGR2 - (Noise Axis in logarithm)

Table 4.5: Output noise and ΔV_{REF_NOISE} for BGR1, BGR2 and BGR3

	BGR1	BGR2	BGR3	Unit
RMS Output Noise	90	261	262	μV
Impact on V_{REF} (ΔV_{REF_NOISE})	270	783	786	μV

To reduce the noise in V_{REF} it is necessary to study the noise sources. There are five common noise sources in electronic circuits: Shot, Flicker (1/f), Thermal, Burst (Popcorn) and Avalanche noise. However, the major contributions of the noise in BGR are flicker and thermal noise of MOSFET´s, as well as the thermal noise of the resistors. The Bipolar devices usually do not contribute in any significant way to output noise because their shot, thermal noise and 1/f noise are frequently much smaller than those of MOSFET´s (Holman, 1994).

The 1/f drain noise current of MOSFET´s is given by equation 4.9 (Lee, 1998); where K_F is a device-specific constant, f is frequency, and gm is the transconductance. As can be seen, for a given gm, the noise decreases when transistors dimensions increases. Physically, this fact can be explain by the reason that large transistors presents large capacitances that smoothes the fluctuations in the channel charge leading to less noise.

$$\overline{i^2} = \frac{K_F}{f} \cdot \frac{gm^2}{W \cdot L \cdot C_{OX}^2} \cdot \Delta f \tag{4.9}$$

The contribution of each noise source in the output noise was identified through the Noise Analysis of Spectre Simulator (Spectre, 2003) for the designed BGRs. Table 4.6 shows the noise contribution for BGR1 and BGR2. The noise contribution of BGR3 is almost the same of BGR2.

Table 4.6: Noise contribution of each noise source for BGR1 and BGR2

BGR1			BGR2		
Device	Type of noise	Contribution	Device	Type of noise	Contribution
M_1	Channel Thermal	35%	M_{N0}	Flicker	22%
M_2	Channel Thermal	13%	M_{N1}	Flicker	21.2%
R_1	Thermal	11.3%	M_{P0}	Channel Thermal	10.5%
M_3	Channel Thermal	8%	M_{P3}	Channel Thermal	10.5%
M_4	Channel Thermal	8%	M_{P0}	Flicker	10.2%
M_4	Flicker	5.4%	M_{P3}	Flicker	10.2%
M_3	Flicker	5%	M_{N0}	Channel Thermal	5%
M_1	Flicker	5%	M_{N1}	Channel Thermal	5%
Others	-	9.3%	Others	-	4.3%

For BGR1, devices M_1 and M_2 are the current source; and M_3 and M_4 are the cascode devices. One can see that the channel thermal noise is the major noise source with about 65% of the total output noise. Since the transistors in this circuit were designed with a very large area, the flicker noise contribution was reduced.

For BGR2, devices M_{N0} and M_{N1}, and M_{P0} and M_{P3} are respectively the load and input of the differential pair of the Op-Amp. It is possible to verify that the error-amplifier is the major noise generator in the circuit, producing about 95% of the noise in the voltage reference. This high-contribution happens because the input-referred noise of the Op-Amp is amplified by the closed-loop gain. Other conclusion is that almost the total noise generated by the Op-Amp comes from the input stage – what it is in close agreement with results reported in Laker (1994).

Thus based on above observations it is possible to suggest some good design practices for BGR2 topology. The noise performance can be optimized if the recommendations below are taken into account in the design of the differential pair. The drawbacks of these advices are area overhead and increased power consumption:

(a) To design the devices with large area to reduce the flicker noise since this noise source contribution is inversely proportional to the transistor area.

(b) To increase transconductance (gm) of the devices to reduce the channel thermal noise (Allen, 2004).

(c) To minimize the transconductance ratio of the load by the input transistors (gm_{LOAD}/gm_{INPUT}) to reduce the noise gain to the output node (Allen, 2004).

Besides evaluating the intrinsic noise generated by integrated devices, it is also important to evaluate the vulnerability of the circuit to the noise injected through the input supply. For this proposal, the power supply rejection (PSR) is evaluated. This parameter is calculated by dividing the ac noise signal present on V_{REF} by the ac noise signal present on VDD. It is desired that PSR will be as high as possible, as for instance, 60 dB or higher. The PSR was simulated for the designed circuits and is presented in chapter 3. Its value at 10 kHz is equal to 29, 47 and 47 dB for BGR1, BGR2 and BGR3, respectively. In fact, these topologies are not efficient against the noise coming from supply voltage. One way to improve this performance is using folded-cascode operational amplifier in BGR2 and BGR3. For BGR1, inserting cascode devices would increase the PSR since the output resistance is increased. It is evident that cascode devices require higher voltage headroom and can be a problem in low-voltage designs.

As discussed in this section, the output noise can limit the accuracy of BGR´s and its impact on the voltage reference tends to be critical in the high-accuracy and low-voltage design using new technologies. Therefore, low-noise BGR´s architectures have been the concern of many works.

In Sudha (1997) a low noise BiCMOS Bandgap with high-order temperature compensation is presented. As discussed, bipolar devices present less noise than MOSFET´s and accordingly, low-noise performance is achieve in these design. Nevertheless the use of BiCMOS process increases the cost of fabrication.

More recently, in Jiang (2005) a pure CMOS low-noise BGR was proposed. The architecture proposed in that work uses a chopper stabilizing technique directly applied in the design of the op-amp to allow a low 1/f noise performance. The RMS output

noise found in their circuit was only 67 μV, which is almost 4 times less than the noise measured in the designed BGR2.

4.4 Trim range limited by Noise

As discussed in section 4.2, the tolerance variations and mismatches among electrical parameters, both generated by imperfections in the fabrication process, are one of most relevant factors that degrade the accuracy of the reference voltage. Hence, many of the recommendations presented in the variability section should be applied to mitigate the process-induced errors. However, when the expected variation in output voltage is higher than the acceptable for the application, a trim circuit is usually inserted in the design to minimize this fabrication effects (Leung, 2004), (Malcovati, 2001), (Hsiao, 2006). Unfortunately, inserting a trim circuit usually leads to longer test time, and also increases die area, leading to a higher product cost. Therefore, it is fundamental not to over estimate the trim range. Reduced trim range achieves shorter test times and saves die area. To achieve this goal, reliable techniques to predict the maximum precision achieved are demanded.

As also investigated, the output noise also degrades the accuracy of the reference voltage. And once high-accuracy and low-power design using new technologies is desired, the performance degradation due the noise in BGR´s tends to be more critical. For instance, device low-frequency noise increases as the inverse of the device area, and hence becomes of ever increasing interest as device dimensions are scaled down.

In previous works (Brito, 2007) and (Hsiao, 2006), trim circuits to mitigate the process variation effects were proposed but without considering the impact of the output noise on the voltage reference accuracy. Nevertheless once parameter variations and noise can limit the accuracy the reference voltage design can achieve, both should be taken into account in the design of a BGR and its trim circuit. If noise performance is not properly taken into account, the precision that can be achieved may be misevaluated. The noise may impose a limit on the precision that may be achieved. If this limited is not taken into account, the trim circuit may expend area and test time, targeting at a precision that never will be achieved.

This section studies how the output noise and variability due to process variations can impact the design and applicability of trim circuits. We propose that the RMS output noise should be incorporated in the methodology (Rincon-mora, 2002) to specify the trim range. To develop our investigation the three designed BGR´s were used as case studies, and the data presented in sections 4.2 and 4.3 are utililized.

4.4.1 Trim circuits

Trim circuit is typically a set of switches that allows making one adjustment in the circuit and modify the output voltage, then reducing the errors caused by fabrication process. For example, by increasing or decreasing the PTAT current it is possible to adjust the output voltage of the fabricated circuit to the nominal value that leads to optimum temperature performance. There are many types of trim circuits, such as Fusible links, Laser-Trimmable resistor, resistor trimming (several resistors connected in parallel), transistor trimming (several transistors connected in parallel) and so on.

Figures 4.7 and 4.8 shows examples of trim circuits presented in Brito (2007) and Malcovati (2001) respectively.

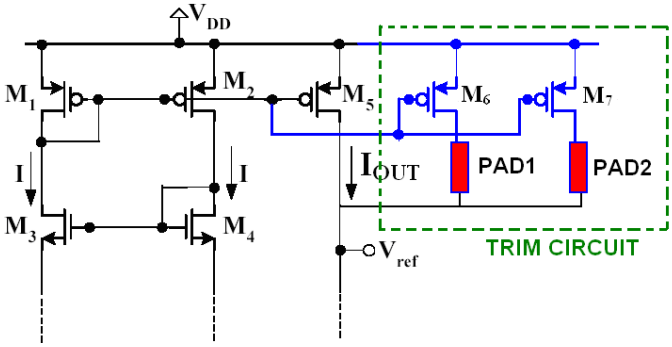

Figure 4.7: Trim circuit presented in Brito (2007)

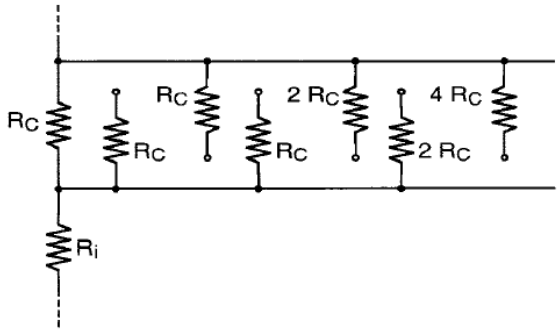

Figure 4.8: Trim circuit presented in Malcovati (2001)

Trim circuit of Brito (2007) is composed by many transistors of different sizes connected to the supply voltage (for simplicity figure 4.7 shows only 2 devices). Through the connection of PADS, it is possible to connect them in parallel with M_5, modifying the PTAT current and accordingly the output voltage. The trimming technique in figure 4.8 works in a different way. The key resistors of the Bandgap proposed in this work were implemented by one fixed resistor in series with an array of resistors whose value is a multiple of a given value R_C. With 8 terminals of the network connected to external pins it is possible to increase the value of R_i by 30% with steps of 1%. Accordingly, it is possible to modify the value of resistors to achieve one value that generates the optimum temperature performance.

4.4.2 Trim range

To calculate the number of bits necessary to trim the circuit to achieved the desired accuracy, equations 4.10 and 4.11 are used (Rincon-mora, 2002). The parameters of these equations are explained in table 4.7.

$$N_{BITS} \geq \frac{\ln\left(\frac{V_{FS}}{V_{LSB}} + 1\right)}{\ln(2)} \tag{4.10}$$

$$V_{LSB} \leq \frac{V_{ACCURACY}}{K_C} \tag{4.11}$$

Due the fabrication process effects it is expected that there is a limit for the accuracy of output voltage that can be achieved by trimming techniques. As already discussed, the errors such as resistor temperature coefficient and mechanical stress can not be trimmed, and accordingly a remaining error still will be present in the output voltage. Moreover, there is a tradeoff between the number of bits, area overhead and time testing. Thus reliable techniques to predict the maximum precision achieved by one trim circuit are demanded (Colombo, 2007-a).

In the Bandgap presented in Malcovati (2001), making use of three trimmable resistors where each one has the resistive network shown in figure 4.8 was possible to adjust the circuit to achieve a temperature variation of only 300 μV over the range of 0 to 80°C. The drawback was 8 external pins for each resistor, what results to 24 additional pins required for resistor trimming.

Table 4.7: Parameters of equations 4.10 and 4.11

Parameter	Description	Unit
N_{BITS}	Number of bits needed to trim the circuit and achieve the desired accuracy.	-
V_{FS}	The value of initial full-scale tolerance expected. It corresponds to the accuracy of V_{REF} after circuit fabrication, for the untrimmed reference.	V
V_{LSB}	The value of the least significant bit, that is, the variation step of V_{REF} during the trimming procedure.	V
$V_{Accuracy}$	The target accuracy (after trimming)	mV
K_C	“Safety Factor” used to reduce the value of V_{LSB}	-
V_{REF}	Reference Voltage	V

4.4.3 Trim range for BGR1, BGR2 and BGR3

In section 4.2 it was shown that the fabrication process effects damages the temperature performance of the designed BGR´s to more than 100 ppm/°C. Therefore, trim circuit should be inserted in these designs to mitigate the process-induced errors. The calculated number of bit to mitigate the process impact over V_{REF} for each circuit is presented in table 4.8.

Table 4.8: Number of bit for each BGR

Parameter	BGR1	BGR2	BGR3	Units
V_{FS}	30.32	67.52	74.52	mV
V_{LSB}	3.25	1.6025	0.1965	mV
K_C	2	2	2	-
$V_{Accuracy}$	6.5	3.205	0.393	mV
ΔV_{REF_VDD}	3.5	0.085	0.093	mV
ΔV_{REF_TEMP}	3	3.12	0.3*	mV
N_{BITS}	4	6	9	-

The value of full-scale (V_{FS}) is estimated based on 3σ behavior of Monte Carlo Analysis presented in table 4.4. The values of V_{LSB} and the N_{BITS} are estimated using equations 4.10 and 4.11. For simplicity, the value of K_C was chosen to be 2. Larger values of K_C results in lesser value of V_{LSB}, what can lead to a bigger trim range.

The target accuracy ($V_{ACCURACY}$) was determined by equation 4.12. This equation represents an estimation of the theorical maximum accuracy that the output voltage can achieve. Frequently, the maximum accuracy is estimated based on the summing of error sources of the circuit (Rincon-Mora, 2002). In our case, the maximum accuracy is stipulated by means of the errors caused by temperature operation and supply voltage variations. The value of ΔV_{REF_VDD} is given by the line regulation error divided by two.

$$V_{ACCURACY} = \Delta V_{REF\_TEMP} + \Delta V_{REF\_VDD} \tag{4.12}$$

As expected, due to the larger full-scale and the best target accuracy, BGR3 requires more bits than the other references. The value of ΔV_{REF_TEMP} is assumed to be 300 μV, although the value obtained by simulation were 51μV and 143 μV for a temperature range of 0 to 100°C, and -55 to 125 °C respectively. This assumption makes sense because the nominal values of ΔV_{REF_TEMP} are only theorical simulation results that not correspond to the behavior of fabricated circuits. In a real chip there are a lot of errors that can not be corrected and consequently degrades the accuracy.

However, considering that there are trimming techniques proposed in literature, such as described by Malcovati (2001), that allows the BGR design to achieve a temperature variation of output voltage of only 300 μV, the value of $V_{ACCURACY}$ is estimated as 300 μV (ΔV_{REF_TEMP}) + 93 μV (ΔV_{REF_VDD}) = 393 μV, what represents a realist value.

Therefore, considering the traditional method to evaluate the trim range necessary to mitigate the performance degradation due the fabrication process, N_{BITS} equal to 4, 6 and 9 were found for the BGR1, BGR2 and BGR3 respectively.

4.4.4 New trim range for BGR1, BGR2 and BGR3

As discussed in the begging of this section, once the output noise also limits the accuracy achieved by one BGR, it is necessary to reconsider the maximum accuracy that can be achieved. Thus, we propose that equation 4.12 should be changed by 4.13,

where ΔV_{REF_NOISE} is given by equation 4.8, and was estimated for each BGR in table 4.5.

$$V_{ACCURACY} = \Delta V_{REF\_TEMP} + \Delta V_{REF\_VDD} + \Delta V_{REF\_NOISE} \quad (4.13)$$

Therefore, the trim range for each BGR is again estimated and the results are presented in table 4.9. As can be seen, the number of bits for BGR3 was estimated to be 7 bits, what means a reduction of up to 2 bits compared to the results in the last section. For BGR1 and BGR2, there is no change in the number of bits necessary to achieve the desired accuracy. This happens because the accuracy degradation in first-order bandgaps due to the output noise is not as significant as those errors caused by temperature variation and/or line regulation.

To be clearer, table 4.9 shows that the use 9 bits of trimming for BGR3 will not help to improve the accuracy, and therefore, area and test timing will be wasted. In this case, the design has then to be properly adjusted: (i) either by accepting a lower precision and reducing the trim range to avoid unnecessary area overhead and test time; or (ii) apply low-noise techniques, for instance, exchanging the operational amplifier by one chopper-stabilized amplifier to try achieve more accuracy.

Table 4.9: Number of bit for each BGR considering the output noise

Parameter	BGR1	BGR2	BGR3	Units
V_{FS}	30.32	67.52	74.52	mV
V_{LSB}	3.3158	1.994	0.5895	mV
K_C	2	2	2	-
$V_{Accuracy}$	6.77	3.988	1.179	mV
ΔV_{REF_VDD}	3.5	0.085	0.093	mV
ΔV_{REF_TEMP}	3	3.12	0.3*	mV
ΔV_{REF_NOISE}	0.27	0.783	0.786	mV
N_{BITS}	4	6	7	-

Therefore, the conclusion of this section is that the output noise should be incorporated in the methodology to evaluate the trim range in high-accuracy BGR´s (Colombo, 2007-a) and (Colombo, 2007-b). The adequate equations were provided to help the designer to properly evaluate the maximum accuracy achieved. The proposed methodology presents two benefits. The first one is to avoid application failure or performance worse than design specification, due to the assumption made in the design phase that the insertion of a trim circuit will always be able to mitigate the performance degradation due the fabrication process. The second benefit results from reduced trim range, which avoids unnecessary area overhead and reduces test time, what leads to reduced fabrication cost.

5 CONCLUSIONS

More than forty years have passed since the Bandgap technique was proposed and today it is a commercial standard used in integrated circuits design for many applications. This work covers in detail the issues involving the design of Bandgap Voltage References. It discussed the principle of operation, traditional topologies used to implement the concept and a historical view about the development of this technique.

The study and discussions were supported by three cases of studies: BGR1, BGR2 and BGR3. The first two architectures are first-order references, while the third achieves second-order compensation through resistor ratio with different materials. These circuits were designed (Schematic and Layout view) in a 0.18 μm IBM CMOS technology. Besides the information such as power dissipation and silicon area, post-layout simulations were run to verify the performance parameters such as temperature coefficient, line regulation and power supply rejection rate.

Due to the large demand for portable equipments, the designed circuits were investigated with respect to low-voltage and low-power requirements. These topologies did not perform well with supply voltage less than about 1.5 V, and then, other architecture should be used. The three main methods presented in the literature to overcome this restriction were discussed.

The impact of fabrication process effects on the performance of the Bandgap reference was investigated. Besides the identification of the main error sources due to the variability, the possible variation of the output voltage after fabrication was estimated by means of simulations. It was shown that V_{REF} of real circuits can have a variation of more than 50 mV compared with the nominal value. This variation leads to a temperature performance worse than 100 ppm/°C. For the mitigation of these effects, some design and layout techniques were presented in the text.

The noise in integrated Bandgap references was also studied in this work. The noise generated by integrated devices was estimated by means of Noise Spectrum Simulations and the main noise sources were identified. Through the PSR simulations, the vulnerability of the references circuits to the noise coming from supply voltage also was analyzed.

Finally, special investigation about the impact of variability and noise in the performance of Bandgap references was presented. It was shown that the noise can limit the accuracy achieved by one circuit and then, this parameter should be incorporated in the methodology to define the trim range.

As future works the author intends to finish the chip containing the designed Bandgap references, for example, adding noise protection, guard rings and PADs. Then, the future chip will be sent to fabrication and real measurements will support this work. Moreover, the author intends to continue the investigation about the impact of noise and variability in the performance of submicrometer analog CMOS circuits. Blocks such as data converters, sample and hold, voltage references and operational amplifier will be studied.

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ANNEX A EXAMPLES OF COMMERCIAL BGR´S CHIPS AND THEIR PERFORMANCE PARAMETERS

Table A.1: Examples of Commercial BGR chips

Parameters	Devices		
	ADR380	LM4121	REF3212
Output Voltage (V)	2.048	1.250/Adjustable	1.25
Initial Accuracy (± mV)	5	2.5	2.5
Typical TC (ppm/ºC)	5	14	4
Worse TC (ppm/ºC)	25	50	7
Temp. Range (ºC)	-40 to +85	-40 to +85	0 to +125
Line Regulation (ppm/V)	25 (92 dB)	70 (83 dB)	65 (84 dB)
Load Regulation (ppm/mA)	70	70	60
Voltage Noise (µV) p-p (0.1 Hz to 10 Hz)	5	20	17
Supply Voltage	2.4 to 18	1.8 to 14	1.8 to 5.5
Max Quiescent Current (µA)	120	250	120
Number of Pins	3	5	6
Manufacturer	Analog Devices (2000)	National Semiconductor (2004)	Texas Instruments (2006)

ANNEX B MAIN PARAMETERS OF IBM 0.18 μM 7RF TECNOLOGY

Table B.1: Model Parameters of IBM 0.18 Micron 7RF technology

	NMOS	PMOS	Unit	Description
Minimum Channel L	0.18		μm	Minimum Channel Length
VDD	1.8		V	Power supply
C_{OX}	7.81135E-7		F/ cm^2	Oxide Capacitance/unit area
μ_0	273.85	121.47	cm^2/V.S	Carrier Mobility
β	106.96	47.44	μA	$\beta=1/2.\ \mu_0.\ C_{OX}$
V_{T0}	0.3	-0.42	V	Threshold voltage
T_{OX}	4.5		nm	Thickness of the oxide
CGB0	1E-12		F/μm	gate-bulk overlap capacitance/channel length
CGD0	4.24E-10	4.88E-10	F/μm	gate-drain overlap capacitance/channel length
CGS0	4.24E-10	4.88E-10	F/μm	gate-source overlap capacitance/channel length
N_{CH}	2.3549E17	4.1589E17	cm^{-3}	Channel Doping Concentration
I_{DSAT}	600	260	mA	Maximum Current
I_{OFF}	<80 at 25 °C		pA/μm	Gate leakage

Below there is a list all the typical SPICE parameters for the NMOS and PMOS devices in this fabrication process for a specific run presented in June of 2007 – (MOSIS.).

```
T74P SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jun 27/07
* LOT: T74P                  WAF: 2001
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                 LEVEL = 49
+VERSION = 3.1            TNOM    = 27              TOX   = 4.5E-9
+XJ      = 1E-7           NCH     = 2.3549E17       VTH0  = 0.2966698
+K1      = 0.482494       K2      = -0.0118737      K3    = 1E-3
+K3B     = 5.0195709      W0      = 1E-7            NLX   = 2.443731E-7
+DVT0W   = 0              DVT1W   = 0               DVT2W  = 0
+DVT0    = 0.6100514      DVT1    = 0.2724406       DVT2 = -0.1878828
+U0      = 273.8484866    UA      = -1.525788E-9    UB   = 2.786859E-18
+UC      = 4.943779E-11   VSAT    = 9.768529E4      A0   = 0.9881723
+AGS     = 0.1424763      B0      = 6.152611E-7     B1   = 5E-6
+KETA    = -3.304026E-4   A1      = 5.748842E-4     A2   = 0.8367628
+RDSW    = 150            PRWG    = 0.2308827       PRWB = -0.1982018
+WR      = 1              WINT    = 5.351515E-9     LINT = 2.047149E-8
+DWG     = 6.185345E-9    DWB     = 1.497881E-8     VOFF = -0.0821831
+NFACTOR = 2.2623633      CIT     = 0               CDSC = 2.4E-4
+CDSCD   = 0              CDSCB   = 0               ETA0 = 4.046676E-3
+ETAB    = -8.738959E-4   DSUB    = 6.503103E-3     PCLM = 0.1698941
+PDIBLC1 = 0.1699085      PDIBLC2 = 0.01            PDIBLCB = -0.1
+DROUT   = 0.718344       PSCBE1  = 6.626429E9      PSCBE2= 5.0049E-10
+PVAG    = 3.150808E-3    DELTA   = 0.01            RSH     = 6.3
+MOBMOD  = 1              PRT     = 0               UTE     = -1.5
+KT1     = -0.11          KT1L    = 0               KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18       UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0               WLN     = 1
+WW      = 0              WWN     = 1               WWL     = 0
+LL      = 0              LLN     = 1               LW      = 0
+LWN     = 1              LWL     = 0               CAPMOD  = 2
+XPART   = 0.5            CGDO    = 4.24E-10        CGSO    = 4.24E-10
+CGBO    = 1E-12          CJ      = 8.15989E-4      PB      = 0.8275674
+MJ      = 0.5396637      CJSW    = 1.810068E-10    PBSW    = 0.8
+MJSW    = 0.2976049      CJSWG   = 3.3E-10         PBSWG = 0.8
+MJSWG   = 0.2976049      CF      = 0               PVTH0= -8.56735E-3
+PRDSW   = 1.000265       PK2     = 8.303493E-3     WKETA= -4.059848E-3
+LKETA   = 7.331573E-3    PU0     = -5.6063179      PUA  = -4.59486E-11
+PUB     = 8.833639E-25   PVSAT   = 264.8251904     PETA0= 4.288957E-5
+PKETA   = -0.0330423)
*
.MODEL CMOSP PMOS (                                 LEVEL   = 49
+VERSION = 3.1            TNOM    = 27              TOX     = 4.5E-9
+XJ      = 1E-7           NCH     = 4.1589E17       VTH0  = -0.4202777
+K1      = 0.6047591      K2      = 6.28672E-5      K3     = 0.0894478
+K3B     = 19.8158346     W0      = 1E-6            NLX  = 3.630182E-8
+DVT0W   = 0              DVT1W   = 0               DVT2W   = 0
+DVT0    = 0.6580732      DVT1    = 0.5053159       DVT2    = -0.3
```

```
+U0      = 121.4745117    UA      = 1.651983E-9    UB   = 2.065745E-21
+UC      = -1E-10         VSAT    = 1.862502E5     A0     = 0.7274068
+AGS     = 0              B0      = 1.301942E-6    B1     = 5E-6
+KETA    = 0.0239822      A1      = 0.0619585      A2     = 0.4356847
+RDSW    = 803.0213469    PRWG    = -0.1160769     PRWB = -0.4734383
+WR      = 1              WINT    = 0              LINT = 2.903067E-8
+DWG     = -2.848501E-8   DWB     = -1.216193E-8   VOFF  = -0.1297937
+NFACTOR = 1.4885005      CIT     = 0              CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0              ETA0 = 1.131083E-11
+ETAB    = -2.286341E-3   DSUB    = 3.993284E-3    PCLM    = 0.1076345
+PDIBLC1 = 0.0708272      PDIBLC2 = 0.0235091      PDIBLCB = -1E-3
+DROUT   = 0.4412591      PSCBE1  = 1.64623E9      PSCBE2  = 5E-10
+PVAG    = 7.05729E-3     DELTA   = 0.01           RSH     = 6
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 4.88E-10       CGSO    = 4.88E-10
+CGBO    = 1E-12          CJ      = 1.165977E-3    PB      = 0.8214639
+MJ      = 0.4256548      CJSW    = 1.220056E-10   PBSW    = 0.8008
+MJSW    = 0.1001         CJSWG   = 4.22E-10       PBSWG   = 0.8008
+MJSWG   = 0.1001         CF      = 0              PVTH0= 1.02743E-4
+PRDSW   = -5             PK2     = 9.320893E-5    WKETA   = 0.0307312
+LKETA   = -0.0129391     PU0     = 1.7611588      PUA  = 1.189658E-10
+PUB     = 0              PVSAT   = 50             PETA0   = 1E-4
+PKETA   = -3.992172E-3)
*
```

APPENDIX A SUMMARY IN PORTUGUESE (RESUMO DA DISSERTAÇÃO)

REFERÊNCIAS DE TENSÃO BANDGAP EM TECNOLOGIAS CMOS SUBMICROMÉTRICAS

1 INTRODUÇÃO

Um circuito referência de tensão provê uma tensão estável e precisa que é usada para a polarização de outros circuitos do sistema eletrônico. Referências são consequentemente circuitos essenciais no projeto de diversos blocos analógicos, como por exemplo, reguladores de tensão, conversores de dados e conversores de potência.

A referência produz uma saída que é independente da tensão de alimentação, temperatura de operação e dos efeitos causados pelo processo de fabricação. Além disso, esse circuito deve ter alta precisão, baixo ruído de saída e boa estabilidade em termos de tempo de uso. Por fim é portante acrescentar que devido a atual larga demanda por produtos embarcados alimentados por bateria, os circuitos referência de tensão devem operar sob baixa tensão de alimentação e consumindo pouca potência.

O circuito Bandgap é a forma mais popular de se implementar referências de tensão. A origem dessa técnica foi o trabalho publicado por Hilbiber em 1964. Este trabalho apresenta um estudo detalhado das referências de tensão Bandgap. Serão estudados o princípio de operação, as topologias tradicionalmente usadas para implementar esse método e suas limitações principalmente quando novos processos de fabricação são utilizados. Além disso, será apresentada uma visão geral das principias tendências de pesquisa nessa área. Também serão investigadas questões como alta precisão, baixa tensão de operação e baixo consumo de potência e ruído de saída.

Uma investigação especial sobre o impacto do processo de fabricação na performance do circuito Bandgap também será apresentado. Para desenvolver nosso trabalho, três circuitos de referência Bandgap foram projetados (esquemático e leiaute) usando a tecnologia IBM 0.18 Micron 7RF.

2 REFERÊNCIAS DE TENSÃO BANDGAP

O circuito de referência de tensão Bandgap produz uma tensão de saída (V_{REF}) com baixa dependência com a temperatura e tensão de alimentação. O nome “Bandgap” é porque o valor da tensão de referência é aproximadamente 1.166 V, que é a banda de energia proibida do silício extrapolado para zero Kelvin.

Por meio de um circuito Bandgap é possível gerar, por exemplo, uma tensão de referência com coeficiente térmico da ordem de 40 (Brito, 2007) ou até 3 ppm/°C (Yao, 2005). Existem muitos circuitos que implementam a técnica Bandgap, e geralmente, cada um deles alcança uma determinada performance e precisão. Portanto, é o tipo da aplicação que irá definir qual circuito Bandgap deve ser usado no projeto.

A pequena dependência de V_{REF} com relação à faixa de temperatura de operação é obtida através da soma de duas tensões com coeficientes de temperatura opostos, como descrito pela equação 2.2. Normalmente a tensão que aumenta com a temperatura é chamada de tensão proporcional à temperatura absoluta (PTAT), e a tensão que diminui com a temperatura é chamada de complementarmente proporcional à temperatura absoluta (CTAT) (Razavi, 2001).

A técnica mais difundida para gerar as tensões com coeficientes térmicos opostos faz uso da tensão do diodo ou base-emissor do bipolar. Seu grande uso é devido à alta estabilidade contra o processo de fabricação e sua bem conhecida dependência com a temperatura.

Através dos bipolares, é possível criar uma tensão que é proporcional à tensão térmica. Uma soma balanceada da tensão térmica com a tensão base-emissor de um transistor bipolar gera a tensão de saída do circuito bandgap. No entanto, devido não-linearidades presentes nessa soma, é possível que a tensão de saída apresente um coeficiente térmico da ordem de 20 até 100 ppm/°C.

3 TRÊS CIRCUITOS DE REFERÊNCIA BANDGAP

O capítulo 3 apresenta os três circuitos de referência de tensão Bandgap projetados em tecnologia CMOS IBM 0.18 μm. São apresentadas as simulações da tensão de saída em função da temperatura de operação e tensão de alimentação. Também são apresentados as simulações de PSRR (*power supply rejection rate*).

O primeiro circuito usa uma fonte de corrente e transistores *cascode* para gerar a tensão proporcional com a temperatura. Então, a soma balanceada dessa tensão com a tensão base-emissor de um transistor bipolar vertical parasita gera a tensão de referência. Esse circuito atinge uma performance térmica de 26 ppm/°C e uma dependência com relação à alimentação de 35 mV/V.

O segundo circuito usa um amplificador operacional para gerar a tensão proporcional com a temperatura, e consequentemente a tensão de saída. A performance térmica alcançada é igual ao primeiro circuito, no entanto a dependência com relação à alimentação é reduzida de 40 vezes.

O terceiro circuito usa técnicas de compensação de não-linearidades para alcançar uma dependência com relação à temperatura de 3 ppm/°C. Essa topologia difere do BGR2 por apenas um resistor extra. A tensão não-linear gerada no circuito para se alcançar essa compensação das não-linearidades intrínsecas é gerada através da razão de dois resistores fabricados com diferentes materiais.

4 QUESTÕES SOBRE BAIXA TENSÃO DE ALIMENTAÇÃO/POTÊNCIA CONSUMIDA, RUÍDO E VARIABILIDADE

Este capítulo trata de três assuntos pertinentes no projeto de referências de tensão: (a) necessidade de operação com baixa tensão de alimentação e baixo consumo, (b) variabilidade causada pelo processo de fabricação e (c) ruído de saída.

Inicialmente é mostrado que as topologias tradicionais são limitadas a serem usadas com uma tensão de alimentação de pelo menos 1.5 V, o que pode não ser viável que requerem baixo consumo e baixa alimentação. Então são mostrados os três principais

métodos difundidos na literatura para superar esse obstáculo e projetar circuitos Bandgap com tensões de alimentação até menores que 1 V.

O impacto do processo de fabricação na performance dos circuitos de referência Bandgap também é investigado. São mostradas quais são as principais fontes de erros, e então os três circuitos projetados são usados como caso de estudo para se estimar a degradação de performance.

Depois da variabilidade, é discutido outro fator que também limita a precisão da tensão de saída: o ruído. Como no caso dos efeitos de fabricação, cada fonte de ruído é identificada e os três circuitos são simulados para se checar qual é o impacto total do ruído na tensão de referência. Por fim, o ruído e a variabilidade são juntos levados em conta no projeto de circuitos de referência e seus circuitos de ajuste.

5 CONCLUSÕES

Mais de 40 anos se passaram desde que à técnica Bandgap foi proposta, e hoje, este tipo de circuito é usado em muitos circuitos comerciais. Sua comprovada performance em relação à temperatura de operação faz com que este método seja o mais difundido em se tratando de referência de tensão.

Três circuitos Bandgap foram projetados e estudados em detalhes. As referências apresentadas são as topologias bases para o projeto de muitas referências complexas propostas na literatura. Portanto a partir do conhecimento mostrado aqui é possível entender o funcionamento básico de qualquer referência de tensão Bandgap.

Como o desempenho do circuito Bandgap depende da variabilidade causada pelo processo de fabricação e do ruído de saída, essas questões foram investigadas. Por meio de simulações Monte Carlo, e simulação do espectro do ruído foram possíveis estimar o impacto do ruído e do processo de fabricação no desempenho da referência Bandgap. Além disso, especial investigação foi realizada à respeito do impacto final do ruído e da variabilidade no projeto de circuitos de ajuste.

Por fim, os circuitos projetados também foram estudados em termos dos requisitos de baixa tensão de alimentação e baixo consumo. Uma vez identificada a limitação de essas topogias operarem com uma alimentação abaixo de aproximadamente 1.5 volts, foram sugeridos outras técnicas que superaram essa restrição.

APPENDIX B FIGURES

This appendix presents some figures not shown in the text.

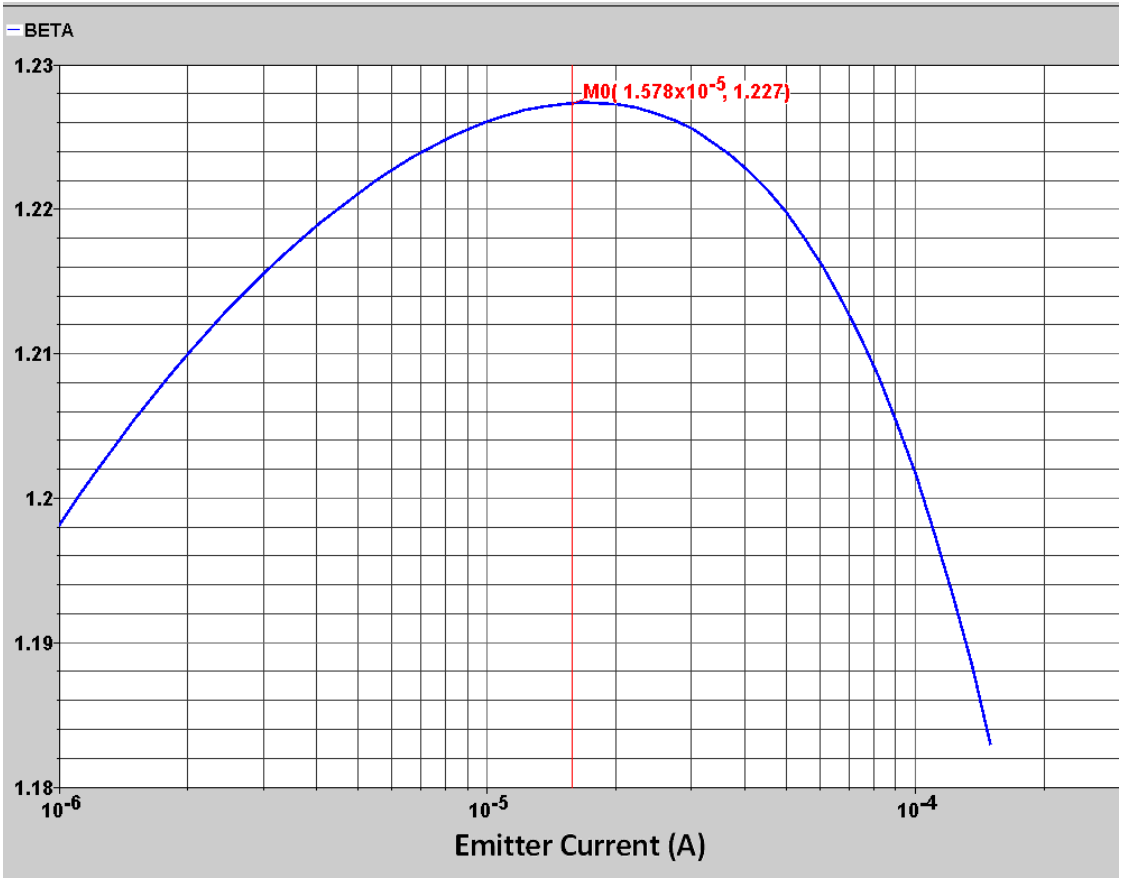

Figure B.1: βF as a function of Emitter Current

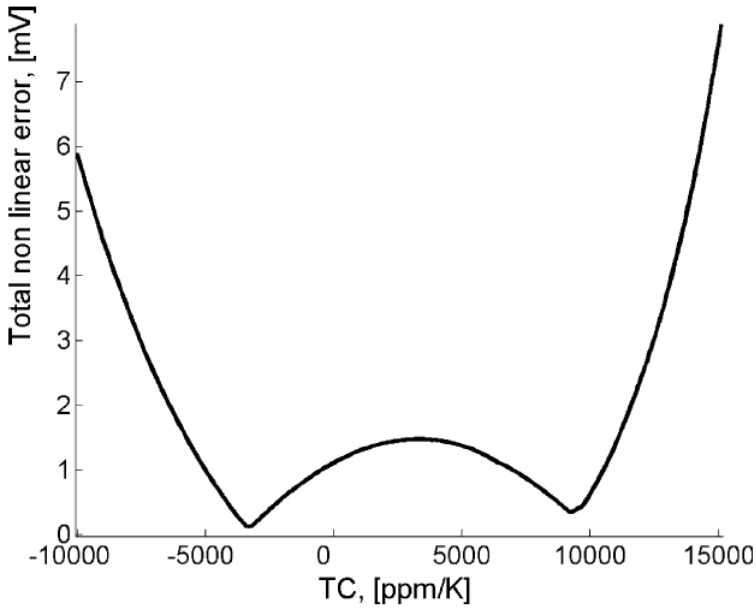

Figure B.2: Non-Linear output error in a function of temperature coefficient of the resistor (FALCONI, 2005)

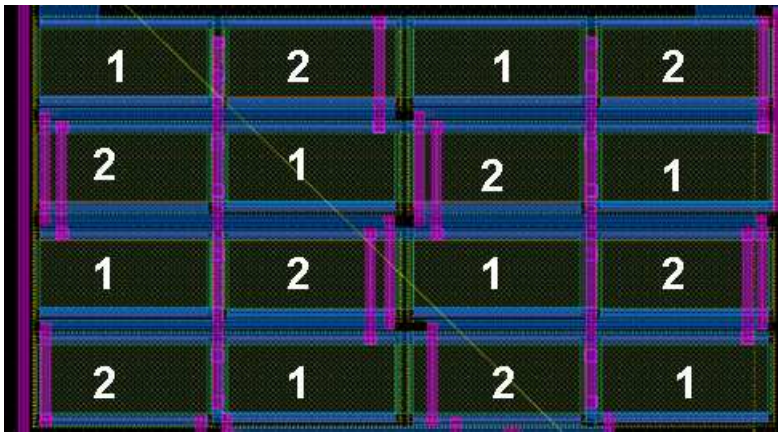

Figure B.3: M_1 and M_2 in common centroid configuration – BGR1

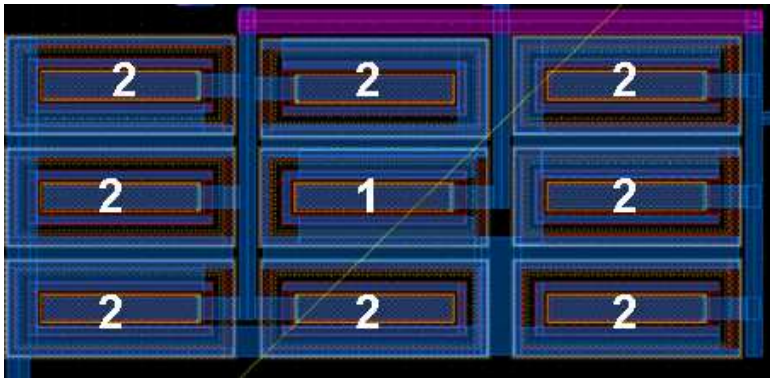

Figure B.4: 8x1 BJT´s in common centroid configuration – BGR1, BGR2 and BGR3

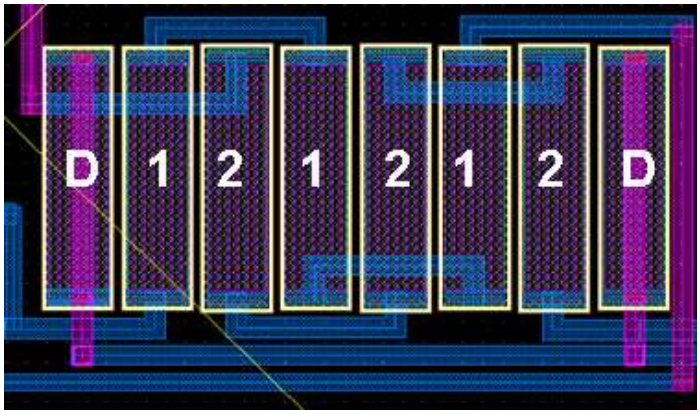

Figure B.5: Matched Resistors in common centroid configuration of BGR1

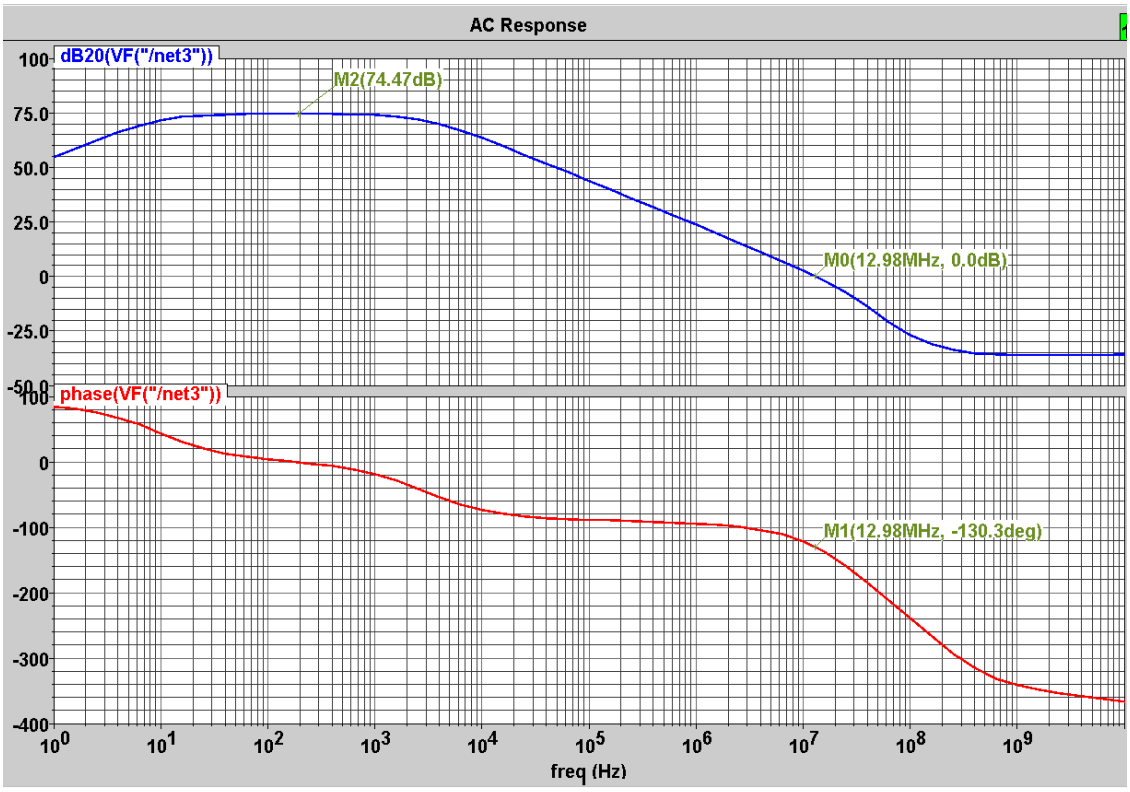

Figure B.6: Bode Diagram of Operational Amplifier used in BGR2 and BGR3

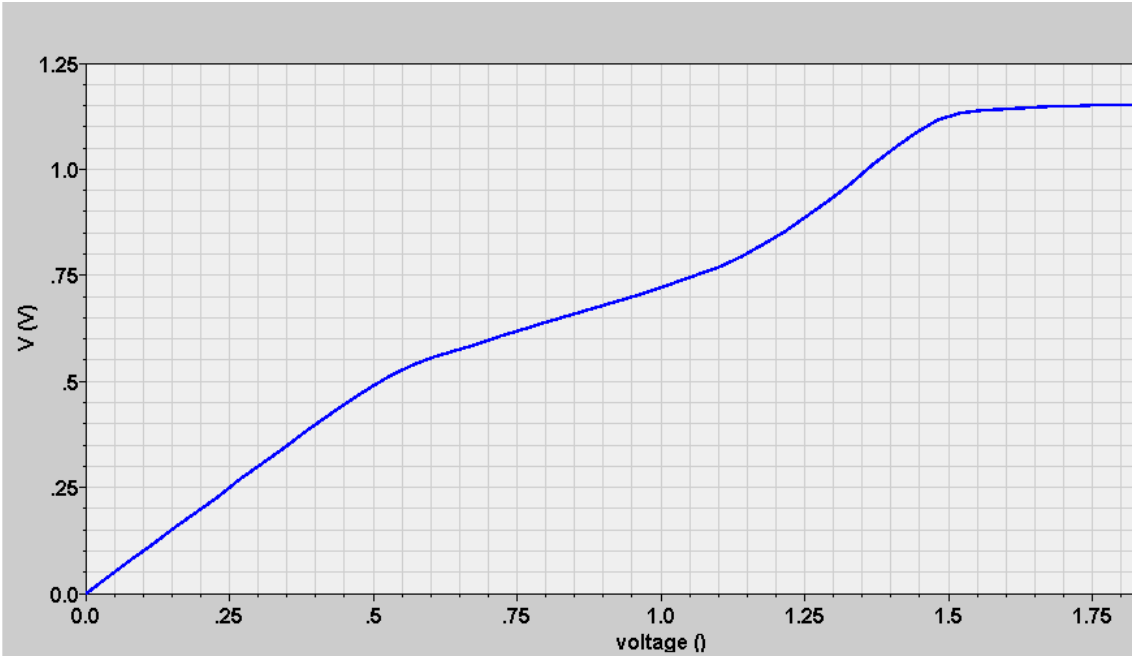

Figure B.7: V_{REF} as a function of supply voltage of BGR1

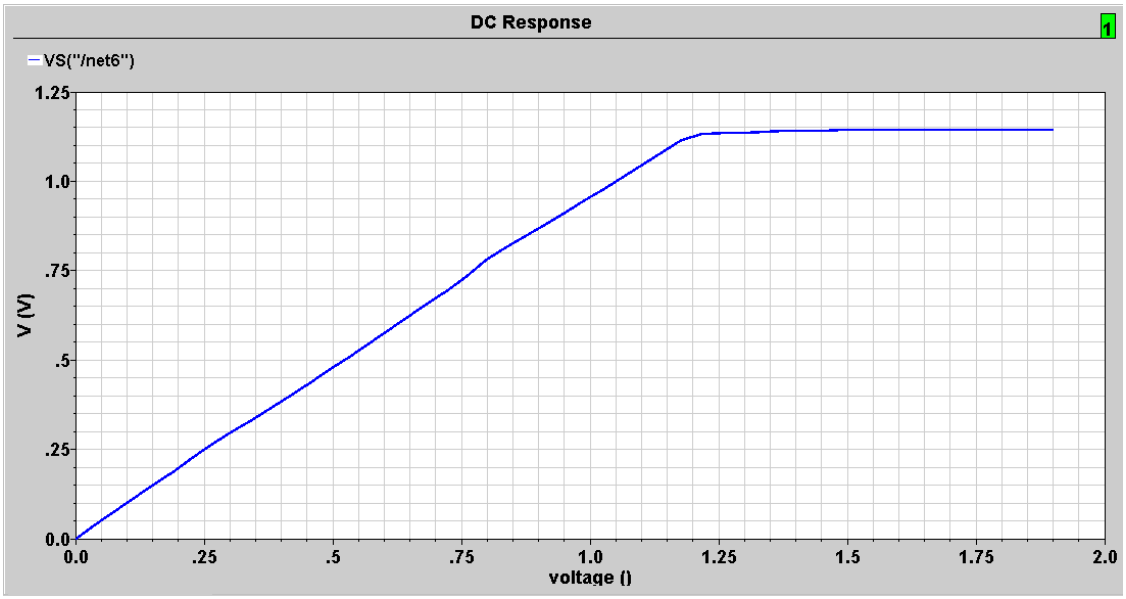

Figure B.8: V_{REF} as a function of Supply Voltage for BGR3

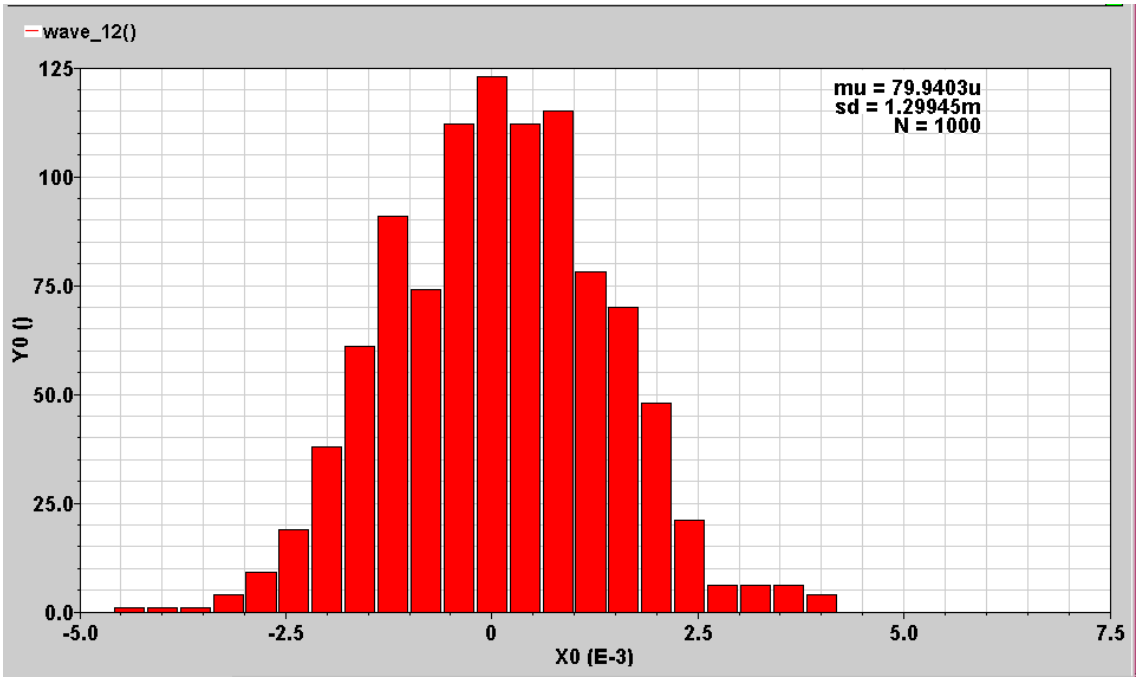

Figure B.9: Monte Carlo Analysis of V_{OS} for opamp used in BGR2 and BGR3

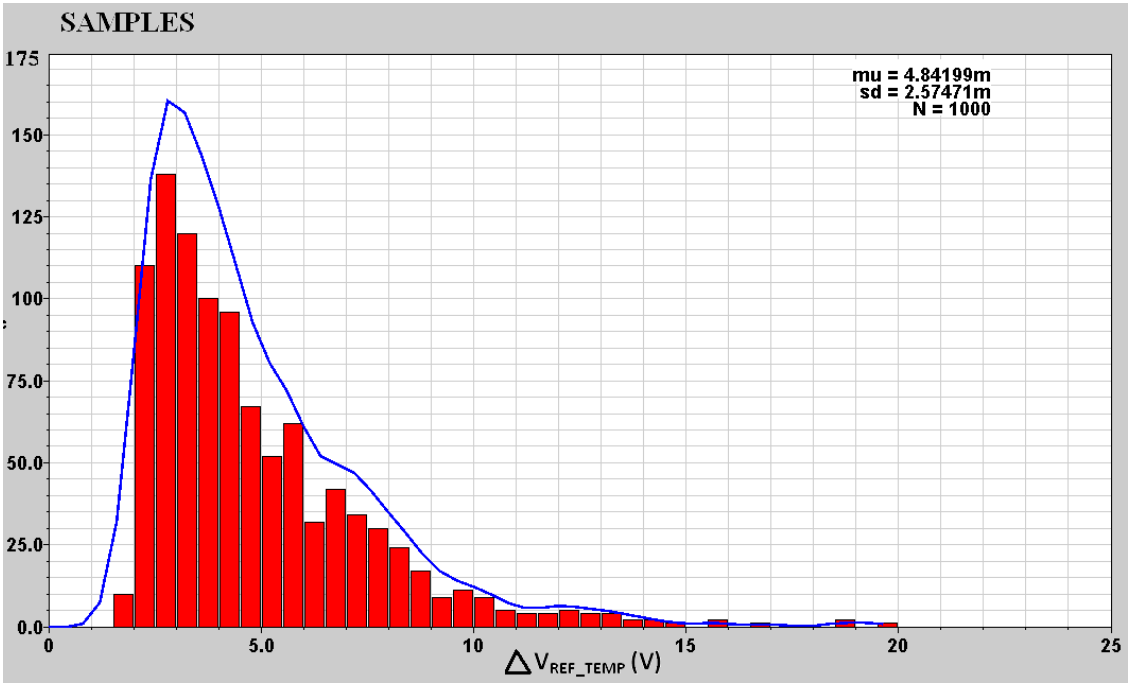

Figure B.10: Monte Carlo Analysis of ΔV_{REF_TEMP} for BGR2

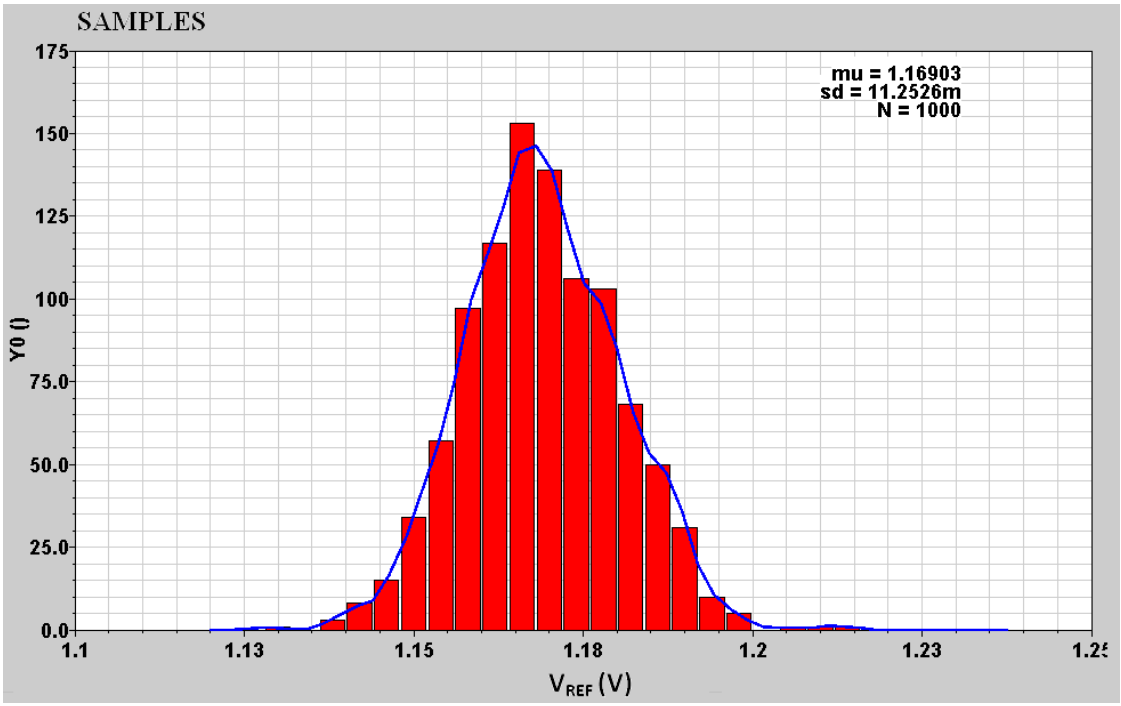

Figure B.10: Monte Carlo Analysis for V_{REF} of BGR2

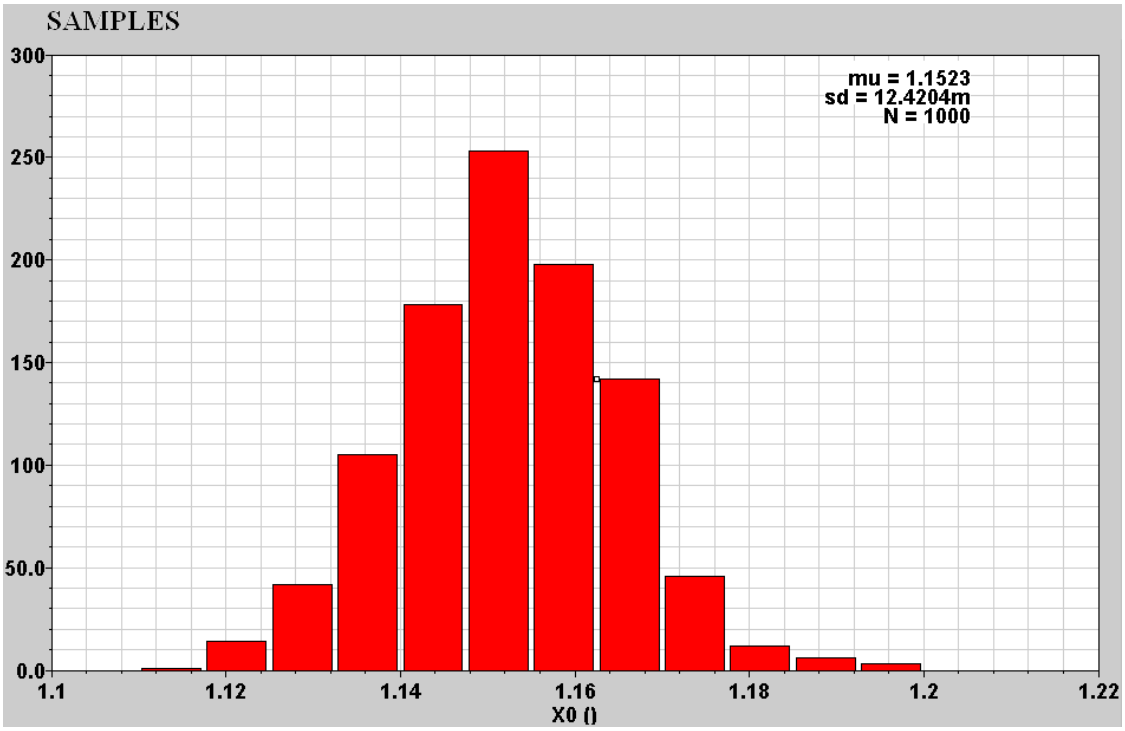

Figure B.11: Monte Carlo Analysis for V_{REF} of BGR3

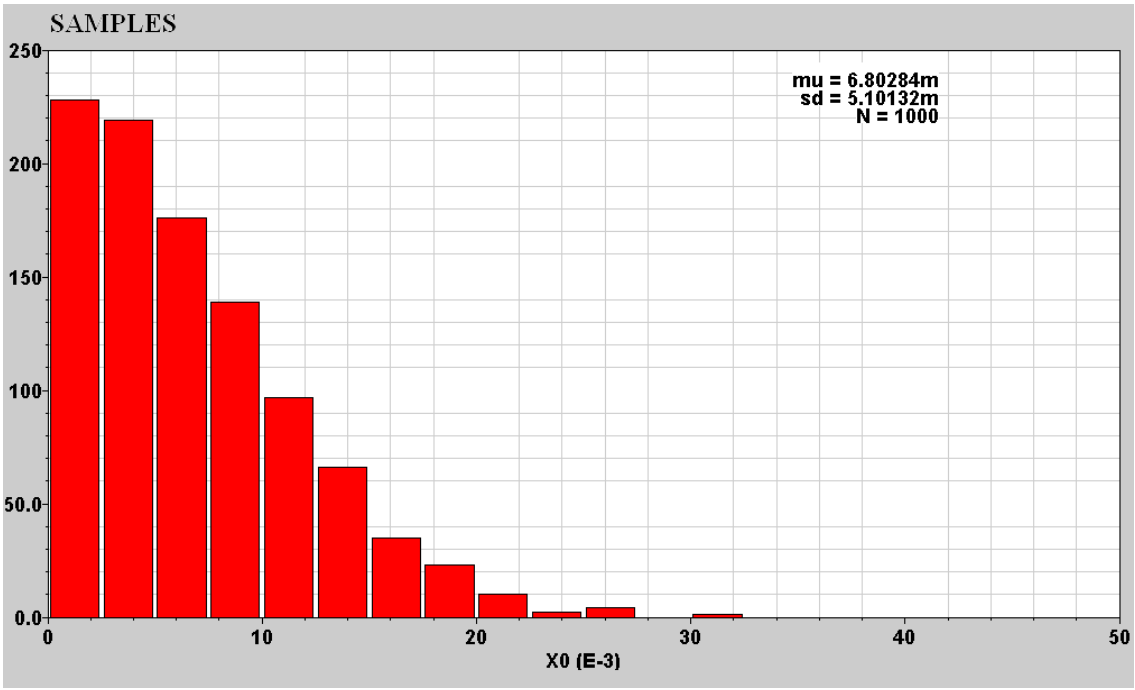

Figure B.12: Monte Carlo Analysis of ΔV_{REF_TEMP} for BGR3

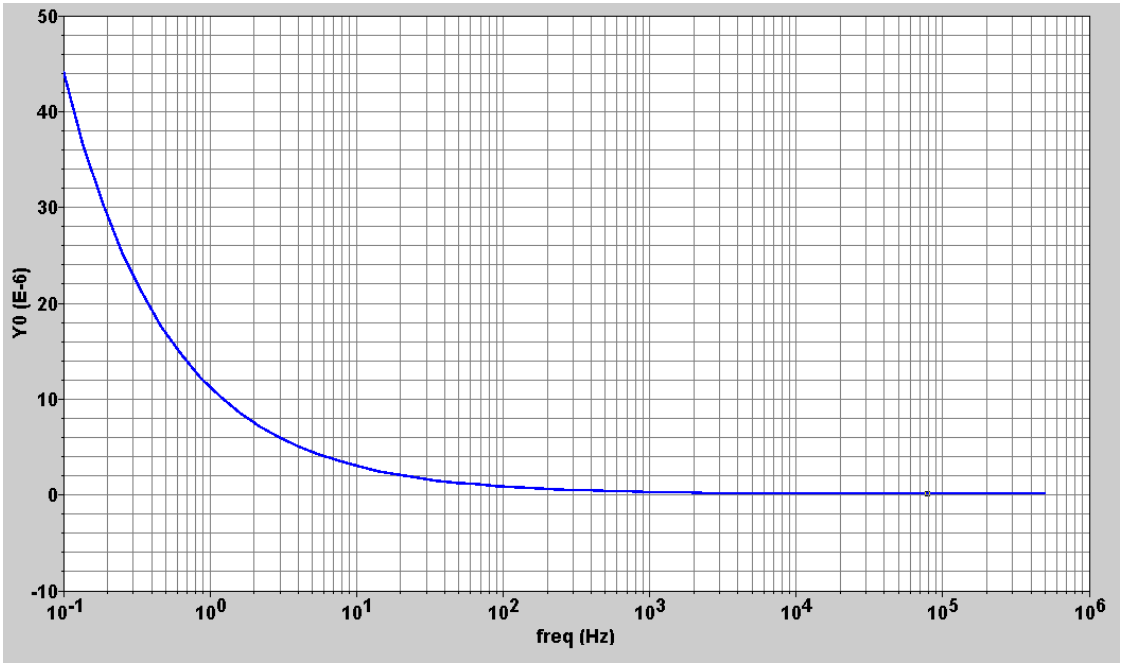

Figure B.13: Output noise Spectrum for BGR1

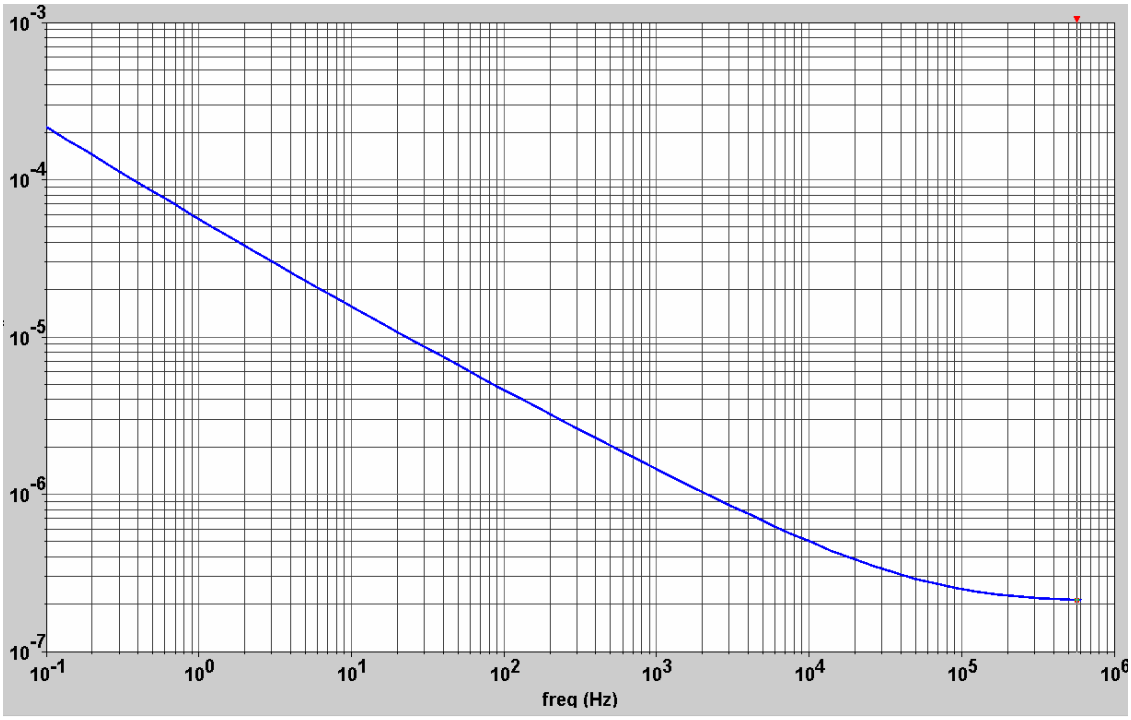

Figure B.14: Output noise Spectrum for BGR3 (Noise axis in log)

APPENDIX C DERIVATION OF V_{REF} FOR BGR3

Equations C.1 and C.2 represent the output voltage of BGR3 and the temperature coefficient of one resistor respectively.

$$V_{REF} = V_{TH} \cdot \ln(n) \cdot \frac{R_2}{R_1} + V_{TH} \cdot \ln(n) \cdot \frac{R_4}{R_1} + V_{BEQ2} \tag{C.1}$$

$$TC = \frac{1}{R} \cdot \frac{\partial R}{\partial T} \tag{C.2}$$

Using equation C.2, the temperature dependency of the ratio R_4/R_1 is showed bellow.

$$\frac{R_4(T)}{R_1(T)} = \frac{R_4(T_0) + TC_{Pdiff} \cdot \Delta T \cdot R_4(T_0)}{R_1(T_0) + TC_{poly} \cdot \Delta T \cdot R_1(T_0)} = \frac{R_4(T_0) \cdot \left(1 + TC_{Pdiff} \cdot \Delta T\right)}{R_1(T_0) \cdot \left(1 + TC_{poly} \cdot \Delta T\right)} \tag{C.3}$$

Multiplying C.3 by $\left(1 - K_{poly} \cdot \Delta T - K_{poly}^2 \cdot \Delta T^2\right)$, equation C.4 is found.

$$\begin{aligned} \frac{R_4(T)}{R_1(T)} = \frac{R_4(T_0)}{R_1(T_0)} \cdot \frac{1 + \Delta T\left(TC_{Pdiff} - TC_{poly}\right) + \Delta T^2\left(-TC_{poly}^2 - TC_{poly} \cdot TC_{Pdiff}\right)}{\left(1 - TC_{poly}^3 \cdot \Delta T^3\right)} \\ - \frac{\Delta T^3\left(TC_{poly}^2 \cdot TC_{Pdiff}\right)}{\left(1 - TC_{poly}^3 \cdot \Delta T^3\right)} \end{aligned} \tag{C.4}$$

If one despises the high-order terms and consider a temperature range (ΔT) at maximum of 100°C, equation C.4 is simplified in C5.

$$\frac{R_4(T)}{R_1(T)} = \frac{R_4(T_0) \cdot \left[1 + \left(TC_{Pdiff} - TC_{poly}\right) \cdot \Delta T\right]}{R_1(T_0)} \tag{C.5}$$

Then, if C.5 is substituted in C.1, equation C.6 is provided – Output voltage of BGR3.

$$\begin{aligned} V_{REF} = & \left(\frac{R_2}{R_1} + \frac{R_4(T_0)}{R_1(T_0)}\right) \cdot \ln(n) \cdot V_{TH} \\ & + \frac{R_4(T_0)}{R_1(T_0)} \cdot \left(TC_{Pdiff} - TC_{poly}\right) \cdot \ln(n) \cdot \Delta T \cdot V_{TH} + V_{BEQ2} \end{aligned} \tag{C.6}$$