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**High Efficiency MPPT Switched Capacitor
DC - DC Converter for Photovoltaic Energy
Harvesting Aiming for IoT Applications**

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of the requirements for the degree of
Master of Microelectronics

Advisor: Prof. Dr. Hamilton Klimach

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*“The saddest aspect of life right now is that Science gathers
Knowledge faster than Society gathers Wisdom”*

— ISAAC ASIMOV

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ABSTRACT

This work presents a six phase Switched Capacitor (SC) DC - DC converter for photovoltaic Energy Harvesting designed in a 130 nm CMOS process for commercial motes application and Internet of Things (IoT). It tracks the Maximum Power Point (MPP) of a commercial 3 cm x 3 cm 60 mW polycrystalline photoelectric panel through switching frequency modulation aiming battery recharge. Open-circuit voltage ratio was the chosen Maximum Power Point Tracking (MPPT) strategy. The converter achieves a maximum power conversion efficiency of 90 % for input power higher than 30 mW and is designed to operate with input voltages from 1.25 V to 1.8 V, resulting output voltages from 2.5 V to 3.6 V, respectively. Peripheral circuitry also includes an output over-voltage protection of 3.6 V and the control circuits, that consumes a total of 850 μ A at 3.3 V of static power. Complete layout consumes 300 x 700 μ m² of silicon area. The only external components are 6x100 nF capacitors.

Keywords: Switched Capacitor. DC-DC converter. Photovoltaic Energy Harvesting. IoT. MPPT. CMOS.

Conversor DC - DC de Alta Eficiência baseado em Capacitores Chaveados usando MPPT com o Objetivo de Coletar Energia Fotovoltaica com Foco em Aplicações IoT

RESUMO

Este trabalho apresenta um conversor CC - CC baseado em Capacitores Chaveados de 6 fases e tempos intercalados com o objetivo de coletar energia fotovoltaica projetado em tecnologia CMOS de 130 nm para ser usado em aplicações em Internet das Coisas e Nós Sensores. Ele rastreia o máximo ponto de entrega de energia de um painel fotovoltaico policristalino de 3 cm x 3 cm através de modulação da frequência de chaveamento com o objetivo de carregar baterias. A razão da tensão de circuito aberto foi a estratégia de rastreamento escolhida. O conversor foi projetado em uma tecnologia CMOS de 130 nm e alcança uma eficiência de 90 % para potências de entrada maiores do que 30 mW e pode operar com tensões que vão de 1.25 até 1.8 V, resultando em saídas que vão de 2.5 até 3.6, respectivamente. Os circuitos periféricos também incluem uma proteção contra sobre tensão na saída de 3.6 V e circuitos para controle, que consomem um total máximo de potência estática de 850 μ A em 3.3 V de alimentação. O layout completo ocupa uma área de 300 x 700 μ m² de silício. Os únicos componentes não integrados são 6x100 nF capacitores.

Palavras-chave: Capacitor Chaveado, Conversor CC - CC, Coleta de Energia Fotovoltaica, IoT, MPPT, CMOS.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternate Current
CMOS	Complementary Metal-Oxide-Silicon
CP	Charge-Pump
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
EH	Energy Harvesting
ESR	Equivalent Series Resistance
FSL	Fast-Switching Limit
IoT	Internet of Things
MOS	Metal-Oxide-Silicon
MOSFET	Metal-Oxide-Silicon Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NMOS	N-type Metal-Oxide-Silicon Field-Effect Transistor
PCB	Printed Circuit Board
PMOS	P-type Metal-Oxide-Silicon Field-Effect Transistor
PV	Photovoltaic
RF	Radio Frequency
SC	Switched Capacitor
SSL	Slow-Switching Limit
TEG	Thermoelectric Generator
ULP	Ultra-Low Power
VCO	Voltage - Controlled Oscillator
WSN	Wireless Sensor Network

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1 INTRODUCTION

Internet is one of the most important and powerful tools developed by the human race. It molded our society, education, business and connected the world. In 2010, there were 12.5 billion devices connected to the internet, what is a number higher than the global population. This absurd amount is responsible for letting the Internet in continual evolution and the Internet of Things (IoT) is the next step in this path. (EVANS, 2011)

Internet of Things is the concept of connecting all possible devices to the Internet. Cisco IBSG of 2011 predicts that will be 50 billion of connected devices by 2020. This huge amount and variety of devices will generate an amount of data traffic never seen before. This "Big Data" is a challenge to be faced together by academy, governments, business, and industry. (EVANS, 2011)

Wearables, implantables, medical devices and local sensors are part of the IoT world. These kind of devices face their own challenges, the main one is Autonomy. The desirable is that the gadgets could last as much as possible without the need of a battery recharge. It brought the necessity of Ultra-Low Power (ULP) devices that can sense, process data and communicate consuming the minimum possible.

These two challenges: Big Data and Autonomy are trend topics in academy and industry. The most important international conferences and journals receive a significant amount of works focused on those problems. They face these problems at different levels: applications, systems, architectures, blocks and circuits.

Internet of Things and Wireless Sensor Networks (WSN) were born together. Also called motes or smart dust, WSN is the concept of building networks with smart autonomous compact-device sensor units to obtain different kinds of information. Fig. 1.1 shows a generic scheme of a WSN. The sensor nodes must be capable of collect, receive and transmit information consuming the minimum possible of energy. They create a communication path to the network Gateway that deliveries the collected information to the internet. (ASHTON, 2009)

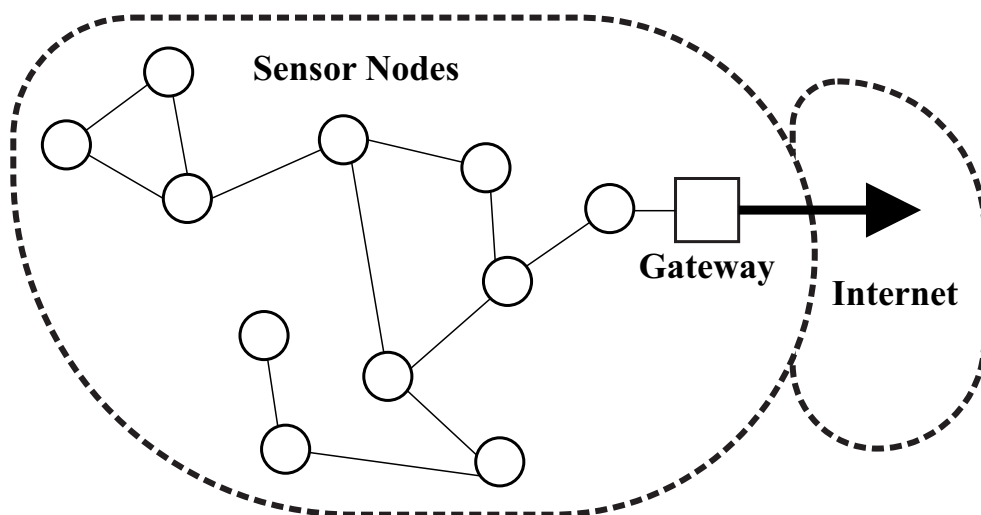
There are countless challenges and trade-offs in the design of a smart node but, two of the critical ones are the operation lifetime and device compactness. An important object that impacts in those aspects, lifetime x compactness, is the battery. Battery density have been increasing and the trade-off limit between sensor nodes operation time and devices size have been pushed towards together, but this is still an object of investigation. (NOORDEN, 2014)

Not only the reducing of consumption is a way to increase autonomy. It is possible, also, to use some Energy Harvesting (EH) strategy. There exists a considerable amount of potential

sources of energy that can be collected by a compact transducer, *e.g.* Thermoelectric Generators (TEGs), Photovoltaic (PV) cells, Ambient RF Signals and Piezoelectric Materials. (SOYATA; COPELAND; HEINZELMAN, 2016)

The MICA2, Fig. 1.2, is an example of a commercial sensor node that has a large variety of integrated sensors in one platform with a multi-channel radio transceiver. This platform includes an Atmel ATmega 128L low power microcontroller and its energy is supplied by two standard alkaline AA batteries that deliver from 2.7 to 3.3 V and supply enough energy for one year of operation using sleep mode. (CROSSBOW TECHNOLOGY, 2010)

Figure 1.1: Wireless Sensor Network: Generic Scheme.



Source: Author.

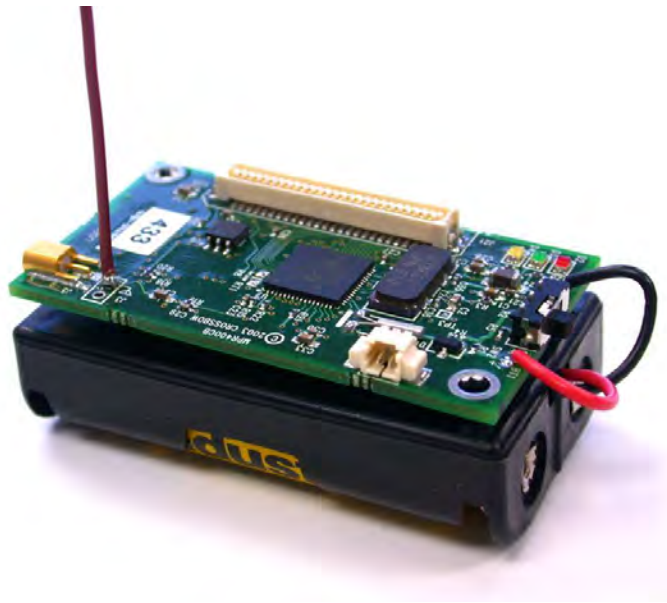
Alkaline AA battery capacity is in the range of 1800 to 2600 mAh of charge or 2700 to 3900 mWh of energy, meaning that one year of active sensor operation with two batteries results in a circuit consumption around 0.6 to 0.9 mW. So if an energy harvesting power source could supply an average power around 0.3 to 0.5 mW every day the sensor node autonomy of MICA2 would be doubled.

The extra power could be harvested from many kinds of environmental sources but usually available high density energy sources are 'light' (using PV cells) and 'heat' (using TEGs). Among the available environmental sources of energy, 'light' is the one that offers higher power density (output electrical power per area or volume) with relatively high output voltage levels, especially for outdoor applications where sunlight can reach PV panels all over the day.

PV cells and TEGs are non-ideal sources of energy, so, the maximum power transfer theorem must be taken into account if one wants to collect the maximum available energy.

Although, it is not possible to achieve the MPP by a direct connection between source and load. A DC-DC converter between the power supply and an energy storage element (battery, capacitor or super-capacitor) overcome this problem and a post DC-DC converter is used to regulate the output voltage. Fig. 1.3 shows a generic scheme described for a PV panel source.

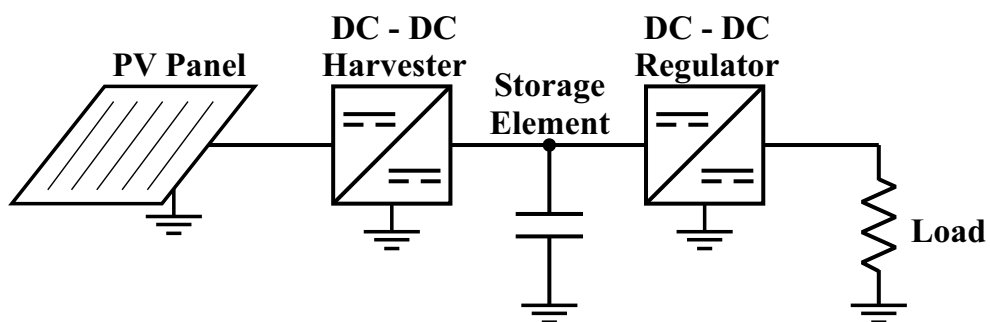
Figure 1.2: MICA2.



Source: (CROSSBOW TECHNOLOGY, 2010)

Usually boost step-up converters based on inductors are employed for this job, like the works (IM et al., 2012) and (BANDYOPADHYAY; CHANDRAKASAN, 2012). But, some newly proposed topologies are based on Switched-Capacitor (SC) strategy for this purpose, like in (LIU et al., 2016) and (LIU; SÁNCHEZ-SINENCIO, 2015), due to the lower intrinsic losses of these kinds of converters. (SANDERS et al., 2013)

Figure 1.3: Generic scheme of a Energy Harvesting DC-DC Conversion.



Source: Author.

1.1 Objectives

In this context, this work proposes an integrated CMOS Switched-Capacitor (SC) DC-DC Converter for Photovoltaic (PV) Energy Harvesting (EH) using a Maximum Power Point Tracking (MPPT) strategy aiming to be employed in Sensor Nodes (SN) at outdoor applications to increase its autonomy. Specifically, the main objectives of this work are to:

1. Energy Harvesting

- Make a review about Energy Harvesting sources;
- Make a review about PV cells;
- Choose and characterize a small PV panel;

2. DC - DC Conversion

- Make a review about DC - DC conversion;
- Make a review about SC DC - DC converters;
- Propose a SC DC - DC converter architecture suitable for the chosen PV panel and battery;
- Design and send for fabrication the proposed converter;

3. Simulation & Measurements

- Obtain and analyze simulation results of the complete DC - DC converter and internal blocks;
- Design, fabricate and montage of the Printed Circuit Board (PCB) for the chip tests;
- Design of an automatic measurement setup;
- Perform and analyze measurements results of the complete DC - DC converter and internal blocks;

1.2 Organization

The work is organized as follows: Chapter 2 presents a review of EH sources like TEGs, RF, piezoelectric and a broad look at PV cells. Chapter 3 gives the basis about DC - DC conversion with a focus on the modeling and behavior of the SC DC - DC ones. The proposed architecture and the design methodology are in Chapter 4. Simulation and some measurement results are presented in Chapter 5. Conclusions and considerations are the focus of Chapter 6.

Finally, the parameters extraction of the used CMOS technology and some tools used in the work are in the Appendix.

2 ENERGY HARVESTING

Energy harvesting happens when a transducer intercepts a "force" carried by a wave or matter and converts into electricity. These waves can be classified in mechanical or electromagnetic, depending on its nature. Wind, sound, and vibration are examples of mechanical waves. Light, microwave, and X-rays are examples of electromagnetic. (SOYATA; COPELAND; HEINZELMAN, 2016)

Each form of energy has its transducer capable of converting it into electricity. Wind turbines convert energy transported by the wind, Thermoelectric generators (TEGs) the heat, Photovoltaic (PV) cells the energy present in photons and piezoelectric materials the energy from vibration. (SOYATA; COPELAND; HEINZELMAN, 2016)

An engineer may want to choose one of these kinds of energies to harvest and use it in an application. The availability of the power source and the transducer characteristics defines if the energy can be collected efficiently or not, this outlines the pros and cons that must be taken into account for the intended application.

The most common energy harvesting sources are ambient RF, piezoelectric, that can be by vibration or push buttons, thermal and solar. Each of these energies has their characteristics and particularities. Tab. 2.1 presents a comparison among them. (KIM et al., 2014)

Table 2.1: Comparison of the energy harvesting sources.

	PV Energy	Thermal Energy	Ambient RF Energy	Piezoelectric Energy	
				Vibration	Push Button
Power Density	100 mW/cm ²	60 μW/cm ²	0.0002 - 1 μW/cm ²	200 μW/cm ³	50 μJ/N
Output	0.5 V (single Si cell) 1.0 V (single a-Si vcell)	-	3 - 4 V (Open circuit)	10 - 25 V	100 - 10000 V
Available Time	Day time (4 - 8 Hrs)	Continuous	Continuous	Activity dependent	Activity dependent
Weight	5 to 10 g	10 to 20 g	2 to 3 g	2 to 10 g	1 to 2 g
Pros	- Large energy - Well developed tech	- Always available	- Ant. integrated - Widely available	- Well developed tech - Light weight	- Well developed tech - Light weight - Small volume
Cons	- Need large area - Non-continuous - Orientation issue	- Need large area - Low power - Rigid and brittle	- Distance dependent - Available source	- Need large area - Variable output	- Highly variable output - Low conversion efficiency (high volt./low amps.)

Source: (KIM et al., 2014).

The ambient RF energy is still a technology in development. It presumes a considerable distance between the transmitter and the receiver, >5 m, so a small amount of energy can be

collected and, alone, it is not capable of supplying the most of the applications. Like the TEGs, it is possible to harvest ambient RF energy all day.

Piezoelectric energy is a well-developed technology, but depends on the activity of the application, since, mechanical force must be applied continuously. Also, a little amount of energy can be harvest due to power density and critical electrical characteristics, high voltage and low current, what is not suitable for a high-efficiency voltage conversion. (KIM et al., 2014)

Thermoelectric Generators (TEGs) is a well-developed technology. In wearable applications, where the temperature gradient is small, <2 K, the power density, and the delivered voltage are small, at dozens of μW and mV respectively. A good point is that is possible to harvest the energy all day.

Photovoltaic energy is one of the most well-developed technologies of all the energy harvesters. At outdoor applications, where a high intensity of light reaches the panel, it can achieve a power density of dozens of mW/cm^2 . At indoor applications, this density reduces to $\mu\text{W}/\text{cm}^2$. But, in both, outdoor and indoor application, the output voltage are suitable to be converted, at least hundreds of mV. The drawback is that the energy is not available always and intensities vary along the time.

The high power density, dozens of mW, and relatively high output voltage, hundreds of millivolts, are excellent characteristics that make the solar energy to be elected as the best option for outdoor applications and a good one for indoor applications. A better insight in this technology will be presented in the next section.

2.1 Photovoltaic Energy

PV cell is the current technology responsible for converting the energy of photons into electricity. They can be arranged in different ways to construct panels or modules to obtain more output current or voltage and, consequently, more power. Fig 2.1 shows a image of a 10 cm x 10 cm PV cell. (BOXWELL, 2017)

The construction of a PV cell is based on a p-n semiconductor junction. It transforms energy through, first, absorption of light, generating either electron-hole pairs, two, separation of charge carriers of opposite types and, three, separate extraction of those carriers to an external circuit. Fig 2.2 shows the construction structure of a PV cell.

There are plenty of ways to construct the semiconductor part of the PV cell. But, the technologies that dominate, due to the cost of manufacturing, are the polycrystalline and monocrystalline silicon. The difference of construction is illustrated in the Fig.2.3. The monocrys-

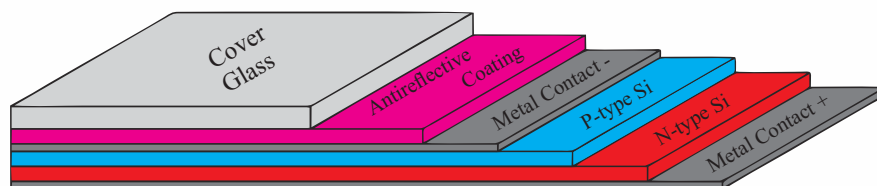
talline technology creates a homogeneous silicon crystal, that achieves a conversion efficiency in the range of 14 to 21%. The polycrystalline is a fusion of different silicon crystals and achieves a conversion efficiency in the range of 13 to 16.5%. Polycrystalline PV cell is cheaper to be made, due to the simplest process of fabrication, so, the trade-off between cost and efficiency depends on the application. (SOLAR, 2017)

Figure 2.1: 10 cm x 10 cm PV cell.



Source: <http://www.sunlinkpv.com>.

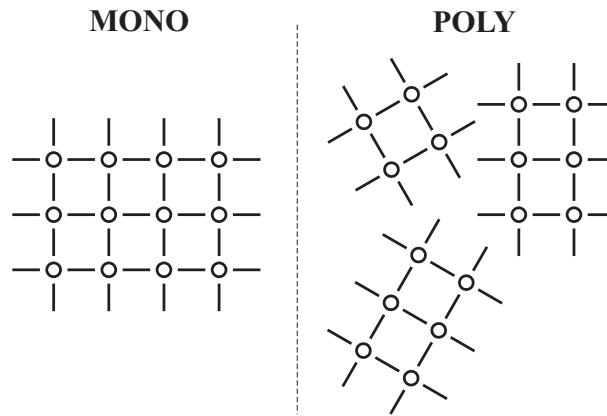
Figure 2.2: PV cell construction.



Source: Author.

Independent of the technology used in the construction, the p-n junction is intrinsic, and it firmly commands the electrical behavior of the PV cell. The next section will treat about the power response of a PV cell.

Figure 2.3: Crystal structure of monocrystalline and polycrystalline Photovoltaic cells.

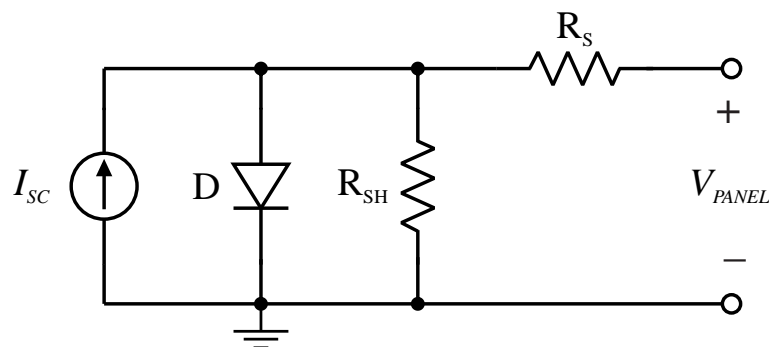


Source: Author.

2.2 PV Cell Electrical Model

The Fig. 2.2 shows the structure of a PV cell. It consists of a p-n junction with metal contacts to access the semiconductors and some dielectrics to enhance the performance. This structure is translated to an electric model as a diode with an injection of electrons due to light incidence and some ohmic losses due to construction and contacts. Fig 2.4 shows the electrical model of a PV cell.

Figure 2.4: Electrical model of a PV cell.



Source: Author.

In Fig. 2.4, D is the intrinsic diode, I_{SC} is the injected current due to the incidence of photons, R_{SH} represents the ohmic losses due to construction of the PV cell and the R_S is the equivalent series resistance of the contacts to external connection.

It is possible to write the relationship between the output current, I_{PANEL} , and the internal currents of the PV cell, Eq. 2.1.

$$I_{PH} = I_D + I_{SH} + I_{PANEL} \quad (2.1)$$

The current behavior of a diode is well known, and it is described by Eq. 2.2. I_D is the current in the diode, I_{SAT} is the current in the diode when it is reverse biased, V_D is the voltage across the diode, n is the ideality factor, and V_T is the thermal voltage.

$$I_D = I_{SAT} \left(e^{\frac{V_D}{nV_T}} - 1 \right) \quad (2.2)$$

It is possible to relate V_D and V_{PANEL} with I_{PANEL} through Eq. 2.3 and use it to relate V_{PANEL} and I_{PANEL} with I_{SH} , Eq. 2.4

$$V_D = V_{PANEL} + R_S I_{PANEL} \quad (2.3)$$

$$I_{SH} = \frac{V_{PANEL} + R_S I_{PANEL}}{R_{SH}} \quad (2.4)$$

Replacing Eq. 2.2 and Eq. 2.4 into Eq. 2.1, an equation that represents the behavior of the PV cell is achieved, Eq. 2.5.

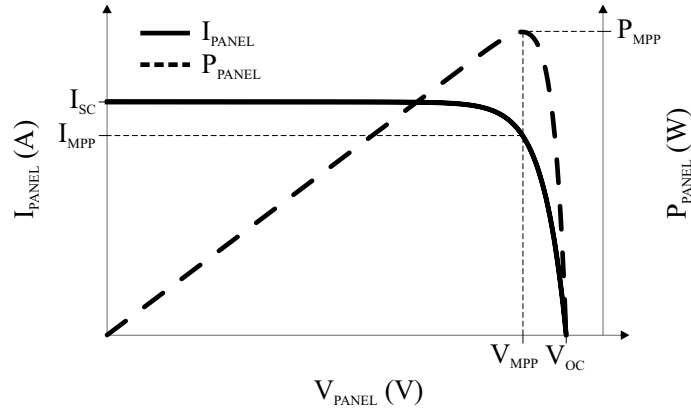
$$I_{PANEL} = I_{PH} - I_{SAT} \left(e^{\frac{V_{PANEL} + R_S I_{PANEL}}{nV_T}} - 1 \right) - \frac{V_{PANEL} + R_S I_{PANEL}}{R_{SH}} \quad (2.5)$$

The relationships I_{PANEL} vs. V_{PANEL} and P_{PANEL} vs. V_{PANEL} are presented in Fig. 2.5, based on Eq. 2.5.

Fig. 2.5 shows that the current I_{PANEL} behaves as a current source for low voltage levels of V_{PANEL} . For V_{PANEL} equals zero (short circuit), the current is maximum, I_{SC} , and the current drops quickly as the V_{PANEL} increases until the current goes to zero at V_{OC} (open circuit). The power of the panel has a point of maximum power delivery (MPP), V_{MPP} and I_{MPP} , what is natural for a non-ideal source of energy.

The injected current depends strongly on the intensity of light, S [W/m^2], and slightly of the temperature T [K]. Eq. 2.6 shows this relationship, where $I_{SC}(T_O)$ is the injected current measured at a temperature T_O and at a irradiation S_O , α is a second order temperature coefficient, T is the temperature and S is the irradiation.

Figure 2.5: I-V and P-V PV cell characteristic.



Source: Author.

$$I_{PH}(S, T) = [I_{PH}(S_O, T_O) + \alpha T(T - T_O)] \frac{S}{S_O} \quad (2.6)$$

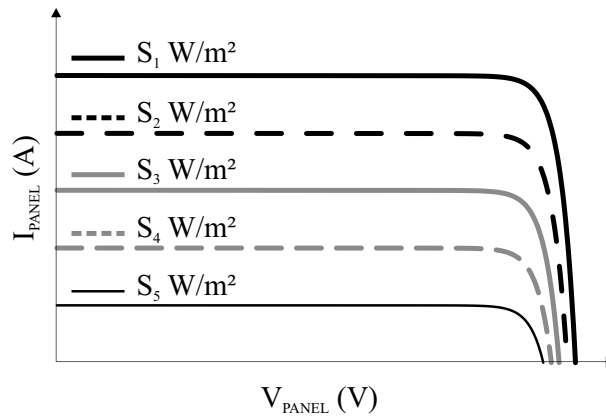
The saturation current strongly depends on the temperature and, because of it, the V_{OC} . The dependence of the I_{SAT} with temperature is given by Eq. 2.7.

$$I_{SAT} = I_S \left(\frac{T}{T_O} \right)^3 e^{\left[\frac{qE_g}{nk} \left(\frac{1}{T_O} - \frac{1}{T} \right) \right]} \quad (2.7)$$

Eq. 2.6 and Eq. 2.7 relate the behavior of the PV cell with irradiation and temperature. Fig. 2.6, Fig. 2.7, Fig. 2.8 and Fig. 2.9 present these relationships reflected on the I_{SC} and V_{OC} , where $S_1 > S_2 > S_3 > S_4$ and $T_1 < T_2 < T_3 < T_4$.

Fig. 2.6 shows that the injected current, I_{SC} , increases linearly with the irradiation, but the open-circuit voltage, V_{OC} , change slightly it.

Figure 2.6: I-V PV cell characteristic for various S.



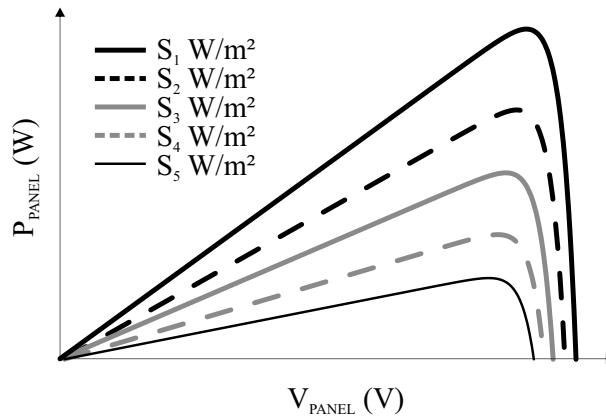
Source: Author.

The overall delivered power, P_{PANEL} , also increases with irradiation, as presented in Fig. 2.7.

Fig. 2.8 shows that the injected current, I_{SC} , increases slightly with the temperature, but the open-circuit voltage, V_{OC} , changes inversely and strongly with it.

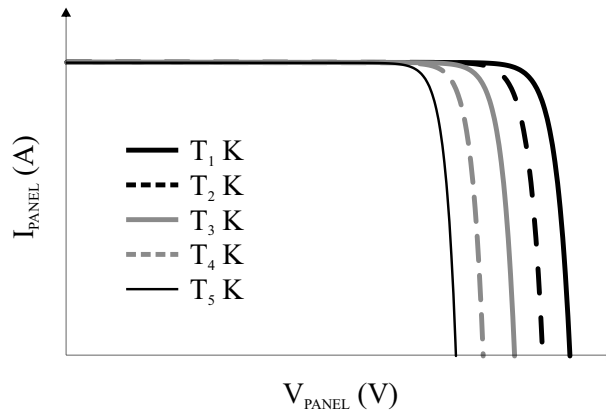
The maximum delivered power, P_{MPP} , increases linearly inversely with temperature, as presented in Fig. 2.10.

Figure 2.7: P-V PV cell characteristic for various S .



Source: Author.

Figure 2.8: I-V PV cell characteristic for various T .

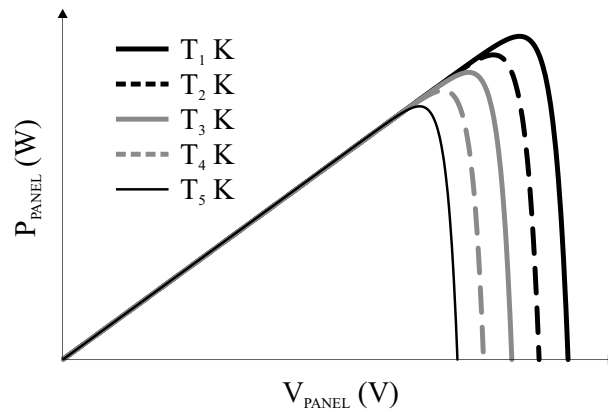


Source: Author.

Eq. 2.5 describes the behavior of voltage and current of a PV cell. It is an equation non-linear and transcendental, so, to fully characterize a PV panel, diode behavior, shunt and series resistance values, it is necessary to make some simplifications or to use a computational method. In this work, a computational method was used to this task. But, first, a PV cell was

chosen in the market and measurements in different irradiation situations were performed. The next section will treat about it.

Figure 2.9: P-V PV cell characteristic for various T.



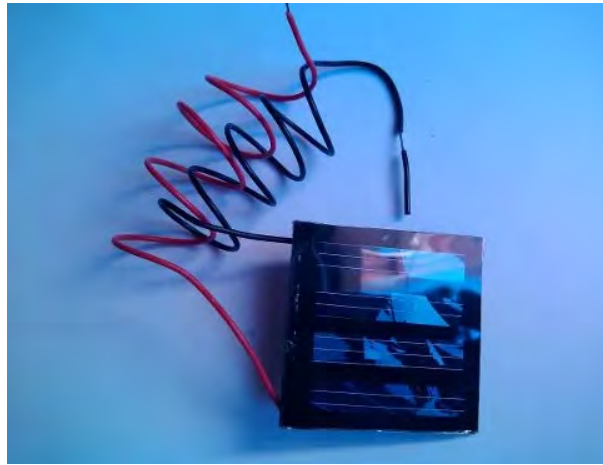
Source: Author.

2.3 Selected PV Panel

A designer of a Wireless Sensor Node aims to increase the autonomy of the node while keeping the device compactness and small price. So, it is natural to look for a small size PV panel. Fig. 2.10 shows the KS-M4030, a small dimension and light weight polycrystalline solar panel, $3.0 \times 3.0 \text{ cm}^2$ and 3.7g respectively, that can deliver up to 60 mW of power at outdoor applications. It is manufactured by China Solar LTD.

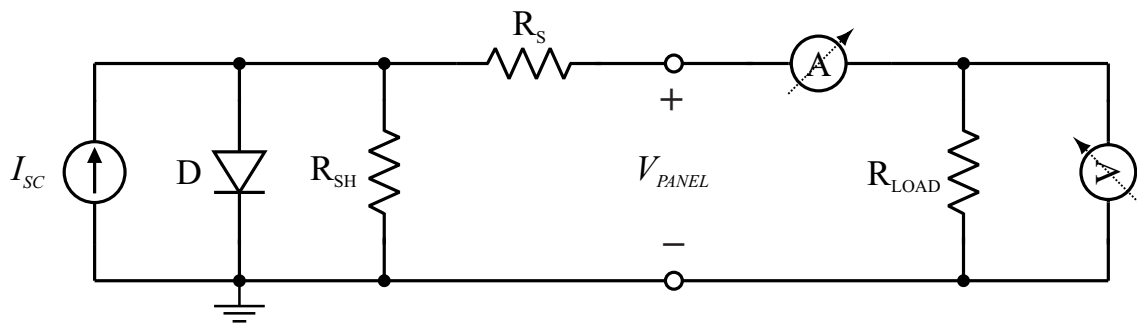
The presented PV panel is cheap, small and easy to find in Brazil, so it was the chosen for the application. It is necessary to obtain its electrical characteristics to design the DC - DC harvester properly.

Figure 2.10: Selected PV panel.



Source: Author.

Figure 2.11: Schematic of the setup test for PV panel characterization.



Source: Author.

2.4 PV Panel Electrical Characterization

The setup test presented in Fig. 2.11 was implemented to characterize the PV panel. The measurements were performed at three irradiation levels, $S_1 = 1000 \text{ W/m}_2$, $S_2 = 200 \text{ W/m}_2$ and $S_3 = 50 \text{ W/m}_2$. These irradiation levels were measured using the illuminance meter 510 01 of Yokogawa. For each irradiation level, V_{PANEL} and I_{PANEL} was measured at different loads, R_{LOAD} .

Fig. 2.12 shows the implemented board to perform the measurements.

The Fig. 2.13 presents the measurements for $S_1 = 1000 \text{ W/m}_2$ performed at the midday of a summer day. Fig. 2.14 presents the measurements for $S_2 = 200 \text{ W/m}_2$ performed at the late afternoon of a summer day and Fig. 2.15 presents the measurements for $S_3 = 50 \text{ W/m}_2$ performed at a closed room artificially illuminated.

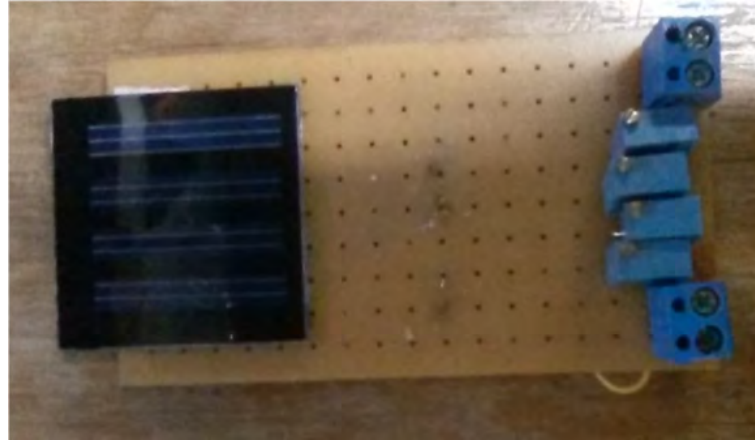
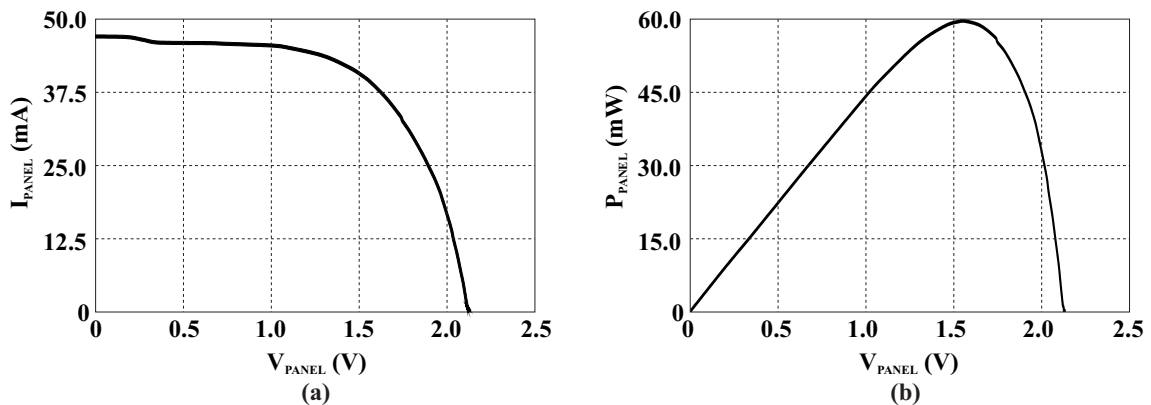


Figure 2.12: Characterization PV panel board.

An analysis of the results shown a high dynamic range of PV panel power with respect to the irradiation. At the midday of a summer day, with the maximum possible irradiation intensity, the maximum power delivered by the PV panel is 60 mW, while the same PV cell delivers a maximum power of $22 \mu\text{W}$ at indoor. Also, at late afternoon, almost night, the PV cell delivers a maximum power of 4 mW.

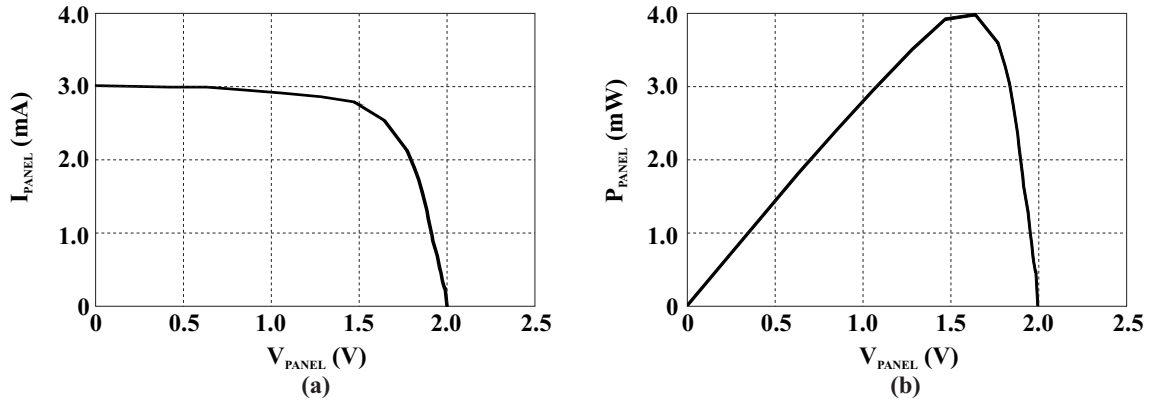
Figure 2.13: Measurements for $S_1 = 1000 \text{ W/m}^2$ (a) I-V (b) P-V.



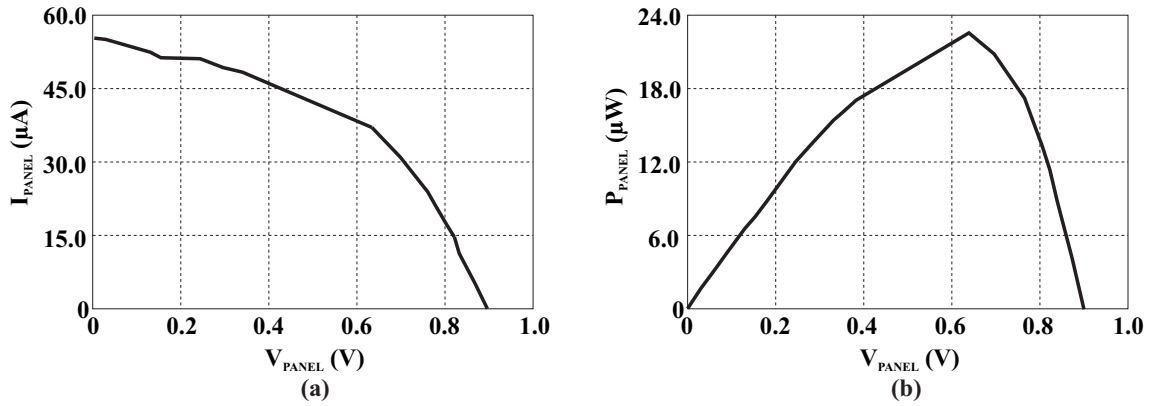
Source: Author.

The focus of this work are in outdoor applications, so the power limits considered were from 4 to 60 mW.

Once the measurements were performed, the behavior of the intrinsic diode D and the values of R_{SH} and R_{S} can be obtained through a computational method, that will be presented in the next section.

Figure 2.14: Measurements for $S_2 = 200 \text{ W/m}_2$ (a) I-V (b) P-V.

Source: Author.

Figure 2.15: Measurements for $S_3 = 50 \text{ W/m}_2$ (a) I-V (b) P-V.

Source: Author.

2.5 PV Panel Parameters Extraction

The Fig. 2.4 shows the schematic model of a PV Panel. It shows the parameters to be extracted. They are R_{SH} , R_S and the parameters of the diode D , n and I_{SAT} . So, it is necessary to extract parameters that makes Eq. 2.5 true for each measured pair V_{PANEL} and I_{PANEL} . From Eq. 2.5, it is possible to write the error equation Eq. 2.8.

$$Error(i) = I_{PH} - I_{SAT} \left(e^{\frac{V_{\text{PANEL}}(i) + R_S I_{\text{PANEL}}(i)}{nV_T}} - 1 \right) - \frac{V_{\text{PANEL}}(i) + R_S I_{\text{PANEL}}(i)}{R_{SH}} - I_{\text{PANEL}}(i) \quad (2.8)$$

The objective is to estimate the parameters that minimize the error of all the measured points to the expected curve. For it, the $Error(i)$ is calculated for each measured pair $V_{\text{PANEL}}(i)$

and $I_{\text{PANEL}}(i)$. Then, the sum of the absolute value of each error is minimized, Eq. 2.9.

$$S_{\text{Errors}} = \sum_{i=1}^N |\text{Error}(i)| \quad (2.9)$$

With the equation to be minimized defined, the second step is to use or create a tool to minimize it.

2.5.1 PV Parameters Extraction Tool

Excel © was the tool chosen for this task. The supplement Solver was used to minimize Eq. 2.9. It can minimize a specific spreadsheet cell varying other defined cells by the user. It is possible choose among three algorithms of optimization, Evolutionary, LP Simplex and GRG Non-Linear. LP Simplex is better to optimize linear problems, Evolutionary to high derivative curves and GRG Non Linear to non-linear low derivative curves. The behavior of a PV panel is non-linear and the curves are soft, so the GRG Non-Linear was the algorithm chosen to the task. Fig. 2.16 presents the spreadsheet designed to perform the parameters extraction.

To present the functionality of the tool, Fig. 2.17 compares the measured curve for S_2 and the estimated curve based on a first kick for the parameters. Once the I_{SC} is a parameter measured, the error for small values of V_{PANEL} is little. But, the error gets higher as the value of V_{PANEL} increases.


Then, One iteration was performed using the designed spreadsheet, and the error reduced for higher values of V_{PANEL} , but it is still far from the measured points, Fig. 2.18.

Finally, a target of S_{Errors} of less than 0.005 was set and after 32 iterations, the error got small enough and the estimated curve got closer of the measurements, Fig. 2.19.

Tab. 2.2 shows the errors and the parameters calculated for the three presented cases. With the parameters extracted, it is possible to generate a accurate model o the selected PV panel to be used in simulations of the converter.

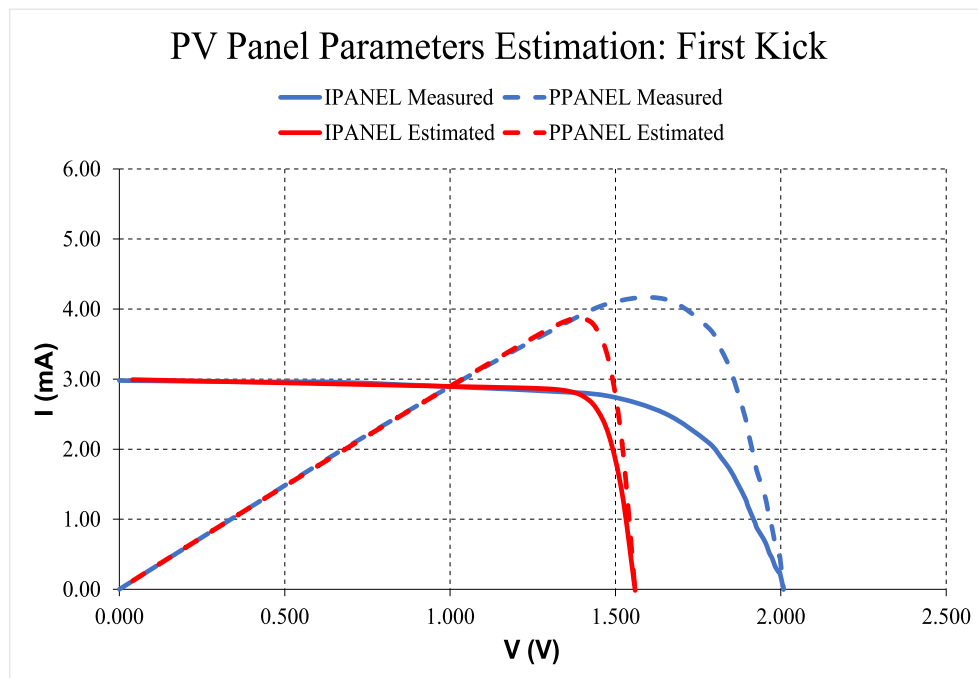
The measurements shown that the PV panel presents a Maximum Point of Power (MPP) delivery. It is desirable to extract the maximum power available in the PV panel, so a strategy of MPPT must be employed. The next section will talk about this subject.

Figure 2.16: Spreadsheet for parameters extraction PV panel.

		Fitting Spreadsheet			
		Known			
	k	1.38E-23	Isc	0.00298	
	q	1.60E-19			
	T	303			
$\text{Erro} = I_{SC} - I_{SAT} \left(e^{\frac{R_S I_{PANEL} + V_{PANEL}}{n V_T}} - 1 \right) - \frac{V_{PANEL}}{R_{SH}} - I_{PANEL}$		Unknown			
		I _{SAT} (10 ⁻²⁰)	1.00	R _{SH}	10000.00
		n	1.50		
		R _s	10.00		
		Sum of Errors			
		986.036			
		Measured		Erro	ABS Erro
		V _{PANEL} (V)	I _{PANEL} (A)		
		0.000	0.0030	0.000000	0.000000
		0.218	0.0030	-0.000012	0.000012
		0.421	0.0030	-0.000022	0.000022
		0.635	0.0030	-0.000044	0.000044
		0.856	0.0029	-0.000026	0.000026
		1.064	0.0029	-0.000006	0.000006
		1.288	0.0028	0.000017	0.000017
		1.477	0.0028	-0.000409	0.000409
		1.650	0.0025	-0.037064	0.037064
		1.780	0.0021	-0.929145	0.929145
		1.821	0.0019	-2.496505	2.496505
		1.846	0.0017	-4.537695	4.537695
		1.867	0.0015	-7.408720	7.408720
		1.893	0.0013	-13.534175	13.534175
		1.901	0.0012	-16.141344	16.141344
		1.922	0.0010	-26.018770	26.018770
		1.927	0.0009	-29.037869	29.037869
		1.952	0.0007	-52.251277	52.251277
		1.966	0.0005	-71.491412	71.491412
		1.973	0.0005	-84.224180	84.224180
		1.981	0.0003	-100.576320	100.576320
		1.985	0.0003	-110.286420	110.286420
		1.994	0.0002	-136.455999	136.455999
		1.997	0.0002	-147.167503	147.167503
		2.008	0.0000	-183.441304	183.441304

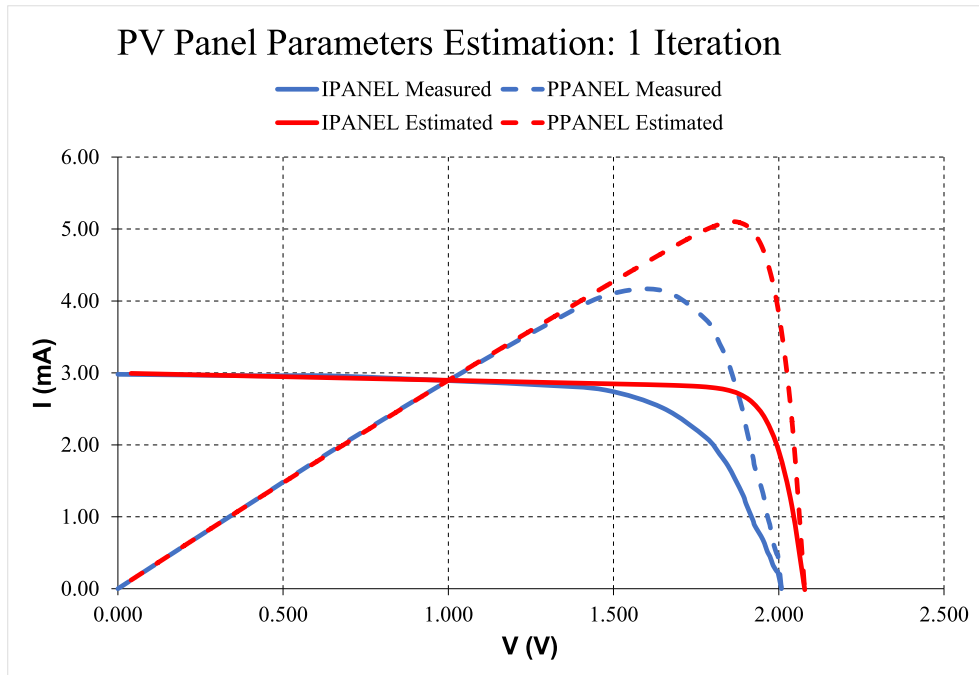
Source: Author.

Figure 2.17: Measured and estimated: initial kick.



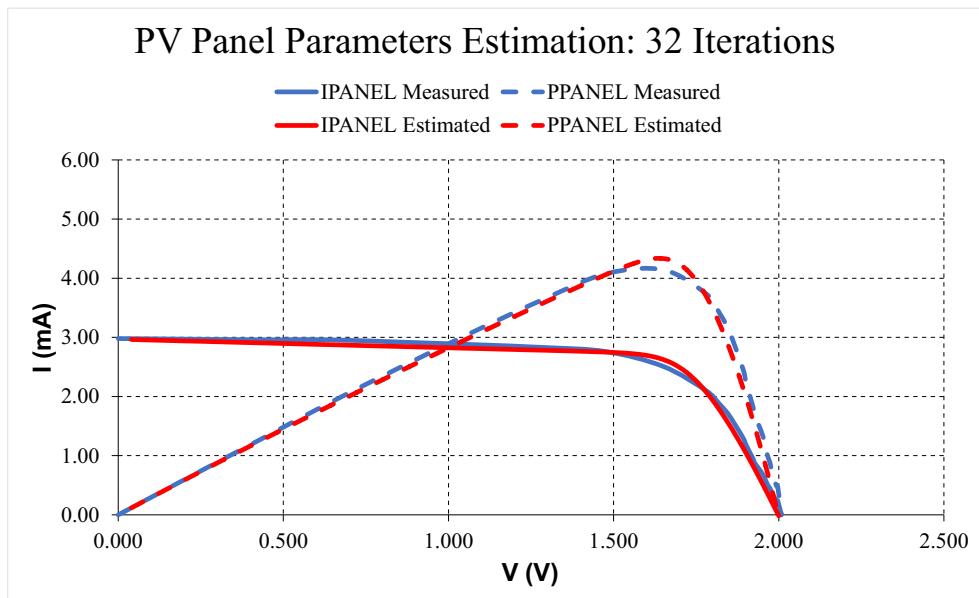
Source: Author.

Figure 2.18: Measured and estimated: 1 iteration



Source: Author.

Figure 2.19: Measured and estimated: 32 iterations



Source: Author.

2.6 Maximum Power Point Tracking - MPPT Techniques

There are a lot of ways to track a reference for the MPP. The most common are the methods, Perturb and Observe (P and O), Incremental Conductance (IC), Fraction of V_{OC} and

Table 2.2: Error and estimated parameters for each iteration for $S_2 = 200 \text{ W/m}^2$.

Iterations	$S_{\text{Errors}}(\text{A})$	n	$I_{\text{SAT}}(\text{A})$	$R_{\text{SH}}(\Omega)$	$R_{\text{S}}(\Omega)$
0 (kick)	986.036	1.50	1.00×10^{-20}	10000.00	10.00
1	0.028	2.00	0.99×10^{-20}	10000.00	9.99
32	0.002	1.96	2.05×10^{-20}	6815.95	69.98

Source: Author.

Fraction of I_{SC} . (XIAO et al., 2011)

The MPPT method P and O is a computational method that needs that the current and the voltage, and consequently the power, of the PV panel be continuously measured and compared. The comparison is performed following the flowchart of Fig. 2.20.

For each sample phase, the P and O algorithm observes the value of the actual values of current and voltage of the PV panel, $V_{\text{PANEL}}(n)$ and $I_{\text{PANEL}}(n)$, and calculate the actual power $P_{\text{PANEL}}(n)$. Then, it compares it with the previously calculated power $P_{\text{PANEL}}(n-1)$. If the actual power is higher than the previous one, $V_{\text{PANEL}}(n)$ is compared with $V_{\text{PANEL}}(n-1)$, depending on the result, it means that the actual power is in the descending/ascending part of the P_{PANEL} curve. If in the descending part, the reference voltage V_{REF} must be reduced, in the other case, the V_{REF} must be increased.

Table 2.3: Comparison among MPPT Techniques

Technique	Analog or Digital	TRUE MPPT?	Convergence Speed	Complexity	Sensors
P and O	Both	Yes	It depends	Low	V, I
Incram. Conduc.	Digital	Yes	It depends	Medium	V, I
Fraction of V_{OC}	Both	No	Medium	Low	V
Fraction of I_{SC}	Both	No	Medium	Medium	I

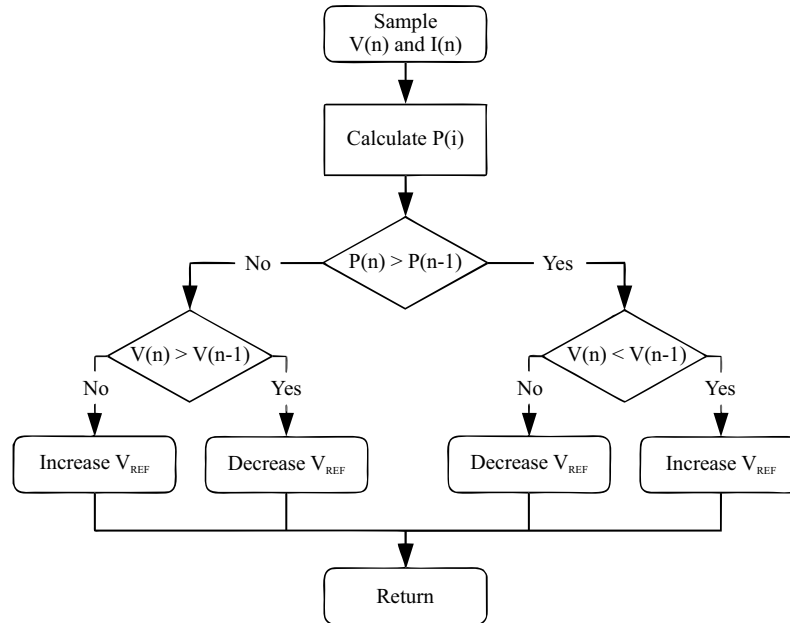
Source: Author, based on (XIAO et al., 2011).

Besides the fact that this method is widely used, it has some drawbacks. The tracking time is large, it includes some oscillations, and the voltage variation is significant around the V_{MPP} .

The Incremental Conduction (IC) method came to suppress some of the P and O methods. Fig. 2.21 shows the flowchart of the algorithm. It is a computational method like P and O.

For each sample phase, the actual value of current and voltage of the PV panel is observed. Differently from the P and O method, it calculates dP/dV indirectly through the relationship between dI/dV and $-I/V$, as described in equations.

Figure 2.20: Flowchart of P and O MPPT algorithm



Source: <http://coder-tronics.com/>

$$\frac{dP}{dV} = \frac{d(VI)}{dV} = I \frac{dV}{dV} + V \frac{dI}{dV} \quad (2.10)$$

The MPP is characterized by the relation Eq. 2.11.

$$\frac{dP}{dV} = 0 \quad (2.11)$$

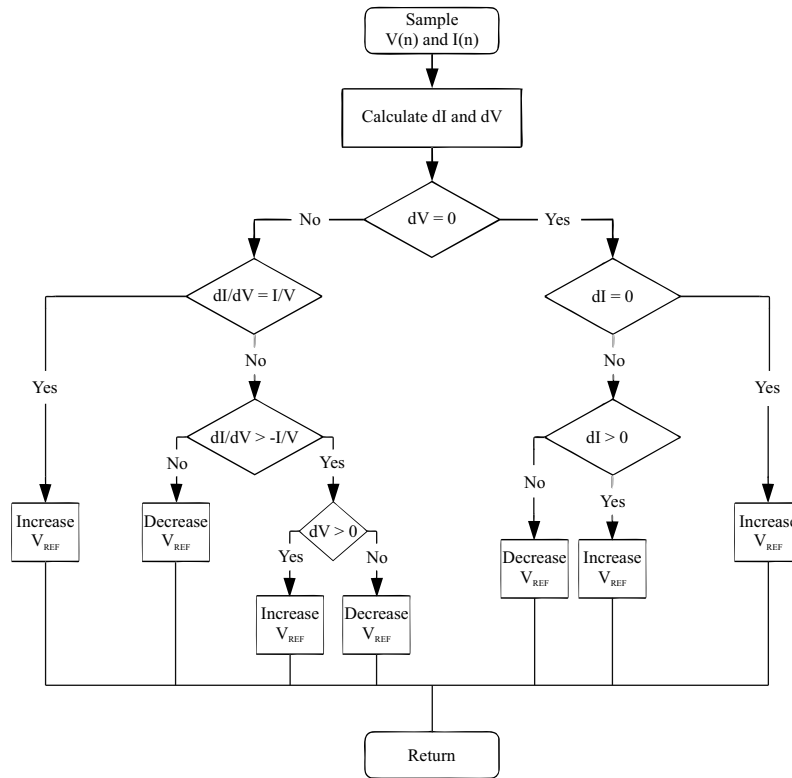
Eq. 2.11 leads to the relation described by Eq. 2.12.

$$\frac{dI}{dV} = -\frac{I}{V} \quad (2.12)$$

The relationships described by equations Eq. 2.10, Eq. 2.11 and Eq. 2.12 are used by IC algorithm. These calculus based on the voltage and current variations improve the tracking time and reduces the oscillation around the MPP.

Both methods, P and O and IC, try to reach the real MPP of the PV panel using sophisticated algorithms and measuring input current and voltage continuously. These methods use

Figure 2.21: Flowchart of Incremental Conductance MPPT algorithm



Source: <http://coder-tronics.com/>

the property that the V_{MPP} and I_{MPP} are a ratio of the V_{OC} and I_{SC} , respectively, that is why it is called fraction of V_{OC} or I_{SC} . The ratio of V_{MPP} and V_{OC} normally relies in between 70 and 80%. (SHRIVASTAVA et al., 2015)

The Fraction method is the most used from all MPPT method, since it is simpler to be implemented, uses only one sensor, consumes less power and achieves good MPPT result. These advantages made this method to be the chosen one by this work.

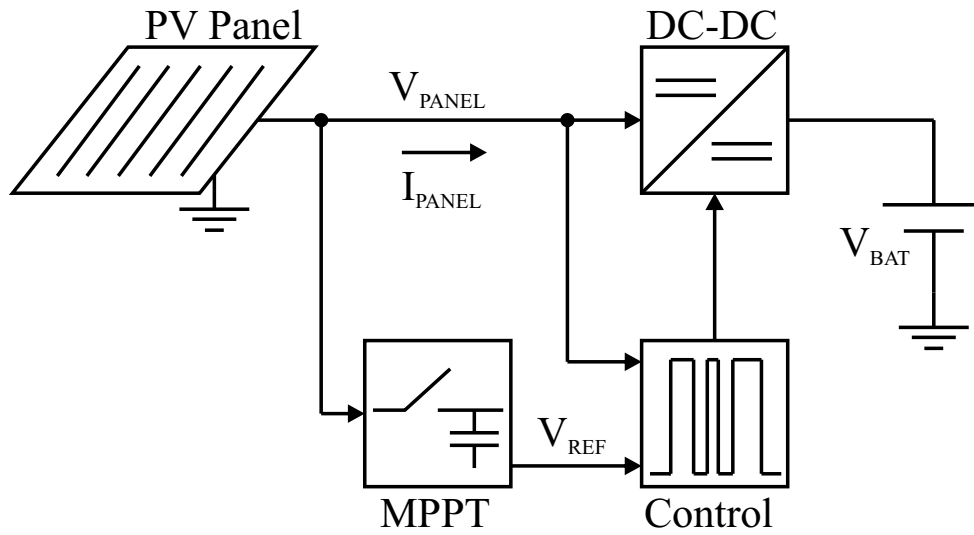
A voltage sensor is simpler and cheaper to implement than a current sensor, so the Fraction of the V_{MPP} is usually the used method. To obtain this value, the PV panel must stay an instant without supply any energy, so the open-circuit voltage can be measured. It lowers down the efficiency, but the duty-cycle can be as small as possible considering Sample & Hold leakage and charge/discharge constant times, making the impact be minimized.

The advantages of the V_{OC} fraction made this method to be the elected for this work.

To accomplish a MPPT strategy, the load must be isolated from the PV panel. It is done using a DC-DC converter in between the PV panel and an energy storage element. It can be a battery, super cap or just a large capacitor. So, the MPPT generates the reference for the control of the DC-DC converter. Fig. 2.22 shows this block diagram.

There are a plenty of ways of implement a DC-DC converter, different topologies and storage elements can be used. The next chapter will give an insight into this subject.

Figure 2.22: MPPT complete scheme.



Source: Author.

3 DC-DC CONVERTERS

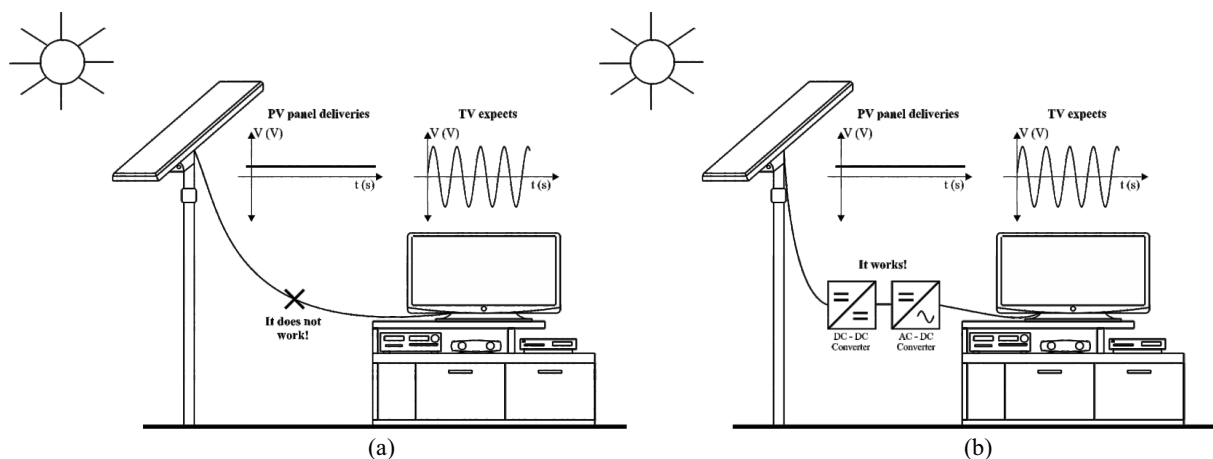
"What is the best way of generating and distributing energy, at Alternate Current (AC) or Direct Current (DC)?" This question was a subject of arguing between two monsters of the electrical engineer, Thomas Edison and Nikola Tesla. AC won, and most of the energy generated and transported in the world use this form. Because of it, the electronic devices are worldwide developed to receive AC power.

The scarcity of natural resources brought the concern on the renewable energy sources like wind, photovoltaic and thermal. Photovoltaic and thermal supply power in DC form and at low levels, dozens of volts at maximum. So, to use this source to supply out nowadays electronic devices, it is necessary to convert the form of energy from DC to AC.

In Brazil, there are two AC nominal voltages, 220 V_{RMS} and 127 V_{RMS} , with 60 Hz of nominal frequency. If someone wants to use a commercial PV panel of 20 V_{DC} to supply some electronic devices in the house, it will be necessary to convert the 20 V_{DC} in 220/127 V_{RMS} AC.

To accomplish this task, normally a DC-DC up-converter is used to elevate the DC voltage to a level that a DC-AC converter (inverter) could create a 60 Hz and 220 V_{RMS} , so it can be used to supply the electronics devices of the house. Fig. 3.1 shows this scenario.

Figure 3.1: PV energy conversion. (a) Wrong way to connect (b) Right way to connect



Source: Author.

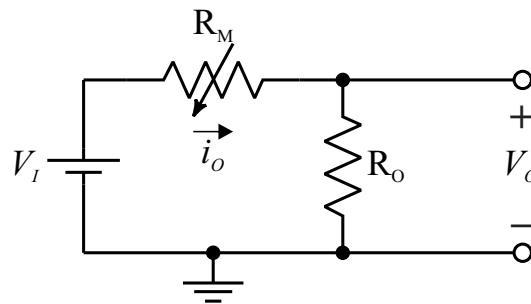
In Internet of Things (IoT), the compact devices expect a DC voltage to work and usually are supplied by a battery. The PV panel also delivers a DC voltage, so the focus of the converter in this work will be DC-DC ones only.

The next sections will present an analysis of different converters. These analysis consider that the converters are in steady-state, so no transitional analysis will be presented.

3.1 Linear DC-DC Conversion

The simplest way to regulate and convert a DC voltage into another is the linear conversion. Fig. 3.2 shows the conceptual schematic of a linear DC-DC converter. (ERICKSON, 2001)

Figure 3.2: Linear DC-DC converter conceptual schematic.



Source: Author.

For a given load R_O input voltage V_I , it is possible to set a R_M that defines the output voltage V_O . However, this is done through power dissipation over R_M .

It is possible to calculate the voltage convert ratio A_V of V_O and V_I , Eq. 3.1.

$$A_V = \frac{V_O}{V_I} = \frac{R_O}{R_M + R_O} \quad (3.1)$$

The conversion efficiency of this ideal linear DC-DC converter is described by Eq. 3.2. Without considering any loss that a real converter would have, the conversion efficiency is limited by the ratio V_O/V_I .

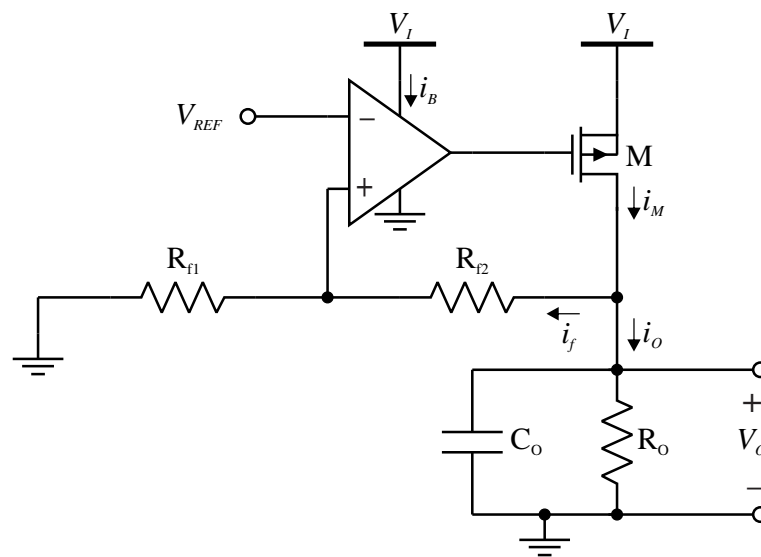
$$\eta = \frac{V_O I_O}{V_I I_I} = \frac{R_O}{R_M + R_O} = A_V = \frac{V_O}{V_I} \quad (3.2)$$

The most common way to implement a linear DC-DC converter is the Low-Dropout (LDO) DC-DC converter, Fig.3.3. (ERICKSON, 2001)

In a LDO, the transistor M performs the work of the resistor R_M , Fig. 3.1. The transistor works as a variable transconductor, that changes the impedance across the drain and source

terminals, r_{DS} , as the load changes, always keeping V_O in the desirable level. To accomplish it, a sample of the output voltage, the division between R_{f1} and R_{f2} , is feedback in the positive terminal of the operational amplifier and then it is compared to a reference of tension V_{REF} . This comparison and amplification generate a signal that controls the gate voltage of transistor M, which controls the voltage V_{DS} .

Figure 3.3: Low-Dropout DC-DC converter.



Source: Author.

Resistor R_O represents the load and the capacitor C_O is sized to compensate the feedback loop to avoid instability.

Besides the intrinsic loss in transistor M, this implementation includes some losses, the quiescent power of the operational amplifier, the consumed current of the transistors R_{f1} and R_{f2} , and the power consumed to generate V_{REF} and the bias to the amplifier. Due to it, the conversion efficiency gets lower than the theoretical, Eq. 3.2.

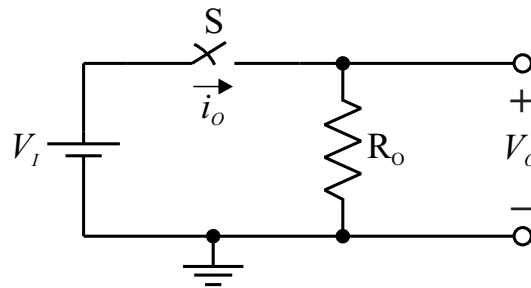
The efficiency of a converter is important in two cases. At low available energy and high output power. When the energy is scarce, it is problematic to spend power only converting the voltage levels. When the output power is high, a low efficiency will cause great power dissipation in the converter. This leads to an overheating of the circuit, what will require a large thermal dissipator, increasing size cost of the circuit. So, in these situations, a linear converter is not well-suited. Also, normally, in energy harvesting, it is necessary to convert the voltage level of the power source up, what is not possible to achieve with a linear converter. (ERICKSON, 2001)

These problems of linear converters can be suppressed using switched DC-DC converters. They avoid the intrinsic theoretical losses and can be used to convert voltage levels up. The next section will give some insight about them.

3.2 Switched DC-DC Conversion

A switched DC-DC converter can be employed to avoid the intrinsic losses that the linear DC-DC converter presents. Fig. 3.4 shows the conceptual schematic of a step down switched DC-DC converter.

Figure 3.4: Switched DC-DC converter conceptual schematic.



Source: Author.

Differently from the linear case, in this case the mean output voltage is controlled by the time that the switch is on. Let T_S be the switching period, and t_{ON} and t_{OFF} be, respectively, the time that the switch is closed and the time that the switch is open, where:

$$T_S = t_{ON} + t_{OFF}. \quad (3.3)$$

It is possible to calculate the voltage conversion ratio A_V between the mean value of V_O to V_I , Eq. 3.4, where D is the duty-cycle.

$$A_V = \frac{\bar{V}_O}{V_I} = \frac{t_{ON}}{T_S} = D \quad (3.4)$$

This conceptual converter has a theoretical conversion efficiency of 100 %, considering that the switch S is ideal (ON: zero resistance, OFF: infinite resistance) and that there is no overlapping of voltage and current in the switch transitions.

It generates a pulsed output voltage, although a stable DC voltage is desired. Usually, a LC filter is used in the output to overcome this problem. In the next section, it will be shown

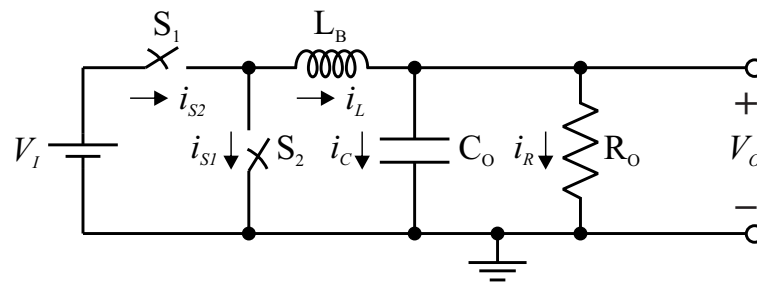
that this conceptual topology together with a LC filter forms one of the most used switched DC-DC converters, the Buck converter, Fig. 3.5. The Buck converter is a step-down DC level converter. It is an example of a switched inductor DC-DC converter.

The next sections will treat about the ways that a switched DC-DC converter can be implemented and how they work. First, the inductor based DC-DC converters and second, the switched-capacitor DC-DC converters.

3.3 Inductor Based DC-DC Conversion

The step down Buck converter, Fig. 3.5, is created adding a LC filter and a switch that is a current path to the inductor of the LC filter in the conceptual switched DC-DC converter, Fig. 3.4.

Figure 3.5: Buck converter.



Source: Author.

The Buck uses the inductor as the energy storage element. Power is transferred from the input source voltage to the inductor when the switch S_1 is closed and S_2 is open. The energy stored in the inductor is transferred to the output when S_2 is closed and S_1 is opened. Capacitor C_O filters the harmonics and let the output voltage V_O at a stable DC level.

It is a step-down converter, so the output voltage can never exceed the input voltage level, and the ideal voltage conversion ratio is given by Eq. 3.5.

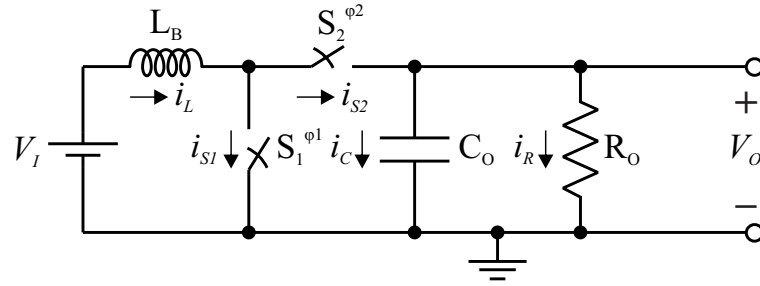
$$A_V = \frac{\bar{V}_O}{V_I} = D \quad (3.5)$$

Usually, energy harvesting sources as small PV panels and TEGs deliver voltage levels that are lower than the desired voltage level, that can be the voltage of a battery. So, harvesters are, usually, step-up converters.

3.3.1 The Boost Converter

The Boost converter, Fig. 3.6, is a inductor one that elevates the input DC voltage level. It works in two phases and can have two or three operation steps. Phase 1 (ϕ_1) happens when S_1 is closed and S_2 is opened. Phase 2 (ϕ_2) happens when S_2 is closed and S_1 is opened.

Figure 3.6: Boost converter.



Source: Author.

In ϕ_1 , energy is transferred to the inductor L_B through switch S_1 and the energy consumed by the load R_O is delivered by the capacitor C_O , Fig. 3.7 (a). In ϕ_2 , the energy stored in the inductor is transferred to the output, recharging the output capacitor and supplying the load through S_2 , Fig. 3.7 (b). The converter can operate at two different modes. It can be Continuous Conduction Mode (CCM), when i_L does not achieve zero at the end of ϕ_2 , or Discontinuous Conduction Mode (DCM), when i_L achieves zero at the end of ϕ_2 . If in DCM, a third phase appears, where S_1 and S_2 are open and there is current only flowing from the output capacitor to the load, Fig. 3.7 (c).

The generic curves of currents of the Boost converter are presented in Fig 3.8 and the curves of voltage are presented in Fig. 3.9 for the two cases of CCM and DCM.

For CCM and in steady-state (output voltage is stable at V_O , the ripple across the output capacitor is neglected, the mean current of the output capacitor and the average across the terminals of the inductor are zero), the current i_L is described by Eq. 3.6 and Eq. 3.7, considering that the switches are ideals.

$$i_L(t)^{\phi_1} = I_{MIN} + \frac{V_I}{L_B}t \quad (3.6)$$

$$i_L(t)^{\phi_2} = I_{MAX} - \frac{V_O - V_I}{L_B}t \quad (3.7)$$

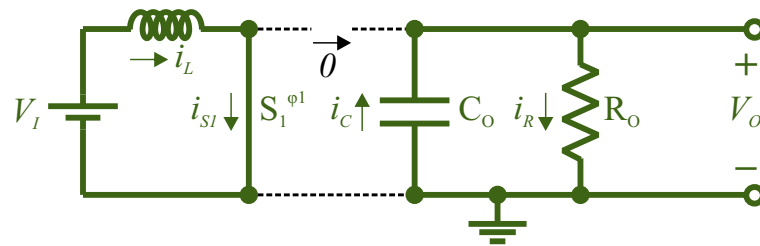
The time duration of ϕ_1 is t_{ON} , that is DT_S and time duration of ϕ_2 is t_{OFF} , that is $(1-D)T_S$ for CCM. So, it is possible to calculate I_{MAX} and I_{MIN} from Eq. 3.6 and Eq. 3.7, Eq. 3.8 and Eq. 3.9 and define the ripple current of the inductor as in Eq. 3.10.

$$I_{MAX} = I_{MIN} + \frac{V_I}{L_B}DT_S \quad (3.8)$$

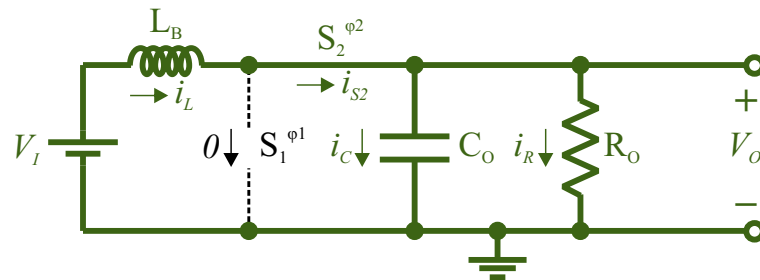
$$I_{MIN} = I_{MAX} - \frac{V_O - V_I}{L_B}(1 - D)T_S \quad (3.9)$$

$$\Delta i_L = I_{MAX} - I_{MIN} \quad (3.10)$$

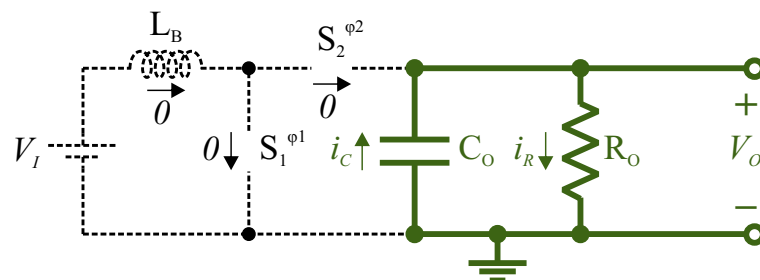
Figure 3.7: Boost converter operation steps.



(a) ϕ_1



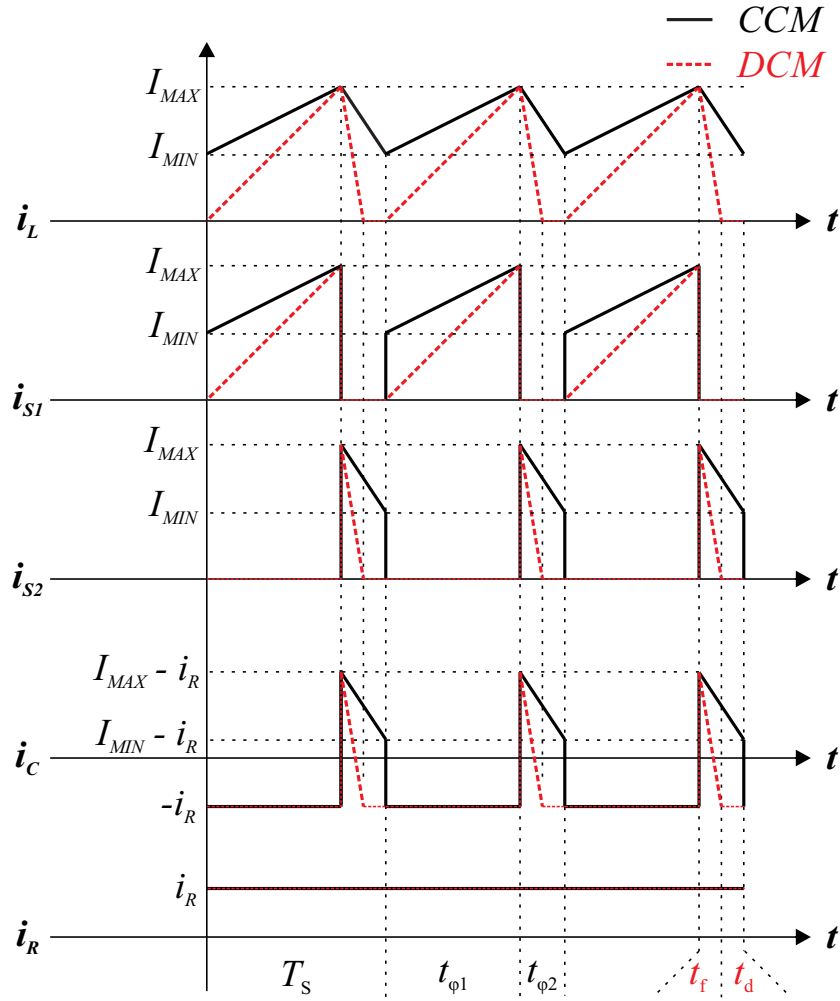
(b) ϕ_2



(c) ϕ_2' (if in DCM)

Source: Author.

Figure 3.8: Current waveforms.



Source: Author.

It is possible to write the voltage conversion ratio of the Boost converter in CCM, Eq. 3.11.

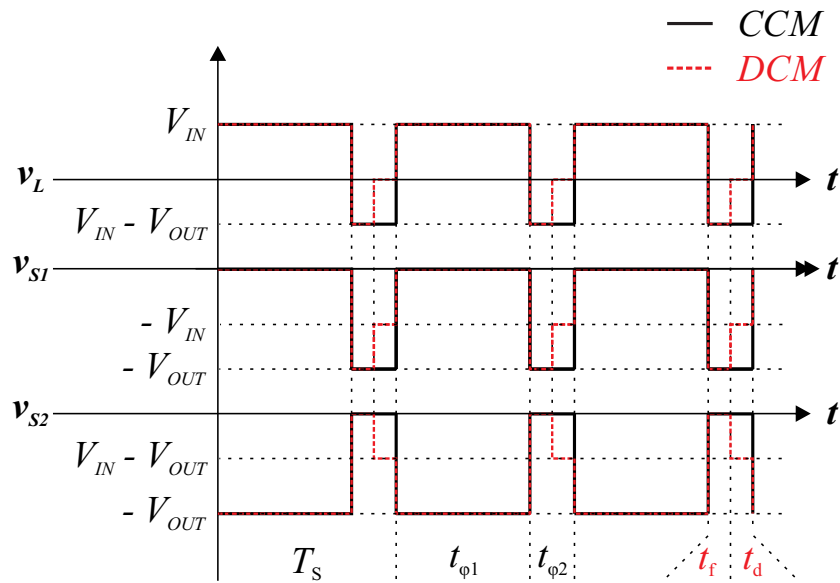
$$A_{V-CCM} = \frac{1}{1-D} \quad (3.11)$$

Also, it is possible to write the voltage gain for the DCM case using the same analysis methodology, but considering that the inductor current goes zero at the end of ϕ_2 , Eq. 3.12 and Eq. 3.13.

$$A_{V-DCM} = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} \quad (3.12)$$

$$K = \frac{2L_B}{R_O T_S} \quad (3.13)$$

Figure 3.9: Voltage waveforms.



Source: Author.

For both cases, DCM and CCM, the minimum output voltage, for $D = 0$, is V_1 , and can go, theoretically, to infinite for $D = 1$.

Current ripple, voltage ripple and the limit between CCM and DCM are defined by the relation among the passives L_B and C_O and the switching frequency for a particular input and output voltages and power. The increase in the switching frequency, for fixed values of L_B and C_O , reduces voltage and current ripples and makes the boost converter tend to operate in CCM. The increase of inductor size reduces, for a fixed switching frequency, the inductor current ripple and makes the converter tend to work in CCM. The increase in capacitor size, for a fixed switching frequency, reduces the capacitor voltage ripple.

The output capacitor presents an Equivalent Series Resistance (ESR), and it increases the output voltage ripple due to the inductor current ripple. So, due to this nonideality, the growth in the inductor size allows a reduction in the capacitor size and switching frequency.

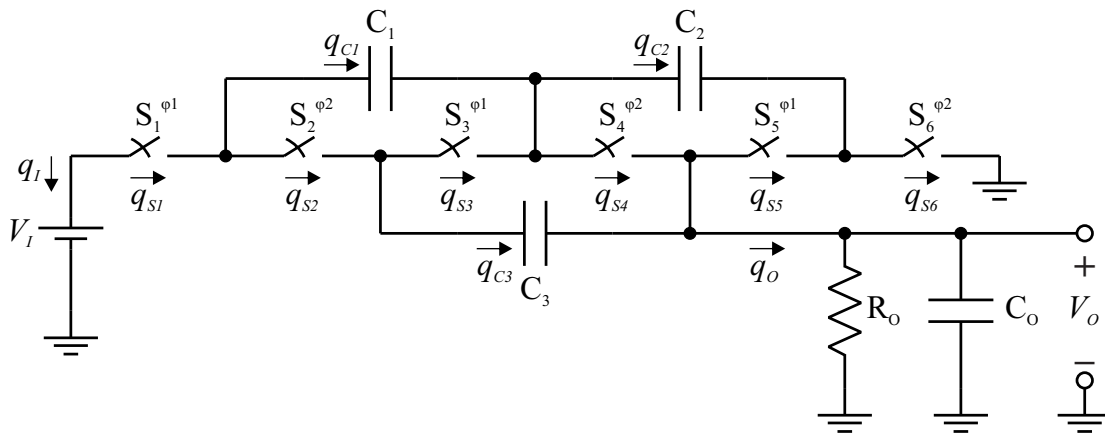
An alternative for switched DC-DC Converters are the switched-capacitor DC-DC converters. The next section will give some insight about them.

3.4 Capacitor Based DC-DC Conversion

Also known as Charge Pumps (CPs), the Switched-Capacitor (SC) DC-DC converter only use capacitors as energy storage elements. It leads to a considerable number of differences to the inductor based. First, the ideal conversion voltage ratio A_V is defined by the topology.

Also, differently from the inductors ones, that can perform the DC-DC conversion with no losses (in theory), the SC DC-DC converters present intrinsic losses due to charge redistribution among the capacitors. A last important characteristic of an ideal SC DC-DC converter is the interchangeability between the input and output terminals. Fig. 3.10 presents an example of an 1-to-3 SC DC-DC voltage converter using a topology called Ladder.

Figure 3.10: 1-to-3 SC DC - DC Converter.



Source: Author.

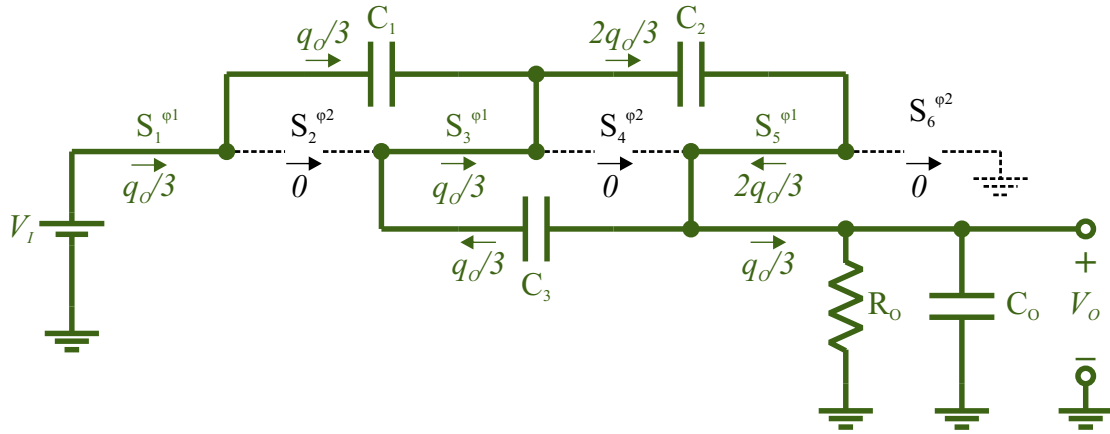
The presented converter counts with six switches and three flying capacitors with the same capacitance (the name fly is given because of the terminals voltages of the capacitors changes regularly) and works in two phases, as the boost converter.

In phase 1 (ϕ_1) switches S_1 , S_3 and S_5 are closed and S_2 , S_4 and S_6 are opened. In phase 2 (ϕ_2), switches S_1 , S_2 and S_5 are opened and S_2 , S_4 and S_6 are closed. Fig. 3.10 shows the two operation phases, where q_o is the total charge that is transferred to the output in the two phases.

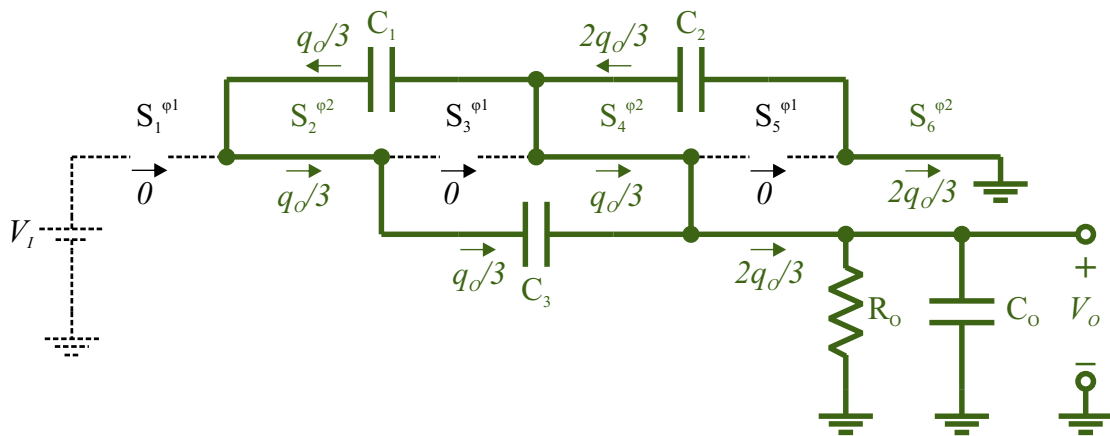
In ϕ_1 , $q_o/3$ is transferred from the input source voltage to capacitor C_1 . Also, C_1 and C_3 transfer, each, $q_o/3$ to capacitor C_2 . So, a charge of $q_o/3$ is transferred to the output V_o .

The topology defines the ideal voltage converter ratio, as a perfect transformer, but for DC voltage. Also, the losses of the converter limit the maximum output power. So, it is possible to draw a static model for the SC DC-DC converter like an ideal DC transformer with an output impedance. The Fig. 3.12 shows it, where N is the ideal conversion ratio (3 in the case of the presented example).

The output impedance R_{OUT} limits the maximum output power and changes the ideal output voltage. It is compound by the losses due to the switches resistances, charge redistribution, charge loss due to switching of parasitic capacitances and switches capacitances and quiescent power of drives and controls. The next sections will treat about these mechanisms.



(a) ϕ_1

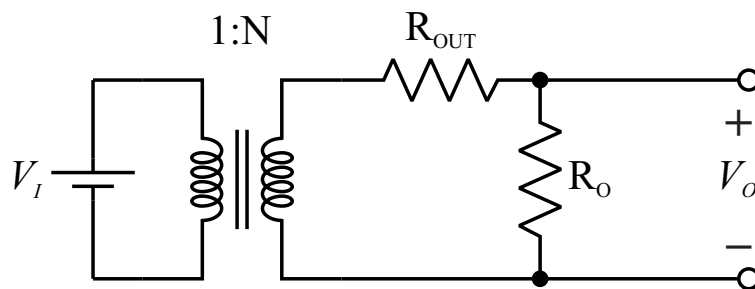


(a) ϕ_2

Figure 3.11: 1-to-3 SC DC - DC Converter operation steps.

Source: Author.

Figure 3.12: Boost converter operation steps.

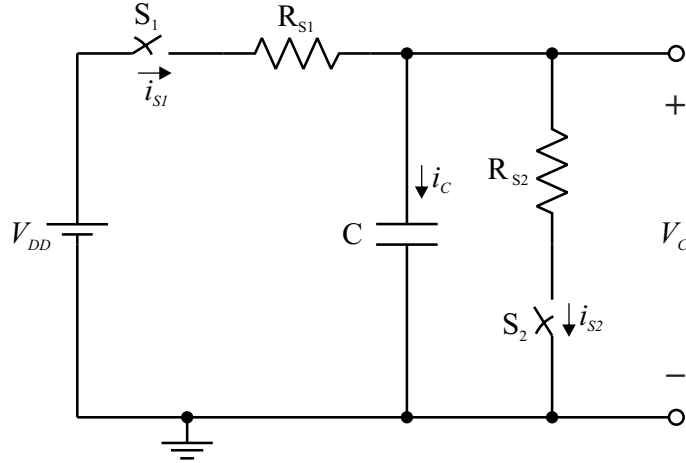


Source: Author.

3.4.1 Switched Capacitor Losses

The SSL and FSL losses will be explained by the simple circuit presented in Fig. 3.13.

Figure 3.13: Didactic circuit to explain SSL and FSL losses.



Source: Author.

In the circuit of Fig. 3.13, the switches S_1 and S_2 work in two alternate phases. When S_1 is opened, S_2 is closed and when S_1 is closed, S_2 is opened. This occurs continuously with a period T_S (frequency f_S), where each phase lasts half of T_S . The equivalent series resistances of switch S_1 is the R_{S1} and the equivalent series resistance of the switch S_2 is R_{S2} . It will be considered that R_{S1} and R_{S2} are equal and it will be used a generic value of R_S to represent them.

Imagine that the period T_S is slow enough that the constant time τ_C formed by the switches resistances and the capacitance are pretty smaller than it. In this case, the capacitor C is fully charged and discharged each period. In charging time, it is possible to write the current, the voltage and the power in the capacitor like in Eq. 3.23, Eq. 3.15 and Eq. 3.16.

$$i_C(t) = \frac{V_{DD}}{R_S} e^{-\frac{t}{R_S C}} \quad (3.14)$$

$$V_C(t) = V_{DD} \left(1 - e^{-\frac{t}{R_S C}}\right) \quad (3.15)$$

$$P_C(t) = \frac{V_{DD}^2}{R_S} \left(1 - e^{-\frac{t}{R_S C}}\right) e^{-\frac{t}{R_S C}} \quad (3.16)$$

So, it is possible to write the energy stored in the capacitor in the charging phase for $R_S C$ much smaller than T_S , Eq. 3.17.

$$E_C = \int_0^{T_S/2} P_C(t) dt = \frac{CV_{DD}^2}{2} \quad (3.17)$$

Also, it is possible to calculate the power and the energy delivered by the voltage source in this same period, Eq. 3.18 and Eq. 3.20.

$$P_{VDD}(t) = \frac{V_{DD}^2}{R_S} e^{-\frac{t}{R_S C}} \quad (3.18)$$

$$E_{VDD} = \int_0^{T_S/2} P_{VDD}(t) dt = CV_{DD}^2 \quad (3.19)$$

The energy transfer efficiency is described by Eq. 3.20.

$$\eta_{trans} = \frac{E_C}{E_{VDD}} 100\% = 50\% \quad (3.20)$$

It is interesting that the voltage source delivers twice the energy stored in the capacitor. Also, the power loss does not depend on the value of the switches resistance, since the constant time is much smaller than the switching period. It means that, if the resistance R_S is zero (the constant time will always be less than the switching period) and even in that case, energy is lost, what is curious, since no dissipation element would be present. In this case, the energy would be dissipated through radiation or in the dielectric breakdown when the switch is almost closed.

At the beginning of the capacitor charging, the voltage across the terminals is zero. The electrons delivered by the voltage source having an energy of eV_{DD} reaches a capacitor with a near zero voltage, so, a "good" electron, eV_{DD} is lost and become a "bad" electron, $e(0)$. This transfer has bad efficiency, near zero, since almost all the electron energy is lost.

The transferred electrons start to increase the capacitor voltage. When it happens, the transfer efficiency starts to rise, since the "good electron" starts to become a "not so bad" one. When the capacitor voltage reaches $V_{DD}/2$, the transfer efficiency is 50% and increase beyond that "threshold." At the end of the charging period, the efficiency is practically 100%, since almost no voltage difference exists between the voltage source and the capacitor. The curious part is that at the end of the charging, the total transferred efficiency is 50%.

These losses also occurs when two capacitors charge each other, that is why this called charge redistribution loss.

Now, imagine that the switching period is much smaller than the constant time, in this

case, the capacitor is only slightly charged and discharge each phase, so, almost no voltage difference appears across its terminals. Similarly, as described before, it is possible to write Eq. 3.21, Eq. 3.22.

$$E_C = \frac{V_{DD}^2 T_S}{8R_S} \quad (3.21)$$

$$E_{V_{DD}} = \frac{V_{DD}^2 T_S}{4R_S} \quad (3.22)$$

Again, the transfer efficiency is 50%. The characteristics of the circuit that discharge the capacitor energy in each phase and makes the capacitor voltage to be half of the input voltage, but now, all the lost power and the storage energy depends only on the switches resistance and the time that they are on. So, this case describes the losses only to the switch resistance.

Usually, the converter operates in between these two situations, the capacitor is not fully charged and discharged in each phase and both, charge redistribution and switch resistance influences in the losses. These asymptotic losses are modeled by (SANDERS et al., 2013) like resistances and are called Resistance of Slow-Switching-Limit (R_{SSL}) to model the charge redistribution losses, and resistance of Fast-Switching-Limit (R_{FSL}) to model the losses to switches resistance. These both resistance impacts in the output resistance R_{OUT} of the static model and will be presented in the next section.

Another source of loss is the switching of parasitic and Gate capacitance of the MOS switches. These losses are similarly modeled as in Eq. 3.23. In the equations, C_{OX} is the gate capacitance, V_{OX} is the voltage across the gate capacitance, C_{Pi} is the equivalent parasitic capacitance in a point i of the SC converter net, V_{Pi} is the voltage in that point and N_P is the number of points with parasitic capacitance.

$$P_{SWITCH-LOSS} = f_S C_{OX} V_{OX}^2 + \sum_{i=1}^{N_P} f_S C_{Pi} V_{Pi}^2 \quad (3.23)$$

3.4.2 R_{SSL} and R_{FSL}

In a generic network of switches and capacitances, like the one in Fig. 3.10, the objective is to obtain expressions to calculate the impact of the losses due to charge redistribution, Slow Switching Limit R_{SSL} , and due to switches resistance, Fast Switching Limit R_{FSL} .

Like described in (SEEMAN; SANDERS, 2008), the analysis will be performed using the Tellegen's theorem. It says that for an arbitrary network, a voltage array that respects the

Kirchoff Voltage Law is orthogonal to a current array that respects the Kirchoff Current Law. This theorem can be applied in each phase of a SC DC-DC converter, like $\mathbf{v}_{\phi 1} \cdot \mathbf{q}_{\phi 1} = \mathbf{0}$ and $\mathbf{v}_{\phi 2} \cdot \mathbf{q}_{\phi 2} = \mathbf{0}$.

It is possible, then, to write two vectors for each phase, one for the voltages over the capacitors and one for the charge flow in the capacitors, Eq. 3.24 and Eq. 3.26 respectively. In those equations, $\mathbf{a}_{\phi i}$ is the vector of the charge flow in the network normalized to the output total charge flow q_O . The $\mathbf{a}_{\phi i}$ are called charge multiplier.

$$\mathbf{q}_{\phi 1} = [q_O^{\phi 1} \quad q_1^{\phi 1} \quad \dots \quad q_N^{\phi 1} \quad q_I^{\phi 1}] / q_O \quad (3.24)$$

$$\mathbf{a}_{\phi 1} = [a_O^{\phi 1} \quad \mathbf{a}_C^{\phi 1} \quad a_I^{\phi 1}] \quad (3.25)$$

$$\mathbf{v}_{\phi 1} = [v_O \quad \mathbf{v}_C^{\phi 1} \quad v_I] \quad (3.26)$$

The internal product $\mathbf{v}_{\phi 1} \cdot \mathbf{q}_{\phi 1} = \mathbf{0}$ and $\mathbf{v}_{\phi 2} \cdot \mathbf{q}_{\phi 2} = \mathbf{0}$ added leads to the relationship described by Eq. 3.27, where N_C is the number of capacitors with the input voltage kept null since the objective is to calculate an output impedance that reflects the losses of the converter.

$$v_O(a_O^{\phi 1} + a_O^{\phi 2}) + \sum_{i=1}^{N_C} (a_{C,i}^{\phi 1} v_{C,i}^{\phi 1} + a_{C,i}^{\phi 2} v_{C,i}^{\phi 2}) = 0 \quad (3.27)$$

This analysis is performed considering steady-state, so all the charge that a capacitor receives in one phase is delivered in the other, so $a_{C,i}^{\phi 1} = -a_{C,i}^{\phi 2} = a_{C,i}$. Also, the normalization consider that $a_O^{\phi 1} + a_O^{\phi 2} = 1$ and $q_i = a_{C,i} q_O$. With it in mind and multiplying Eq. 3.27 by q_O , the Eq. 3.27 is formed, where Δv_i is the voltage variation across the i -th capacitor from $\phi 1$ to $\phi 2$.

$$q_O v_O + \sum_{i=1}^{N_C} q_i \Delta v_i = 0 \quad (3.28)$$

The voltage variation across the terminals of the capacitors depends on the capacitance and the charge flow. It is possible to calculate the value of Δv_i using Eq. 3.29.

$$\Delta v_i = \frac{q_i}{C_i} \quad (3.29)$$

Replacing Eq. 3.29 in Eq. 3.28, and dividing all by q_0^2 , leads to Eq. 3.30.

$$\frac{v_O}{q_0} + \sum_{i=1}^{N_C} \frac{q_i}{q_0} \frac{1}{C_i} = 0 \quad (3.30)$$

It was already shown that q_i/q_0 is the charge multiplier $a_{C,i}$. Also, the output current i_O is defined by the switching frequency, f_S , times the output charge q_0 , so dividing the Eq. 3.30 by f_S and isolating v_O/i_O leads to Eq. 3.31.

$$R_{SSL} = -\frac{v_O}{i_O} = \sum_{i=1}^{N_C} \frac{(a_{C,i})^2}{C_i f_S} \quad (3.31)$$

Eq. 3.31 calculates the loss contribution of charge redistribution among the capacitors regarding an output impedance, R_{SSL} . It is an asymptotic limit that does not consider the switches resistances, what it the subject of the following analysis.

At the FSL asymptotic limit, the switching period is pretty smaller than the constant time of the circuit, so, no voltage variation is appreciated between the capacitor terminals and all the losses will be calculated considering the switches resistances. Like, before, it is possible to write the vector of charge flow for all the switches in the network. In this case, each switch conducts charge in one of the phases, so only one vector for the two phases is constructed where K is the number of switches, Eq. 3.32.

$$\mathbf{a}_r = [a_{r,1} \ a_{r,i} \ a_{r,K}] \quad (3.32)$$

When the converter is in FSL, the charge flows through the switches like a piece-wise constant current, in this case, the Duty-Cycle (D) matters to the loss calculations. In here it will be assumed that ϕ_1 and ϕ_2 have the same duration, so $D = 0.5$. Considering that, it is possible to calculate the current that a switch R_i conducts each period by Eq. 3.34.

$$q_{r,i} = \int_0^{T_S/2} i_{r,i} dt \quad (3.33)$$

$$i_{r,i} = 2q_{r,i} f_S \quad (3.34)$$

Considering that $q_{r,i} = a_{r,i} q_0$ and $q_0 = i_O/f_S$, it is possible to write Eq. 3.35.

$$i_{r,i} = 2a_{r,i} i_O \quad (3.35)$$

The power dissipated in the case of FSL is described as in Eq. 3.36, where K is number of switches.

$$P_{FSL} = \sum_{i=1}^{N_K} \frac{1}{2} R_i (2a_{r,i} i_O)^2 \quad (3.36)$$

Since the power loss of the circuit is being approximated by the power loss on the resistor R_{FSL} , the equivalent resistance R_{FSL} can be calculated by Eq. 3.37.

$$R_{FSL} = 2 \sum_{i=1}^{N_K} R_i (a_{r,i})^2 \quad (3.37)$$

With Eq. 3.36 and Eq. 3.37, it is possible to calculate the output impedance R_{OUT} , Eq. 3.38, of a generic SC DC-DC converter considering a network of N capacitors and K switches.

$$R_{OUT} = \sqrt{R_{FSL}^2 + R_{SSL}^2} \quad (3.38)$$

Eq. 3.39, Eq. 3.40 and Eq. 3.41 present the capacitors and switches resistance vectors for the example of the ladder 1-to-3 topology of Fig. 3.10.

$$\mathbf{a}_{\phi 1} = [1/3 \quad 2/3 \quad -1/3 \quad 1/3 \quad -1/3] \quad (3.39)$$

$$\mathbf{a}_{\phi 1} = [2/3 \quad -2/3 \quad 1/3 \quad -1/3 \quad 0] \quad (3.40)$$

$$\mathbf{a}_r = [-2/3 \quad -2/3 \quad 1/3 \quad 1/3 \quad 1/3 \quad 1/3] \quad (3.41)$$

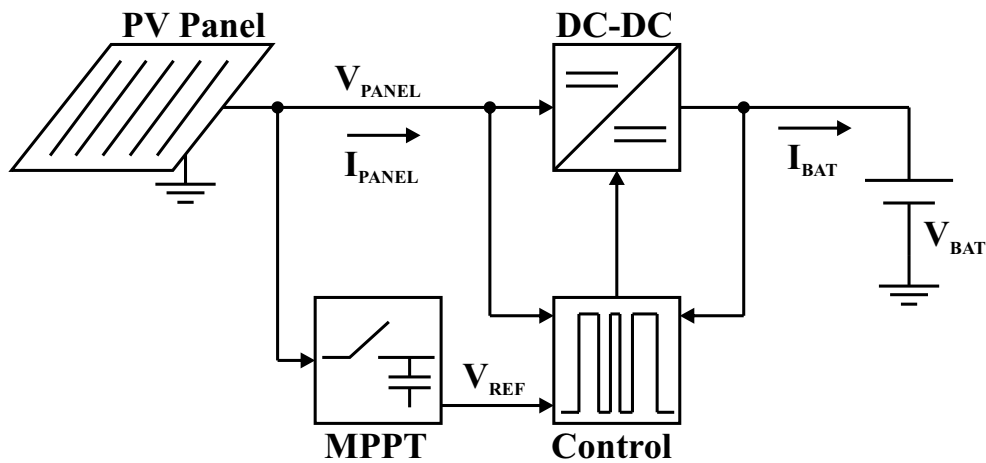
The calculus of the output impedance involves topological parameters, $a_{C,i}$ and $a_{r,i}$, and parameters than can be chosen to achieve the best design for an specify topology, C_i , R_i , and f_s .

This section presented the basis about the DC - DC conversion. The next sections will treat about the work itself, the application, proposed architecture, design methodology, tests and results.

4 ARCHITECTURE AND DESIGN METHODOLOGY

The objective of this work is to implement a harvester that can drain power from a small PV panel at its MPP and deliver it to an energy storage element, like a super cap, capacitor or battery. A LiFePO₄ battery with a 3.3 V nominal was chosen for it. Fig. 4.1 presents the block diagram of the application.

Figure 4.1: Application's block diagram.



Source: Author.

It was presented that the V_{MPP} of the chosen PV panel relies in a value between 1.6 V and 1.8 V. Since these values relies in almost half of the battery, an 1-to-2 SC DC-DC converter is proposed. Fig. 4.2 presents the complete proposed architecture.

Due to silicon area issues, the flying capacitors were not integrated, so, the first objective was to reduce board footprint area. The minimum package size of surface-mount-technology is 01005, imperial code. The highest general purpose capacitance value that manufacturers allow for purchase is up to 100 nF of capacitance (MURATA, 2017). The capacitance and the switching frequency are complementary design parameters and higher switching frequencies implies in higher losses. Higher values of capacitance can be achieved putting a N number of capacitors in parallel or higher virtual values of capacitance can be achieved adding more time-interleaved switching cores in parallel. Adding time-interleaved parallel cores has the advantage of reducing input voltage ripple (WENS, 2011), so the power of the PV panel can be drained continually without escape from the MPP. This advantage made it be the strategy chosen. For this work, six phases was chosen, due to limitations in the number of pads.

The 1-to-2 SC core, MPP Tracker, Control, Protection and Start-up are the five main blocks that compound the architecture of the converter.

The core is a time-interleaved 6-phase 1-to-2 SC DC - DC converter, where the ideal conversion ratio is 2. The six phases make the voltage ripple of input reduces, what helps the MPPT, once the voltage oscillation across the tracked point reduces considerably.

The MPPT was implemented using a Sample & Hold circuit (S&H) controlled by a 1 Hz timer, which opens the circuit and samples the open-circuit voltage of the PV panel.

An error amplifier compares the PV panel voltage with the voltage reference generated by the S&H and set the Voltage Controlled Oscillation (VCO) and tunes the switching frequency that is delivered to the Driver that creates non-overlapped pulses to drives the switches of the core.

The thick-oxide transistors and the battery have a maximum rated voltage of 3.6 V, so a protection circuit that consists of a hysteretic comparator and band gap reference was included not to allow that the output voltage suppresses that value.

Finally, the converter can operate with an output capacitor and without a battery, in this case, a start-up circuit is needed. So, a passive low-efficiency doubler is added in parallel with the main converter.

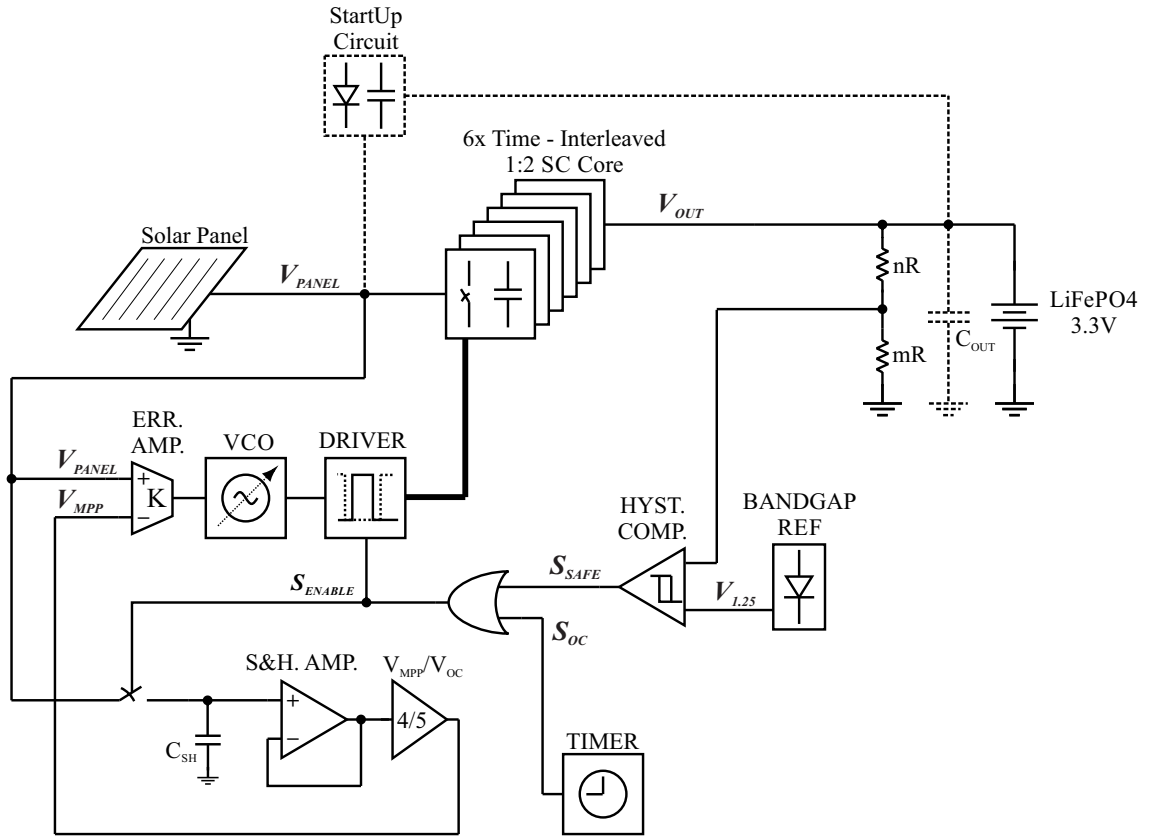
The next section will present the design of each block of the presented architecture.

4.1 1-to-2 Switched - Capacitor Core

The core of the converter is a 1-to-2 SC DC - DC converter, topology presented in Fig. 4.3. Due to the voltage levels in the transistors terminals, when the input voltage and output voltage are at their nominal values, 1.65 V and 3.3 V, respectively, thick oxide transistors of the chosen CMOS technology were used. S_2 conducts 3.3 V, so a PMOS is suitable for this case, S_4 conducts zero, so an NMOS is appropriate. Transistors S_1 and S_3 conducts an intermediate voltage, in this case, the best option would be a switch based on NMOS, but a PMOS was chosen due to a start-up strategy, that will be presented later.

It operates in two phases. In phase 1 (ϕ_1), Fig. 4.4 (a), switches S_1 and S_4 charges the flying capacitor C_{FLY} putting it in parallel with the input voltage source, in this case, switches S_2 and S_3 are closed. In phase 2 (ϕ_2), Fig. 4.4 (b), switches S_2 and S_3 are closed making the charge stored in ϕ_1 flows to the output putting the input voltage source in series with the C_{FLY} , in this case, switches S_1 and S_4 are closed. This parallel/series variation lets the output voltage to be, ideally, the double of the input voltage.

Figure 4.2: Proposed architecture.



Source: Author.

Since the capacitors are already defined to be 100 nF, the objective here is to size the transistors. For this task, the parasitic and the control losses will be ignored. So, SSL, FSL and the switching losses will be the considered ones. First, let's write the charge multipliers for the C_{FLY} and for the switches in form of vectors, Eq. 4.1, Eq. 4.2 and Eq. 4.3 according with the charge flow presented in Fig. 4.4.

$$\mathbf{a}_C^{\phi 1} = [0 \ 1 \ 1] \quad (4.1)$$

$$\mathbf{a}_C^{\phi 2} = [1 \ -1 \ 1] \quad (4.2)$$

$$\mathbf{a}_R = [1 \ 1 \ 1 \ 1] \quad (4.3)$$

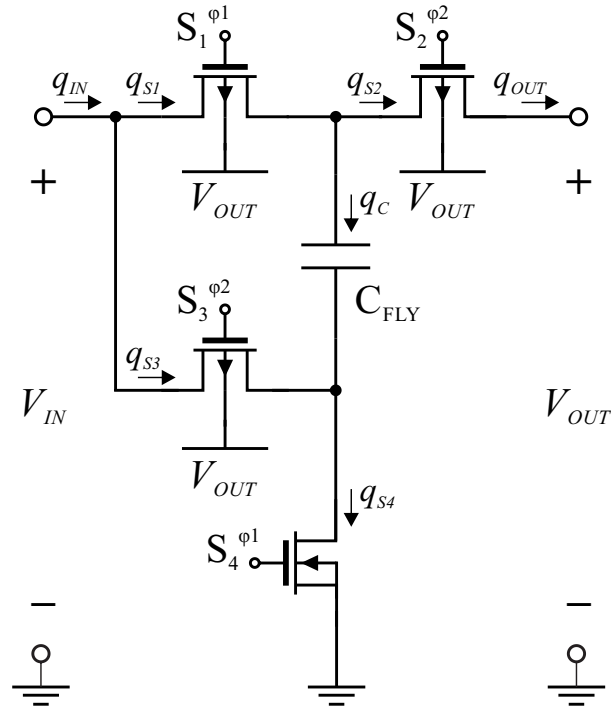
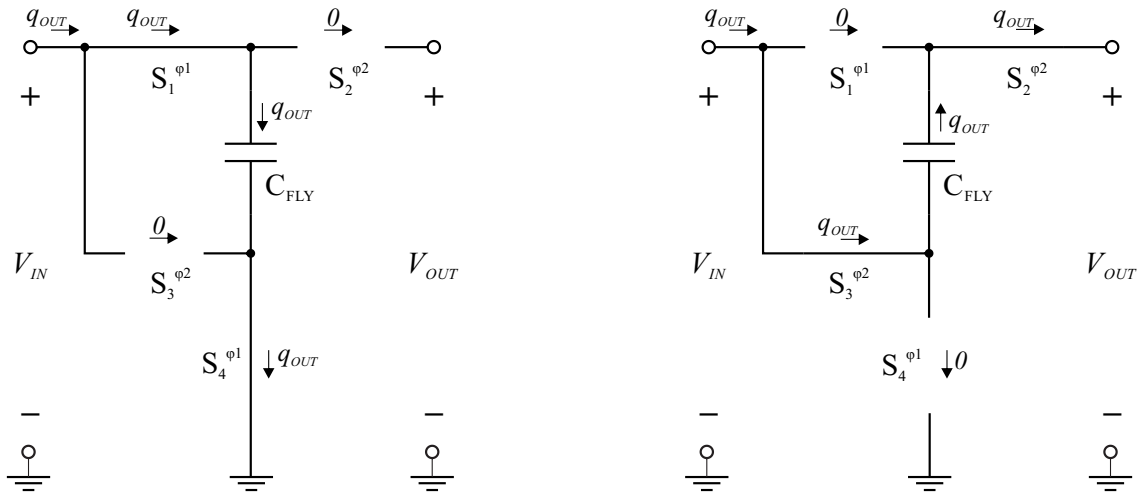


Figure 4.3: 1-to-2 SC Topology.

Source: Author.

Figure 4.4: 1-to-2 SC operation.



Source: Author.

Based on these vectors, it is possible to calculate the R_{SSL} and R_{FSL} resistances, like in Eq. 4.4 and Eq. 4.5.

$$R_{SSL} = \sum_{i=1}^{N_C} \frac{(a_{C,i})^2}{C_i f_S} = \frac{1}{f_S C_{FLY}} \quad (4.4)$$

$$R_{FSL} = 2 \sum_{i=1}^{N_K} R_i (a_{r,i})^2 = 2(R_{S1} + R_{S2} + R_{S3} + R_{S4}) \quad (4.5)$$

The values of the resistances of the switches S_i are defined by Eq. 4.6, where R_N is the resistivity (inverse of the g_{DS} for minimum channel length) of the transistor NMOS, R_P the resistivity of the PMOS, W_P is the width of the PMOS, W_N is the width of the NMOS α is a derating coefficient that changes the resistivity due to the voltage level that the transistor conducts.

$$R_{S_i} = \alpha \frac{R_{N(P)}}{W_{N(P)}} \quad (4.6)$$

Transistors PMOS were chosen to have twice the size of the NMOS, minimizing area for a given resistance (BAWA; GHOVANLOO, 2009), so $W_P = 2W_N$, Eq. 4.8 calculates the resistance R_{FSL} with respect to the NMOS size W_N ($W = W_N$) and with $\alpha = 2$.

$$R_{FSL} = 2 \left(\alpha \frac{R_P}{2W} + \frac{R_P}{2W} + \alpha \frac{R_P}{2W} + \frac{R_N}{W} \right) \quad (4.7)$$

$$R_{FSL} = \frac{5R_P + 2R_N}{W} \quad (4.8)$$

With the R_{SSL} and R_{FSL} calculated, it is possible to obtain the output impedance R_{OUT} , Eq. 4.9.

$$R_{OUT} = \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\left(\frac{1}{C_{FLY} f_S} \right)^2 + \left(\frac{5R_P + 2R_N}{W} \right)^2} \quad (4.9)$$

So, the power loss due to the SSL and FSL effects, can be calculated considering an output rms current I_{OUT} , like in Eq. 4.10.

$$P_{SSL-FSL-LOSSES} = R_{OUT} I_{OUT}^2 = I_{OUT}^2 \sqrt{\left(\frac{1}{C_{FLY} f_S} \right)^2 + \left(\frac{5R_P + 2R_N}{W} \right)^2} \quad (4.10)$$

The next step is to calculate the losses due to switching. There are four switches with three PMOS and one NMOS, so, the total width is $7W$, with all transistors with minimum channel length. Considering that all the transistors have piratically the same capacitance density, it is possible to write the switching losses like in Eq. 4.11.

$$P_{SW-LOSSES} = 7W C_{GG} f_S V_{OUT}^2 \quad (4.11)$$

Eq. 4.12 sets the expression that compounds the switching losses, SSL and FSL depending only of the size W and the switching frequency f_S .

$$P_{LOSSES} = 7W C_{GG} f_S V_{OUT}^2 + I_{OUT}^2 \sqrt{\left(\frac{1}{C_{FLY} f_S} \right)^2 + \left(\frac{5R_P + 2R_N}{W} \right)^2} \quad (4.12)$$

The values of resistivity and capacitance density were extracted of the CMOS GF RF 130 nm technology and they are presented in Appendix A.

Chapter 3 presented the measurements of the PV panel and it shows the power limits presented in Tab. 4.1. Those limits were used to design the power switches using a script in MATLAB.

Table 4.1: Power Limits of the PV panel.

Time	Power (mW)	V_{MPP} (V)	I_{MPP} (mA)
12:00	60.0	1.70	35.4
18:00	4.4	1.65	2.73

Source: Author.

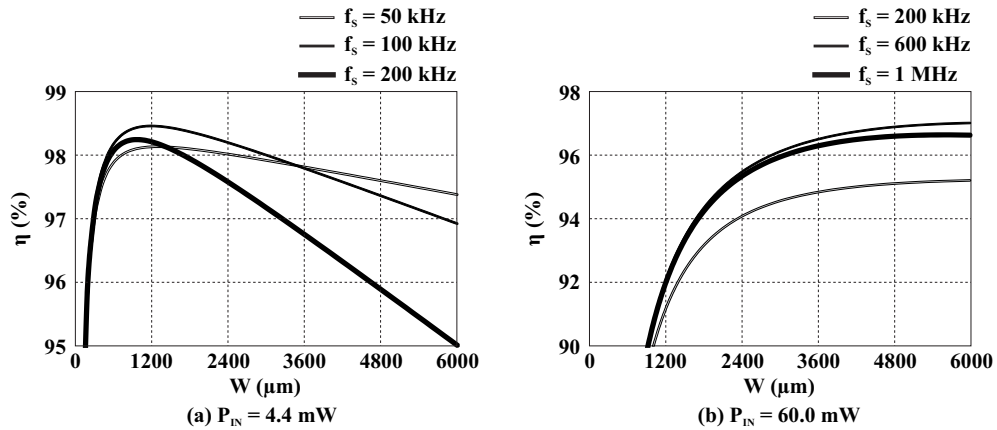
Six phases splits the input current in six. It makes the switches sizes of each phase to be reduced by six too. To simplify calculations, the design methodology presented here consider just one phase to obtain the size of transistors. In the next sections, the design of the blocks will be presented

The objective of the MATLAB script was to optimize the size of the switches for the maximum possible efficiency using Eq. 4.13, where P_{IN} is considered to be the input power at maximum power point of the solar panel for a particular point of irradiation. The flying capacitor was chosen 600 nF of total capacitance in the script, due to the 6 phase strategy. The MPPT strategy tunes the switching frequency, what makes it scales with the input power, so there is an optimum f_s for each input power. These optimum switching frequencies were found using MATLAB plotting a matrix of efficiency, $\eta_{LOSSES}(W, f_s)$ for the two limits of input power. Fig. 4.5 presents the efficiency per switch width for three different frequencies. In (a) is possible to notice that the peak of efficiency for the minimum input power appears for the switching frequency of 100 kHz. In (b) is possible to notice that the peak of efficiency for the maximum input power appears for the switching frequency of 600 kHz.

$$\eta = 100\% \frac{P_{IN} - P_{LOSSES}}{P_{IN}} \quad (4.13)$$

$$P_{IN} = V_{MPP} I_{MPP} \quad (4.14)$$

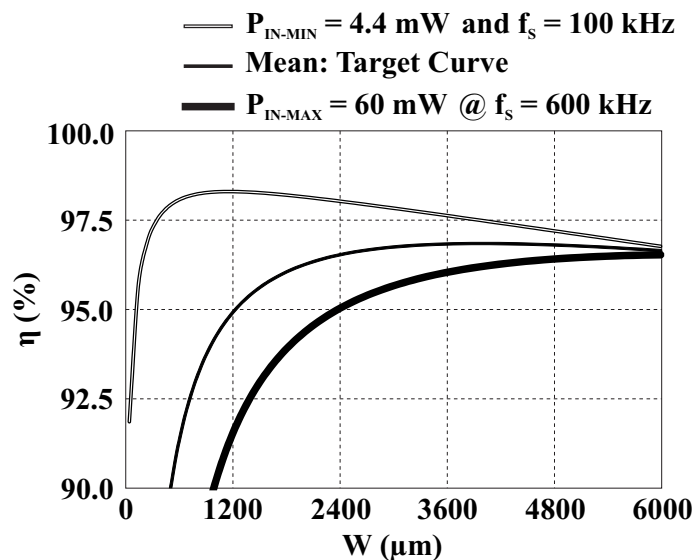
Figure 4.5: Optimum switching frequencies for different input powers.



Source: Author.

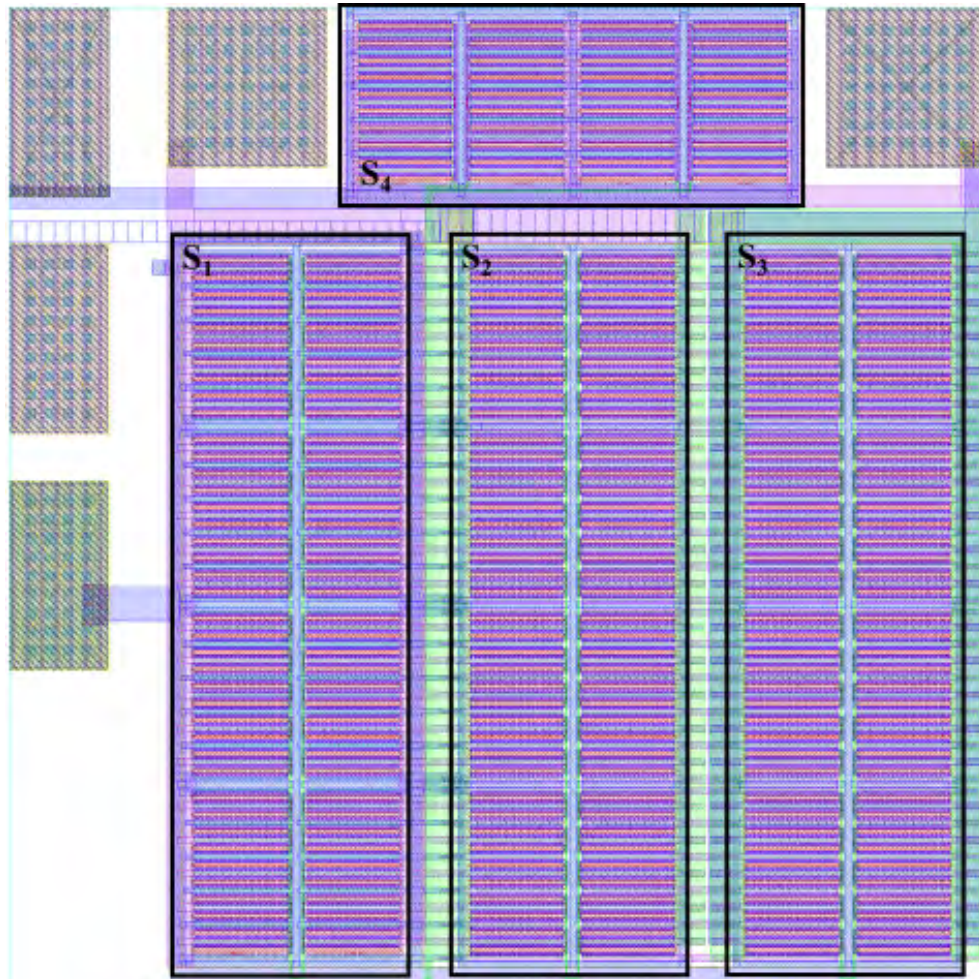
These two pair, frequency-input power, was used to find the best W . Fig 4.6 presents these two curves together with the means between them. This mean curve was used to find the optimum W . It is possible to notice that for W larges than $2400 \mu\text{m}$ there is no much increase in efficiency, so, to minimize area, this was the size chosen for W .

Finally, the total size of the NMOS transistors was $2400 \mu\text{m}$ and the PMOS ones $4800 \mu\text{m}$. It was considered one phase to calculates these values and since there are 6 phases in parallel, the size of each phase was devided by six, so NMOS and PMOS sizes for each phase are $400 \mu\text{m}$ and $800 \mu\text{m}$ respectively, for a minimum channel length of 400 nm . The layout of a phase core is presented in Fig. 4.7.

Figure 4.6: Optimum W curves.

Source: Author.

Figure 4.7: Layout of the converter core (105 μm x 105 μm).



Source: Author.

4.2 MPP Reference Generator & Protection

This section will describe the design of the MPP Reference Generator and the circuit of Protection.

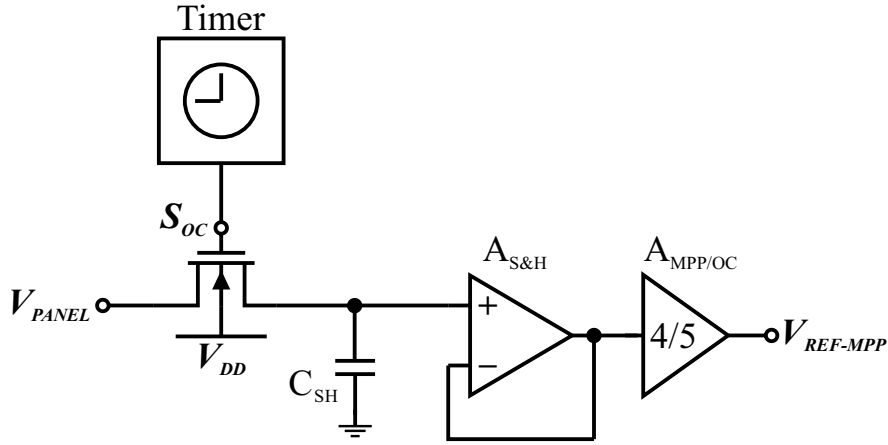
4.2.1 MPP Reference Generator

The voltage reference generator for MPPT is accomplished by a periodic measurement of the PV panel open-circuit voltage. The implementation of this task is performed by a S&H circuit, Fig. 4.8, that enables and disables the converter pulses, samples the open-circuit voltage

of the PV panel and multiply by a $4/5$ coefficient to generate the maximum power point voltage. The next subsection will treat about each sub block.

The timer frequency is not a main concern of the overall project, some commercial ICs define this frequency to be 0.062 Hz with a duty cycle of 1% (TEXAS, 2011). It is done in a way that it does not impact in the efficiency of the converter. Of course, larger the period, larger must the sampling capacitance, due to charge loss for leakage of the switches. For this work, 2 Hz timer was chosen to accomplish the task of sampling the open-circuit voltage and then using a reduced area of an integrated capacitor. The timer topology was based on a current starving Ring-Oscillator, Fig. 4.9.

Figure 4.8: Sample & Hold circuit topology.



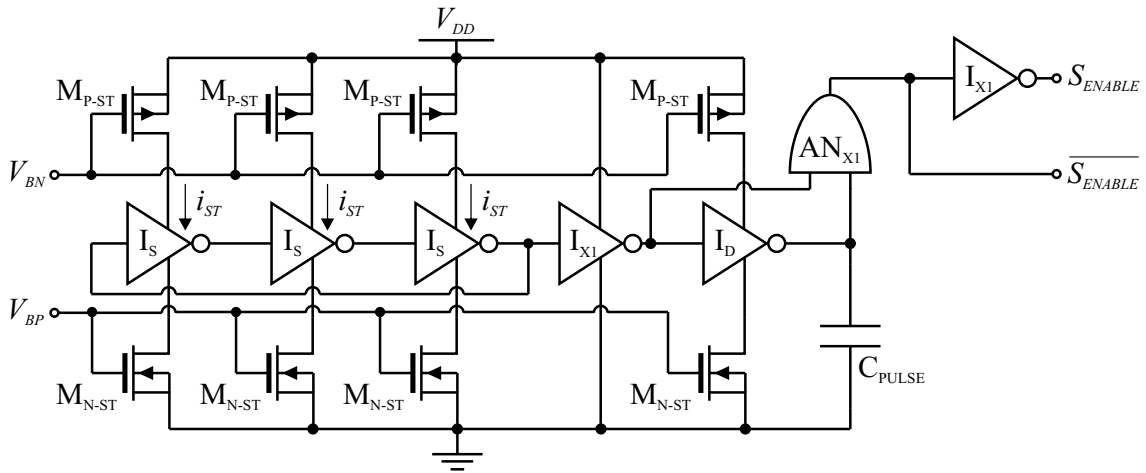
Source: Author.

In Fig. 4.9, the transistors M_{P-ST} and M_{N-ST} limit the maximum supply current, i_{ST} , of the inverters I_S . This limitation controls the time that the gate capacitance of those inverters charges and discharges. Also, these transistors are designed to have a size that creates a specific capacitance. Controlling gate supply current and the gate capacitance, the switching frequency can be controlled.

An RO of three stage generates an oscillation frequency that can be calculated by Eq. 4.15, where t_D is the propagation delay of the inverter. Six delays are necessary to form the output signal, three high-to-low and three low-to-high.

$$f_S = \frac{1}{6t_D} \quad (4.15)$$

Figure 4.9: Timer topology.



Source: Author.

The propagation delay is the time to the output voltage of the inverter reaches half of the supply voltage in a transition. The voltage change is controlled by current sources charging gate capacitance, the value of t_D can be calculated as in Eq. 4.16, what leads to the value of the oscillation frequency, Eq. 4.17, for a supply voltage of 3.3V.

$$t_D = \frac{C_{GG}V_{DD}}{2i_{ST}} \quad (4.16)$$

$$f_S = \frac{i_{ST}}{10C_{GG}} \quad (4.17)$$

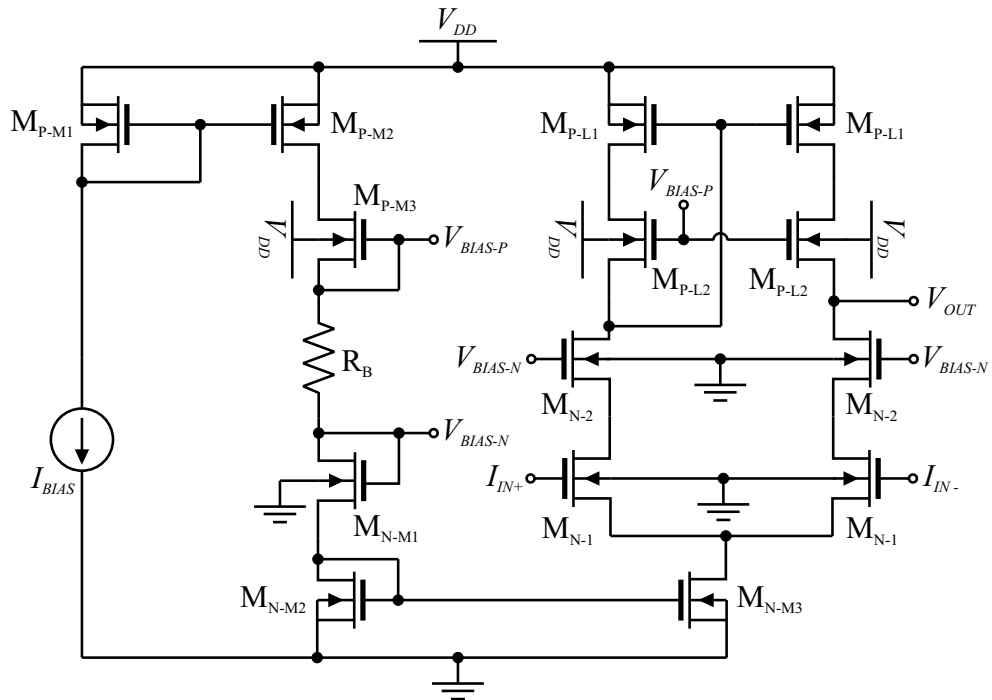
The circuit of Fig. 4.10 defines i_{ST} as 500 pA, that is a current mirror that generates the V_{BN} and V_{BP} voltages. The bias I_{BIAS} is 20 nA, and it is generated by a bias circuit that will be presented later in this work.

Inverter I_S was sized to have an equivalent total gate capacitance of 25 pF. This capacitance with a current i_{ST} of 500 pA implies in a f_S of 2 Hz, Eq. 4.18.

$$f_S = \frac{500pA}{10 \times 25pF} = 2Hz \quad (4.18)$$

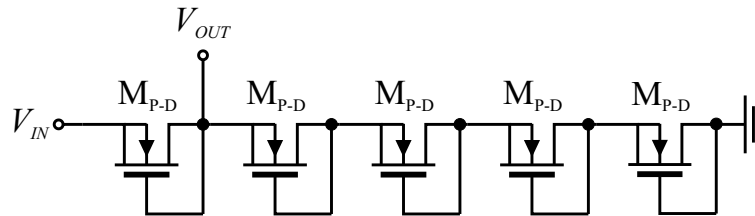
Two pulses were generated, one with a small duty-cycle to close the sample-&-hold switch and the complement of it to enable/disable the pulses of the converter core. It is accomplished adding in the final stage a capacitor C_{PULSE} that poses a capacitance different from the inverter I_S gate capacitance, what leads to a difference in the propagation delay. These two signals are "multiplied" in an AND logic gate and inverted, then two complementary signals

Figure 4.11: Telescopic op-amp topology.



Source: Author.

Figure 4.12: PMOS divider.



Source: Author.

The switch of the Sample & Hold was chosen to have the minimum size to reduce leakage and the capacitance based on it.

The sizes of the transistors, resistor and capacitors are presented in Tab. 4.2, Tab 4.3 and Tab. 4.4. The digital blocks will be presented later.

Table 4.2: Timer sizing.

	L (μm)	W (μm)	C (fF)
M_{P-ST}	1.0	1.0	-
M_{N-ST}	1.0	0.5	-
M_{P-M1}	1.0	6.0	-
M_{P-M2}	1.0	6.0	-
M_{P-M3}	1.0	1.0	-
M_{N-M1}	1.0	20.0	-
M_{N-M2}	1.0	0.5	-
C_{PULSE}	8.5	8.5	680.0

Source: Author.

Table 4.3: Op-amp sizing.

	L (μm)	W (μm)	R (kΩ)
M_{P-M1}	0.4	0.5	-
M_{P-M2}	0.4	16.0	-
M_{P-M3}	4.0	8.0	-
M_{N-M1}	4.0	1.0	-
M_{N-M2}	0.4	5.0	-
M_{N-M3}	0.4	10.0	-
M_{N-1}	10.0	1.0	-
M_{N-2}	4.0	8.0	-
M_{P-L1}	4.0	8.0	-
M_{P-L2}	4.0	8.0	-
R_B	0.28	160	50.0

Source: Author.

Table 4.4: S&H sizing and Divider.

	L (μm)	W (μm)	C (pF)
M_{P-SH}	0.4	0.5	-
C_{SH}	20.0	20.0	2.5 p
M_{P-D}	5.0	0.5	-

Source: Author.

4.2.2 Protection

The maximum voltage that the battery and the thick-oxide transistors can handle is 3.6 V. Because of it, a circuit of protection stops the charging process when the output voltage reaches it. Fig. 4.13 presents the circuit of protection chosen.

A hysteresis comparator makes a comparison between the output voltage divided by the resistors nR and mR and a voltage reference. If the signal is larger the 3.6 V, a safety signal is generated. Once the output voltage falls below 3.2 V the signal is released. Fig. 4.14 presents the comparator topology.

Transistors M_{N5} and M_{N6} are sized in order to create the intended hysteresis. Larger the conductance difference of them, larger the hysteresis loop, the M_{P4} ones sense the input signals, M_{P3} bias the circuit, M_{N4} and M_{P2} create a single output through current mirroring. The value of I_{BIAS} is 700 nA and the sizing of transistors are presented in table Tab. 4.5.

Figure 4.13: Circuit of protection.

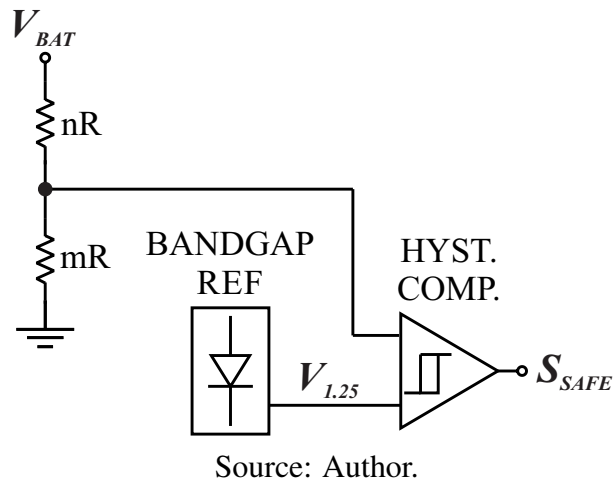


Figure 4.14: Comparator topology.

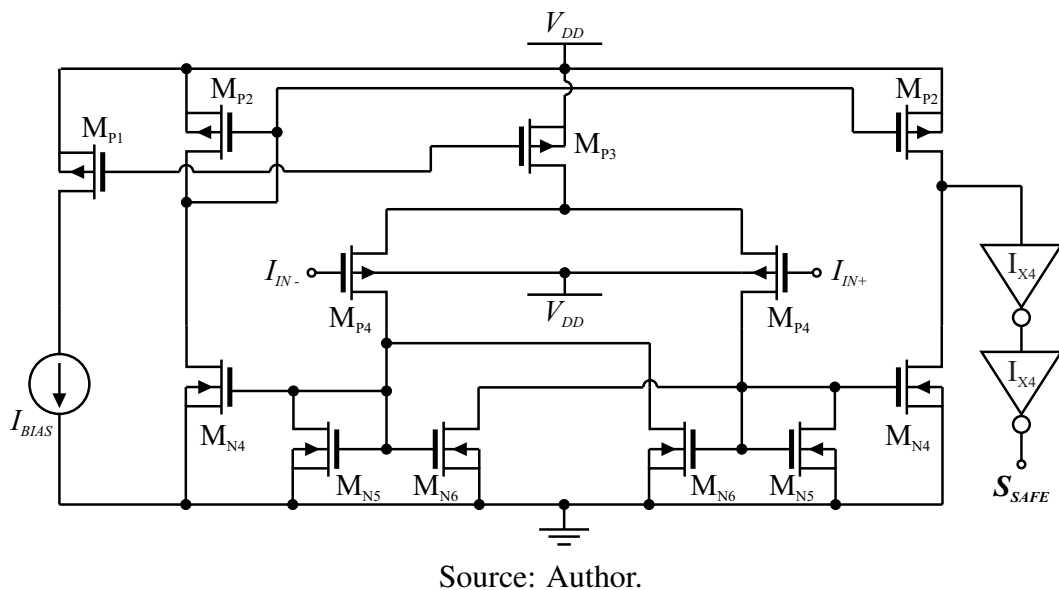


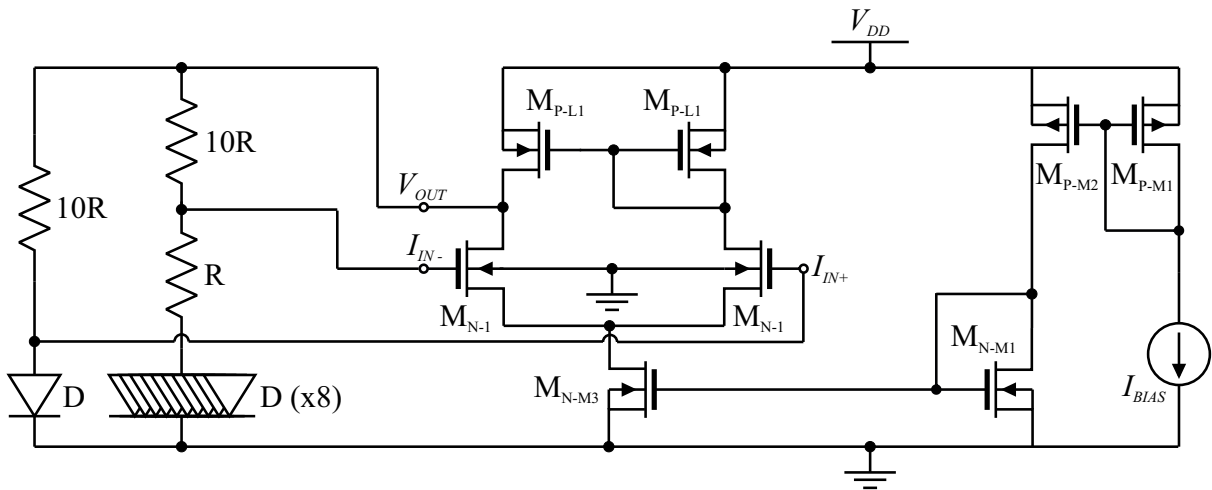
Table 4.5: Comparator sizing

	L (μm)	W (μm)
M_{P1}	2.0	5.0
M_{P2}	1.0	10.0
M_{P3}	2.0	5.0
M_{P4}	1.0	2.0
M_{N4}	1.0	5.0
M_{N5}	1.0	2.0
M_{N6}	1.0	5.0

Source: Author.

A bandgap reference topology like in Fig. 4.15 was designed using the designed method presented in (RAZAVI, 2001). The feedback is performed by an ordinary differential amplifier.

Figure 4.15: Bandgap voltage reference topology.



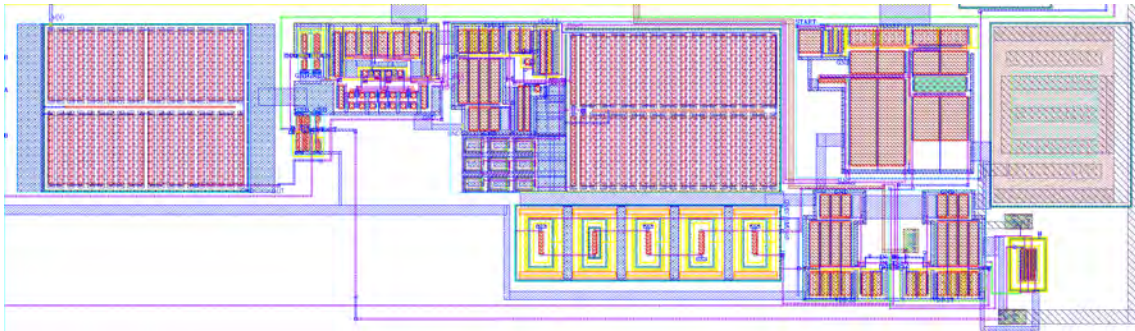
Source: Author.

The size of the devices are presented in table Tab. 4.6 and the layout of the complete MPP Reference Generator & Protection is presented in Fig. 4.16.

Table 4.6: Bandgap sizing.

	L (μm)	W (μm)	R ($\text{k}\Omega$)
M_{N-1}	2.0	20.0	-
M_{P-L1}	2.0	10.0	-
M_{N-M1}	1.0	1.0	-
M_{N-M3}	1.0	10.0	-
M_{P-M1}	1.0	1.0	-
M_{P-M2}	1.0	20.0	-
D	1.0	2.0	-
R	0.740	16.0	40.0

Source: Author.

Figure 4.16: MPP Reference Generator & Protection ($150 \mu\text{m} \times 260 \mu\text{m}$).

Source: Author.

4.3 Control & Driver

To control the power that the converter drains from the PV panel, an error amplifier was placed to amplify the difference between V_{PANEL} with the reference voltage generated by the MPP Reference Generator. This signal tunes the Voltage Controlled Oscillator (VCO), that generates the pulses for the driver. This last one is responsible for generating all the 24 signals necessary to turn-on and turn-off the switches correctly with no overlap to avoid short circuits. Fig. 4.17 shows the control and drive scheme.

The error amplifier topology chose was a simple differential amplifier, Fig. 4.18 with the same sizing of the used in the bandgap. Its gain was tuned by simulations in order to reduce oscillations and stabilize the closed loop.

The output voltage of the error amplifier was used to set the oscillation frequency of a Ring-Oscillator based VCO. Fig. 4.19 presents the VCO chosen topology. The optimum switching frequencies for the power limits defined in this work were 100 kHz and 600 kHz. So, the range of frequencies that the VCO must cover must contain these two limits. It was

designed a 10 kHz to 1 MHz VCO ring-oscillator, for an input voltage variation that goes from 1 V to 3 V in the input V_{CTRL} .

Figure 4.17: Control & Drive scheme.

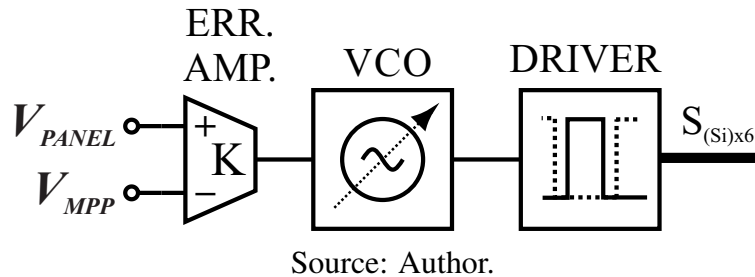
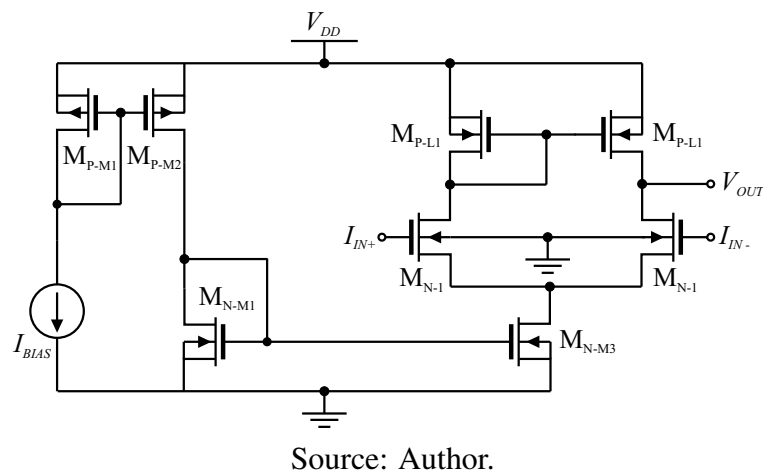
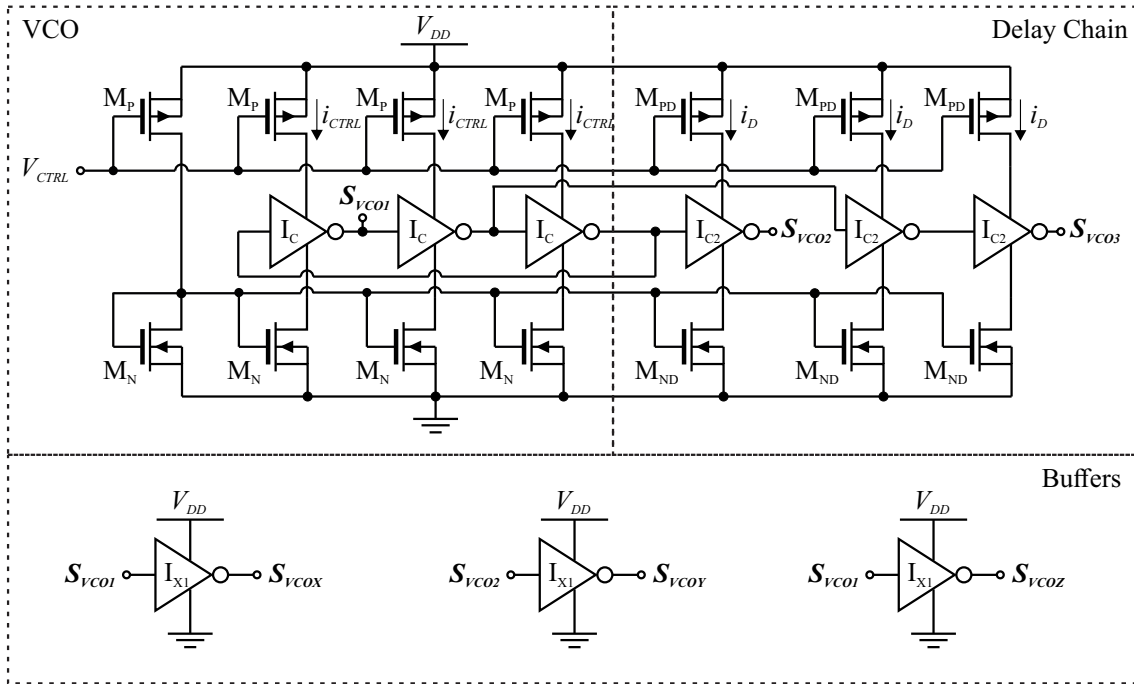


Figure 4.18: Differential amplifier.



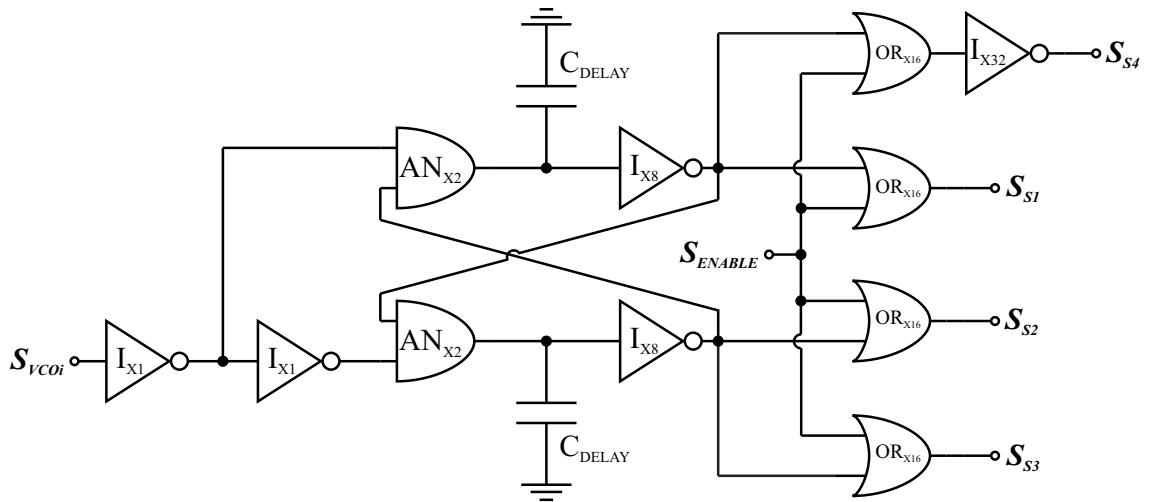
Signals S_1 and S_4 can not overlap with the signals S_2 and S_3 , so a non-overlapping clock driver was implemented. It is presented in Fig. 4.20. Each driver creates 4 signals to drive the power switches. It is compound by a cross-coupled circuit with a line of delay that controls the dead-zone. These non-overlapping signals pass through an OR gate that can enables/disables the pulses that go to the switches. The size of the logic gates is scaled up until the last logic gate has the size enough to drive the large gate capacitance of the power switches with proper timing. The complete layout of the Control & Driver is presented in Fig. 4.21.

Figure 4.19: VCO schematic.



Source: Author.

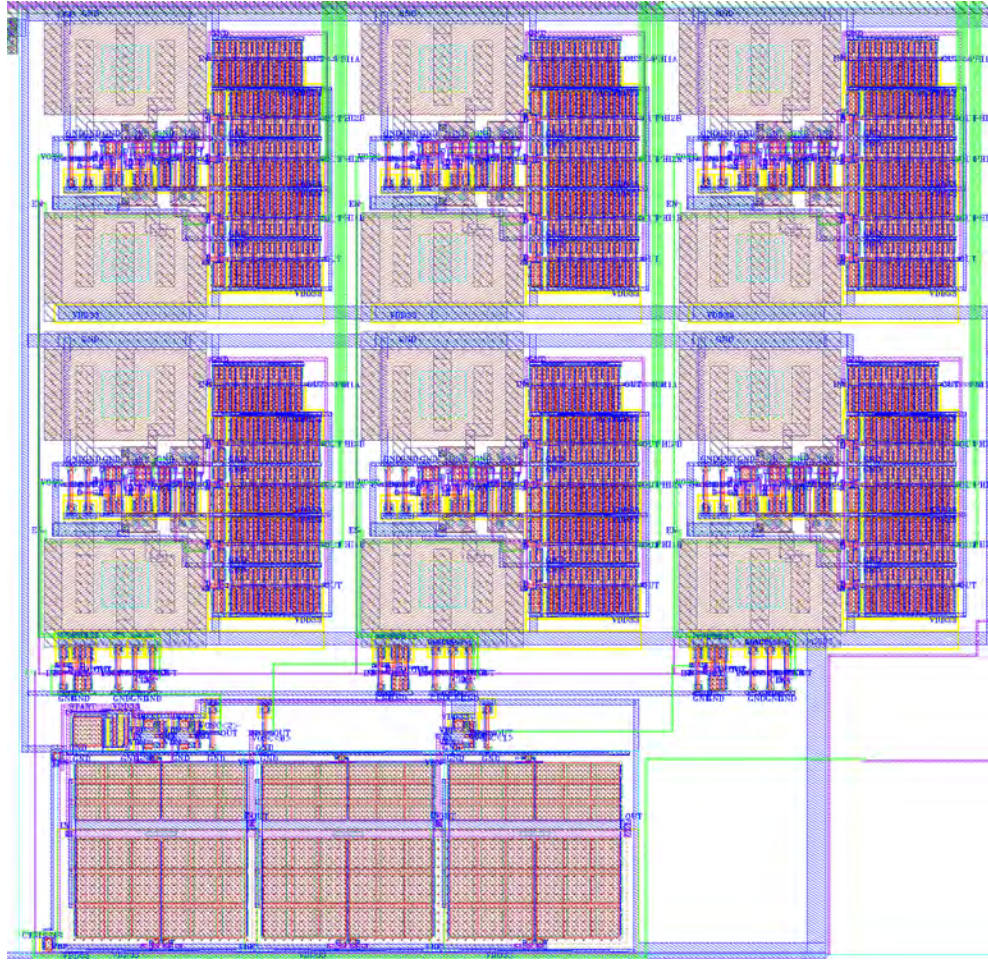
Figure 4.20: Non-overlapping driver schematic.



Source: Author.

4.4 Digital Blocks & Current Bias

All the previous presented blocks needed a current bias and some digital auxiliary blocks. This section will present them.

Figure 4.21: Control & Driver layout (150 μm x 140 μm).

Source: Author.

4.4.1 Current Bias

The current bias circuit topology chosen was the one presented in Fig. 4.22. The circuit is a self-biased mirrored circuit that generate an equal current in both branches. Resistors and the aspect ratio between M_{N2} and M_{N1} defines the current i_{BIAS0} like in Eq. 4.19, Eq. 4.20, where K is the ratio between the sizes of M_{N2} and M_{N1} and V_S is the voltage over R . A voltage reference V_{BN} is generated to mirror the generated reference to the blocks by transistors M_{3-7} .

$$i_{BIAS0} = \frac{\mu_n C_{OX}}{2} \frac{W_{N1}}{L_{N1}} (V_{BN} - V_{TH})^2 \quad (4.19)$$

$$i_{BIAS0} = K \frac{\mu_n C_{OX}}{2} \frac{W_{N1}}{L_{N1}} (V_{BN} - V_S - V_{TH})^2 \quad (4.20)$$

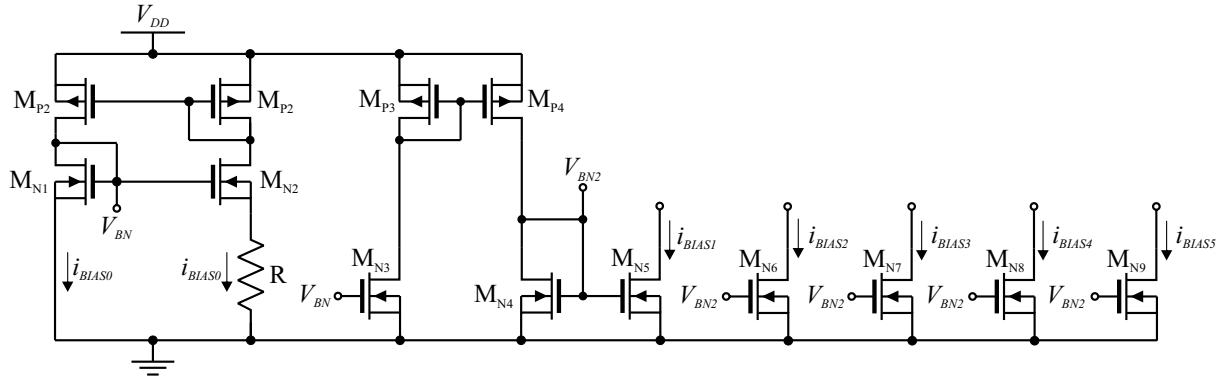


Figure 4.22: Current Bias topology.

Source: Author.

Finally, Eq. 4.21 is constructed replacing Eq. 4.20 in Eq. 4.19 and relates the degrees of freedom of the design.

$$\sqrt{K} = \frac{1}{1 - \frac{i_{BIAS0}R}{V_{BN} - V_{TH}}} \quad (4.21)$$

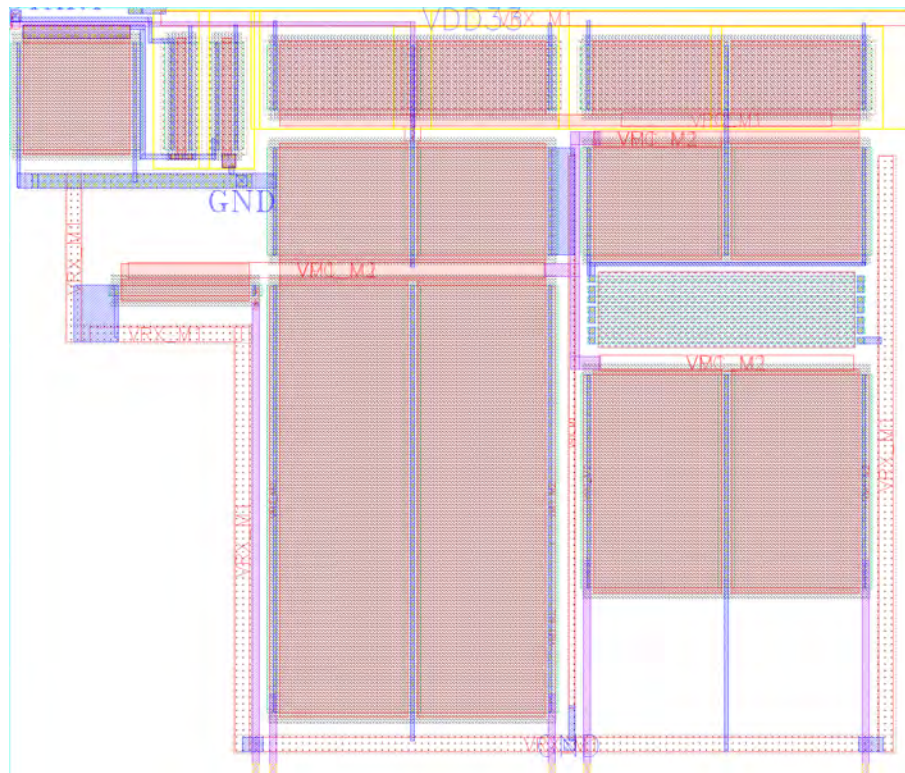
The currents i_{BIAS0} of $10 \mu\text{A}$, i_{BIAS1} of 20 nA , i_{BIAS2} of 400 nA , i_{BIAS3} of 400 nA , i_{BIAS4} of 700 nA and i_{BIAS5} of 700 nA were chosen. The designed was performed using the parameters extracted and presented in Appendix A. Tab. 4.7 presents the sizing.

Table 4.7: Ibias sizing.

	L (μm)	W (μm)	R ($\text{k}\Omega$)
M_{P2}	2.0	12.0	-
M_{P3}	2.0	10.0	-
M_{P4}	2.0	1.0	-
M_{N1}	2.0	1.4	-
M_{N2}	2.0	5.6	-
M_{N3}	2.0	1.4	-
M_{N4}	2.0	20.0	-
M_{N5}	2.0	0.5	-
M_{N6}	2.0	6.0	-
M_{N7}	2.0	6.0	-
M_{N8}	2.0	12.0	-
M_{N9}	2.0	12.0	-
R	0.320	72.0	19.0

Source: Author.

The layout of the the bias circuit is presented in Fig. 4.23.

Figure 4.23: Current Bias layout ($35 \mu\text{m} \times 42 \mu\text{m}$).

Source: Author.

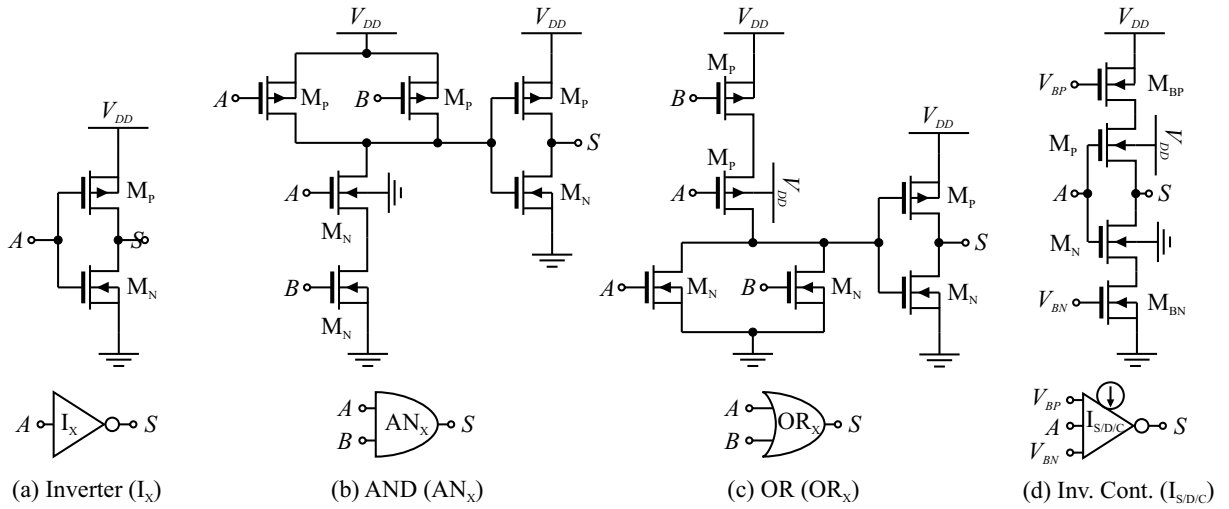
4.4.2 Digital Blocks

It was custom designed four different kinds of digital blocks using the thick-oxide transistors. They are: Inverters; ANDs; ORs; and current controlled inverters. Fig. 4.24 presents them. The sizing of them was done in order to keep the conductance of the PMOS side equals to the NMOS one. The right aspect ratio was found performing a DC sweep at the input of an inverter for different aspect ratios, Fig. 4.25 shows it.

Altogether, 12 blocks were designed, Tab. 4.8 presets all of them and their sizes. Inverters I_{X1-X64} were used for different tasks in the previous presented blocks. I_C, I_{C2}, I_S and I_D are current controlled inverters that were used in the ROs and in the delay chains. AN_{X2}, OR_{X4} and OR_{64} were used in the drivers and to perform some logic tasks.

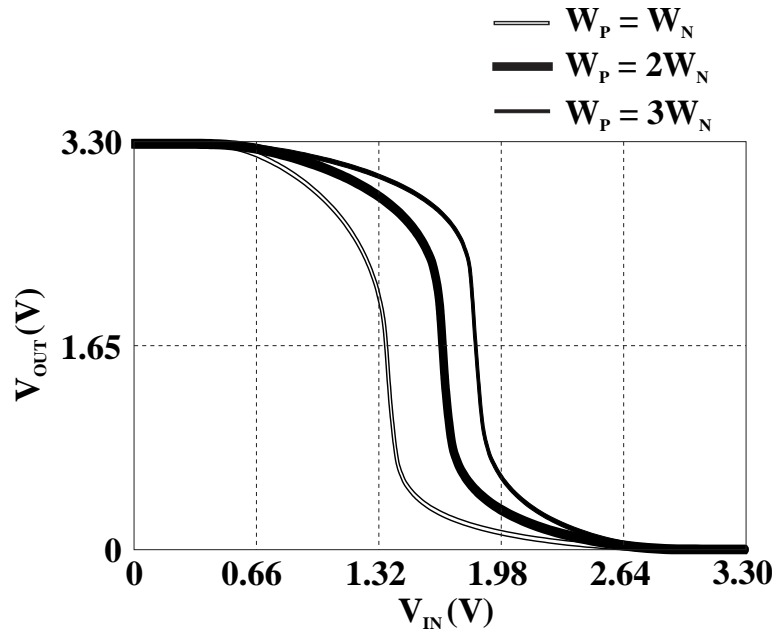
All the layouts of the digital blocks are presenter if the following figures.

Figure 4.24: Digital blocks designed.



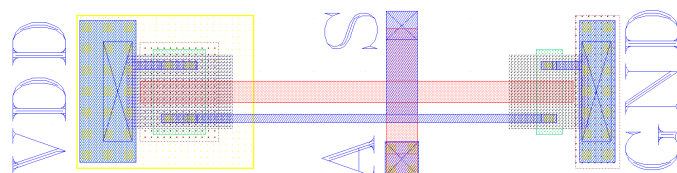
Source: Author.

Figure 4.25: Inverter DC Sweep Simulation for different Aspect Ratios.



Source: Author.

Figure 4.26: INX1 ($2.9 \mu m \times 10.4 \mu m$).

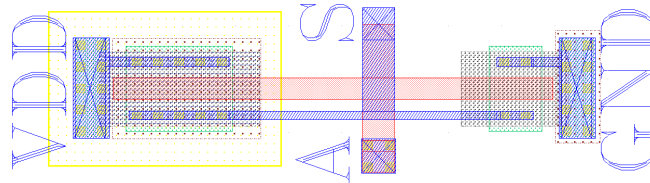


Source: Author.

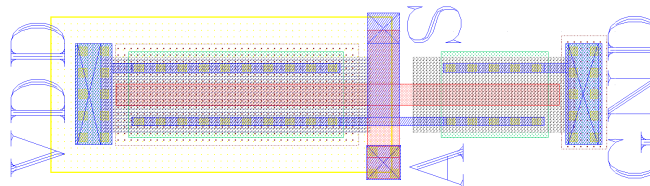
Table 4.8: Digital blocks sizes.

Block	Type	L (μm)	W_N (μm)	W_P (μm)	$L_{BN(P)}$ (μm)	W_{BN} (μm)	W_{BP} (μm)	Size $_{W \times L}$ ($\mu m \times \mu m$)
I_{X1}	INV.	0.4	0.5	1.0	-	-	-	2.9 x 10.4
I_{X2}	INV.	0.4	0.5	1.0	-	-	-	2.9 x 10.4
I_{X4}	INV.	0.4	0.5	1.0	-	-	-	2.9 x 10.4
I_{X8}	INV.	0.4	0.5	1.0	-	-	-	3.9 x 10.4
I_{X64}	INV.	0.4	0.5	1.0	-	-	-	17.6 x 10.4
I_C	INV.	15.0	15.0	30.0	1.0	0.5	1.0	36.5 x 37
I_{C2}	INV.	0.4	1.0	2.0	1.5	0.5	1.0	5.5 x 7.6
I_S	INV.	30.0	30.0	60.0	1.0	1.0	2.0	73.6 x 67.5
I_D	INV.	5.0	5.0	10.0	1.0	1.0	2.0	11.0 x 20.0
AN_{X2}	AND	0.4	2.0	2.0	-	-	-	4.9 x 10.4
OR_{X4}	OR	0.4	2.0	4.0	-	-	-	4.9 x 10.4
OR_{X64}	OR	0.4	32.0	64.0	-	-	-	20.9 x 10.4

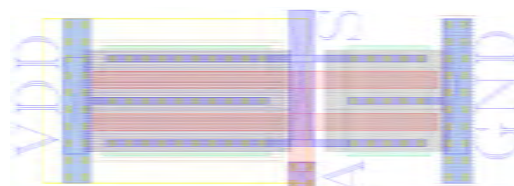
Source: Author.

Figure 4.27: $INX2$ ($2.9 \mu m \times 10.4 \mu m$).

Source: Author.

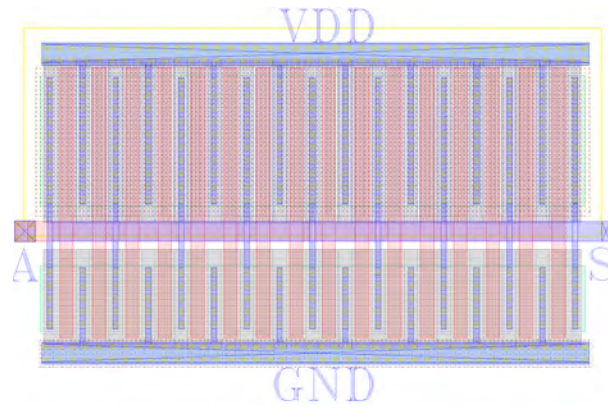
Figure 4.28: $INX4$ ($2.9 \mu m \times 10.4 \mu m$).

Source: Author.

Figure 4.29: $INX8$ ($3.9 \mu m \times 10.4 \mu m$).

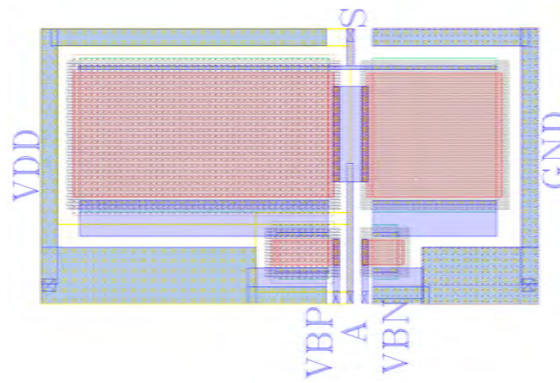
Source: Author.

Figure 4.30: INX64 ($17.6 \mu\text{m} \times 10.4 \mu\text{m}$).



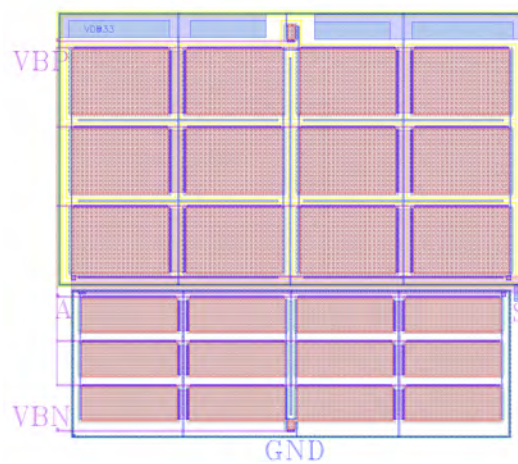
Source: Author.

Figure 4.31: ID ($11.0 \mu\text{m} \times 20.0 \mu\text{m}$).

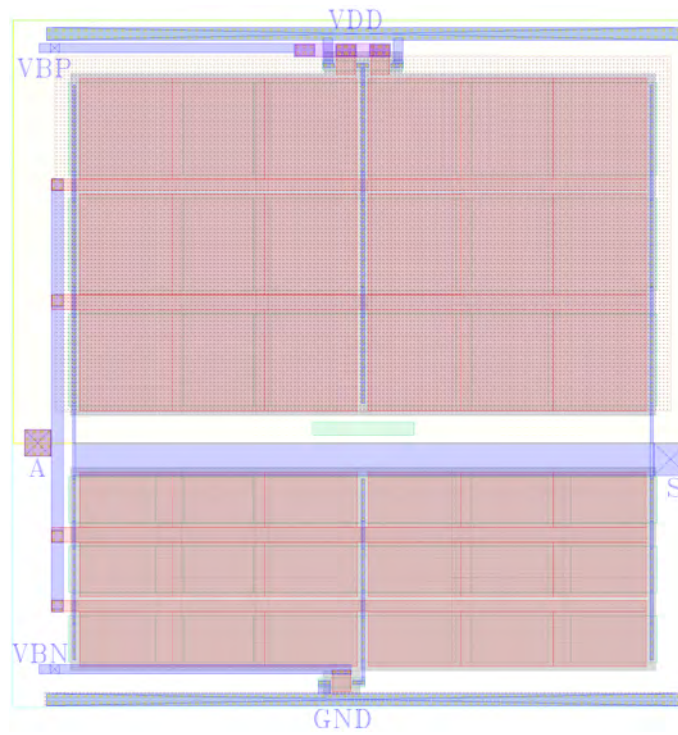


Source: Author.

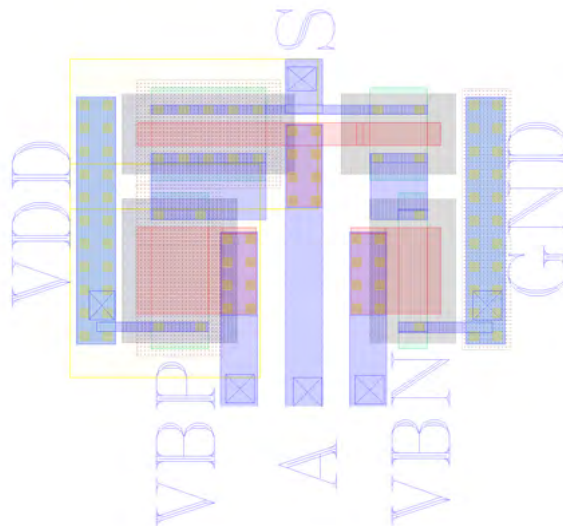
Figure 4.32: IS ($73.6 \mu\text{m} \times 67.5 \mu\text{m}$).



Source: Author.

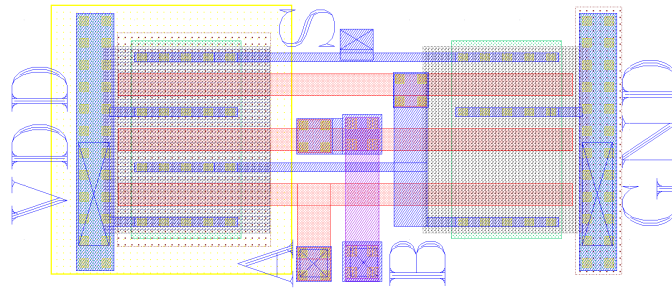
Figure 4.33: IC (36.5 μm x 37.0 μm).

Source: Author.

Figure 4.34: IC2 (5.5 μm x 7.6 μm).

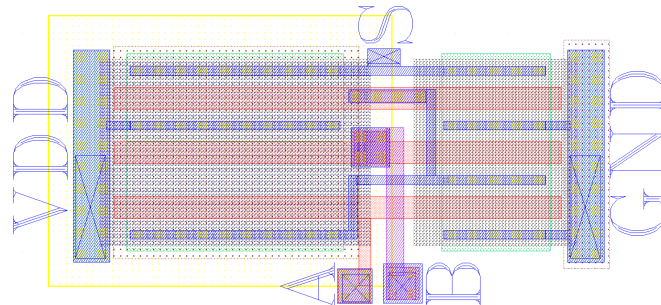
Source: Author.

Figure 4.35: ANX2 ($4.9 \mu\text{m} \times 10.4 \mu\text{m}$).



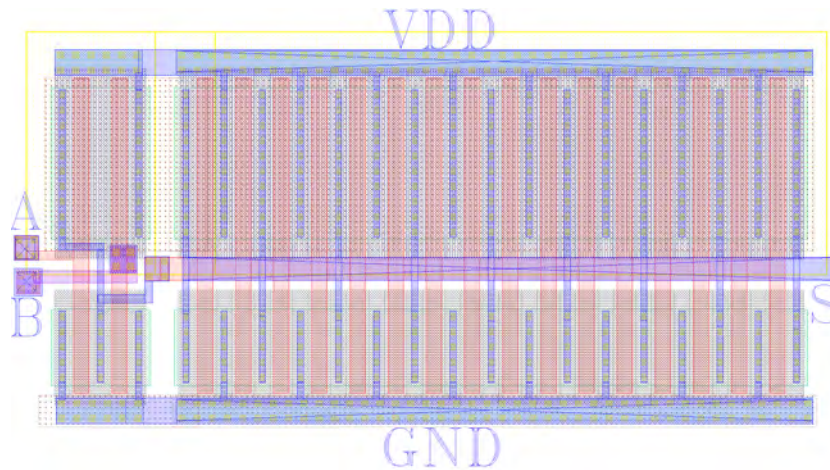
Source: Author.

Figure 4.36: ORX4 ($4.9 \mu\text{m} \times 10.4 \mu\text{m}$).



Source: Author.

Figure 4.37: ORX64 ($20.9 \mu\text{m} \times 10.4 \mu\text{m}$).



Source: Author.

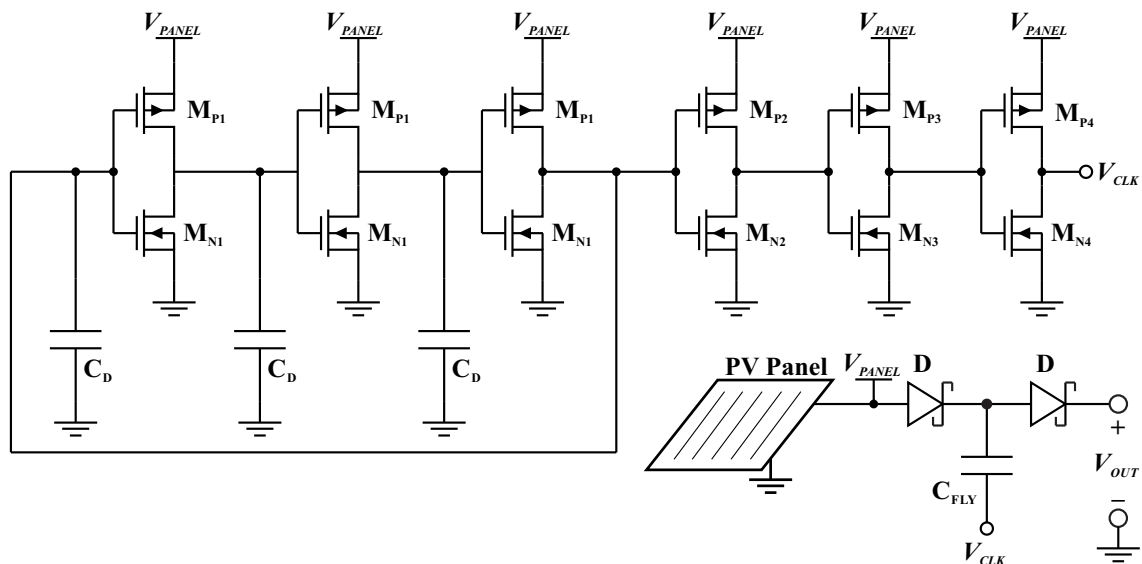
4.5 Start-up

For the main converter work properly, a minimum output voltage is necessary. When there is a precharged battery in the output, the circuits start normally. But a non-precharged capacitor can be used in the output, in this case, a start-up circuit is necessary.

Two start-up strategies were employed in this work, one using the current path that the PMOS transistors of the primary converter create when the output voltage is zero, Fig. 4.40, and one strategy using a passive Dickinson doubler in parallel with the primary converter, Fig. 4.38.

Like the main DC-DC converter, the Dickinson start-up circuit is a 1-to-2 converter using a doubler topology based on integrated Schottky diodes. The energy provided by the PV panel starts the oscillation of a Ring Oscillator (OSC). A driver takes the signals generated and makes one of the terminals of the flying capacitors to float and the diode blocks/allows the flow of energy when the signals are high or low, causing the output voltage to be the double of the input, but with low efficiency and low power.

Figure 4.38: Start-up topology.



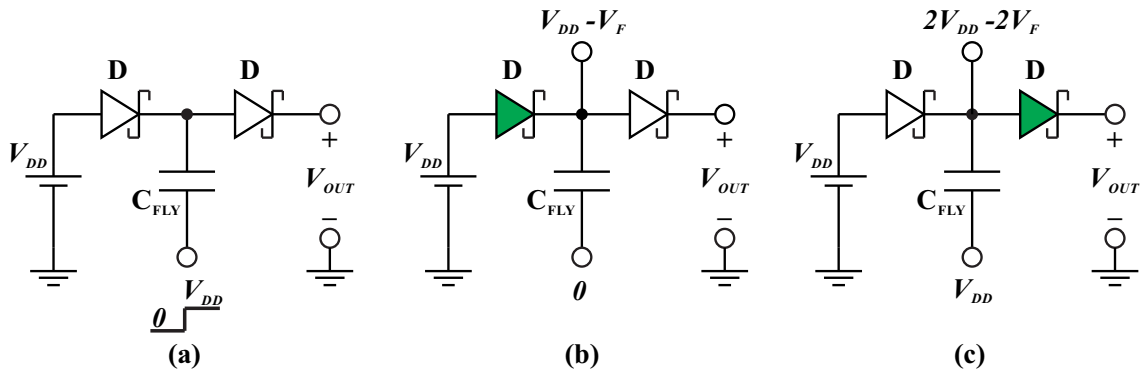
Source: Author.

The circuit works in two phases, one charging phase and one of discharging. Fig. 4.39 shows it. In each phase a forward bias drop, V_F , of the Schottky diodes decreases the output voltage.

The output voltage of the PV panel is practically 2 V of open-circuit, what is a voltage large for the standard transistors and low for the transistor of 3.3, so the transistors of 2.5 V were used to design the Ring-Oscillator and the buffers.

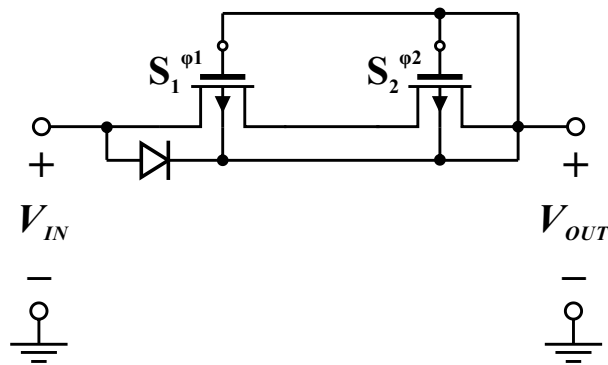
When the output is zero, a voltage path is created by the PMOS transistor of the main converter, Fig. 4.40.

Figure 4.39: Start-up operation phases.



Source: Author.

Figure 4.40: Start-up created by the PMOS transistors of the main converter.



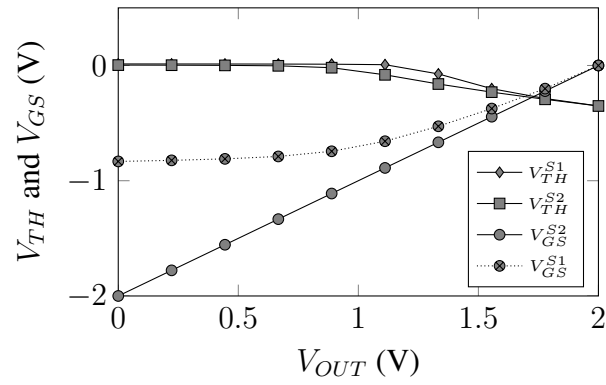
Source: Author.

The structure charges up the output capacitor until a particular value. Once PMOS n-well voltage is tied to the output, such as the gate voltage, the circuit can increase the output voltage until threshold voltage suppresses the gate to source voltage. Figure 4.41 shows an equilibrium point for a 2 V open circuit voltage of the solar panel.

The output voltage can achieve a value of 1.6 V in this start-up strategy, enough to circuits start to work.

The size of the transistors and the layout are presented, respectively, in Tab. 4.9 and Fig. 4.42. Schottky diodes and dualmim capacitors were used to create D and C.

Figure 4.41: Start-up using the PMOS current path.

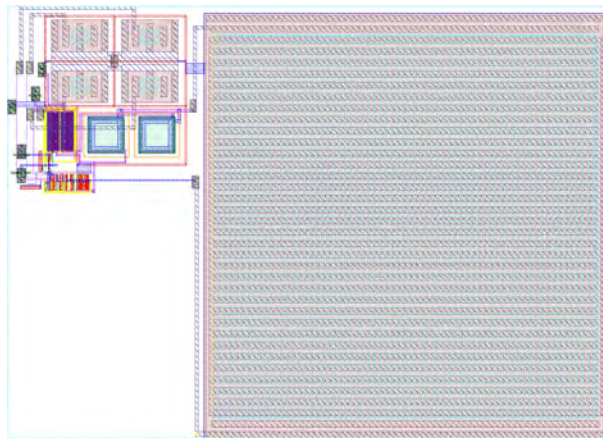


Source: Author.

Table 4.9: Start-up sizing.

	L (μm)	W (μm)	C (fF)
M_{P1}	1.0	4.0	-
M_{N1}	1.0	4.0	-
M_{N2}	0.24	2.0	-
M_{N3}	0.24	4.0	-
M_{N4}	0.24	16.0	-
M_{P2}	0.24	4.0	-
M_{P3}	0.24	8.0	-
M_{P4}	0.24	32.0	-
D	15.0	15.0	-
C	8.5	8.5	680

Source: Author.

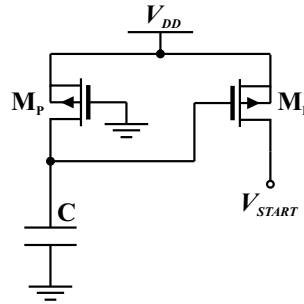
Figure 4.42: Start-up layout (225.0 μm x 320.0 μm).

Source: Author.

4.6 Starting the Blocks

The oscillators and the bias circuits are self-biased, so it is necessary a circuit to give a kicking start. Fig. 4.43 shows the starting topology used.

Figure 4.43: Start-up for the self-biased blocks.

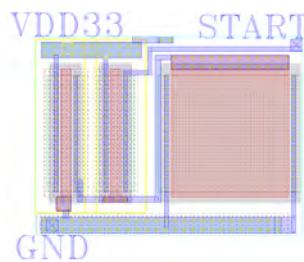


Source: Author.

The node V_{START} creates a ramp-up voltage that can be applied to a node in the circuit intended to be started, so letting it out of the zero stable state. The start time depends on the size of the transistors M_P and the capacitor C , that was implemented using a MOS capacitor.

The layout of the starting circuit is presented in Fig. 4.44 and the size of the devices in Tab. 4.10.

Figure 4.44: Layout of the starting circuit ($7.0 \mu\text{m} \times 10.0 \mu\text{m}$).



Source: Author.

Table 4.10: Starting block.

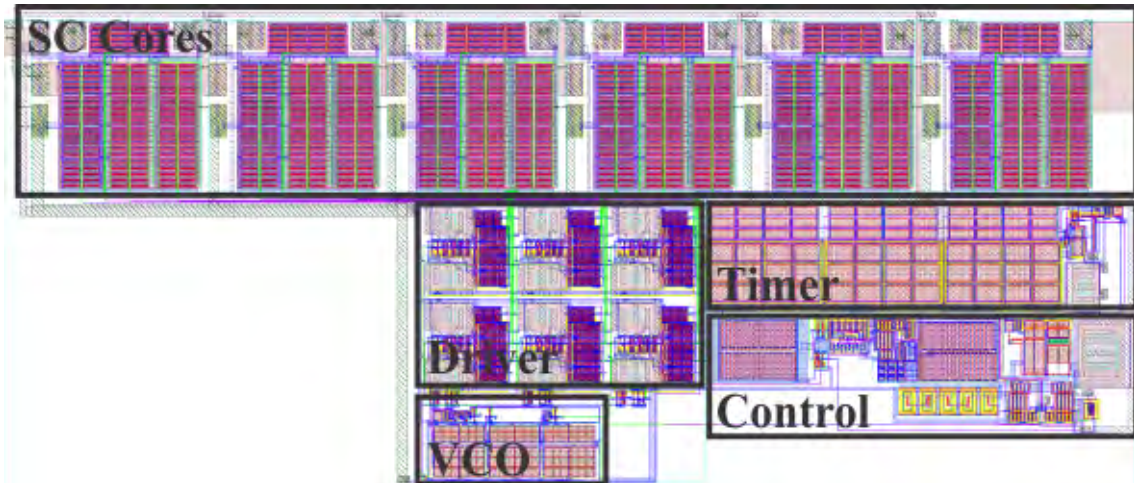
	L (μm)	W (μm)
M_P	0.4	5.0
M_C	5.0	5.0

Source: Author.

4.7 Complete Layout

Finally, the complete layout of the SC DC - DC converter is presented in Fig. 4.45, where all the sub blocks are highlighted.

Figure 4.45: Complete layout of the SC DC - DC Converter ($300 \mu\text{m} \times 700 \mu\text{m}$).



Source: Author.

5 RESULTS

In this chapter, the layout extracted simulation results of the main blocks and the complete DC - DC converter will be presented. Also, the design of the setup test for measurements of the fabricated circuits and the measurement results will be shown.

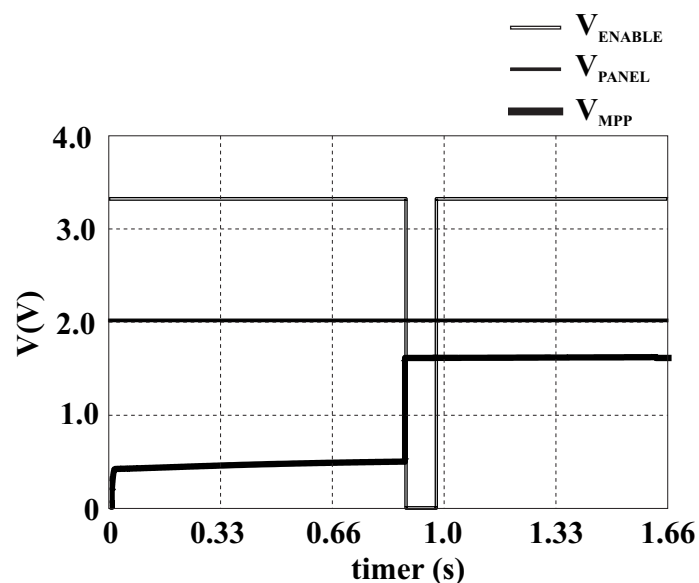
5.1 Simulation Results

The simulation results of the main blocks will be presented in this section.

5.1.1 MPP Reference Generator

Fig. 5.1 presents the layout extracted simulation results of the MPP Reference Generator. The open-circuit voltage of the PV panel stays around 2 V. When the timer generates the disable pulse, the V_{PANEL} is sampled and multiplied by $4/5$, what creates the V_{MPP} . In the simulation, V_{MPP} stays around 1.6 V.

Figure 5.1: MPP Reference Generator layout extracted simulation results.

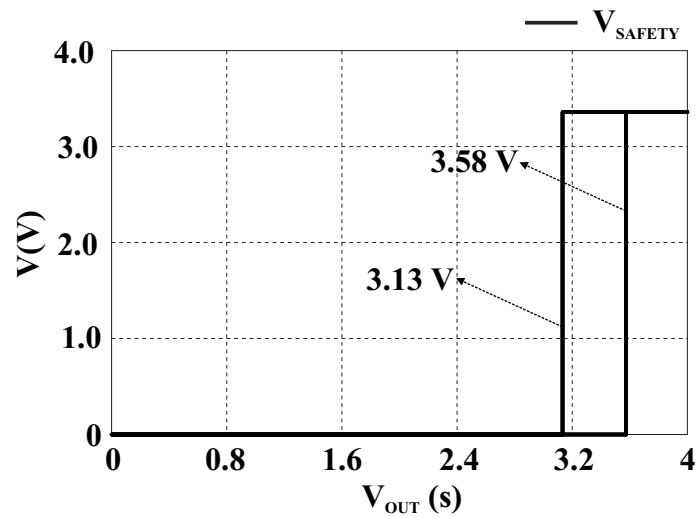


Source: Author.

5.1.2 Protection

The simulation results of this circuit is presented in Fig. 5.2. The comparator, the resistances, and the band-gap reference were designed to create a safety signal when the output voltage suppress 3.6 V. This signal is released in a lower voltage, using the hysteresis of the comparator. Simulations of layout extracted shown that the signal is set when the output voltage suppress 3.58 V and is released when it gets lower than 3.13 V.

Figure 5.2: Protection layout extracted simulation results.

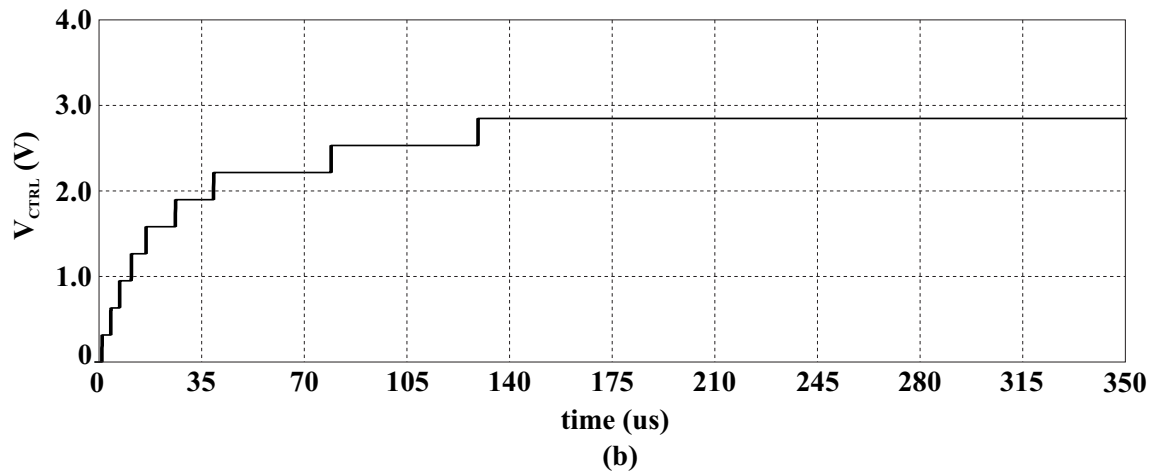
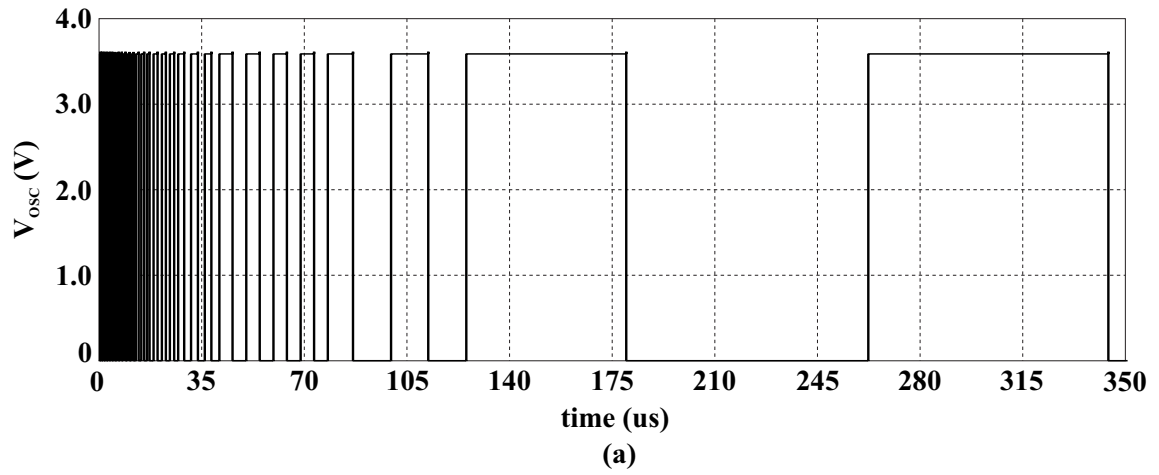


Source: Author.

5.1.3 Driver

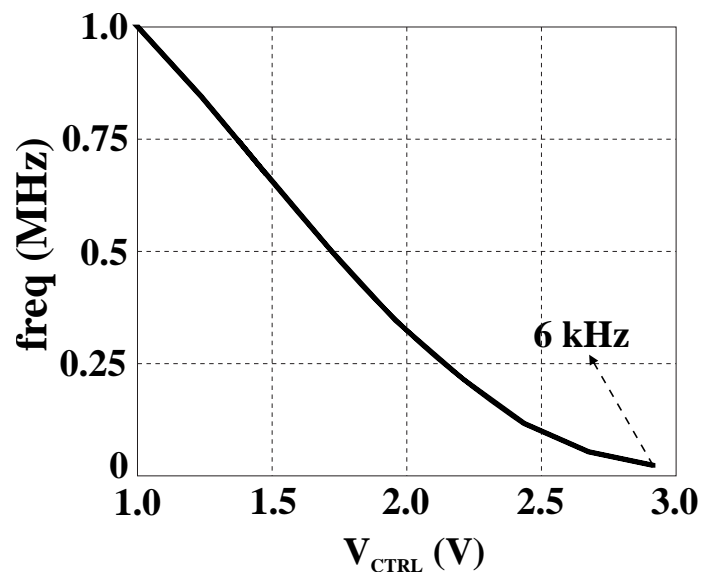
The simulation results of the Driver circuit are presented in Fig. 5.3, Fig. 5.4, Fig. 5.5, Fig. 5.6 and Fig. 5.7. Fig. 5.3 presents one of the pulses delivered to the power switches in function of the voltage error created by the error amplifier comparing the V_{MPP} and V_{PANEL} . Fig. 5.4 shows that the VCO covers a range that goes from 6 kHz to 1 MHz, what comprises the optimum frequencies presented in the design chapter. Fig. 5.4 shows this simulation result.

The Drive signals are shifted to create a time-interleaved strategy. Fig. 5.5 shows it. The signal generated by the VCO is delivered to the drivers and 24 signals (4 signals per phase) are generated to turn-on and turn-off the switches. Fig. 5.6 presents the 4 signals of one phase and Fig. 5.7 the dead-zone created by the non-overlapping circuit, (a) in the rise (b) in the fall.

Figure 5.3: Driver signal with respect to the error signal in time domain (a) Pulses (b) V_{CTRL} .

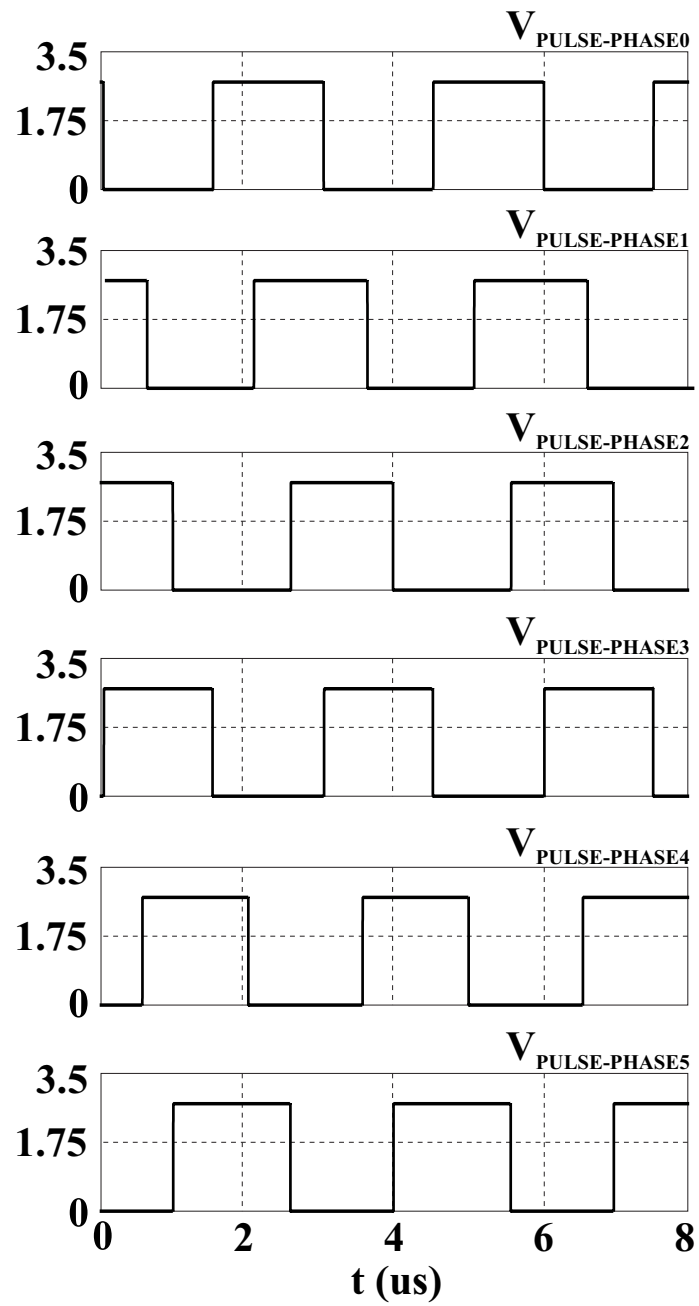
Source: Author.

Figure 5.4: Driver signal frequency with respect to the error voltage.



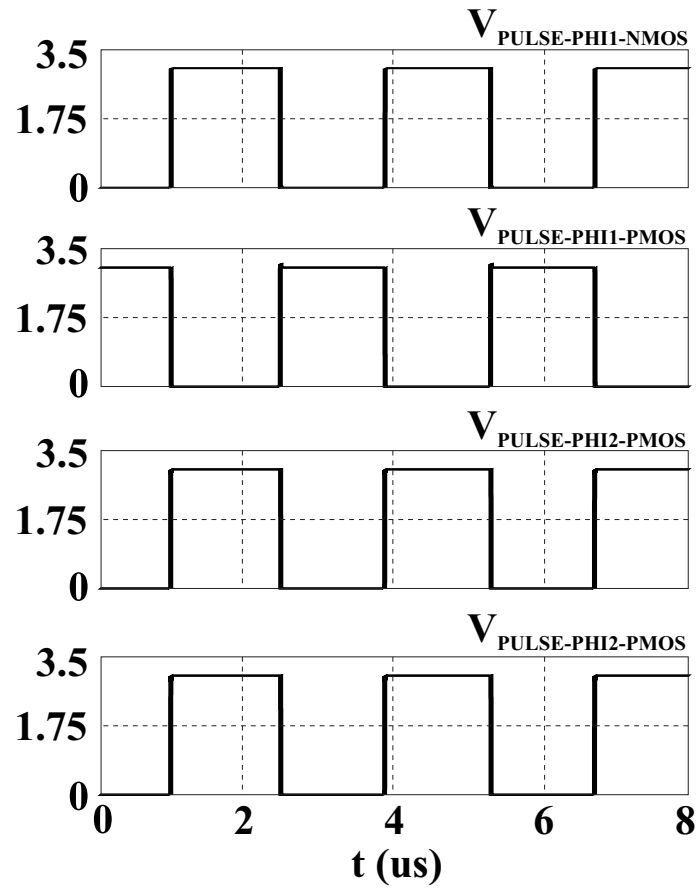
Source: Author.

Figure 5.5: Time-interleaved signals.



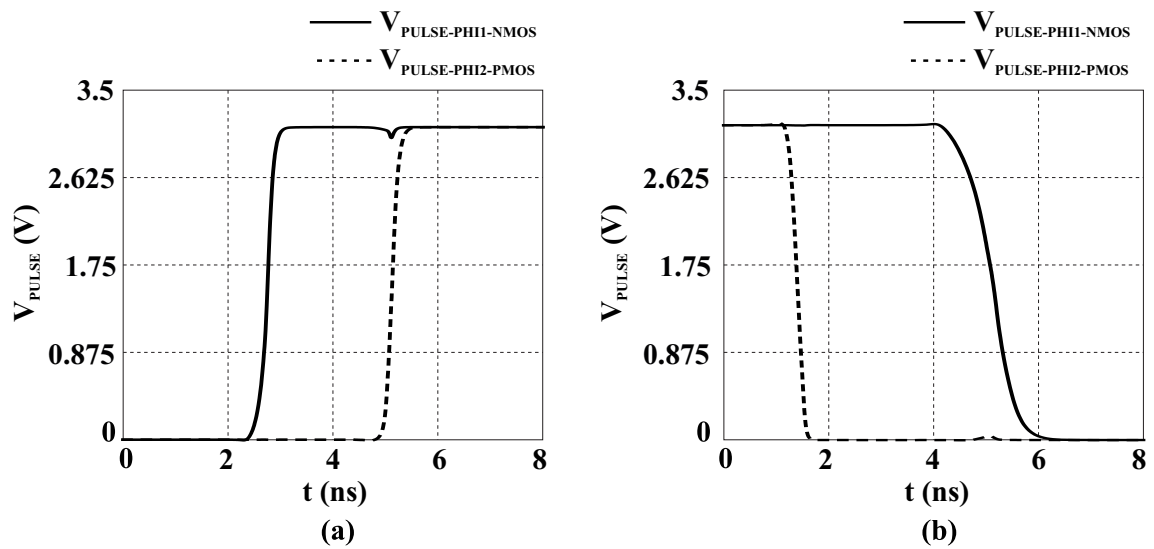
Source: Author.

Figure 5.6: The four drive signals of one phase.



Source: Author.

Figure 5.7: Dead-zone of the drive signals.

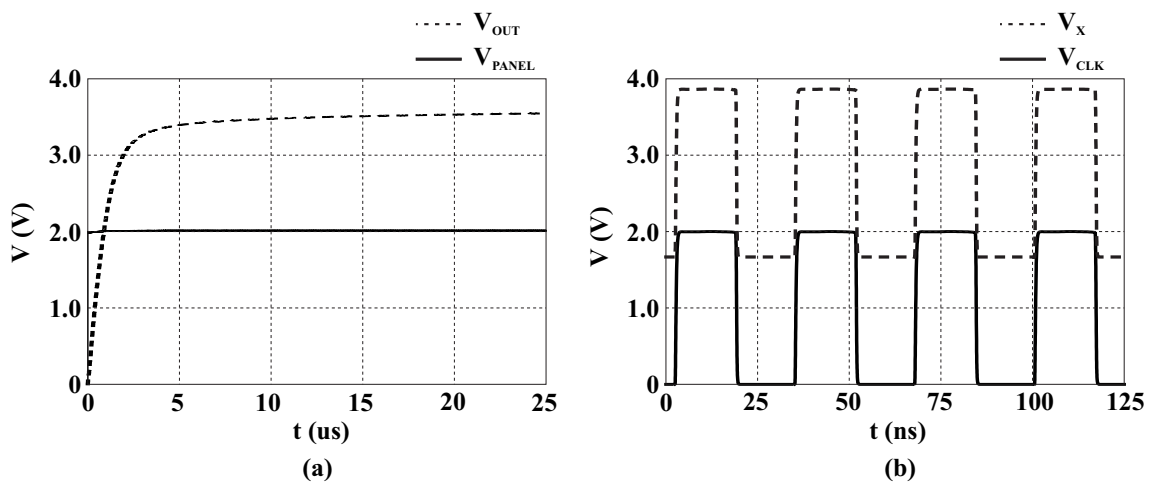


Source: Author.

5.1.4 Start-up

The simulation results of the circuit of the start-up circuit are presented in Fig. 5.8. Fig. 5.8 (a) shows the input voltage of the PV panel at 2 V. The doubler circuit delivers an output voltage of 3.5 V. It would be, ideally, 4 V, but the voltage drop across the Schottky diodes reduces it. Also, Fig. 5.8 (b) shows the generated clock and the intermediate node of the doubler.

Figure 5.8: Simulation results of the start-up circuit.



Source: Author.

5.1.5 Complete SC DC - DC Converter

Until now, all the simulation results of the most important sub-blocks were presented. In this section, the simulation results of the complete proposed DC - DC harvester will be presented.

The converter was simulated in three different light incidence situations in between the two limits already presented in this work, 4 mW and 60 mW.

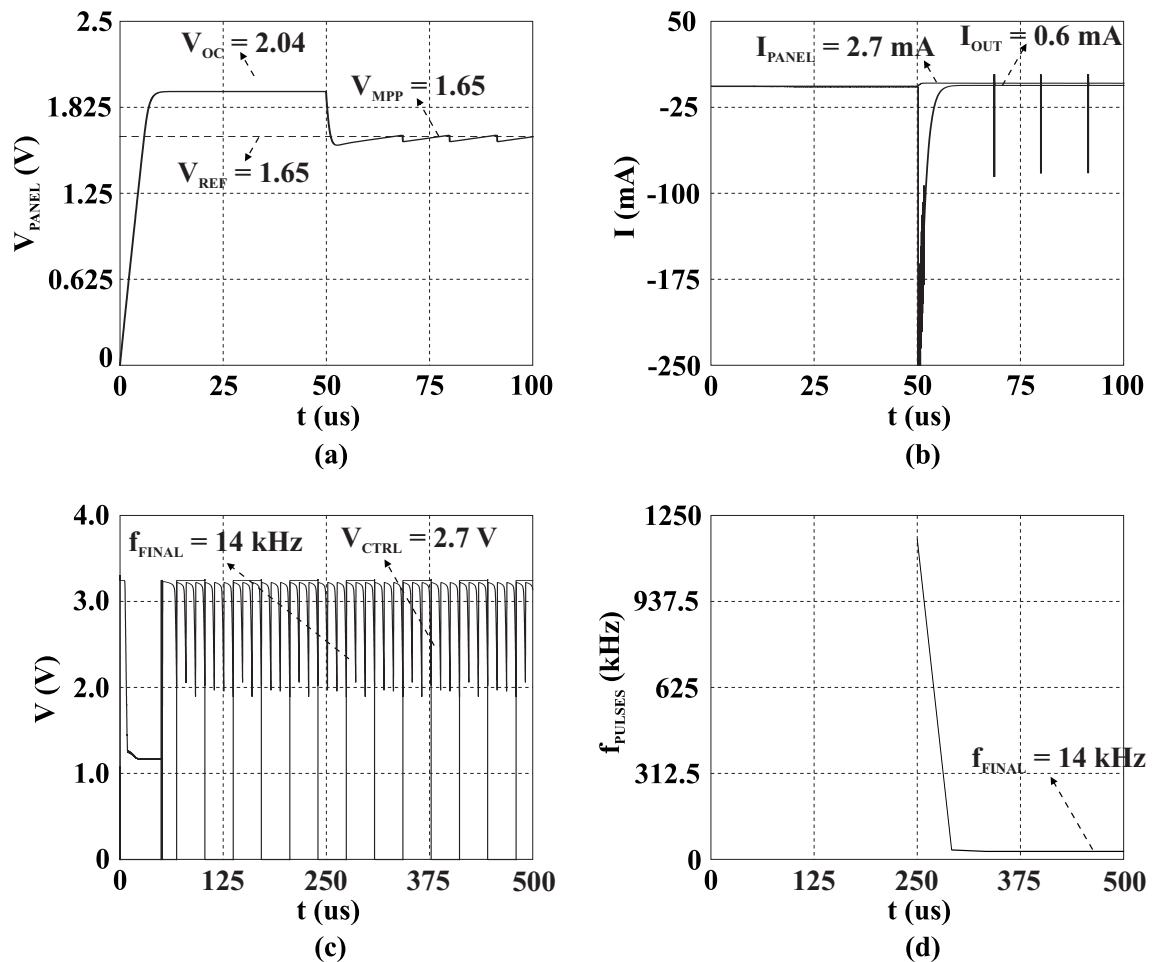
For each situation, four graphs are presented. One for the V_{MPP} track (a), one for the input and output currents (b), one for the control signal and the pulses generated by the VCO and finally, the frequency of the pulses and the final frequency for steady-state operation.

The pulses are disabled until the time 50 μs . In this period, the V_{MPP} reference is sampled and after that, the pulses are released in order to the converter track it and drain power of the panel and deliver to the battery.

In all the simulations, the output voltage was set to stay at 3.2 V.

In Fig. 5.9, the incidence of light is simulated as it was almost at the end of the afternoon, near of the lowest limit of 4 mW. In this situation, MPPT was satisfactory, since the input voltage stayed around the V_{MPP} reference. The i_{MPP} stayed around 2.7 mA and the output current at 600 μ A. The current glitches are due to the switching characteristic of the DC - DC converter. The control voltage stayed in an average value of 2.7 V and the switching frequency at steady-state was 14 kHz.

Figure 5.9: Simulation Results, $I_{SC} = 3$ mA. (a) V_{PANEL} response, (b) I_{PANEL} and I_{OUT} responses, (c) V_{CTRL} and V_{PULSES} responses and (d) I_{PANEL} and switching frequency response until steady-state



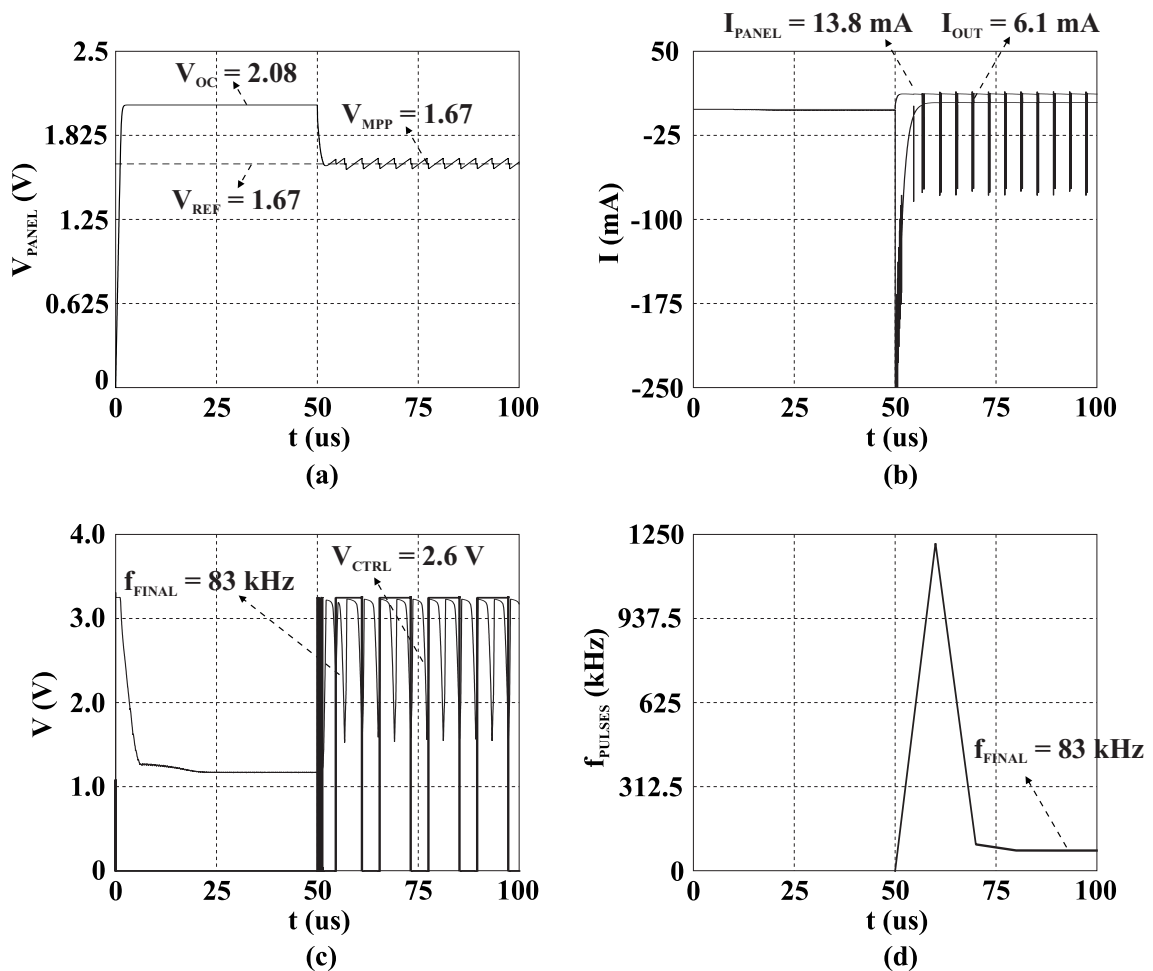
Source: Author.

In Fig. 5.10, the incidence of light is simulated as it was almost at the end of the afternoon also, near of the lowest limit of 4 mW. In this situation, MPPT was satisfactory, since the input voltage stayed around the V_{MPP} reference. The i_{MPP} stayed around 13.8 mA and the output current at 6.1 mA. The current glitches are due to the switching characteristic of the DC - DC

converter. The control voltage stayed in an average value of 2.6 V and the switching frequency at steady-state was 83 kHz.

In Fig. 5.11, the incidence of light is simulated as it was almost at the middle of the afternoon. In this situation, MPPT was satisfactory, since the input voltage stayed around the V_{MPP} reference. The i_{MPP} stayed around 22.0 mA and the output current at 10.5 mA. The current glitches are due to the switching characteristic of the DC - DC converter. The control voltage stayed in an average value of 2.4 V and the switching frequency at steady-state was 150 kHz.

Figure 5.10: Simulation Results, $I_{SC} = 15$ mA. (a) V_{PANEL} response, (b) I_{PANEL} and I_{OUT} responses, (c) V_{CTRL} and V_{PULSES} responses and (d) I_{PANEL} and switching frequency response until steady-state



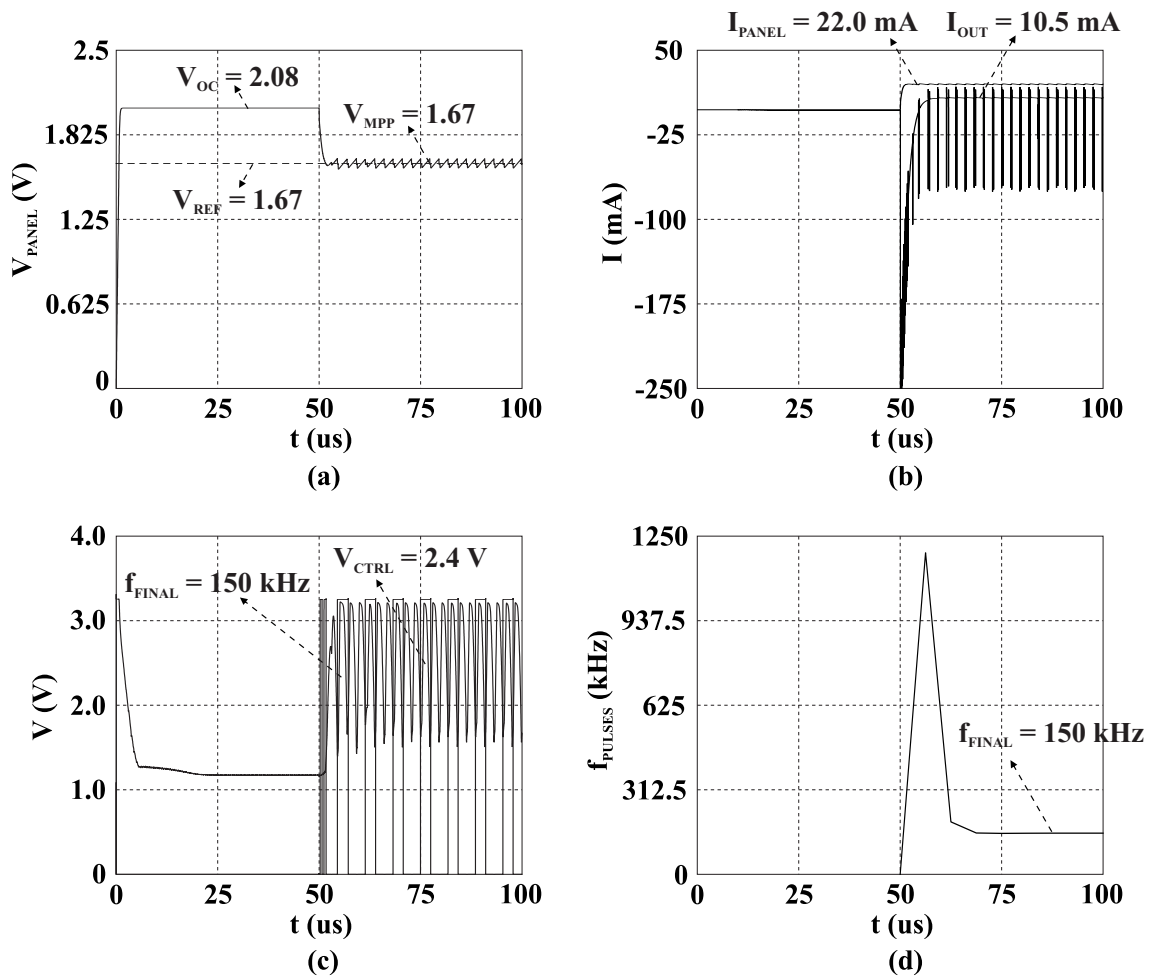
Source: Author.

In Fig. 5.12, the incidence of light is simulated as it was almost at the middle of the afternoon. In this situation, MPPT was satisfactory, since the input voltage stayed around the V_{MPP} reference. The i_{MPP} stayed around 30.0 mA and the output current at 14 mA. The current glitches are due to the switching characteristic of the DC - DC converter. The control voltage

stayed in an average value of 2.0 V and the average switching frequency at steady-state was 350 kHz.

In Fig. 5.14, the incidence of light is simulated as it was almost at the middle of the afternoon. In this situation, MPPT was satisfactory, since the input voltage stayed around the V_{MPP} reference. The i_{MPP} stayed around 35.0 mA and the output current at 16.0 mA. The current glitches are due to the switching characteristic of the DC - DC converter. The control voltage stayed in an average value of 1.5 V and the switching frequency at steady-state was 750 kHz.

Figure 5.11: Simulation Results, $I_{SC} = 25$ mA. (a) V_{PANEL} response, (b) I_{PANEL} and I_{OUT} responses, (c) V_{CTRL} and V_{PULSES} responses and (d) I_{PANEL} and switching frequency response until steady-state

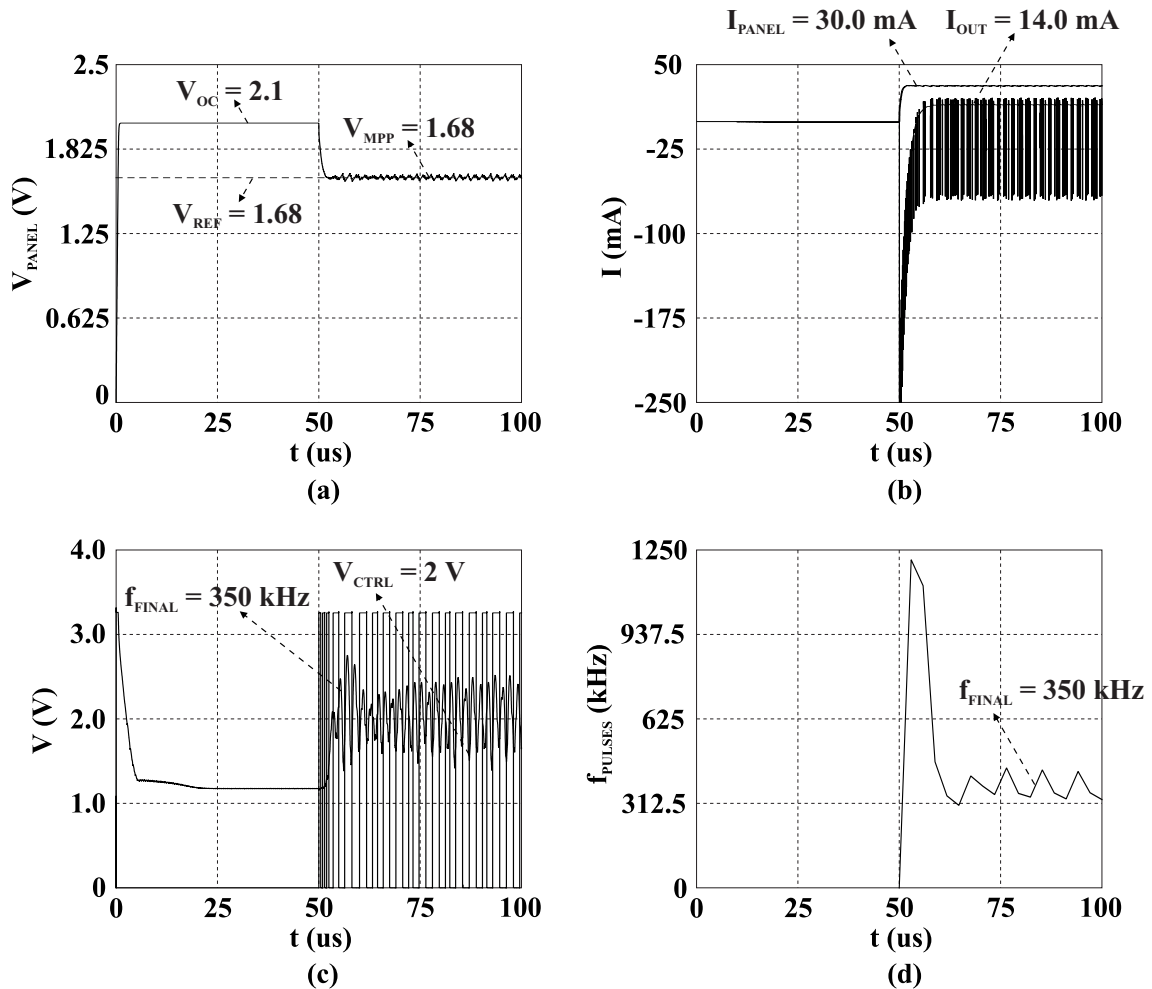


Source: Author.

In a typical application, the incidence of light changes constantly, with the angle that the sun makes with earth and the presence of clouds. So, from times to times the a change in the MPP will occur. Fig. 5.15 presents a step of incidence of light performed by a change in the I_{SC} from 15.0 mA to 45.0 mA.

The past simulations presented a result considering that the voltage across the output energy storage element stayed fixed at 3.2 V. But, this value changes with charging. Fig. 5.16 presents the variation of the output voltage using a small capacitor at the output to simulate it. The process of charging is disabled by the two possible mechanisms, the timer that samples the V_{MPP} and the protection circuit, that generates a safety signal when the output voltage achieves 3.58 V.

Figure 5.12: Simulation Results, $I_{SC} = 35$ mA. (a) V_{PANEL} response, (b) I_{PANEL} and I_{OUT} responses, (c) V_{CTRL} and V_{PULSES} responses and (d) I_{PANEL} and switching frequency response until steady-state



Source: Author.

Finally, Fig. 5.17 presents the conversion efficiency for different input power. It is possible to notice that for the lowest value of power, the efficiency of the converter goes down to almost 50 %, but for the highest input powers (> 30 mW), the efficiency goes up to 90 %.

5.2 Circuit Fabrication

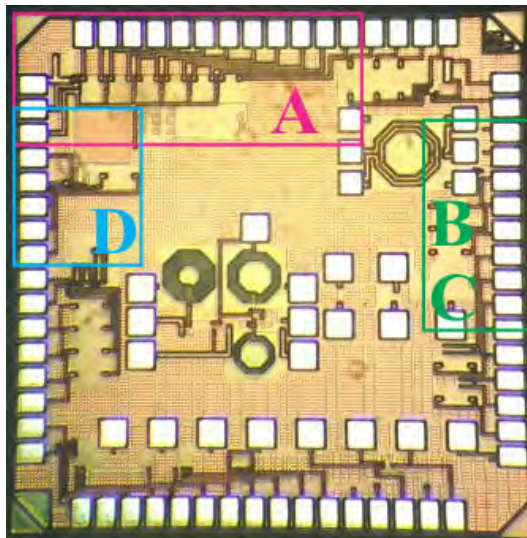
The circuits were fabricated through the MOSIS Educational Program (MEP), that allows Educational Institutions to participate of one tapeout a year for free. They allow the institutions to send a GDS of a maximum size of 2 mm x 2 mm and return 40 bare dies and the possibility of packing a maximum of 5 samples for free.

Due to financial problems, the GME - AMS group divides the silicon area among the designers of the team. A total of 8 projects were sent in the run that this work was fabricated.

MOSIS sent 35 bare dies and 5 packed samples in DIP40 in this run.

Fig. 5.13 presented the photograph of the fabricated chip.

Figure 5.13: Fabricated chip (2mm x 2mm).



Source: Author.

There are several blocks from different designers. The circuits A, B, C and D were designed by the author of this work. Circuit A is the complete converter described in this work, B and C are internal blocks replicated separately for tests, they are, respectively, the voltage reference and the timer. Finally, D is the start-up circuit.

Circuit A was packed in the DIP 40 and measured using a test strategy that will be described later in this section. Circuits B and C were tested using the probe station, oscilloscope and a parameter analyzers.

5.3 Experimental Results

The experimental results of the main blocks will be presented in this section.

5.3.1 Test Setup

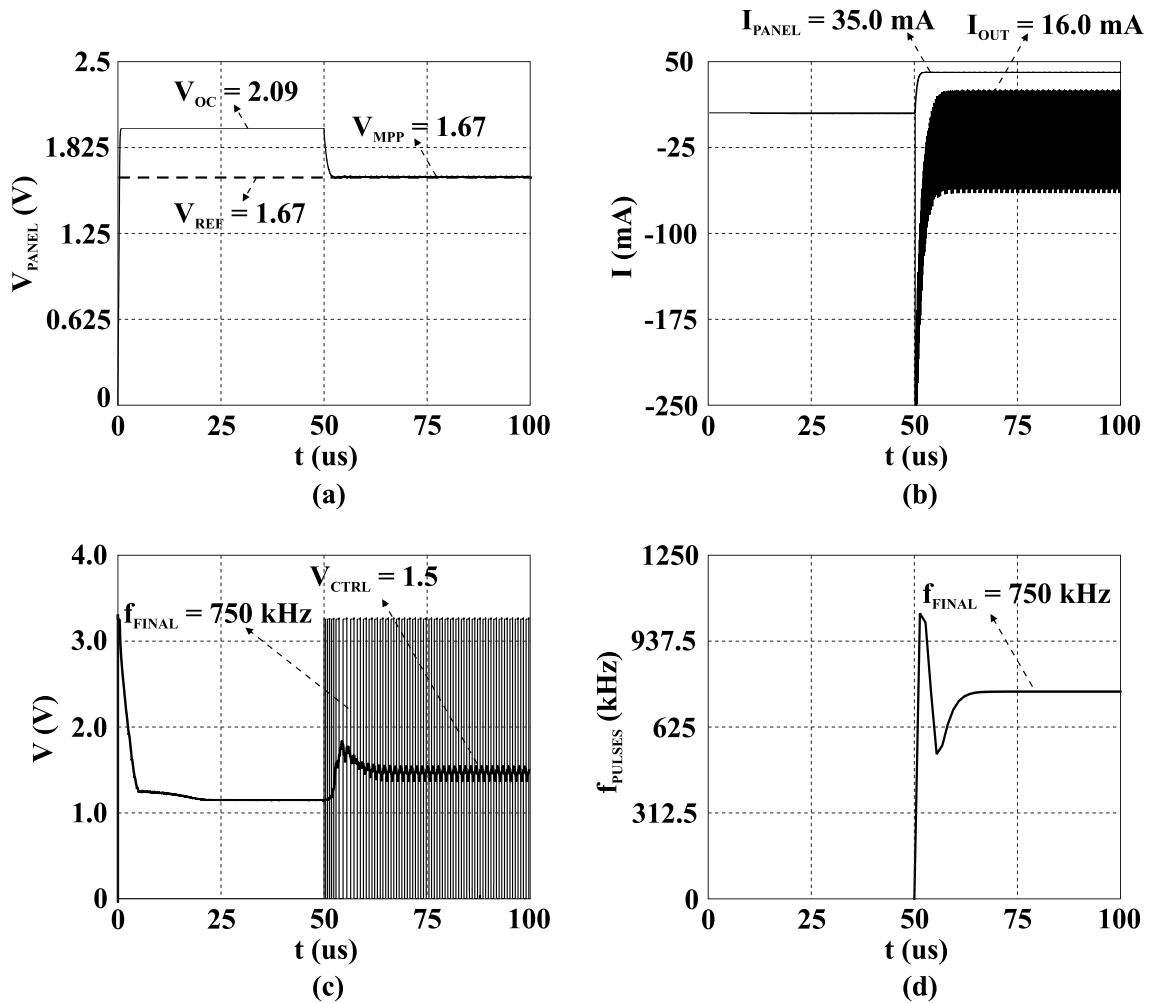
The tests were performed in two environments, one inside the laboratory, where some blocks were tested separately and in open space to use the sunlight to test different illuminations in the PV panel.

The bare dies were tested in the Electrical Characterization Laboratory (LCE) of UFRGS, where it is available a microscope, manipulators, needles, voltage sources, oscilloscopes and a parameter analyzer.

The complete converter was packed in DIP40 and a PCB was designed and fabricated for the tests. To sunlight reaches the PV panel, it is necessary to open space, far from the laboratory and the buildings, so it would be a problem to take all the instruments to performs the measurements outside.

To overcome this problem, an Automatic Test Platform (ATP) was designed and built in a way that the only voltage source needed is the USB of a Notebook with a battery charged. It was done using an Arduino board to acquire the signals and a LabVIEW interface the show in real time the results of current, voltage and illuminance.

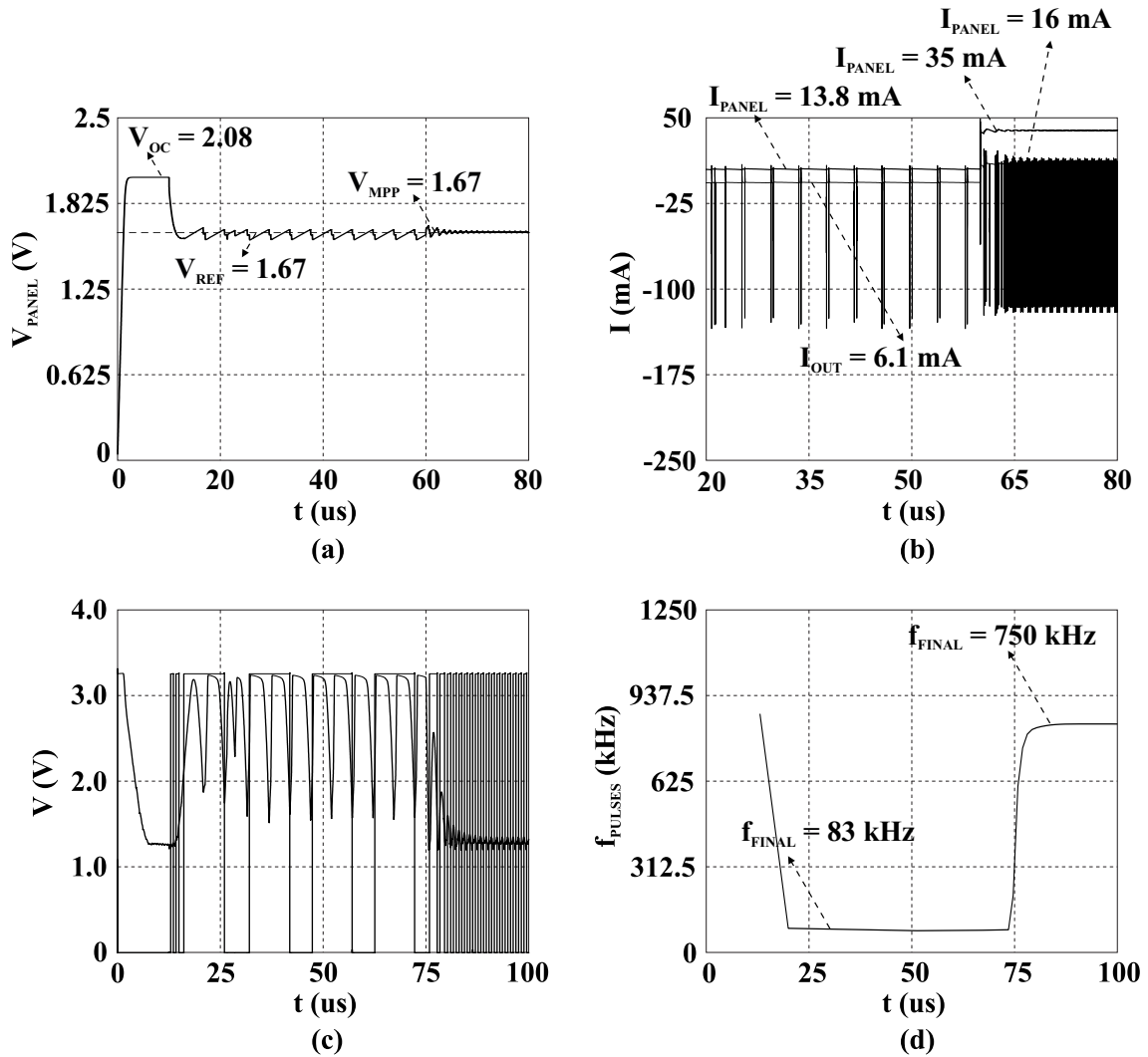
Figure 5.14: Simulation Results, $I_{SC} = 45 \text{ mA}$. (a) V_{PANEL} response, (b) I_{PANEL} and I_{OUT} responses, (c) V_{CTRL} and V_{PULSES} responses and (d) I_{PANEL} and switching frequency response until steady-state



Source: Author.

5.3.2 Automatic Test Platform

The ATP consists of 5 main parts. The test board with the PV panel and the battery, the sense amplifiers that acquire the input and output currents and amplify the signals, an illuminance meter 510 01 of Yokogawa, that receive the incidence of light, an Arduino UNO board and a notebook with an interface designed in LabVIEW. Fig. 5.18 shows the complete scheme of the ATP.

Figure 5.15: Simulation Results, irradiation step, from $I_{SC} = 45 \text{ mA}$ to $I_{SC} = 15 \text{ mA}$.

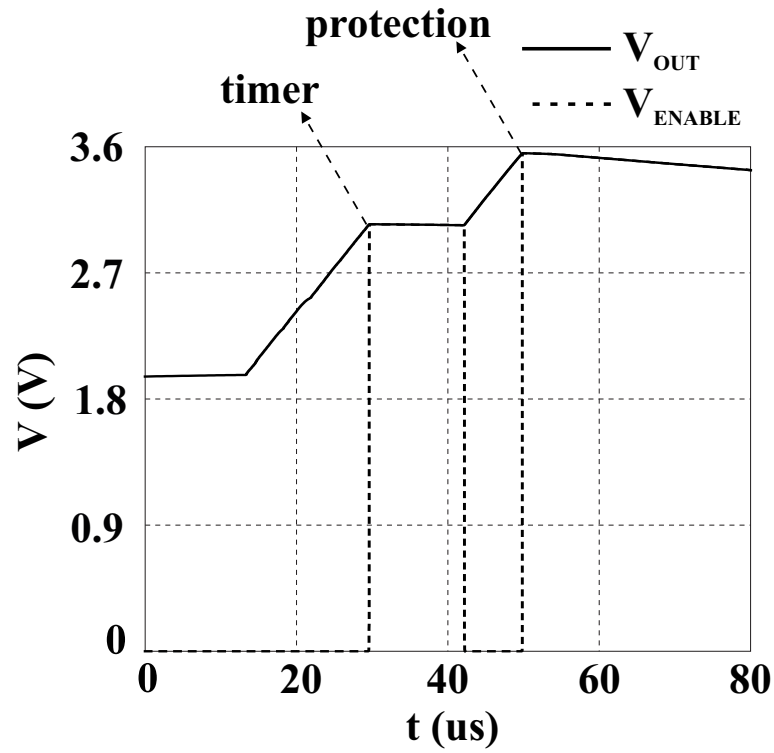
Source: Author.

5.3.2.1 Test Board, PV panel and Battery

The PCB possesses two circuits, one in the SC DC - DC converter of this work and the other one is a circuit designed in the context of a research project developed by a partnership UFRGS & HP Company. The part of interest of this contains the DIP40 packaging of the tapeout sent by UFRGS in 2016, three connectors and eight capacitors, six from the six phases and other two for input and output filtering. Fig. 5.19 presents the designed PCB and Tab. 5.1 shows the list of components used to mount the board.

A structure that allows a change in the PV panel angle and attaches the board and the battery is presented in Fig. 5.20.

Figure 5.16: Simulation Results, signal of enable, due to timer and high output voltage protection.



Source: Author.

Figure 5.17: Efficiency vs. Input Power.

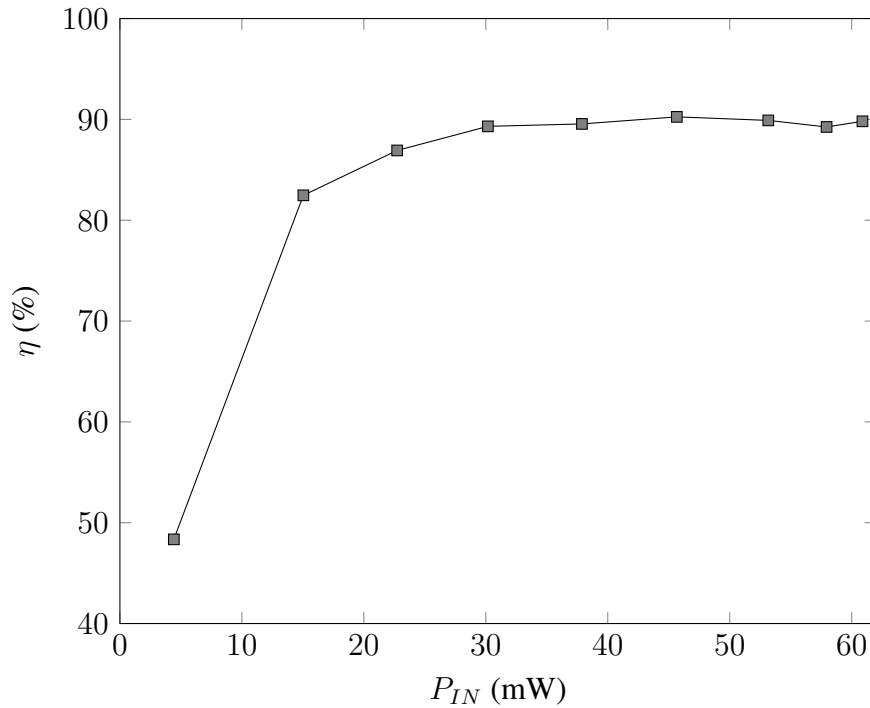
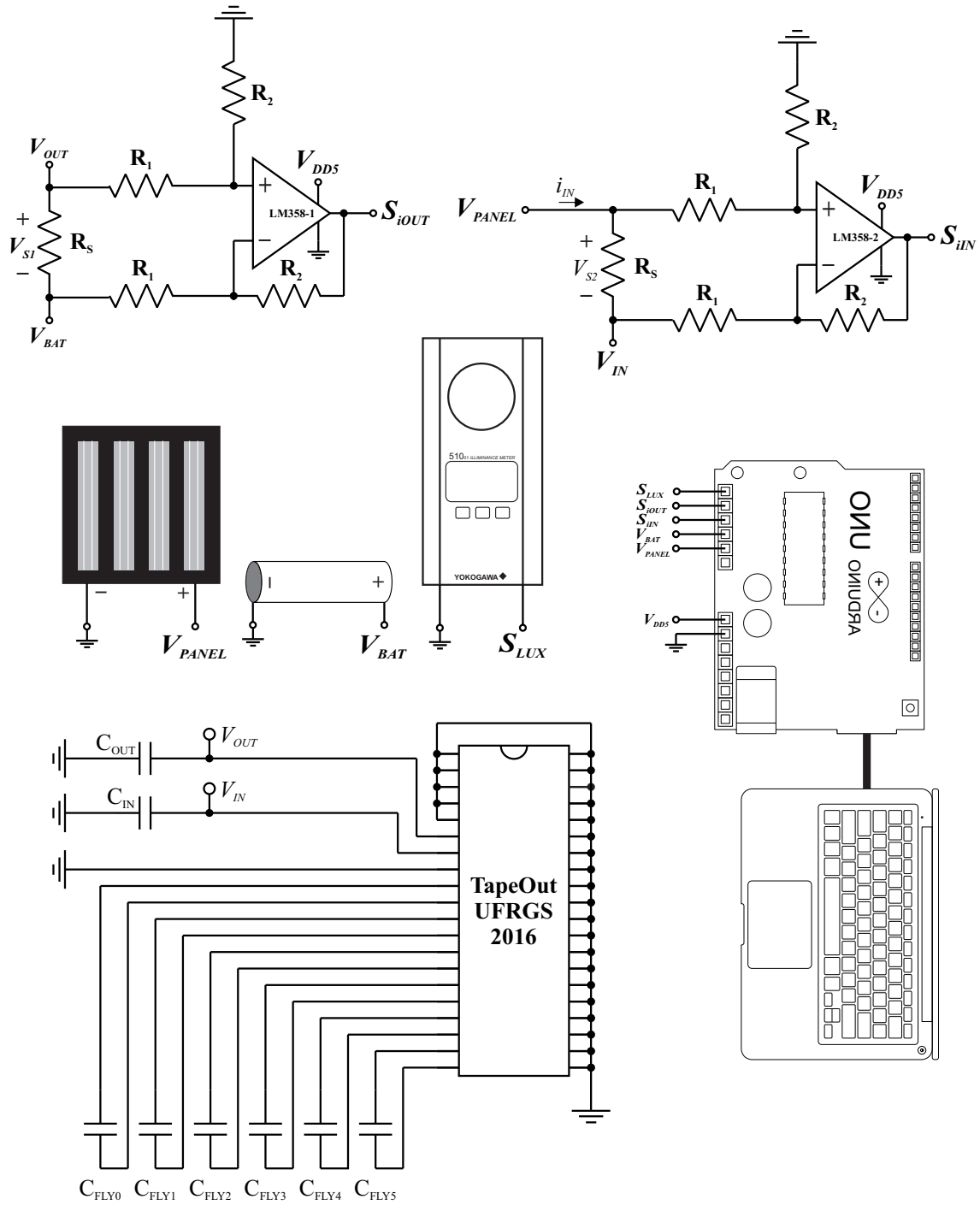


Figure 5.18: ATP scheme.

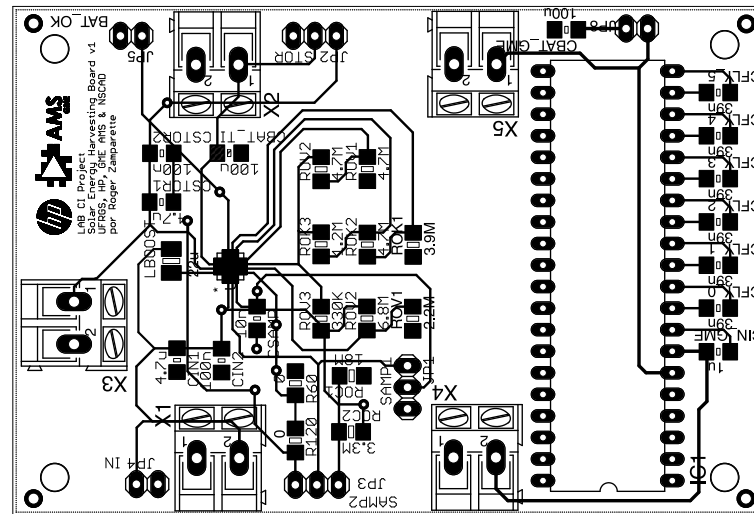


Source: Author.

5.3.2.2 Current Sense Amplifiers

A PCB was design and mounted to acquire the current signals and centralize the voltage and illuminance signals. Fig. 5.22 presents the board.

Figure 5.19: PCB for tests.



Source: Author.

Table 5.1: List of Components.

	$C (\mu\text{F})$
CFLY0	0.1
CFLY1	0.1
CFLY2	0.1
CFLY3	0.1
CFLY4	0.1
CFLY5	0.1
CINGME	1.0
CBATGME	100.0

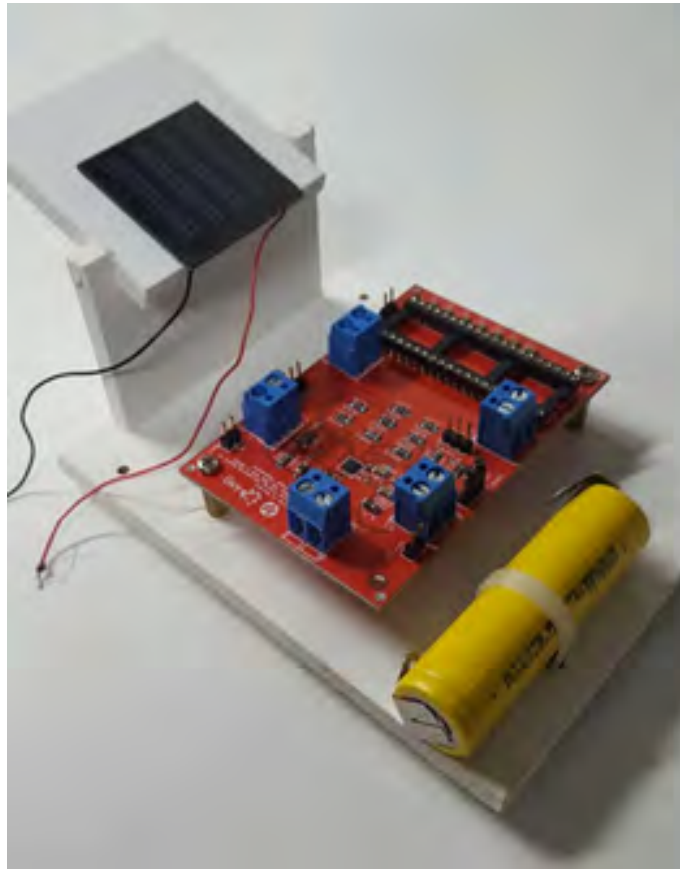
Source: Author.

It was used a LM358 dual operational amplifier in a differential amplifier configuration to sense the input and output currents. Fig. 5.22 shows the schematic of the amplifier with the sizing of the components.

The components were sized to sense current in a range of 1 mA to 35 mA. These limits are the maximum and minimum that a PV panel in a day.

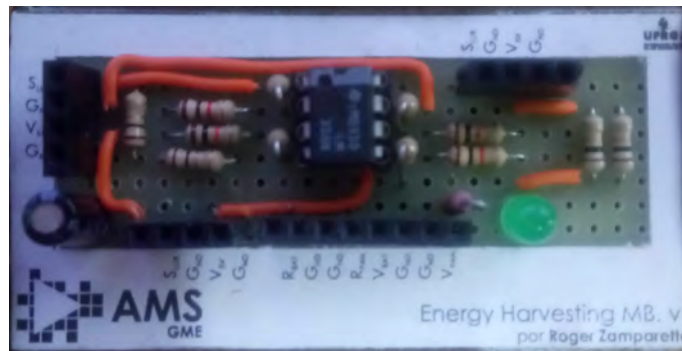
The measurement of the current must be calibrated, since the amplifier has offset and distorts the signal. The calibration was performed using the structure presented in Fig. 5.22, where various output voltages were measured for various values of R_L . The voltage curves for various R_L is presented in Fig. 5.23 and Fig. 5.24.

Figure 5.20: PV panel, board and battery structure.



Source: Author.

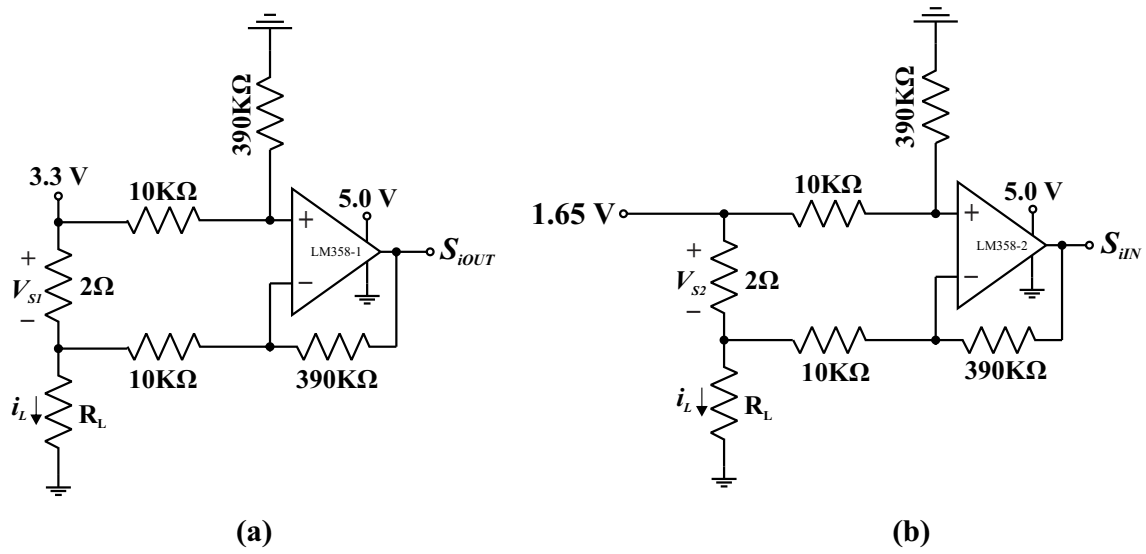
Figure 5.21: Current sense and signal terminal board.



Source: Author.

The characteristic curves are not perfect linear, so a 2ND order fitting was performed. The equations of fitting are presented in the graphs. These equations were used in the Arduino UNO to adjust the read signal to reduce measurement errors.

Figure 5.22: Schematic of the output (a) and input (b) sense amplifiers with the calibration scheme.

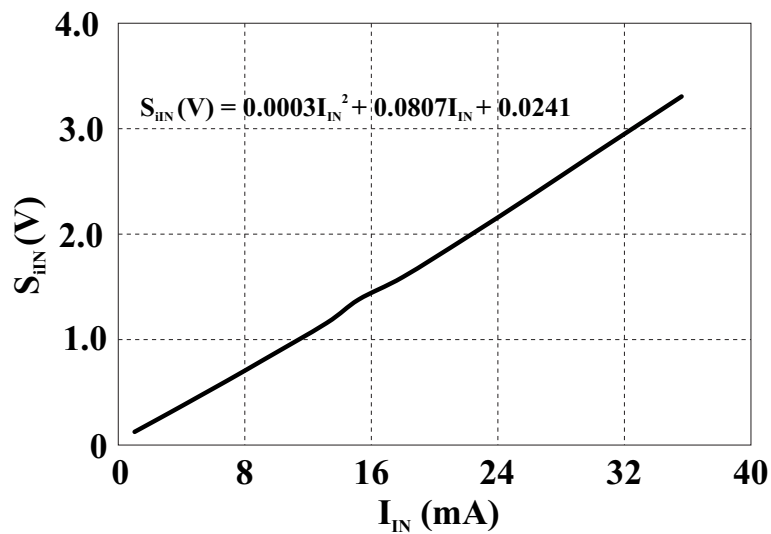


Source: Author.

5.3.2.3 Illuminance meter 510 01 of Yokogawa

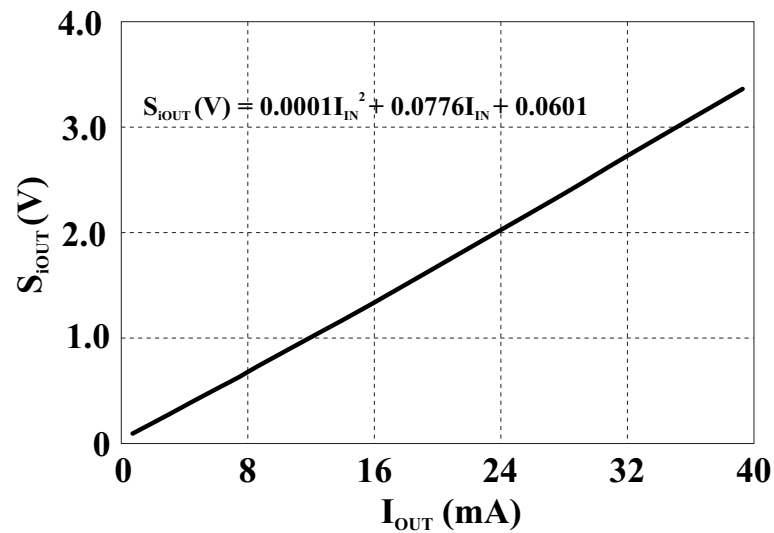
The illuminance measurement was performed by the illuminance meter 510 01 of Yokogawa, Fig. 5.26 shows the image of it. It can measure the illuminance and convert into a voltage level available in a P2 connector. This voltage signal is acquired by the Arduino UNO.

Figure 5.23: Input current sense characteristic.



Source: Author.

Figure 5.24: Output current sense characteristic.



Source: Author.

Figure 5.25: Illuminance meter 510 01 of Yokogawa.



Source: yokogawa.com

5.3.2.4 Arduino UNO

Arduino UNO is very versatile and easy to program platform. It was used in this work to acquire the current, voltage and illuminance signals and send them through a serial RS232 protocol to the LabVIEW interface.

Besides the signal acquisition, the Arduino UNO is responsible to calibrate the input signals and deliver it to the LabVIEW in a certain protocol. The Arduino Code is in Appendix B.

Figure 5.26: Arduino UNO.



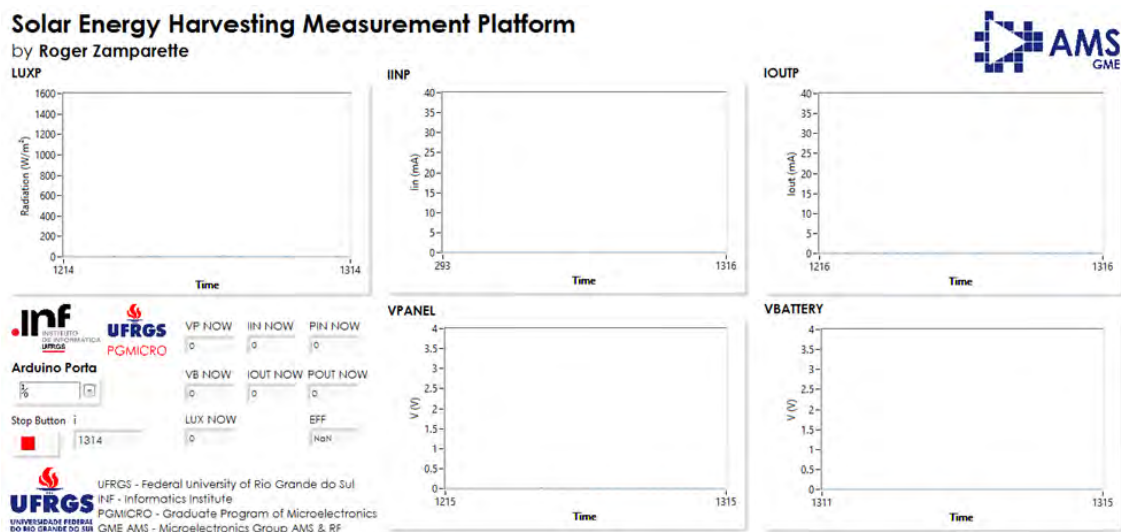
Source: arduino.org.

5.3.2.5 LabVIEW Interface

LabVIEW is very versatile software developed to offer an easy way to design interfaces to control and observing systems. In this work, a supervisory system was designed to present in real time the input and output voltage and currents, and the illuminance value. Fig. 5.27 presents the interface.

LabVIEW has two screens, one is the graph interface, and the other is the programming environment, that is done in a block diagram way. In Appendix C, the "code" is presented.

Figure 5.27: LabVIEW Interface.



Source: Author.

5.3.2.6 Complete ATP

Finally, the complete setup test is presented in Fig. 5.28.

Figure 5.28: Complete ATP.



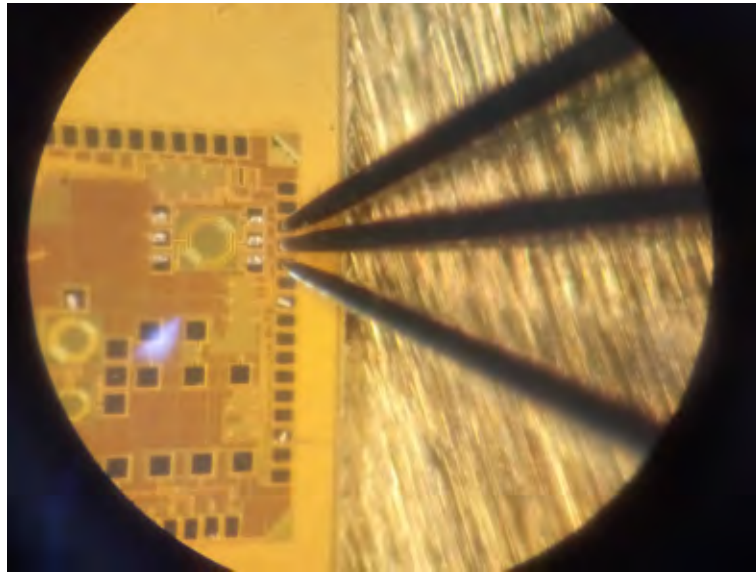
Source: Author.

5.3.3 Bare Die Setup Test

The duplicated circuits that were not packed in the DIP40 were tested using the a probe station, oscilloscope and a semiconductor parameter analyzer.

Fig. 5.29 shows the bare die in the probe station with the needles in the pads. Fig. 5.30 presents the probe station with the microscope and the complete setup test is in the Fig. 5.31.

Figure 5.29: Die in the probe station.



Source: Author.

Figure 5.30: Probe station.



Source: Author.

5.3.4 Measurement Results

The measurement results of the complete DC - DC converter were not satisfactory. No output current appear in the output of the converter, what implies that somehow the converter is not switching properly. The complete converter is a complex circuit with a huge amount of circuits and blocks, what makes difficult the analysis of what went wrong. Also, the number of pads in the DIP40 packaging is reduced due to the need of sharing with other students. This

Figure 5.31: Complete setup test.



Source: Author.

situation did not allow the adding of some internal probe points that could shine path to discover the bad results of the circuit. Although, in the run that the circuits of this work were sent, some silicon area was available to replicate some important circuits of the design. Those circuits were tested in the probe station and the results will be presented in the following subsection.

The static consumption of all the peripheral blocks stayed at $850 \mu\text{A}$ for a power supply of 3.3 V.

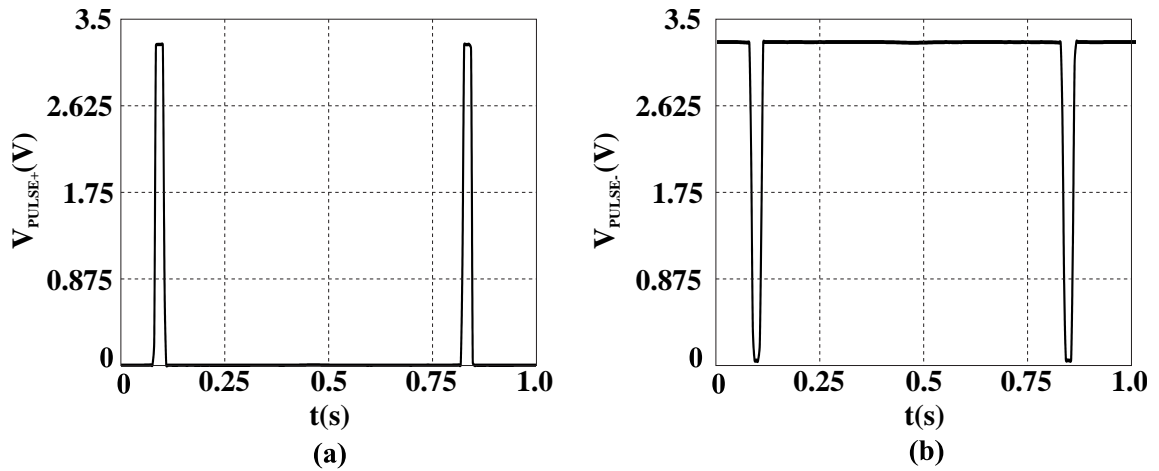
5.3.5 Timer, Bias and Bandgap

The circuits of the Timer and Bandgap were replicated in order to be tested separately. Since these circuits are biased by the circuit bias, it could be testes indirectly.

The timer was tested using the probe station and an oscilloscope. Fig. 5.32 presents the results. It was shown a switching frequency smaller than the simulated. The simulation presented a switching frequency of 2 Hz and the measurement 1.33 Hz. It is natural to expect some difference due to the capacitance of the pads, that were not included in the simulation and also, due to the process variability, that impacts in the conductance of the transistors.

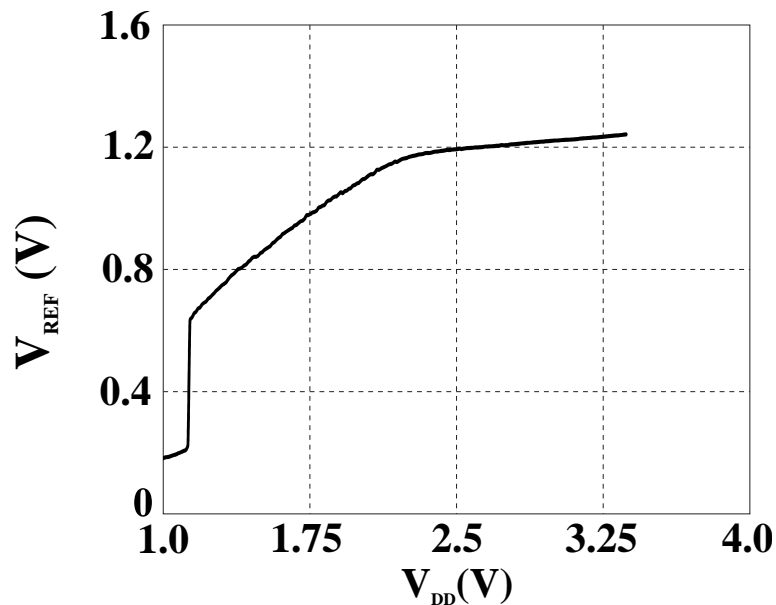
Fig. 5.33 presents the bandgap voltage characteristic with the supply voltage variation. It was measured using the semiconductor parameter analyzer 4156 of HP Company.

Figure 5.32: Timer measurement result (a) Enable Pulse (b) Enable Pulse Inverted.



Source: Author.

Figure 5.33: Bandgap measurement result.



Source: Author.

The circuit worked properly presenting a 1.2 V with low line sensitivity of 0.04 V/V from a minimum supply voltage of 2.5 V.

Measurements with temperature variation were not possible to be performed since the circuits were not packed. It is necessary to be packed to use the thermal chamber existent in UFRGS labs.

These two measurement results shown that some of the designed blocks worked, what discards some possibilities of why the complete circuit did not worked as expected.

5.4 Other Results

The results of this work were summarized and published in the IEEE 8TH Latin American Symposium on Circuits and Systems with the title of **A 90% Efficiency 60 mW MPPT switched capacitor DC — DC converter for photovoltaic energy harvesting aiming for IoT applications.**

6 CONCLUSIONS

This work presented the development of a 1-to-2 six phases Switched Capacitor DC - DC converter for Photovoltaic Energy Harvesting using an open-circuit voltage ratio MPPT strategy. The converter achieved a maximum efficiency of 90 % and drains up to 60 mW of the target PV panel, what is an energy enough to extend the lifetime of commercial motes.

The main objectives described in the introduction were achieved with the exception of the good results in the measures of the complete DC - DC converter.

A complete review about the energy harvesting power sources was done, where the characteristics of TEGs, PV cells, piezoelectric and ambient RF were presented. In this description, the Photovoltaic source was the chosen one to be harvested, since is the one with the highest power density at outdoor applications and presents suitable values of voltage and current to be efficiently converted.

The electrical model of a PV cell was presented. This model shown the non ideal behavior of the PV cell source. It presents a specific point of maximum power deliver, that must be tracked in order to obtain the maximum possible power of the source, what is the objective of a energy harvesting circuit.

Maximum Power Point Tracking techniques were presented. The P&O and IC make tracks the real MPP, but they require measurements of current and voltage and the costs of power and implementation are high. Instead of them, the ratio of the V_{MPP} was the chosen technique. It requires only the observation of the V_{PANEL} and the cost of power and implementation are low.

A small dimension PV panel was chosen in the Brazilian market with respect to cost and size. Measurements at different light intensities were performed and the results were used in a fitting software that obtained the model parameters of it.

Also, a complete review about the basis of DC - DC conversion was done. It was shown that the switched conversion approach is the one that can achieve higher efficiency while can perform DC up conversion, differently from the linear converters ones.

The losses modeling of the Switched Capacitor DC - DC converters were presented using the R_{SSL} and R_{FSL} approach. This approach was used to design the converter core through efficiency curves plotted using a MATLAB script.

All the peripheral blocks necessary for the MPPT, control, drive and protection circuits were custom designed and fabricated.

The simulation results were satisfactory. All the sub blocks worked as expected and the

complete converter deliver energy to an output battery tracking the MPP of the PV panel model with a high efficiency at the power range specified.

Although, the measurement results was not as expected. The replicated blocks Timer and Bandgap worked, but the complete converter did not. The difficulties with relation to access of silicon and packaging did not allow the measurement of the internal nets of the converter. This "black box" situation did not allow the discover of the design mistake.

The developed work can be compared with some recent developed commercial harvesting circuits like (TEXAS, 2011) and (CYPRESS, 2015), Tab. 6.1.

Table 6.1: Comparison among works.

Specification	(TEXAS, 2011) ⁺	(CYPRESS, 2015) ⁺	This Work [*]
Eff. (%) @ 30 mW @ 3.3 V_{OUT}	85 @ 1.65 V_{IN}	91 @ 2 V_{IN}	90 @ 1.65 V_{IN}
Type	Boost	Boost	SC
MPPT (Yes/No)	Yes	Yes	Yes

⁺Measurement | ^{*}Simulation

Source: Author.

The designed converter is competitive in comparison with the presented ones for the range of power that goes from 30 mW to 60 mW and for the input voltage range that goes from 1.6 V to 2. V. Although, it is important to let clear that those converters posses a large input voltage and power ranges, what is a limitation of the designed presented here.

Finally, the efficiency of the converter could be improved using control techniques that did not require static power consumption. Also, a reconfigurable Switched Capacitor architecture would allow a higher input voltage range and the converter and panel could be used at indoor applications, where the supplied voltage reduces considerably.

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SOLAR, P. **Tipos de Painel Solar Fotovoltaico**. 2017. Disponível em: <<http://www.portalsolar.com.br/tipos-de-painel-solar-fotovoltaico.html>>. Acesso em: 6 dez. 2017.

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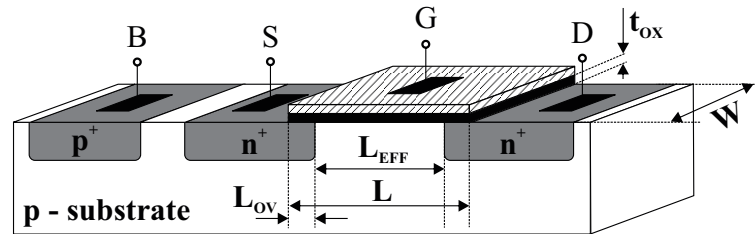
XIAO, W. et al. Overview of maximum power point tracking technologies for photovoltaic power systems. In: **IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society**. [S.l.: s.n.], 2011. p. 3900–3905. ISSN 1553-572X.

APPENDIX A — MOSFET TRANSISTOR & PARAMETER EXTRACTION

In the sixties, the Complementary Metal-Oxide-Silicon (CMOS) technology began to capture the integrated circuits world market; it was a massive revolution that allowed the development of significant part of the existent technologies. The name CMOS is because two types (n-type and p-type) Metal-Oxide-Silicon Field-Effect Transistors (MOSFETs) are made on a single substrate. (RAZAVI, 2001)

Fig. A.1 presents a generic structure of a n-type MOSFET.

Figure A.1: NMOS transistor structure.



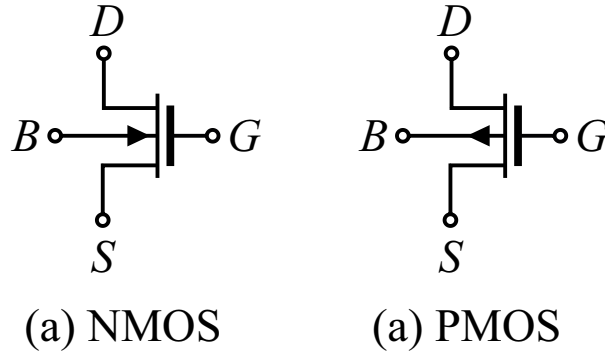
Source: Author.

The MOSFET poses four terminals named Gate (G), Source (S), Drain (D) and Bulk (B). The terminal G is connected to a high conductive plate (metal or polysilicon) that is over a dielectric oxide (SiO_2) with a thickness t_{ox} . The oxide makes the interface with the substrate p-, where the conductive channel is created. Because of this "sandwich", the transistor has the name MOS (Metal over Oxide over Silicon). In the n(p)-type case, the transistor is constructed over the substrate p- (n-well). The terminals S and D are connected to n+(p+) region and the B terminal is connected to a p+(n+) region to make a ohmic contact and properly bias the body of the transistor. Fig. A.2 presents the schematic symbol of the NMOS and PMOS transistors. Fig. A.1 presents a generic structure of a n-type MOSFET.

MOSFETs can work in six different situations. Under the point of view of the V_{GS} voltage, the transistor can be at strong, moderate or weak inversions. Under the point of view of the V_{DS} , the transistors can be at triode or saturation.

This appendix are focused only in the strong inversion, triode and saturation situations. The model and the parameters extraction were performed using the classic quadratic model to describe the behavior of the thick-oxide transistors of the GF-RF 130 nm CMOS technology.

Figure A.2: NMOS and PMOS transistors schematic symbol.



Source: Author.

A.1 Quadratic Model

This model consider that the transistor operates only in strong inversion and suggests three regions of operation, cut-off, triode and saturation. If V_{GS} is lower than a voltage threshold V_{TH} , the transistor is in a cut-off region, and it is considered, by this model, that no current flows though the channel. If V_{GS} is higher than V_{TH} , than there are two possibilities, the transistor may be in triode, when $V_{DS} < V_{GS} - V_{TH}$, or in saturation, when $V_{DS} > V_{GS} - V_{TH}$. These situations are illustrated in Fig. A.3, where the channel current I_D is presented for various values of V_{DS} and V_{GS} .

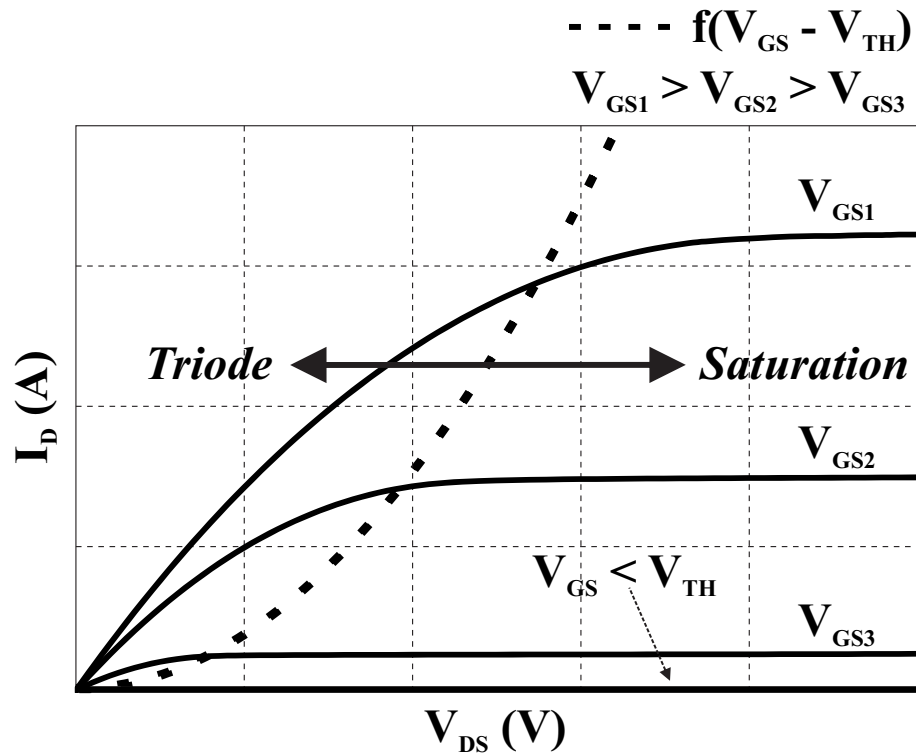
A parabolic curve divides the two operation regions of the MOS transistor, Eq. A.1 provides the current behavior I_D of the transistor channel in triode and Eq. A.2 in saturation, where $\mu_n(p)$ is the charge carrier mobility in the silicon, C_{OX} is the capacitance density of the transistor's gate, W is the width of the gate, L is the length of the gate and Λ is the channel length modulation parameter.

$$I_D = \mu_{n(p)} C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (\text{A.1})$$

$$I_D = \frac{\mu_{n(p)} C_{OX} W}{2 L} (V_{GS} - V_{TH})^2 (1 + \Lambda V_{DS}) \quad (\text{A.2})$$

It is possible to notice that, for small values of V_{DS} , the transistor is in deep triode situation. In this case, the transistor behaves like a resistance controlled by voltage. When the transistor is operating with large V_{DS} , it acts as a non-ideal current source with a parallel impedance defined by the current I_D and the Λ parameter.

Figure A.3: Current Behavior of MOS transistor.



Source: Author.

A transistor can be used in different ways in a circuit. When it is desired that it behaves as a switch, the transistor "switches" from cut-off to triode. When an amplifier is needed, the transistor must be biased to stay at saturation.

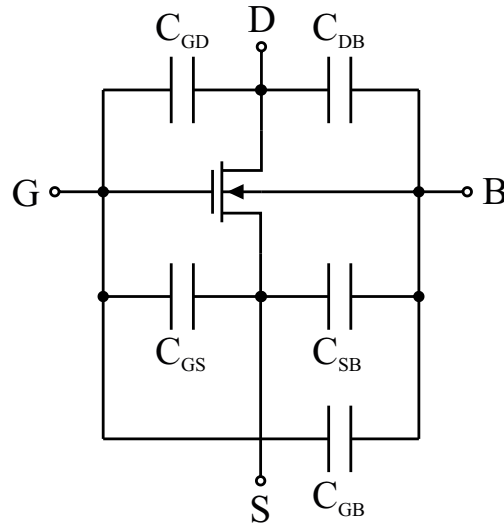
A.2 MOS Gate Capacitance

Besides those static equations, the dynamic behavior of the transistor also needs to be modeled. Fig. A.4 presents the capacitance across the MOS terminals.

For the designs of this work, the most important is the calculus of the gate capacitance when the transistor is in deep triode since it is a concern in the sizing of the power switches. In this case, the total gate capacitance calculus is like in Eq. A.3, where C_{OV} is a parasitic capacitance that appears in the fabrication process when the source and drains diffusions go under the gate oxide.

$$C_{GS(D)} = WLC_{OX} + 2WC_{OV}|_{underV_{GD}} \quad (A.3)$$

Figure A.4: Capacitance across the MOS terminals.



Source: Author.

A.3 Parameters Extraction

In order to design the circuits of this work, the parameters conductive density for deep triode g_{DS} , gate capacitance density for deep triode C_{GG} , $\mu_{n(p)}C_{OX}$, V_{TH} and $\Lambda_n(p)$ of the thick-oxide transistors of GF RF 130 nm were extracted through simulation. These transistors have a minimum channel length of 400 nm.

Tab. A.1 presents the conductivity g_{DS} and the capacitance density (C_{GG}) of the thick-oxide transistors PMOS and NMOS for minimum channel length for the corners SS, TT and FF and for three different temperatures 0°C , 27°C and 80°C .

Table A.1: Conductivity of the Thick Oxide Transistors.

NMOS g_{DS} (S/m)				NMOS C_{GG} (fF/ μm)			
T ($^\circ\text{C}$)	0	27	80	T ($^\circ\text{C}$)	0	27	80
SS	1014	898.5	739.4	SS	2.587	2.584	2.58
TT	1194	1058	870.6	TT	2.421	2.419	2.415
FF	1394	1235	1016	FF	2.266	2.264	2.26
PMOS g_{DS} (S/m)				PMOS C_{GG} (F/ μm)			
T ($^\circ\text{C}$)	0	27	80	T ($^\circ\text{C}$)	0	27	80
SS	255	242.8	225.3	SS	2.439	2.437	2.434
TT	298.4	284.9	265.6	TT	2.256	2.255	2.251
FF	348.2	333.5	312.7	FF	2.074	2.072	2.069

Source: Author.

The channel length modulation Λ was extracted for different channel lengths and V_{GS} . Λ_n is presented in Tab. A.2 and Λ_p in Tab. A.3.

Also, parameters $\mu_{n(p)}C_{OX}$ and V_{TH} were extracted. Fig. A.5 shows $\mu_{n(p)}C_{OX}$ curves for various V_{GS} and channel length of $2 \mu\text{m}$. Fig. A.6 shows V_{TH} curves for various channel lengths.

Table A.2: Channel-Length Modulation Parameter - $\Lambda_{NMOS3.3V}(V^{-1})$

V_{GS} (V)	$L = 0.4 \mu\text{m}$	$L = 1 \mu\text{m}$	$L = 2 \mu\text{m}$	$L = 3 \mu\text{m}$
0.55	260	94	66	57
1.10	85	31	21	18
1.65	44	13	8	7
2.20	27	8	5	4
2.75	20	8	6	6
3.30	18	10	11	11

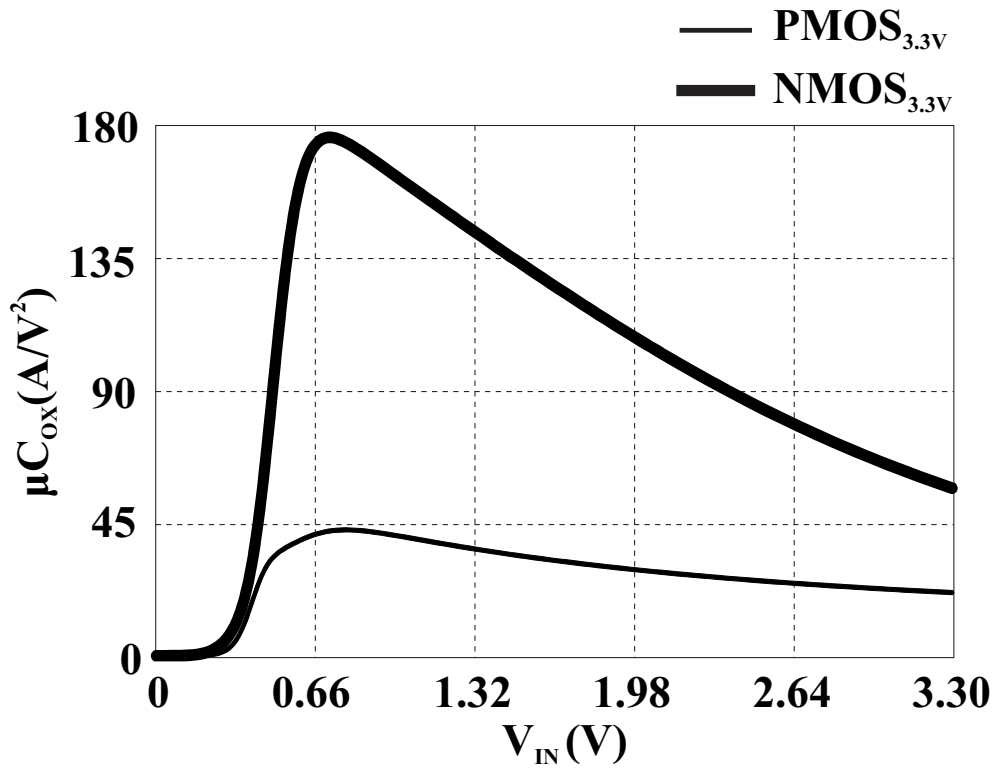
Source: Author.

Table A.3: Channel-Length Modulation Parameter - $\Lambda_{PMOS3.3V}(V^{-1})$

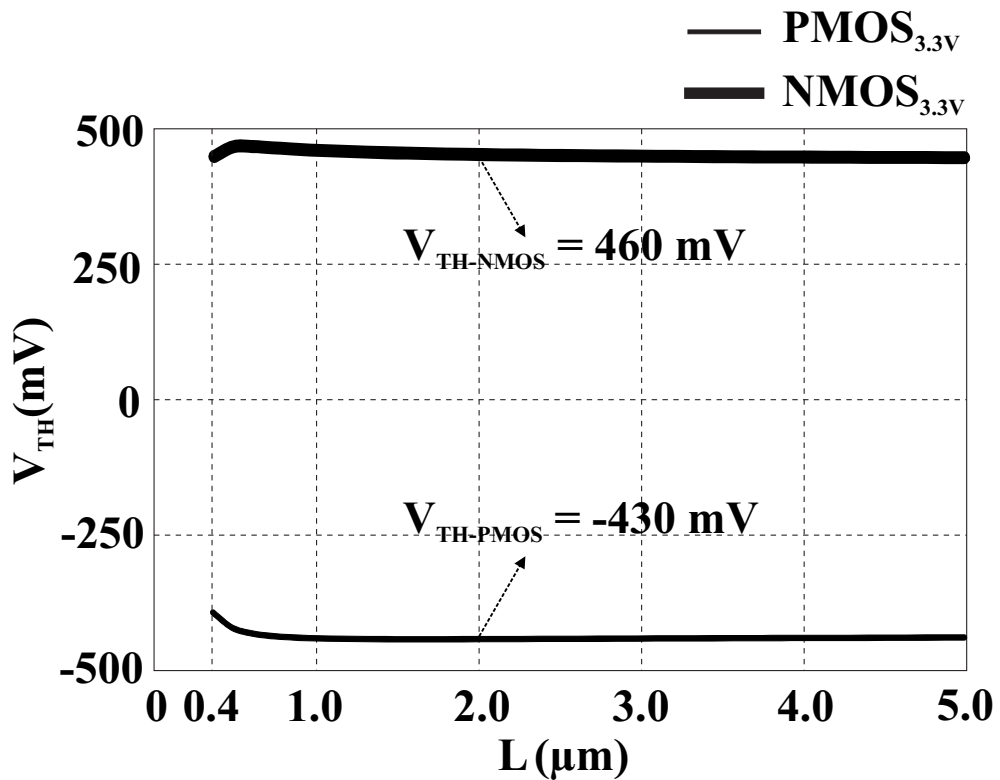
V_{GS} (V)	$L = 0.4 \mu\text{m}$	$L = 1 \mu\text{m}$	$L = 2 \mu\text{m}$	$L = 3 \mu\text{m}$
0.55	165	19	8	5
1.10	61	13	6	4
1.65	50	12	6	4
2.20	44	12	6	4
2.75	41	12	6	4
3.30	43	14	10	8

Source: Author.

The parameters presented here were used in the design of all the circuits presented in this work.

Figure A.5: $\mu_{n(p)}C_{OX}$.

Source: Author.

Figure A.6: V_{TH} .

Source: Author.

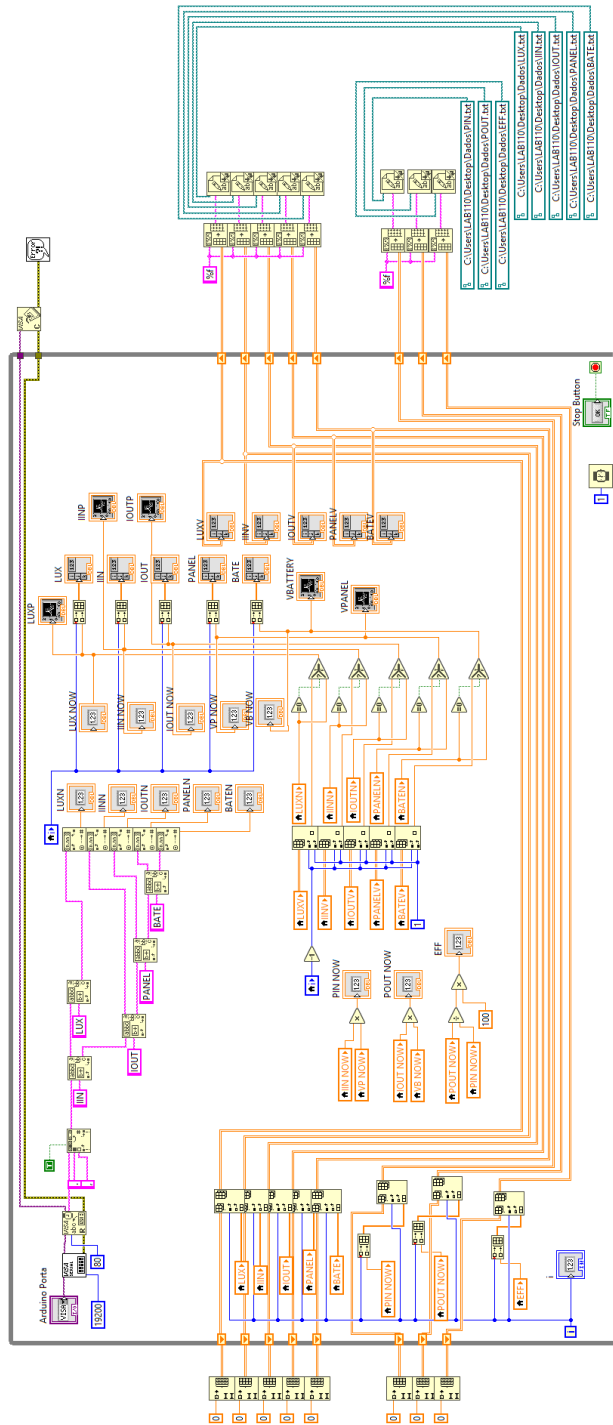
APPENDIX B — ARDUINO CODE

```
1  const int A_LUX = A0;
2  const int A_IIN = A1;
3  const int A_IOUT = A2;
4  const int A_PANEL = A3;
5  const int A_BATE = A4;
6
7  float LUX = 1019.02;
8  float IIN = 1020.02;
9  float IOUT = 1021.02;
10 float PANEL = 1022.02;
11 float BATE = 1023.02;
12
13 int S0 = 0;
14 int S1 = 0;
15 int S2 = 0;
16 int S3 = 0;
17 int S4 = 0;
18
19 void setup() {
20   Serial.begin(19200);
21 }
22
23 void loop() {
24
25   S0 = analogRead(A_LUX);
26   S1 = analogRead(A_IIN);
27   S2 = analogRead(A_IOUT);
28   S3 = analogRead(A_PANEL);
29   S4 = analogRead(A_BATE);
30
31   LUX = 790*(5.00*S0/(1023.00));
32   IIN = 4.036328996*sqrt(1105.448685+1.00000*S1)-134.50;
33   IOUT = 6.991126899*sqrt(3067.83378+1.00000*S2)-388.00;
34   PANEL = 5.00*S3/(1023.00);
```

```
35 BATE = 5.00*S4/(1023.00);
36
37 Serial.print("LIMPA");
38 Serial.print(1618.00);
39 Serial.print("LIMPA");
40 Serial.print(1618.00);
41 Serial.print("LUX");
42 Serial.print(LUX);
43 Serial.print("IIN");
44 Serial.print(IIN);
45 Serial.print("IOUT");
46 Serial.print(IOUT);
47 Serial.print("PANEL");
48 Serial.print(PANEL);
49 Serial.print("BATE");
50 Serial.println(BATE);
51
52 delay(1);
53 }
```

APPENDIX C — LABVIEW CODE

Figure C.1: LabVIEW "code".



Source: Author.