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Design flow methodology for Radiation Hardening by Design CMOS Enclosed Layout Transistor based standard cell library for aerospace applications

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Advisor: Prof. Dr.-Ing. Gilson Inácio Wirth

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“Not explaining science seems to me perverse.
When you’re in love, you want to tell the world.”

— Carl Sagan

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ABSTRACT

Applications exposed to incidence of ionizing radiation, such as aerospace applications, may have their performance and reliability degraded by the interaction of high-energy ions. Thus, applications exposed to incidence levels of such ions can be severely affected over time. In these cases, hardening techniques are required for the proper operation of those devices when subject to harsh environments. Unfortunately, Brazil does not produce radiation-tolerant integrated circuits and, over time, the lack of this expertise not only hinder R&D opportunities but also drastically increases the costs of buying hardened and reliable circuits. For the most part, the increase occurs because in the overwhelming majority of cases these circuits are subjected to territorial regulations by other countries or have restricted availability (proprietary right) or are only discussed within academic institutions. To synthesize complex circuits as, for example, Application Specific Integrated Circuits - ASICS, the use of an automated design flow is inherently necessary mainly due to a huge number of transistors, reaching, in some cases, the order of some billions. To face the lack of reliable foundry-provided Radiation-Hardening by Design (RHBD) cell libraries, this thesis promotes a complete RHBD flow methodology employing enclosed-layout transistors (ELTs) and guard rings, transparent to the designer, and fully compatible with commercial CAD tools and standard fabrication processes. The proposed flow includes the automated calculation of the effective aspect ratio (W/L) of the ELTs, promoting state-of-the-art improvements to key points of the ICs design flow such as the template proposal for digital cells, as well as its series and parallel arrangements. Moreover, it also covers employing for the first time, for the sake of our knowledge, the calculation of PN ratio and output buffers dimension using Logical Effort (LE) methodology, i.e., time optimization approach with enclosed devices. To validate the proposed methodology test structures, enclosing single n,pMOS devices, series and parallel arrangements, inverter cells, ring oscillators, and output buffers, were fabricated in two different technology nodes (600 nm and 180 nm). Subsequently to their electrical characterization, they were compared to SPICE simulations and, after irradiated, the increase in the leakage current and shift in the threshold voltage were compared with related works. Besides, two silicon-proven case studies presented fully functional behavior under typical conditions even after 500 $krad$ of absorbed dose, achieving success in the radiation test. The results and experimental data indicate that the radiation tolerant cells designed with the proposed flow are feasible to implement and their hardness degree is in accordance with the findings in the literature,

where the transistors and circuits were manually designed. Therefore, the novel methodology of automated design flow is an elegant solution to efficiently reduce time and costs for the development of RHBD devices for sensitive applications in harsh environments, consolidating the proposed thesis and contributing with the ability to tape-out such circuits in the Brazilian semiconductor industry.

Keywords: Radiation-Hardening. Aerospace applications. Enclosed Layout Transistor. Standard Cell Library. bulk CMOS. Full-custom design flow.

Metodologia para fluxo de projeto de biblioteca de células CMOS tolerantes à radiação baseada em dispositivos de geometria de gate fechado para aplicações aeroespaciais

RESUMO

Aplicações sujeitas à incidência de radiação ionizante, tais como aplicações aeroespaciais, podem ter sua performance e confiabilidade afetadas devido à interação de íons de alta energia. Para estes casos, a aplicação de técnicas de tolerância à radiação são necessárias a fim de possibilitar o funcionamento prolongado de dispositivos em ambientes sujeitos à incidência de tais íons. Infelizmente, o Brasil não produz dispositivos tolerantes à radiação, o que, no presente momento, não somente prejudica a pesquisa e desenvolvimento destes equipamentos, como aumenta drasticamente seu custo de produção. Em sua grande maioria, esses empecilhos e aumento de custo ocorrem devido às taxas alfandegárias e de importação entre países; por se tratar de propriedade intelectual (patentes registradas); ou, ainda, por serem apenas abordadas no âmbito acadêmico. Como alternativa a esse conjunto de demandas, esta tese apresenta um fluxo de projeto para o desenvolvimento e síntese de circuitos tolerantes à radiação utilizando dispositivos de *gate* fechado (ELTs). O fluxo proposto visa a síntese de circuitos digitais complexos, com um grande número de transistores, na ordem de alguns bilhões. Por este motivo, esta tese implementa a automatização do cálculo da razão de aspecto (W/L) dos ELTs, possibilitando que a síntese seja transparente para o projetista e totalmente compatível com as ferramentas de projeto comerciais. A proposta de fluxo de projeto possui vários aspectos inovadores como, por exemplo, o *template* para células digitais e sua organização em arranjos em série e paralelo. Ademais, de acordo com nosso conhecimento, aplicando também o método do Logical Effort (LE) pela primeira vez no contexto dos ELTs, tanto no cálculo da razão PN quanto no dimensionamento de *buffers* de saída. Para a validação da tese proposta foram fabricadas estruturas de teste com dispositivos de *gate* fechado, tanto n como pMOS, arranjos em série e paralelo, células inversoras, osciladores em anel e *buffers* de saída em dois nós tecnológicos distintos ($600\ nm$ e $180\ nm$). A caracterização elétrica dos dispositivos foi comparada às simulações elétricas SPICE e, após estresse de radiação, seu incremento na corrente de fuga e desvios na tensão de *threshold* foram analisados e comparados com base em trabalhos relacionados. Ambos os chips de teste tiveram sua funcionalidade integralmente verificada já na primeira rodada de fabricação em silício, dentro das margens

de tolerância e condições típicas de funcionamento, atingindo sucesso no teste de radiação mesmo após $500\ krad$ de *Dose*. Os resultados e dados experimentais indicam que as células tolerantes projetadas através do fluxo proposto têm sua implementação viável e o nível de tolerância obtido está de acordo com os referenciados na literatura, nos quais os dispositivos e circuitos são projetados manualmente. Portanto, a nova proposta de projeto de fluxo automatizado é uma solução elegante para a redução, de forma eficiente, de tempo e custo no desenvolvimento de dispositivos tolerantes para aplicações sensíveis à radiação, consolidando a tese proposta e contribuindo para a habilidade de produção de dispositivos tolerantes na indústria Brasileira de semicondutores.

Palavras-chave: Tolerância à radiação. Aplicações aeroespaciais. Geometria de *gate* fechado. Biblioteca de células. *bulk CMOS*. Fluxo de projeto *full-custom*.

LIST OF ABBREVIATIONS AND ACRONYMS

ASIC	Application-Specific Integrated Circuit
BSIM	Berkeley Short-channel IGFET Model
CAD	Computed Aided Design
CLM	Channel Length Modulation
CMOS	Complementary Metal Oxide Semiconductor
DD	Displacement Damage
DRC	Design Rule Checking
ECSS	European Cooperation for Space Standardization
ECT	Edge and Corners Transistors
ELT	Enclosed Layout Transistor
ESA	European Space Agency
ESD	Electrostatic Discharge Protection
FIT	Failure in Time
FoM	Figure of Merit
FOX	Field Oxide
FO4	Fanout-of-four
GDSII	Graphic Database System
HEP	High Energy Physics
IC	Integrated Circuit
ICR	Transient current pulse
IP	Intellectual Property
ITAR	International Traffic in Arms Regulation
LE	Logical Effort
LEF	Layout Extend Format

LET	Linear Energy Transfer
LOCOS	Local Oxidation of Silicon
LVS	Layout Versus Schematic
MOS	Metal Oxide Semiconductor
PCB	Printed Circuit Board
PDK	Process Design Kit
PEX	Parameter Extraction
RTL	Register Transfer Level
RHBD	Radiation-Hardening by Design
R&D	Research and Development
SEE	Single-Event Effects
SPICE	Simulation Program with Integrated Circuit Emphasis
SPT	Sum of Parallel Transistors
S&S	Space and Satellite
STD	Standard Device
STI	Shallow Trench Isolation
TB	Test Bench
TE	Two-Edged Device
TID	Total Ionizing Dose
UFRGS	Federal University of Rio Grande do Sul

LIST OF SYMBOLS

B	Path's branching effort $[-]$
$C_{in,out}$	Input and Output capacitances $[F]$
C_L	Load capacitance $[F]$
$C_{gox_{n,p}}$	Gate oxide capacitance $[F/\mu m^2]$
$C_{g_{n,p}}$	Gate oxide n and p capacitances $[F]$
γ	Gamma ratio (or PN aspect ratio) $[-]$
d_{hor}, d_{ver}	ELT's horizontal and vertical internal diffusion distances $[m]$
D	Absorbed ionized doze $[Gy]$
ΔI_D	Drain current variation $[A]$
$\Delta G_{di,o}$	Output device's conductance variation for drain in- and outside $[-]$
ΔL	Channel length variation $[m]$
$\Delta L_{di,o}$	Pinch-off region variation for drain in- and outside $[m]$
ΔV_{DS}	Source/drain voltage variation $[V]$
E, E_0	Energy dissipation and its value at position $X = 0$ $[J]$
$\bar{e}/h$	Electron/hole pairs $[-]$
f_T	Transition frequency $[Hz]$
L	Transistor's length $[nm]$
F	Path's effort $[-]$
$\hat{f}$	Stage effort $[-]$
G	Path's Logical Effort $[-]$
$G_{area_{n,p}}$	Gate area over an *n* and *p* diffusion $[m^2]$
g_{avg}	Medium value for Logical Effort $[-]$
G_{out}	Output device's conductance $[S]$
g_{sd}	Source/drain conductance $[S]$

$g_{u,d}$	Logical Effort for rising (u) and falling (d) transitions $[-]$
I_0	Current generated by the charges $[A]$
$K_{n,p}(S)$	Series factor for nMOS and pMOS devices $[-]$
H	Electrical Effort $[-]$
LET	Linear energy transfer of ionizing radiation $[MeV/(mg/cm^2)]$
N	Linear density of electron-hole pairs $[LET/eV]$
μ	Gamma ratio for a balanced inverter cell $[-]$
$\hat{N}$	Best number of stages $[-]$
$NM_{H,L}$	Noise margins High and Low $[V]$
P_{avg}	Average power $[W]$
q	Electron charge $[C]$
Q_{crit}	Minimum amount of charge necessary to induce an upset $[C]$
Q_D	Drift charge component $[C]$
Q_DF	Diffusion charge component $[C]$
Q_F	Funnel charge component $[C]$
Q_t	Total Spurious Charge $[C]$
$r_{hi,lo}$	Skewing factors High and Low $[-]$
ρ	Material density $[g/cm^3]$
$\tau_{r,f}$	Transient current rise time and fall time $[s]$
θ	Incident ion hit angle $[^\circ]$
t_{ox}	Oxide thickness $[nm]$
t_p	Propagation delay $[s]$
$t_{rise,fall}$	Rise and Fall times $[s]$
V_{DD}	Positive supply voltage $[V]$
V_{SS}	Negative (or ground) supply voltage $[V]$
V_{th}	Threshold voltage $[V]$

X	Unit cell size current capability or drive strength $[-]$
W	Transistor's width $[nm]$
$W_{n,p}$	n and pMOS transistor's width $[nm]$
(W/L)	Device's aspect ratio $[-]$
$\bar{\mu}$	Carrier mean mobility $[cm^2/V \cdot s]$
λ	Mean separation distance between $\bar{e}/h$ pairs $[nm]$

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1 INTRODUCTION

1.1 Motivation

When observing the success of CMOS technology, it is indubitably necessary to refer to the steady progression of technology scaling. The aggressive increase at an integration level has lead the semiconductor industry to a vertiginous rise, improving Integrated Circuits (ICs) functions and resources in the process (PELLISH, 2012).

To synthesize complex circuits, which demand a huge number of functions and resources (e.g., microprocessors or Application-Specific Integrated Circuits - ASICs), the use of a design flow automation is inherently necessary to reduce design time and production costs. The core of this process is a group of digital cells pre-designed and properly characterized named digital library. These cells are the effective link between Computed Aided Design (CAD) tools, which allow a high-level description of the system (coded in a hardware language, such as VHDL or Verilog), and the actual physical implementation of the system (SCHUCH et al., 2009).

Nonetheless, the incidence of ionizing radiation may result in undesirable effects in the ICs, such as upset and even permanent damage to the device's materials. Therefore, applications exposed to a radioactive environment may behave unpredictably, reducing reliability and expected lifetime (LIU et al., 2014b; KNUDSEN; CLARK, 2006).

Ground-level applications are naturally less susceptible to the incidence of ionizing radiation when compared to Aeronautics and Space & Satellite (S&S) devices, mostly due to the Earth's natural magnetic shielding. The magnetic field traps incoming ionizing particles, especially those ejected from the solar coronal mass, giving rise to radiation belts known as Van Allen belts. However, not only space applications, but also on a ground-level ones, High Energy Physics (HEP) experiments are severely affected by ionizing radiation (VELAZCO et al., 2007, BOUDENOT in).

The robust physical design proposal referred to as Radiation-Hardening by Design (RHBD) provides the possibility to achieve higher levels of tolerance to accumulated effects of ionizing radiation. By employing RHBD techniques it is possible to mitigate even Total Ionizing Dose (TID) or Single Event Effects (SEE) through a combination of layout and design hardening techniques (KNUDSEN; CLARK, 2006). In the context of design flow automation, the main issue lies in the fact that cell libraries employing RHBD techniques are not commercially available being, therefore, proprietary IPs subject

to territorial regulations (CHANG et al., 2014).

While HEP, S&S, reliable control systems and deep space exploration have been studied and supported in other countries (such as USA, China and France) (YIN et al., 2016), here in Brazil they are a relatively recent field of study. In our context (ICs R&D industry in Brazil), the knowledge to design such hardened devices has been a growing interest in the last few years, even in cases where there are no embargoes regarding International Traffic in Arms Regulation (ITAR). Brazil buys these IPs but does not produce it and, over time, the lack of this technology not only usurps R&D opportunities but also drastically increases the costs of buying hardened and reliable circuits.

Therefore, aiming to provide radiation-tolerant ICs, this thesis presents a methodology to develop RHBD cell libraries in bulk CMOS technology, using real world constraints. In this sense, state-of-the-art improvements to key points of the ICs design flow are proposed: the analysis and implementation of core models to predict the device's effective (W/L) aspect ratio; and the design of library cells based on full-custom analog optimizations, generating the necessary characterization files, completely compatible with commercial design flow. These contributions are crucial to improve the ability of the Brazilian semiconductor industry to tape-out RHBD circuits.

Nonetheless, despite all technical analyses and advancements, I conceive that the major contribution of this thesis, which has required great effort (and some experience), was to assemble all the knowledge from the first steps of design (i.e., the layout transistor) to the final steps (i.e., final tape-out of digital cells).

Furthermore, this thesis applies all the RHBD techniques to technology nodes available in the Brazilian semiconductor industry, enabling the whole chain of production to fully incorporate Register Transfer Level (RTL) to the automated design flow of Graphic Database System (GDSII).

1.2 Thesis structure and contributions

Figure 1.1 illustrates the structure of this thesis, highlighting the original aspects and analyses presented throughout this work.

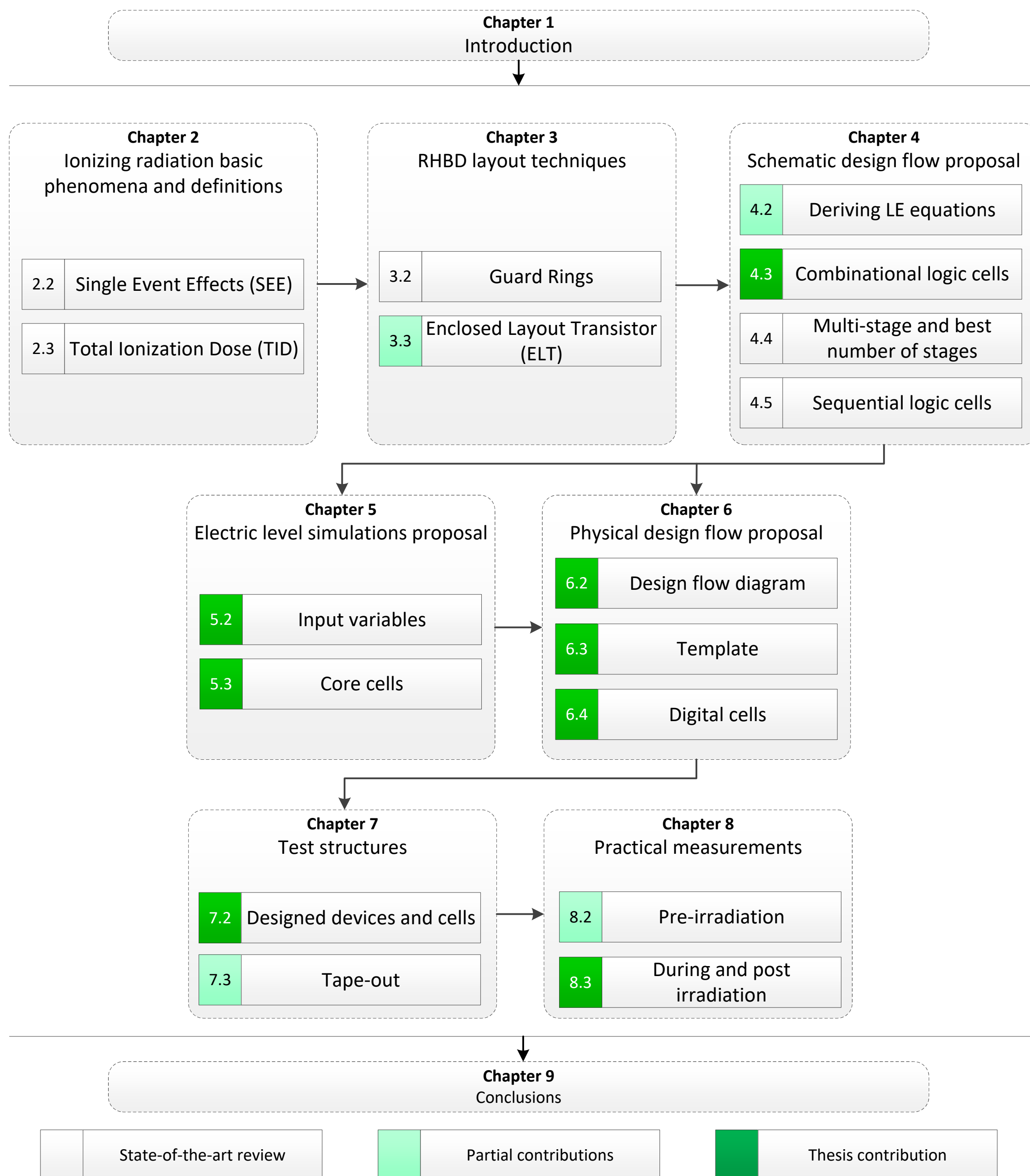
Colored in light green are the sections (or subsections) in which I gave minor contributions, considering original analysis, new data or minor adjustments in equations' parameters. Colored in dark green are the most important contributions of this thesis, i.e., the areas that play a key role in this work, aiming to advance the state-of-the-art (in terms

of what is available in the literature), establishing a solid link throughout all design flow steps.

Following these criteria, after this introduction, Chapter 2 introduces the basic concepts related to the interaction of ionizing radiation with matter. Chapter 3 discusses some hardening techniques, which can be applied through all circuit abstraction levels, under a commercially available fabrication process, facing emblematic challenges of the most common (and effective) employed techniques. Besides, minor expansion in related $(W/L)_{eff}$ predictive equations are proposed (and validated through analysis and simulations) in order to enlighten, and ease, the acquisition of aspect ratios for non-square gate geometries.

Chapter 4 proposes a generalization of the well know Logical Effort method (LE), which takes into account all design variables at the same equation allowing the automation of gate size calculation for n-and p-MOS transistors, and also the PN aspect ratio for the least average delay. Chapter 5 explores the electrical level simulations of digital cells based on enclosed gate topology through their small and large signal behaviors. Chapter 6 presents and explains the proposed design flow methodology. Chapter 7 introduces the laid out test structures in technology nodes of $600\ nm$ and $180\ nm$, aiming to validate the proposed methodology. Chapter 8 presents the pre- and post-irradiation experimental results and, finally, Chapter 9 provides the conclusions and final remarks.

Figure 1.1: Thesis organization and contributions.



Source: Author.

1.3 Important information

In order to be used in the present work, terms related to ionizing radiation, and space projects and applications follow the standards provided by European Cooperation for Space Standardization (ECSS) (ECSS, 2004).

The preceding terms referred as *qualified* or *hardened* device means that device is

designed to properly operate between acceptable error margins (i.e., failure tolerance), with the ability to fulfill specified requirements taking into account the environment specification for baseline application given a time interval. Moreover, the preceding term *mitigation* refers to attenuation or reduction of the impact of the related phenomena, making it less severe.

The compendium of design-oriented *mitigation* and *hardening techniques*, the focus of this work, is proposed in order to substantially reduce the ionizing radiation effects in bulk CMOS. And, for this reason, the origin of the term *Radiation-Hardening by Design* (RHBD).

2 IONIZING RADIATION BASIC PHENOMENA AND DEFINITIONS

2.1 Introduction

The transmission of energy in the form of particles or waves through space or matter is defined as radiation. Moreover, when radiation particles travel through solid materials transferring kinetic energy to atomic electrons, causing them to be liberated (ionized), they are defined as ionizing radiation (FB, 1987).

In the context of integrated circuits, there is a plethora of ionizing particles capable of carrying enough energy to disrupt electric atomic bound, spanning from α-particles to γ- and X-rays (SEONG, 2008). The former (α-particles) are commonly related to metal interconnecting layers as P_b/S_n solder balls and Uranium (^{238}U) and Thorium (^{232}Th), which may be presented in device packaging process (ROCKETT, 2004; SEONG, 2008); and the latter (γ- and X-rays), due to their higher energy, are predominantly referred to space radiation environment, and consequently being a particular issue to space and satellite applications.

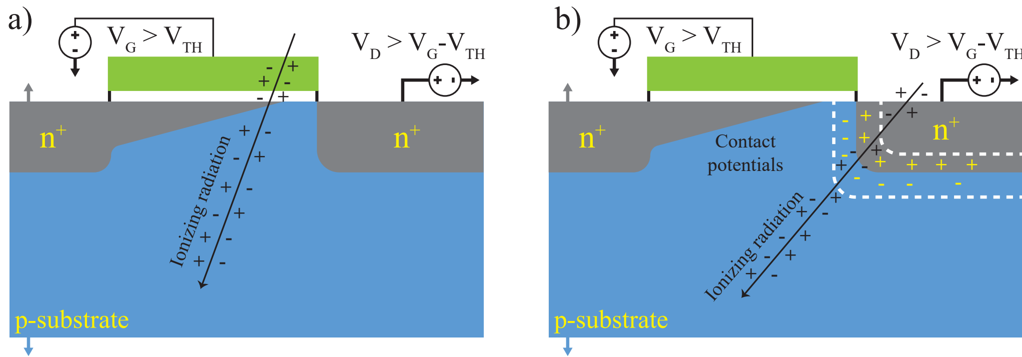
The interaction of ionizing radiation with matter produces a plasma-like track composed by electron-hole pairs ($\bar{e}/h$) in the shape of a cylindrical funnel with a radius in the order of $1\ \mu m$ or even less (OHRING, 1998; ROCKETT, 2004). Additionally, for heavy ions, this damage may slightly vary depending on the mass, charge and kinetic energy of the incident particle and the mass, charge, and density of the target material (FB, 1987; SEONG, 2008).

After the generation, the natural process is a rearrangement of these charges in such a way that free electrons and holes recombine themselves. Indeed, in an unbiased device (i.e., when no external electric field is applied) in a few picoseconds 80% to 90% of these pairs effectively recombine (ANELLI, 2000; VAZ, 2015). In fact, the recombination of charges vary depending on the resistance of the materials: higher recombination rates are observed in materials with lower resistances (VAZ, 2015).

In bulk CMOS transistors, due to the applied electric fields, the generation of $\bar{e}/h$ pairs is a concern not only in reverse-biased PN junctions, Figure 2.1 (b), but also in silicon dioxide (SiO_2) regions (a) (ANDREOU et al., 2015).

In these particular regions, hereafter named as *sensitive regions*, the movement of charges, accordingly to the electric field they experiment, give rise to transient upsets or permanent damages both for analog and digital circuit operations.

Figure 2.1: Electron/hole pairs production through: a) gate oxide region (SiO_2), and b) reversely biased PN junction.



Source: Author.

When the observed or measurable changes in the device's response are caused by a single energetic particle, the effect is defined as Single Event Effect (SEE). On the other hand, the accumulation and long term degradation of changes in semiconductor materials and devices performance is categorized as Total Ionizing Dose effect (TID) (MUNTEANU; AUTRAN, 2008).

The former effect is caused mainly due to heavy charged particles (protons, alpha, and other ions) and the second one is produced, directly and indirectly, by all ionizing radiations (X- and γ rays, electrons, neutrons, protons, α and other heavy ions).

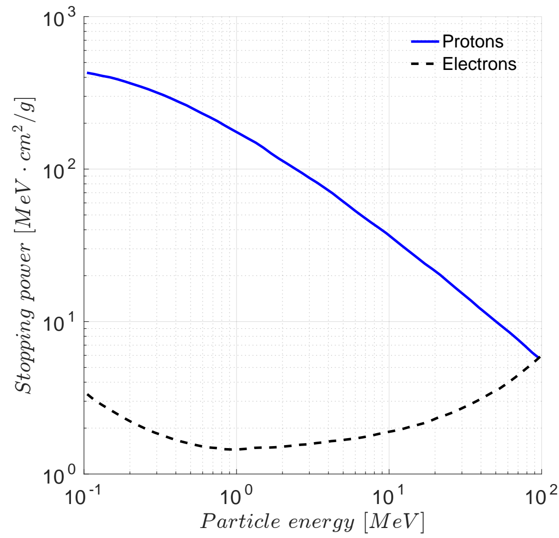
2.2 Single Event Effects (SEE)

Whilst the incident ion crosses the device's material, it loses its energy by the Linear Energy Transfer mechanism (LET), also referred as medium *stopping power*. The LET describes the amount of energy that goes into ionization, in other words, the energy deposited in the target material per unit length of the ion path, expressed in terms of $(MeV \cdot cm^2/g)$, according to:

$$LET = \left(\frac{1}{\rho} \cdot \frac{\partial E}{\partial x}\right), \tag{2.1}$$

where ρ is the material density in (g/cm^3) (FB, 1987). The Figure 2.2 shows the stopping power for incident protons and electrons on silicon material (FB, 1987; SROUR, 1982).

Figure 2.2: Stopping power for electrons and protons on silicon.



Source: Plotted data acquired from (SROUR, 1982).

The energy deposited per gram of material is called absorbed ionized dose (D) and its SI unit is the gray (Gy). Although the radiation effects community historically adopted the unit rad (acronym for radiation absorbed dose), which is equal to:

$$1(Gy) = 1 \cdot \left(\frac{J}{Kg}\right) = 100(rad) = 6.24 \cdot 10^{15} \cdot \left(\frac{eV}{g}\right). \tag{2.2}$$

Moreover, while the energy loss depends on the mass of the target material, it must be specified as rad (Si) or rad (SiO_2), for example. For this purpose, considering the materials commonly used in bulk CMOS technology, the conversion factor presented in 2.3 can be used (SROUR, 1982).

$$1 \cdot rad(Si) = 0.58 \cdot rad(SiO_2) = 0.94 \cdot rad(GaAs) \tag{2.3}$$

It is worth to note that is possible to obtain the number of generated $\bar{e}/h$ pairs by dividing the deposited energy into the energy necessary to create each $\bar{e}/h$ pair and multiply by the material density. The Table 2.1 summarizes these aforementioned parameters for commonly employed MOS materials (SROUR, 1982; ANELLI, 2000; OLDHAM; MCLEAN, 2003).

Table 2.1: Materials and related electron-hole pairs generation energies, densities and pair densities*.

Material	Pair generation energy (E_{eh}) (eV)	Density (P) (g/cm^3)	Pair density generated per rad (g_0) $(pairs/cm^3)$
Si - Silicon	3.6	2.328	$4.0 \cdot 10^{13}$
SiO_2 - Silicon Dioxide	17	2.2	$8.1 \cdot 10^{12}$
$GaAs$ - Galium Arsenide	4.8	5.32	$7.0 \cdot 10^{13}$
Ge - Germanium	2.8	5.38	$1.2 \cdot 10^{14}$

* Complemented data from (FB, 1987; PELLISH, 2012).

In silicon dioxide, the thermalization distance (i.e., the initial separation between a hole and its corresponding electron of the same pair after they reach thermal energy) is evaluated to be ranging from 5 nm to 10 nm with the average of about 8 nm (FB, 1987; ANELLI, 2000). Also, the mean separation distance between $\bar{e}/h$ pairs (λ) is inversely proportional to the LET. With the aim of quantifying its order of magnitude, works such as (FB, 1987; ANELLI, 2000) point out for a LET of 100 $MeV \cdot cm^2/g$ a $\lambda \approx 1\ nm$ and for a LET of 10 $MeV \cdot cm^2/g$ a $\lambda \approx 10\ nm$, which in terms of capacitance per unit length was calculated as $100\ MeV \cdot cm^2/mg \approx 1\ pC/\mu m$ in silicon (MUNTEANU; AUTRAN, 2008).

For an in-depth view on the methods to investigate λ distances, I invite the reader to first consult *Columnar* and *Geminate* models (ANELLI, 2000; FB, 1987; SROUR, 1982).

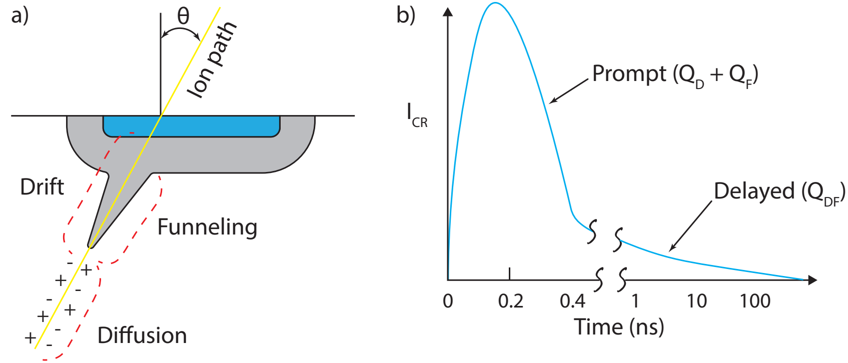
Due to direct interactions, the first amount of energy is converted into $\bar{e}/h$ pairs. Due to indirect interactions, the remaining energy is converted into heat, and a very small quantity into atoms displacement (MUNTEANU; AUTRAN, 2008).

The displacement of atoms disarranges the original structure of the crystal lattice by knocking an atom from its lattice site, giving rise to displacement damage (DD). Nonetheless, the rate of energy deposited during this process is more than three orders of magnitude lower than in SEE, or in TID (SROUR; MCGARRITY, 1988). For this reason, this work is focused on SEE and TID effects. For more information on DD, check (CLAEYS; SIMOEN, 2002; SROUR; MCGARRITY, 1988).

According to Fig. 2.3 (a), the plasma-like track, originated by ion interaction in a reverse biased PN junction, distorts the depletion layer in the metallurgical junction in such a way that it propels equipotential regions into a form of cylindrical funnel, which has duration of the order of 1 ns or less (ROCKETT, 2004). In these regions, the higher electric

field moves electrons to the depletion layer and the holes to the silicon bulk (OHRING, 1998), causing an additional transient current pulse (ICR), whose behavior is illustrated in Fig. 2.3 (b).

Figure 2.3: a) The ion path. b) The main funnel components and the related transient current pulse.



Source: Adapted from (ROCKETT, 2004).

According to the literature, the post interaction of high-energy particle with MOS devices, in the sensitive regions, is usually analyzed by the sum of drift (or conduction component) and diffusion component (MUNTEANU; AUTRAN, 2008; ROCKETT, 2004), pointed out in Fig. 2.3 (a). The integral over time of this transient current, expressed in (2.4), gives the total spurious charge in the silicon structure (Qt) (BARTRA; REIS, 2014),

$$Q_t = \int_0^\infty I_0 \left(e^{-t/\tau_f} - e^{-t/\tau_r}\right) dt, \tag{2.4}$$

$$\text{with } I_0 = q \cdot \bar{\mu} \cdot N \cdot E_0 \cdot \ sec\, \theta, \tag{2.5}$$

$$\text{and } \tau_f = \left[\bar{\mu} \cdot \frac{\partial E}{\partial X}\right]^{-1}. \tag{2.6}$$

Where I_0 is the current generated by the charges; τ_r and τ_f are the rise/fall time of transient current, respectively; q is the electron charge; $\bar{\mu}$ is the mean carrier mobility; E and E_0 are, respectively, the electric field and its value at position $X = 0$, and θ the incident ion hit angle, depicted in Fig. 2.3 (a).

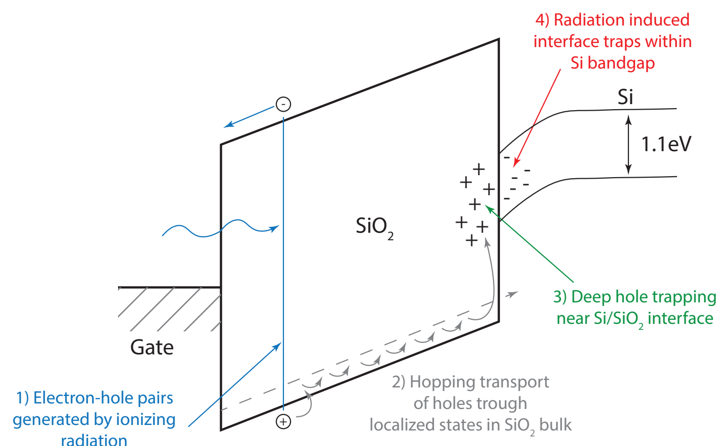
Finally, there are two main metrics to qualify SEEs: the minimum amount of charge necessary to induce an upset (Q_{crit}), and the rate at which occurs an upset, referred as Failure in Time (FIT), expressed in number of failures per 10^9 hours of operation

(MUNTEANU; AUTRAN, 2008).

2.3 Total Ionizing Dose (TID)

For TID effect, the cause is fundamentally the same as for SEEs, i.e., the generation of electron and hole pairs. Yet, in this case, it's a long-term and cumulative effect. While the ionizing radiation hits the oxide regions, such as the gate-oxide (SiO_2), the electric field, inherently existent due to device bias, may disrupt electronic bounds transporting the generated carriers. Through this process, as depicted in Fig. 2.4, the electrons, which have a higher mobility, $(\approx\ 20\,cm^2/V\cdot s)$ are removed from the dielectric, leaving the less mobile holes $(\approx\ 2\cdot 10^{-5}\,cm^2/V\cdot s)$ in the oxide (SROUR, 1982; OLDHAM et al., 1987; SROUR; MCGARRITY, 1988; ANDREOU et al., 2015; VAZ; WIRTH, 2015).

Figure 2.4: Energy band diagram for charge generation and charge transport in SiO_2.



Source: Adapted from (ANDREOU et al., 2015).

The holes within SiO_2 experiment a stochastic hopping transport through localized states toward the cathode direction, until they become trapped near the SiO_2/Si interface. This positive (and accumulated) charge near the interface between the dielectric and silicon bulk may consequently induce the formation of an inversion layer in the channel region (ANDREOU et al., 2015).

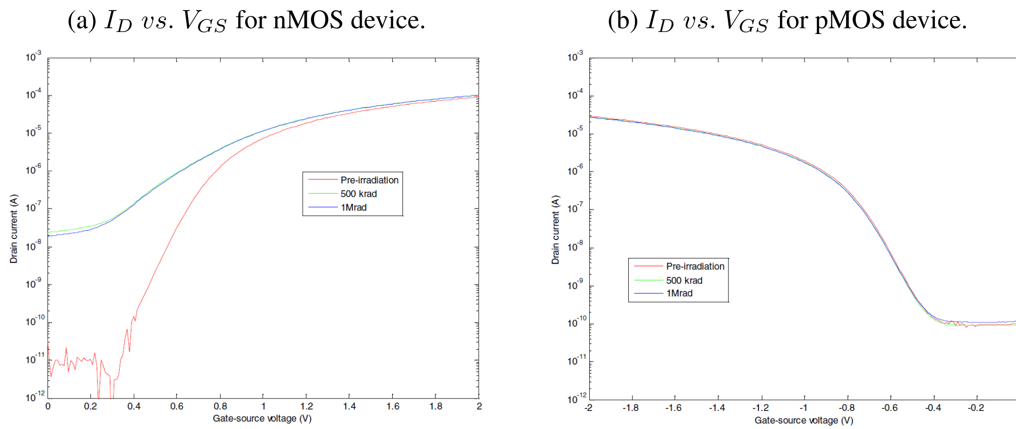
The presence of this positive parasitic charge has observable effects, such as a threshold voltage shift for the device (SROUR, 1982; OLDHAM et al., 1987), increasing the subthreshold voltage swing (MCLAIN et al., 2009) and the leakage current (intra- and inter-device) (SROUR, 1982; VAZ; WIRTH, 2015; OLDHAM et al., 1987; VAZ, 2015; CLAEYS; SIMOEN, 2004), reducing mobility (CLAEYS; SIMOEN, 2004), and

increasing flicker noise (ANELLI, 2000; VAZ, 2015).

Figure 2.5 shows an example of the transfer function (I_D $vs.$ V_{GS}) for n and pMOS devices designed with minimum DRC features (in referred case $W = L = 0.42$ μm) (GREIG et al., 2013). The presented cases are shown in typical conditions for pre- and post-irradiation up to 500 $krad$ and 1 $Mrad$. As can be observed, the effect of increase in leakage current is much more prominent in nMOS (index (a)) than in pMOS devices (index (b)) since the accumulation of positive charge has a negative (decreasing) impact on leakage current (ANELLI, 2000).

Figure 2.5: Transfer function (I_D $vs.$ V_{GS}) for n,pMOS devices in typical conditions (pre-irradiated and post-irradiated up to 500 $krad$ and 1 $Mrad$).

(a) I_D $vs.$ V_{GS} for nMOS device. (b) I_D $vs.$ V_{GS} for pMOS device.



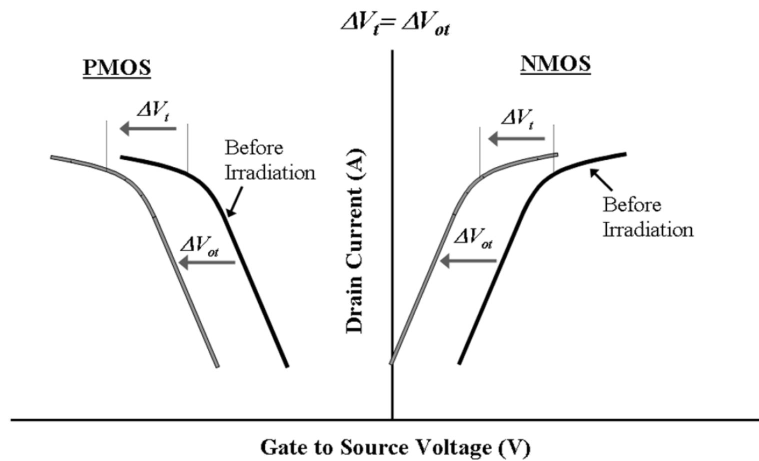
Source: From (GREIG et al., 2013).

In the perspective of ΔV_{th} the shift occurs in a negative way; analyzing Fig. 2.6, which exhibits the output DC characteristic (I_D $vs.$ V_{GS}) for both n,pMOS devices (BARNABY, 2006). In other words, for a fixed I_D, the irradiation tends to lead the V_{GS} to a more negative value.

The transistor scaling reduces the dielectric volumes so the total amount of parasitic trapped charge is reduced as well. Therefore, the scaling down of device geometries intrinsically reduces the threshold voltage deviations (ΔV_{th}). Related works (SAKS; ANCONA; MODOLO, 1984) suggest that oxide thickness (t_{ox}) above 20 nm has a quadratic dependence on ΔV_{th} (i.e., $\Delta V_{th} \propto t_{ox}^2$), rapidly decreasing otherwise, (i.e., $\Delta V_{th} \propto t_{ox}^n$ with $n > 2$).

Nonetheless, despite quantum tunneling effect (in which the holes are removed outside oxide volumes (BENEDETTO et al., 1985)), the literature addresses that for t_{ox} below 2.2 nm (which occurs in gate lengths of about 240 nm) the ΔV_{th} related to ionizing radiation can be neglected (FACCIO et al., 2008; KLOUKINAS et al., 1998).

Figure 2.6: Threshold voltage deviation for n,pMOS devices before and after irradiation.



Source: From (BARNABY, 2006).

As a final consideration, for large dose rates, i.e., near than $1\ Mrad(SiO_2)$ the number of trapped holes tends to saturate (FB, 1987). For such doses, in case of n-channel devices, by expanding the behavior illustrated by Fig. 2.6 a turnaround in threshold voltage deviation is observed.

Thus, a “shifting back” in the positive V_{th} direction occurs at increasing dose levels. For p-channel devices, negative biased at V_{GS}, the interface trapped charge continues increasing, and, therefore, continuing with a negative shift in its V_{th}.

To a more detailed physical phenomena involved for large dose rates, I invite the reader to consult (FB, 1987).

2.4 Summary and Discussion

This Chapter briefly introduced the basic concepts related to the interaction of ionizing radiation with bulk CMOS materials, discussing how it affects their characteristics as a consequence of generated $\bar{e}/h$ pairs along its trajectory.

Depending on the energy of the incident particle or whether the device is in a long term exposure to such ions, two main types of effects may occur; a transient upset (i.e., a momentary voltage spike) at certain device’s regions, or even permanent damages when occurring permanent changes in their physical components.

Indeed, the most sensitive regions to radiation effects that primarily cause failures on MOS devices are the insulating layers and the reversely biased PN junctions. Where even the accumulation of trapped charges or its migration degrade device’s parameters

reducing its reliability and expected lifetime.

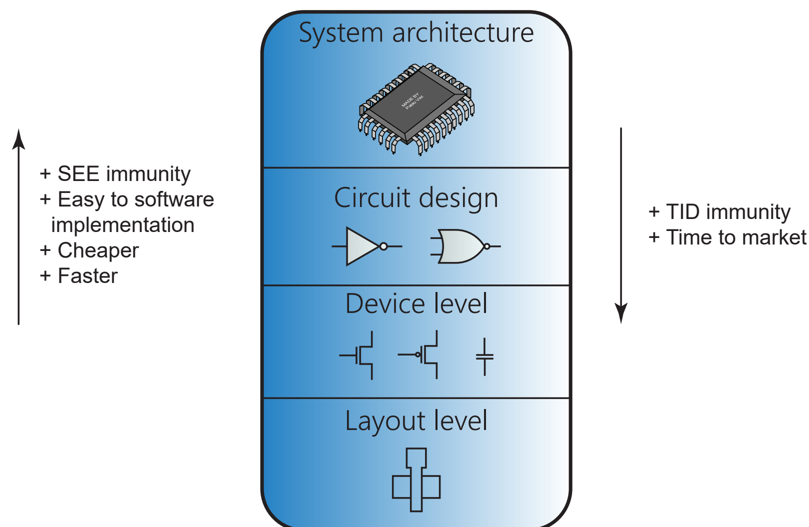
In the next Chapter, it is discussed how to improve the radiation tolerance of MOS devices laid out in a commercial fabrication process.

3 RHBD LAYOUT TECHNIQUES

3.1 Introduction

As illustrated in Fig. 3.1, RHBD mitigation techniques can be applied through all circuit abstraction levels. In the figure, the left and right arrows represent what is better suited for each abstraction level in terms of RHBD techniques.

Figure 3.1: Quantitative insight of hardness degree in terms of circuit abstraction level.



Source: Author.

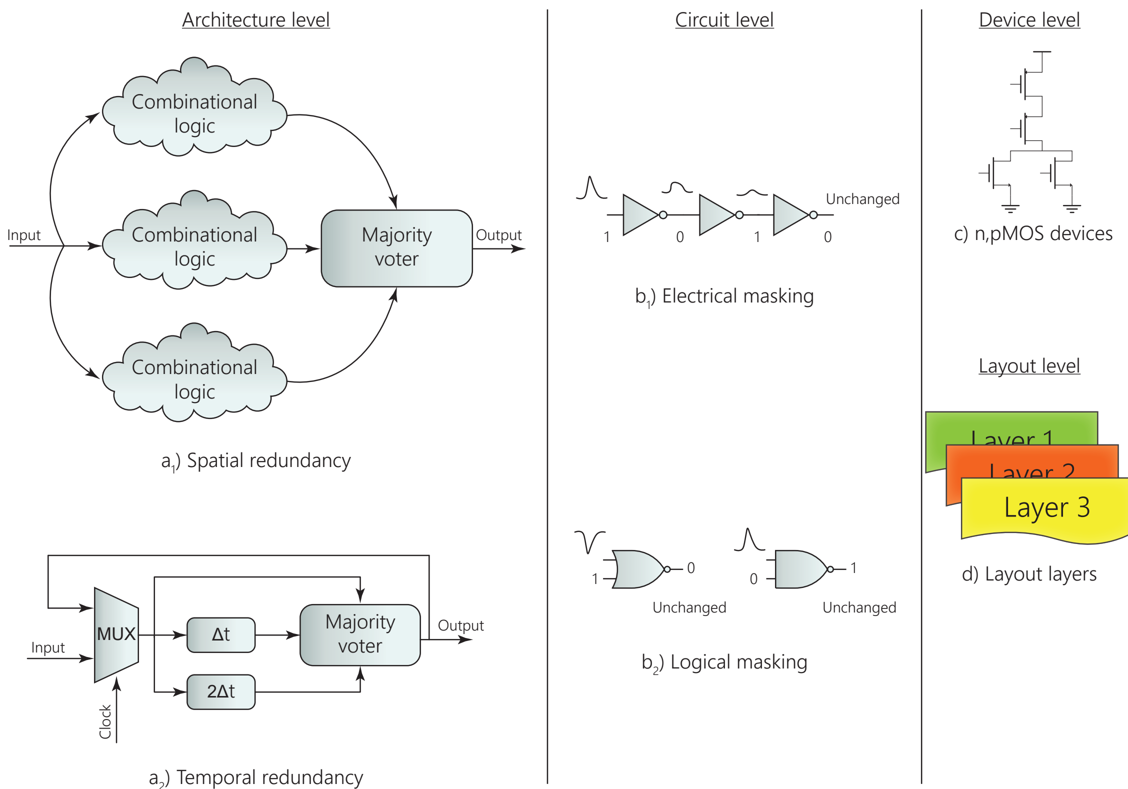
For example, the left arrow indicates that higher abstraction levels tend to have cheaper and faster to implement solutions, since many techniques involve redundancies and voters schemes acting directly on RTL code, easily providing hardening against SEEs.

In contrast, the approach to hardening a circuit against TID, in a standard fabrication process, usually requires modifications at the layout level. Thus, requiring the post-fabrication and characterization of these hardened devices (i.e., the new proposals) in order to be further used in the design flow automation. This process increases design time, costs and, consequently, time to market.

Figure 3.2 summarizes the most fundamental concepts involved in Radiation Hardening on the three major abstraction levels.

In case of spatial redundancy (a_1), the key idea is that if any disturbances occur in a logic block, the parallel processing of the same signal promotes a majority vote between all outputs processed by other multiple physical instances. Besides, it is noteworthy that the voter ought be carefully designed to avoid propagating an error itself; as well as the

Figure 3.2: Summary of emblematic concepts of mitigation techniques embedded at different abstraction levels.



Source: Author.

physical placement of these circuit copies should be laid out as far as possible from each other in order to reduce the probability of a double error occurrence (e.g., caused by a heavy ion crossing a large silicon area). To mitigate such an occurrence (i.e., when occurring multiple bit-flips), a temporal redundancy (a_2), in which a signal delay (supposed to be in the order of strikes settle down $\approx$ hundreds of ps), is proposed to guarantee that a single event does not induce a voting error.

At a circuit level, the electrical masking (b_1) attenuates the transient pulses with bandwidths higher than the CMOS cutoff frequency (i.e., transition frequency - f_T), by reducing its amplitude until it, eventually, becomes a spurious signal that is neglected by the circuit (MUNTEANU; AUTRAN, 2008). Still at a circuit level, the logical masking (b_2) lies in the combinational logic *force* where, as exemplified by the NOR gate, the controlling state (i.e., one input tied to high - V_{DD}) forces the output to be unchanged, independently of the other input signal (analogously, the same applies to other logic gates with equivalent truth table, as the NAND gate with one input tied to low - V_{SS}) (MUNTEANU; AUTRAN, 2008).

On device level, a specific network arrangement can be adopted, i.e., a change

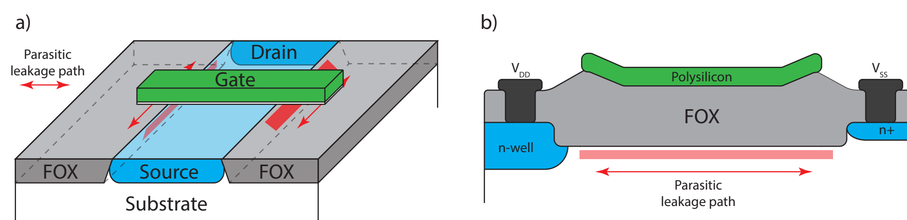
in the way of n,pMOS devices are connected to implement the same logic function (MUNTEANU; AUTRAN, 2008). Finally, proposing changes at the layout level, it is possible to substantially reduce not just SEEs, but also TID effects by avoiding critical sensitive regions responsible, for example, for the increase in the leakage current. This is discussed in the upcoming Sections 3.2 and 3.3.

3.2 Guard Rings

Submicron and deep submicron commercial CMOS technologies have reduced geometry volumes. In these technologies are observed smaller space/charge regions to collect, store, and process data. The movement of charges, in these reduced volumes, is deleterious when a device operates in higher frequencies. Thus, the leakage current has been the first addressed topic to be prevented (or reduced).

As depicted in Fig. 3.3 (a) and (b), the lateral field oxide (FOX) regions introduce susceptible areas for charge buildup when hole trapping occurs. In these regions, where the FOX lateral isolation, in LOCOS (or STI) process, experiment high mechanical stress, a leakage current path may form between the source and drain areas of the same device, as represented by the red regions in Fig. 3.3 (a); or between n-well layers of adjacent devices, depicted in (b).

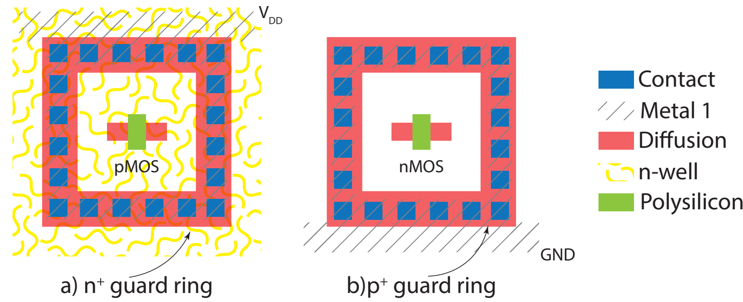
Figure 3.3: Representative cross section of leakage current path between: a) source and drain of the same device (intra-device), and b) adjacent n-well regions of different devices (inter-device).



Source: Adapted from (LEE; LEE, 2013).

In these cases, considering standard commercial fabrication processes, the use of guard rings, Fig. 3.4, can substantially mitigate the leakage current underneath isolation oxides between adjacent devices and n-well layers (inter-device leakage), isolating all n^{+} diffusions that are at different potentials (MCLAIN et al., 2009; KLOUKINAS et al., 1998).

Figure 3.4: Guard rings layout example for: a) pMOS and b) nMOS devices.



Source: Author.

3.3 Enclosed Layout Transistor (ELT)

For intra-device leakage path (i.e., the parasitic current which flows between the diffusion areas of an individual device), the proposal of an Enclosed Layout Transistor (ELT) entails the elimination of the transition region where the polysilicon layer extends over the well-to-substrate boundary, i.e., the red area in Fig. 3.3 (a), (ANELLI, 2000; MCLAIN et al., 2009; SNOEYS; GUTIERREZ; ANELLI, 2002).

Under those circumstances, a myriad of possibilities exist for enclosing diffusion areas, allowing to eliminate leakage paths, as depicted in Fig. 3.5 from (a) to (f). These are some of the classical enclosed gate topologies, largely adopted in literature. Once literature is vast and some topologies may have slight variations, the classical topologies can be generally categorized as follows:

a) Circular (or Radial): (GIRALDO; PACCAGNELLA; MINZONI, 2000; LóPEZ et al., 2009)

b) Rectangular (or Square): (GIRALDO; PACCAGNELLA; MINZONI, 2000; XUE et al., 2011)

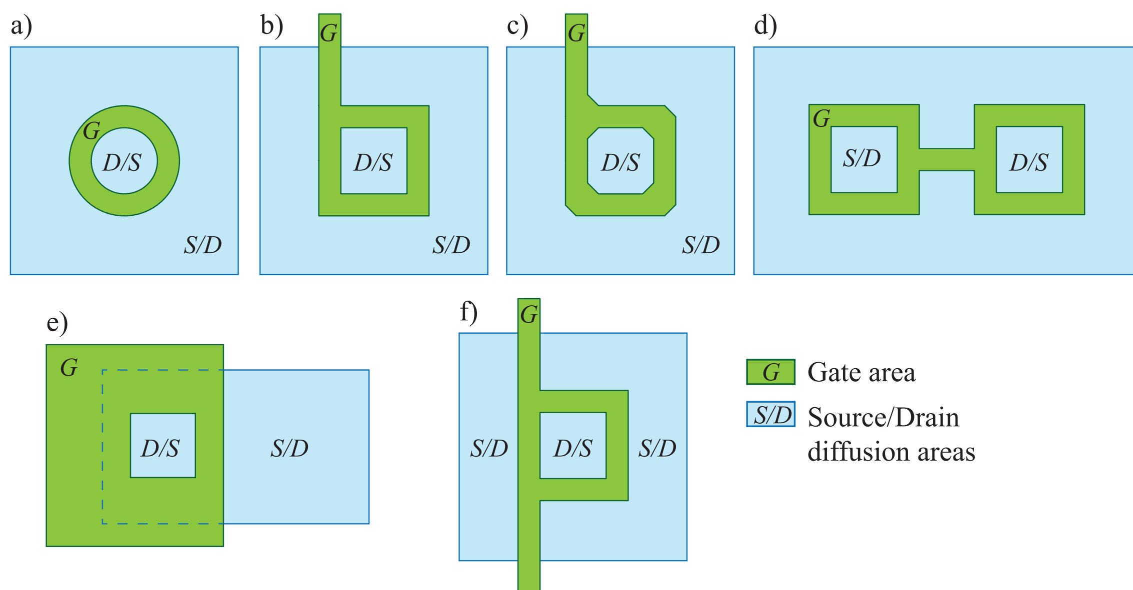
c) Rectangular Broken Corners (or Hexagonal; Annular): (ANELLI et al., 1999; ANELLI, 2000; GIRALDO; PACCAGNELLA; MINZONI, 2000; NOWLIN et al., 2005; CHEN; GINGRICH, 2005; MCLAIN et al., 2009; FLORES-NIGAGLIONI et al., 2015)

d) Dog-bone: (SNOEYS; GUTIERREZ; ANELLI, 2002; LIMA, 2006)

e) Ringed-source: (NOWLIN et al., 2005; MCLAIN et al., 2009; XUE et al., 2011)

f) Under-lap (or Dual-drain Ringed-source): (NOWLIN et al., 2005; MCLAIN et al., 2009)

Figure 3.5: Enclosed gate geometries named as: a) Circular, b) Rectangular, c) Rectangular Broken Corners, d) Dog-bone, e) Ringed-source, and f) Under-lap.



Source: Adapted and complemented from (MCLAIN et al., 2009).

Nonetheless, each topology has its own advantages and disadvantages. The Circular does not comply with many lithography processes; the Dog-bone has the largest area overhead; both Ringed-source & Under-lap require less area than the Dog-bone, but more area when compared to the Rectangular or even to the Rectangular Broken Corners.

In terms of gate style, considerable efforts have been done to investigate and characterize the layout geometry named as *diamond MOSFET* (GIMENEZ, 2016; SEIXAS et al., 2017; SEIXAS et al., 2019). In this structure, the gate is designed to use the corner effect in the longitudinal direction of the channel.

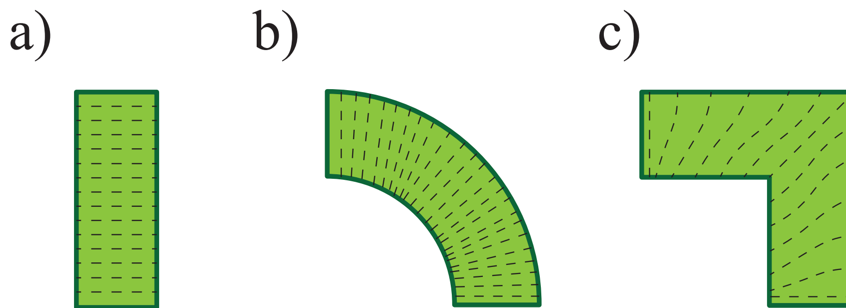
As authors suggest, this layout style has better electrical performance than standard devices and it is also capable to enhance its intrinsically TID tolerance. Nonetheless, in order to provide a more fairly comparison, this work focuses on clear *enclosed* gate disposals.

Thus, between the aforementioned geometries, which are widely investigated in the literature, this work adopted the Rectangular and Rectangular Broken Corners solutions. The main reasons for this choice are the fact that they tolerate doses up to 30 $Mrad(SiO_2)$ (LEE; LEE, 2013); provide the possibility of a re-usable design (such as in Lambda units, scalable for different technology nodes); comply with the design rules of most, if not all, Process Design Kits (PDKs).

3.3.1 Effective (W/L) aspect ratio prediction problem

The classical gate topology, presented in Fig. 3.6 (a), which has single, straight polysilicon stripe, allows for a simple and direct acquisition of its width (W) and length (L), because the electric field is approximately uniform under the gate when the device is biased.

Figure 3.6: Electric field lines under the gate on topologies: a) Standard, b) Circular, and c) Rectangular.



Source: Author.

In Circular geometries, shown in Fig. 3.6 (b), the uniform electric field under the gate allows for an analytical model of the (W/L) ratio of the transistor when, for instance, cylindrical coordinates are employed for basic long channel equations (GIRALDO; PACCAGNELLA; MINZONI, 2000).

Nonetheless, for other topologies, the acquisition of this ratio is not so trivial, mainly because there is not a clear physical equivalent to the width of the transistor, especially due to the electric field fringing effects when the gate has acute angles, as shown, for example, in Fig. 3.6 (c).

Nowadays, there are no available commercial Process Design Kits (PDKs) with native standard cells employing ELTs capable of performing an accurate prediction neither for W nor for L. Thus, the use of ELTs leads to challenges on the estimation of an effective (W/L) aspect ratio. Providing a reasonable estimation is a key factor in order to obtain an accurate transistor output and transfer the curves $(I_D\ vs.\ V_{DS})$ and $(I_D\ vs.\ V_{GS})$.

3.3.2 Effective (W/L) aspect ratio prediction methods

Enclosed gate devices have been researched for decades. They were first proposed in the end of the 70's by the RCA Solid State Division (DINGWALL; STRICKER, 1977),

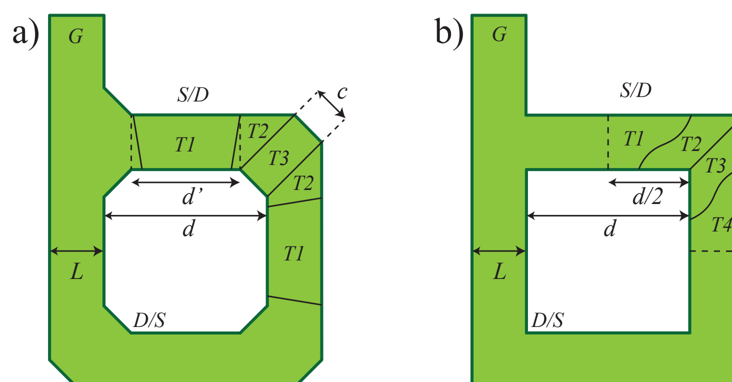
being called C^2L at the time. From that time, the technology scaling and the advances in modeling and simulation of integrated circuits, and components as well, have been leading us to a better understanding of the physical phenomena involved in ultra-scaled CMOS devices, such as quantum effects, tunneling current and ballistic operation (MUNTEANU; AUTRAN, 2008).

In this context, researchers have made a substantial contribution to the High Energy Physics community, which has investigated and characterized commercial devices under ionizing radiation (ANELLI, 2000).

In the field of RHBD, the works of Anelli and Giraldo (ANELLI et al., 1999; ANELLI, 2000; GIRALDO; PACCAGNELLA; MINZONI, 2000) were pioneers in the investigation of ELT device matching. Through several test chips, accurate models to predict the aspect ratio (W/L) were proposed for these devices.

Based on these referred works, in order to provide an analytical methodology to calculate (W/L) in our case study, the gate structure was divided into linear contributions. Each of these parts with its own drain contribution, being the total (W/L) the sum of all individual parts, as shown in Fig. 3.7 (a) and (b) by transistors 1 to 3 ($T1$ to $T3$) and $T1$ to $T4$, respectively.

Figure 3.7: (W/L) prediction methods named as: a) Sum of parallel transistors and b) Edge and Corner transistors.



Source: Adapted from a) (ANELLI, 2000) and b) (GIRALDO; PACCAGNELLA; MINZONI, 2000).

In this methodology, the extraction of the experimental (or simulated) (W/L) values comes from the comparison of the I_D $vs.$ V_{DS} characteristics between enclosed and standard devices with the same L (GIRALDO; PACCAGNELLA; MINZONI, 2000). Thus, the I_D expression can be calculated by integrating the resistance of the infinitesimal element along the channel on the hypothesis of current continuity (no generation or recombination inside the channel) and by integrating the electric field under the gate.

In the analytical model for rectangular devices, which has been derived from a 2-D analysis of the electric field magnitudes under the gate, the distribution of the electric field lines are obtained by solving the electrostatic equations in complex coordinates (through the conformal mapping method). The resulting electric field lines allow to separate the gate topology in several equivalent parts. After the decomposition, the polygonal regions were grouped together, assuming a similar behavior in the electric field lines, preserving the current continuity.

From this analysis, the integration of current contributions leads to equations (3.1) and (3.2) for Rectangular (Rec) and Rectangular Broken Corners (Rec BC) devices, respectively.

$$\left(\frac{W}{L}\right)_{eff}^{Rec.} = 4 \cdot 2 \cdot \left(\left(\frac{W}{L}\right)_{eff}^{T1} + \left(\frac{W}{L}\right)_{eff}^{T2}\right) \tag{3.1}$$

$$\left(\frac{W}{L}\right)_{eff}^{Rec.BC} = 4 \cdot \left(\frac{W}{L}\right)_{eff}^{T1} + 2 \cdot k \cdot \left(\frac{W}{L}\right)_{eff}^{T2} + 3 \cdot \left(\frac{W}{L}\right)_{eff}^{T3} \tag{3.2}$$

For a complete and more detailed explanation about the aforementioned methods, I invite the reader to consult the original references (ANELLI, 2000) for SPT and (GIRALDO; PACCAGNELLA; MINZONI, 2000) for ECT.

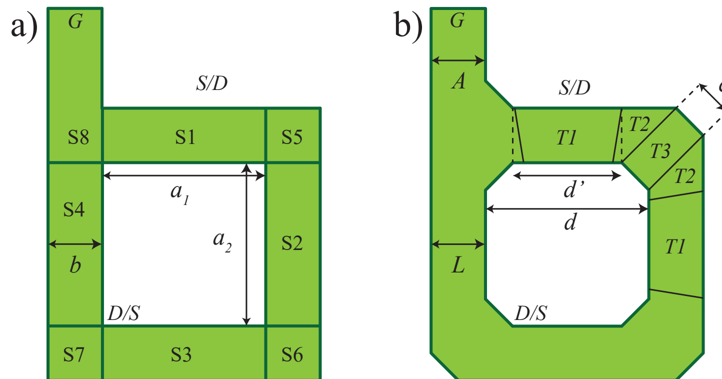
In the final analysis, it is noteworthy that the current of ECT method is only expressed in terms of $T1$ and $T2$ due to the symmetry. In the SPT, the parameter k is geometry dependent and has the value 3.5 for channel lengths smaller than $0.5\mu m$ and the value 4 otherwise; and, the $T3$ contribution is only multiplied by 3 because the tail of the gate substantially reduces the drain current contribution at that point.

More recently, the model proposed by (XUE et al., 2011) introduces a computation inexpensive expression for (W/L). This model also computes the gate geometry as a sum of several parallel transistors, as shown in Fig. 3.8 (a) from $S1$ to $S8$ and modeled by 3.3. The value C_{ab} is an internal method's variable and represents the corner contribution which may vary with the down-scaling of the devices.

$$\left(\frac{W}{L}\right)_{eff} = \frac{2a_1 + 2a_2}{b} + C_{ab} \tag{3.3}$$

There are still some references with slight variations from (3.2) as in (CHEN;

Figure 3.8: (W/L) prediction methods from references: a) (XUE et al., 2011) and b) (CHEN; GINGRICH, 2005).



Source: Adapted from a) (XUE et al., 2011) and b) (CHEN; GINGRICH, 2005).

GINGRICH, 2005), show in Fig. 3.8 (b), in which the tail of the gate exists as a variable value (A). In this case, the constant term $(2 \cdot k)$ preceding the contribution $T2$ in (3.2) is expressed as (K) in (3.4), which, on its turn, is given by $K = 8 - A/L$.

$$\left(\frac{W}{L}\right)_{eff}^{Rec.BC} = 4 \cdot \left(\frac{W}{L}\right)_{eff}^{T1} + K \cdot \left(\frac{W}{L}\right)_{eff}^{T2} + 3 \cdot \left(\frac{W}{L}\right)_{eff}^{T3} \tag{3.4}$$

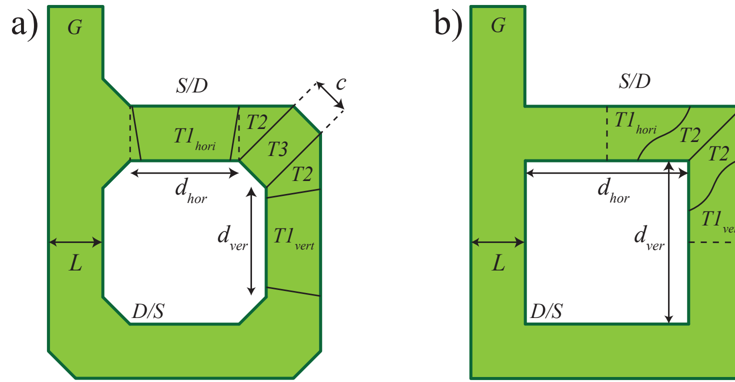
At last, there is still another group of equations that aims to predict the drain current, as in (LOPEZ et al., 2009). Nonetheless, since only the drain current is estimated, it is not possible to use BSIM equations nor to make a direct comparison between other models. For this reason, this work focuses on methodologies to predict the ratio (W/L).

Under these circumstances, this work takes into consideration the same analysis discussed for topologies shown in Fig. 3.7 (a) and (b). Additionally, it is proposed to explicit the horizontal and vertical internal diffusion distances, variables (d_{hor}) and (d_{ver}), respectively, in order to particularize their linear contributions, as represented in Fig. 3.9 (a) and (b).

The purpose of these explicit horizontal and vertical components is to enable the use of a wider range of aspect ratios, i.e., not only square symmetry but also rectangular symmetry. This is of particular importance to the layout phase, in order to satisfy cell pitch in layout template standardization, in which cells have a fixed height and a variable width. Additionally, to the best of our knowledge, this degree of freedom in a design was applied for the first time in the generation of custom RHBD cell library (VAZ et al., 2018).

Thus, (3.5) and (3.6) are adopted throughout this work. Moreover, also throughout this work, the distance c (i.e., the cathetus related to $45°$ corner), shown in Fig. 3.9 (a) is

Figure 3.9: (W/L) prediction methods with horizontal and vertical explicit variables for a) Sum of parallel transistors and b) Edge and Corner transistors.



Source: Author.

conventionalized to be the same for each one of the four corners of internal gate edges of the proposed annular devices, unless indicated otherwise.

$$\left(\frac{W}{L}\right)_{eff}^{Rec.} = 4 \cdot \underbrace{\left[\left(\frac{W}{L}\right)_{eff}^{T1_{hori}} + \left(\frac{W}{L}\right)_{eff}^{T1_{vert}}\right]}_{\left(\frac{W}{L}\right)_{eff}^{T1}} + 8 \cdot \left(\frac{W}{L}\right)_{eff}^{T2} \tag{3.5}$$

$$\left(\frac{W}{L}\right)_{eff}^{Rec.BC} = 2 \cdot \underbrace{\left[\left(\frac{W}{L}\right)_{eff}^{T1_{hori}} + \left(\frac{W}{L}\right)_{eff}^{T1_{vert}}\right]}_{\left(\frac{W}{L}\right)_{eff}^{T1}} + 2 \cdot k \cdot \left(\frac{W}{L}\right)_{eff}^{T2} + 3 \cdot \left(\frac{W}{L}\right)_{eff}^{T3} \tag{3.6}$$

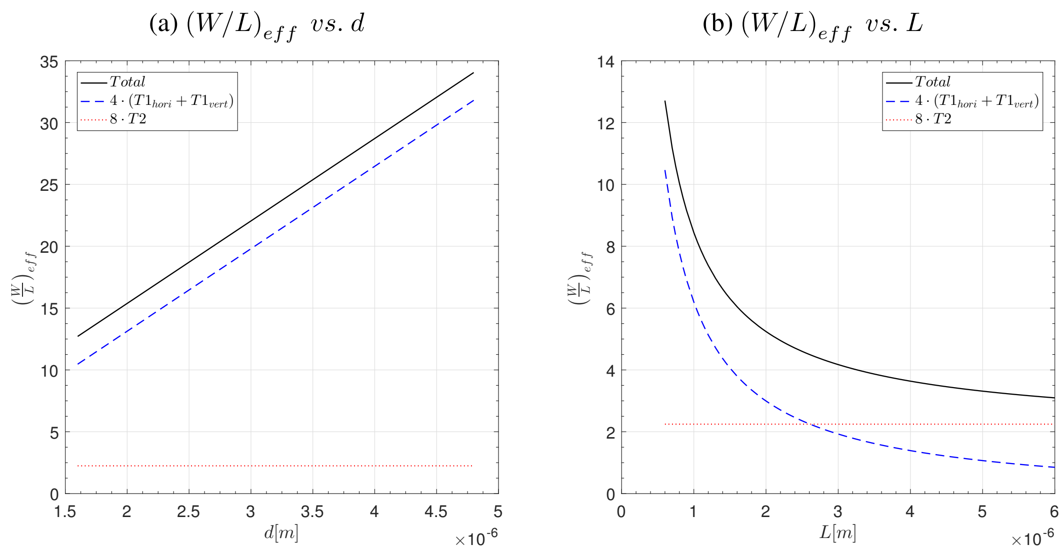
The conceptual support to validate the preceding equations lies in the fact that, as authors claim, each transistor has a *linear* contribution. For this reason, in the context of a cell library, in which each cell should consider fixed height and variable width, it is convenient to explicit these two contributions (i.e., horizontal and vertical) to better fit at the layout phase.

The curves in Figs. 3.10 and 3.11 summarize each individual device's contribution in terms of their (W/L), respectively for Rectangular and Rec. BC. In Figs. 3.10 and 3.11 index (a), it is possible to verify the linear increment from $T1$, $T2$ and $T3$ (expressed in (3.5) and (3.6)). Similarly, in Figs. 3.10 and 3.11 index (b), it is possible to observe the decrescent trend of total (W/L) when increasing the channel length. It is noteworthy that the "discontinuity" seen in Fig. 3.11 (b) (in the term $2K(T2)$) occurs because an internal

method's variable increase their fitting value when the channel length becomes greater than $500\ nm$.

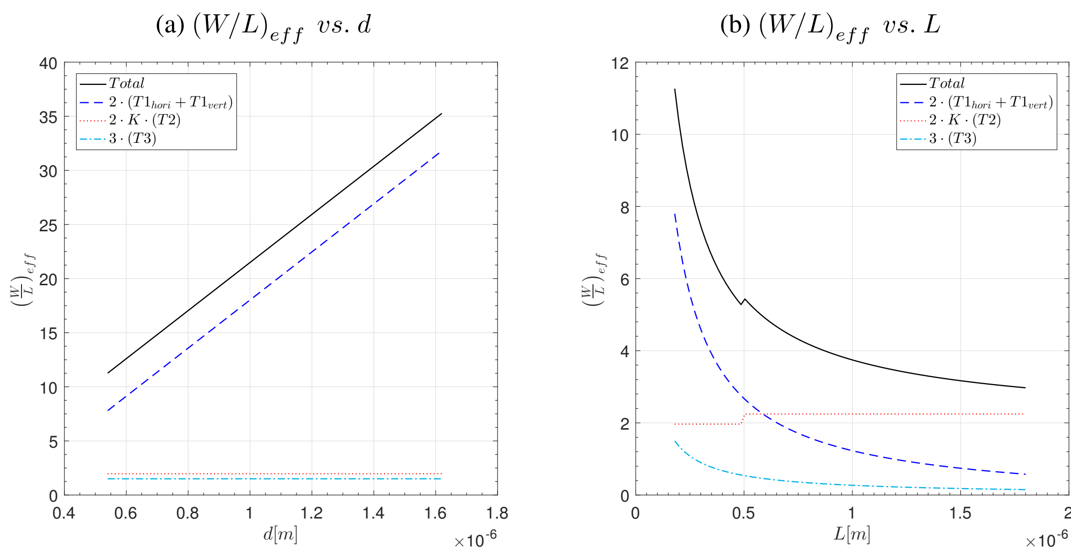
Figure 3.12 summarizes all related methods in terms of their (W/L) contributions. The index (a) presents the Rectangular method's compilation and (b) the RecBC.

Figure 3.10: ELT Rectangular and its (W/L) contributions.



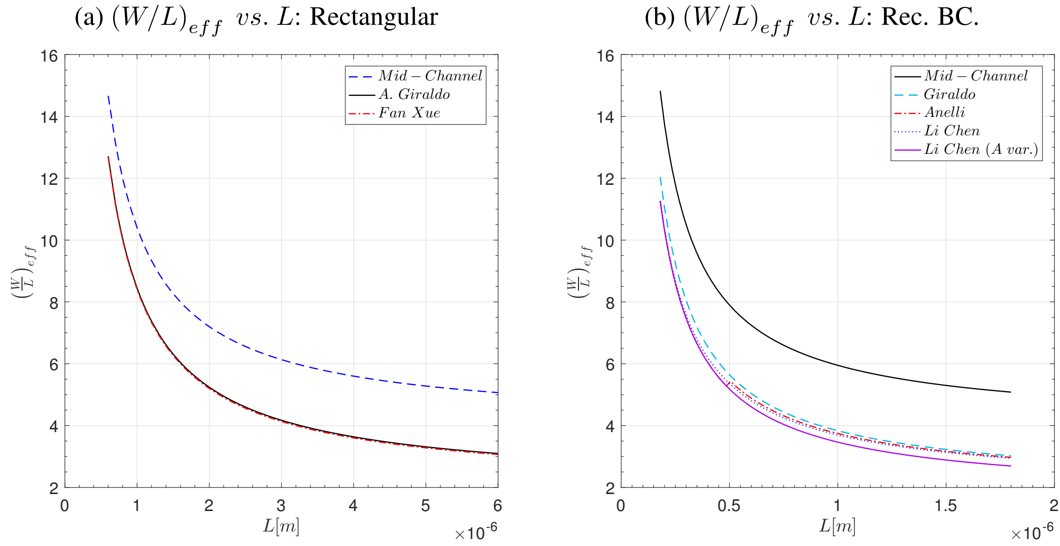
Source: Author.

Figure 3.11: ELT Rectangular BC and its (W/L) contributions.



Source: Author.

Figure 3.12: ELT and its (W/L) contributions for all related methods for: a) Rectangular and b) Rectangular Broken Corners.



Source: Author.

3.3.3 Effective (W/L) aspect ratio limitations

In an Annular device, while it is possible to reduce its (W/L) ratio by increasing the gate length, the required silicon area grows exponentially, with an asymptotic behavior to the value of 2.26 (LEE; LEE, 2013). Figure 3.13 illustrates this behavior for Rectangular Broken Corners (RecBC) and Rectangular geometries. The curves were obtained through simulation using their analytical models, (3.2) and (3.1), respectively. In these cases, the aspect ratio of 3 in SPT is achievable with almost 10 times of the minimum channel length (ANELLI, 2000).

Calculating the (W/L) for 10 and 20 times the channel length leads to:

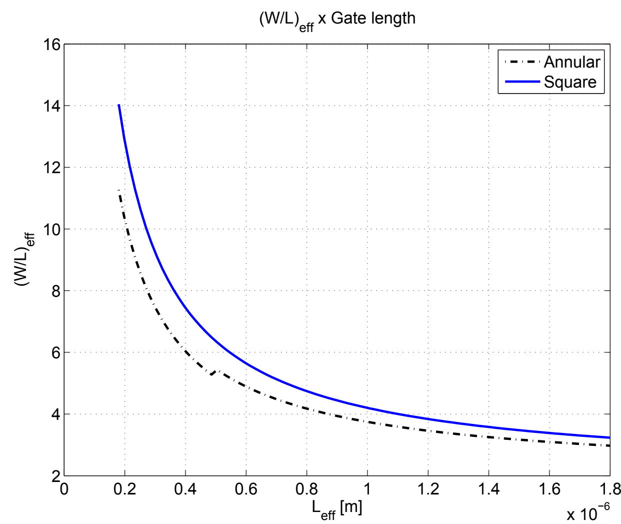
$10 \cdot L_{min} \rightarrow \left(\frac{W}{L}\right)_{annular} = 2.97$ and $\left(\frac{W}{L}\right)_{square} = 3.23$

$20 \cdot L_{min} \rightarrow \left(\frac{W}{L}\right)_{annular} = 2.33$ and $\left(\frac{W}{L}\right)_{square} = 2.61$

3.3.4 Source/drain asymmetry

When the channel region operates in strong inversion, the drain/source voltage (V_{DS}) may strangle the channel region (i.e., the distance between the drain/source and

Figure 3.13: Effective (W/L) aspect ratio for Rec.BC (Annular) and Rectangular (Square) devices in $180\ nm$.

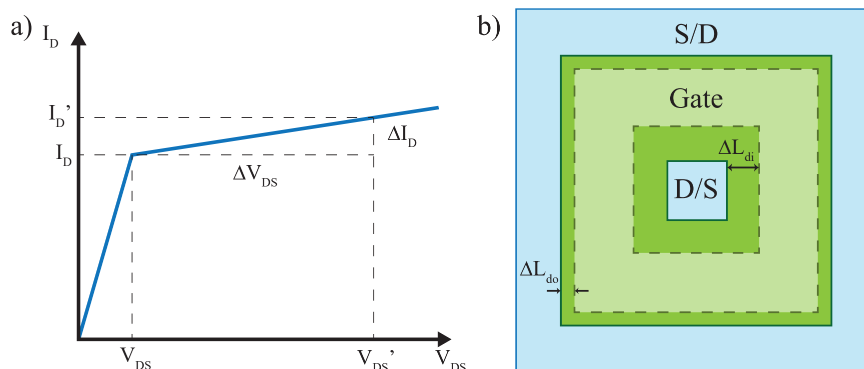


Source: Author.

where the inversion layer charge almost reach zero density). This effect, known as pinchoff, causes the distance between drain and source to be reduced by (ΔL)(TSIVIDIS; MCANDREW, 2011).

These variations, related to channel length modulation (CLM), give origin to non-idealities in the output transfer function $(I_D\ vs.\ V_{DS})$, which can be seen in Fig. 3.14 (a) as the slope comprised for ΔI_D and ΔV_{DS}. This slope refers to the conductance of the output devices (G_{out}) (also known as the source-drain conductance - g_{sd}), expressed in (3.7) (ANELLI, 2000; TSIVIDIS; MCANDREW, 2011).

Figure 3.14: a) Transfer function $(I_D\ vs.\ V_{DS})$ and b) Space/charge distribution for in and outside drain possibilities.



Source: Adapted from (ANELLI, 2000).

$$G_{out} = g_{sd} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS},V_{BS}=const} \tag{3.7}$$

Moreover, these variations in CLM correspond to a certain space/charge density distribution which, in Two-Edged (TE) devices, regarding its symmetry, the interchangeable source and drain terminals causes an equal slope. In other words, independently whether the drain or source is assigned to the left or right position, the pinchoff region should ideally be the same.

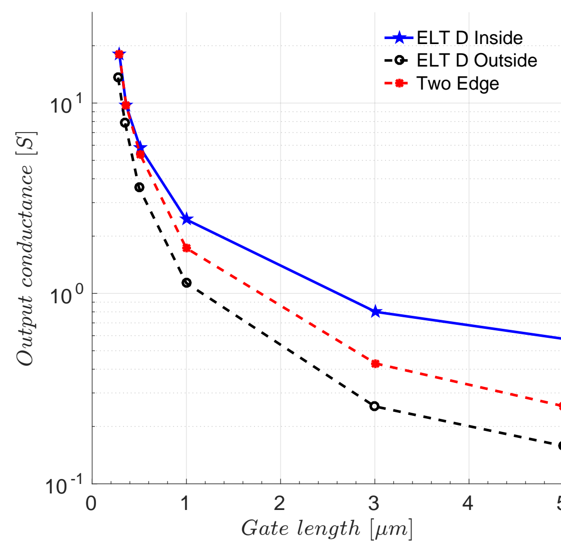
In ELT designs, the channel length variations are different when enclosing the drain or the source. As depicted in Fig. 3.14 (b), if the drain is enclosed, then the pinchoff region, represented for ΔL_{di}, should be higher (larger) than if the drain stands outside (ΔL_{do}). These 2-D different areas result in an equal 3-D carrier volumes (i.e., space/charge density distribution).

Indeed, when taking ΔL into account when calculating G_{out}, it is possible to verify that if ΔL increases, then the total G_{out} also increases, as expressed in (3.8) for an Rectangular device (ANELLI, 2000).

$$G_{out} = \frac{I_D}{\Delta V_{DS}} \cdot \frac{\Delta L_{i,o}}{L - \Delta L_{i,o}} \tag{3.8}$$

On this perspective, it is possible to surmise that if the drain is placed on the inner (enclosed) diffusion area, the output conductance should be higher (worse), which is not ideal. The curve presented in Fig. 3.15 corroborates this fact. It is possible to visualize the output conductance in terms of gate length variation for TE, as well as both drain inside and drain outside ELT devices.

Figure 3.15: Comparison between output conductance for Two-Edged device and ELT device for drain as inner and outer diffusion regions (ANELLI, 2000).



Source: Data plot from (ANELLI, 2000).

This case study also reveals that when gate length is increased, the difference between ELT and TE devices approximates the arithmetic mean between G_{di} and G_{do} (ANELLI, 2000).

However, due to a small area, the inner terminal capacitance is lower than the outer and, when a high frequency operation is desirable, the terminals with higher capacitance (outer diffusion regions) should be assign to fixed (or more stable) potentials, such as V_{DD} or V_{SS}. In this case, there is a clear tradeoff between speed and gain if is considered designing amplifiers (ANELLI, 2000). Thus, designers usually prefer to assign the drain inside.

A comparison between the transition times of inverter cells using TE and ELT devices with inside-placed drain was performed. Results indicate that the ELTs were up to 12% faster than the TE counterparts. Even though these devices were reasonably faster, the area penalty related to enclosing a gate geometry was at least 15% for a single transistor and 150% for an inverter cell. For more complex cells, the area overhead is expected to increase for ELT devices (VAZ; JUNIOR; WIRTH, 2015; VAZ; WIRTH, 2015).

3.4 Summary and Discussion

Techniques to harden a device against ionizing radiation effects can be applied through the entire IC design flow hierarchy: from the higher levels (e.g., system architec-

ture) to the basic building blocks or circuits, i.e., the single transistor.

To decide at which level(s) the technique(s) should be implemented is not a trivial task. It depends on several aspects, such as where the device will operate, how long it will operate and how many ions should cross the device in a given time interval (or unit area).

In a rough comparison, thinking the transistor of an entire DIE as a single brick of an entire building, a hardened wall can be built with various layers of bricks or by a more ingenious interlacing (with a minor number of them).

Nowadays, in technology nodes that are in the deep submicron range ($180\ nm$, $130\ nm$, $90\ nm$, $45\ nm$ and beyond), gate oxides are about $2\ nm$ thick. These thin gate oxides are almost immune to total ionizing dose effects. FOX lateral isolation, however, is about $100\ nm$ thick; in these oxides, TID effects may increase leakage path between source and drain, increasing leakage current (FACCIO et al., 2008; ANELLI, 2000).

In some cases, neither various layers of bricks (i.e., multiple redundancies or voters schemes) nor ingenious interlacing (i.e., place structures at different regions or designing sensors to detect current spikes) are sufficient to produce a circuit capable of properly operate in harsh environments, as, for instance, is required to be qualified for space and satellite applications.

Indeed, higher levels of tolerance are reached through a combination of many techniques. Independently of which abstraction level, what is quite inevitable to qualify some device as *radiation hardened* is to harden the basic building block of ICs, i.e., the single transistor. This task, when using a standard commercial fabrication process, is done by employing changes in the layout perspective.

The process of design full-custom cells is usually much more expensive and requires longer time to market. This mainly happens due to a practical implementation, fabrication, and, characterization of the new devices. Under these circumstances, this Chapter discussed different models to estimate the effective (W/L) aspect ratio, which is one of the major challenges - to estimate the device current when employing ELTs to harden a single transistor.

The state-of-the-art review spanned from widely adopted models to simplified equations that require less computational effort. Additionally, in order to simplify the current calculation in some devices with different enclosed distances (horizontal and vertical), a slight parameter modification was proposed.

The following Chapter proposes a general equation to calculate the gate sizes of n- and p-MOS devices and also the calculation of the aspect ratio between pull-up and down

networks (i.e., PN ratio).

4 SCHEMATIC DESIGN FLOW PROPOSAL

4.1 Introduction

This Chapter proposes a design methodology to calculate the gate sizes of any logic function. For this reason, a small group of cells are discussed as case analysis and the foundations necessary for the reader to compose a RHBD cell library of any complexity.

The optimization criteria adopted in this work is to achieve the minimum possible delay (i.e., time optimization approach). Thus, the Logical Effort (LE) method introduced by Ivan Sutherland *et al.* (SUTHERLAND; SPROULL; HARRIS, 1999) has been chosen to rule the gate sizing process.

Moreover, since standard commercial CAD tools do not recognize enclosed gate topology, they are unable to properly extract (or calculate) the device's W, L gate area, and its perimeter, when running electrical level simulations. Thus, from Section 4.2.1, additionally to the ELT's W and L, this work also proposes an update to source/drain diffusion areas and their perimeters in SPICE simulations.

4.2 Deriving Logical Effort equations

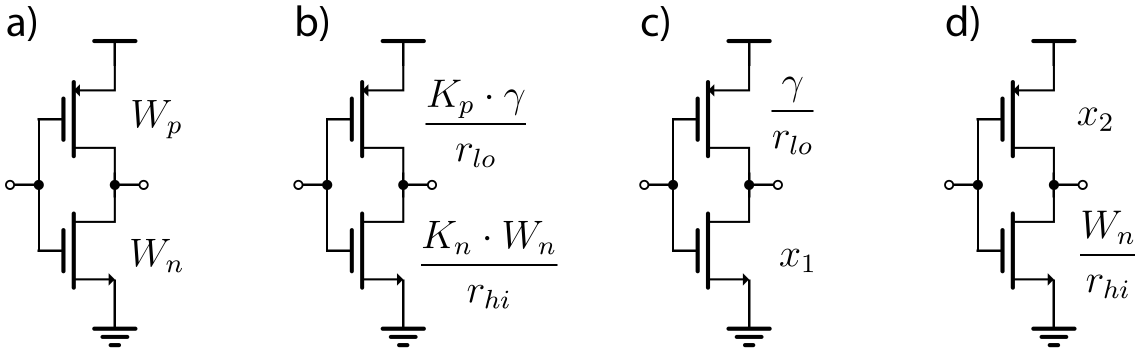
The theory of Logical Effort considers how difficult it is for a gate to drive its output, and how that is related to its delay. In this context, the minimum-sized inverter cell is referenced as the basic building block to achieve a technology independent delay model.

In the LE of an inverter cell, the ratio between the pMOS and nMOS widths is defined as gamma-ratio (γ). In this work, the specific value of γ that produces equal rise (t_{rise}) and fall times (t_{fall}) (i.e., balanced rise and fall drive strengths, also known as balanced inverter cell) is defined as mu (μ).

Figure 4.1 (a) illustrates a balanced inverter cell where the variables (W_n) and (W_p) represent the widths of an n- and a pMOS devices, respectively. In this case, it is expected the minimum channel length for both pull-up and pull-down networks where if the device is balanced, then $\gamma = \mu = W_p/W_n$.

When more than one device is connected in series between the output node and V_{DD} (or V_{SS}), the factor $K\ (S)$ is introduced. The term S represents the number of stacked device in series, and its magnitude represents the amount by which the width of each device has to be increased in order to produce the same output current as if only one device

Figure 4.1: LE variables of Inverter cells for: (a) Standard Inverter cell; (b) derived skewed version; (c) derived unskewed version - for equal rise resistance; and (d) derived unskewed version - for equal fall resistance.



Source: Author.

was connected. The subscript n or p in this factor (i.e., $K_n(S)$ or $K_p(S)$) indicates whether it refers to an n- or a pMOS device, respectively.

For the sake of clarification, the concepts of drive strength (X) and the series factor $K_{n,p}$ are quite similar. Both are multiplicative factors of the equivalent (W/L) of the device, i.e., its current drive capability. Specifically, $K_{n,p}(S)$ multiplies each transistor (of drive strength X) of a series association so that the current drive capability of the resulting association is equivalent to that of the single transistor.

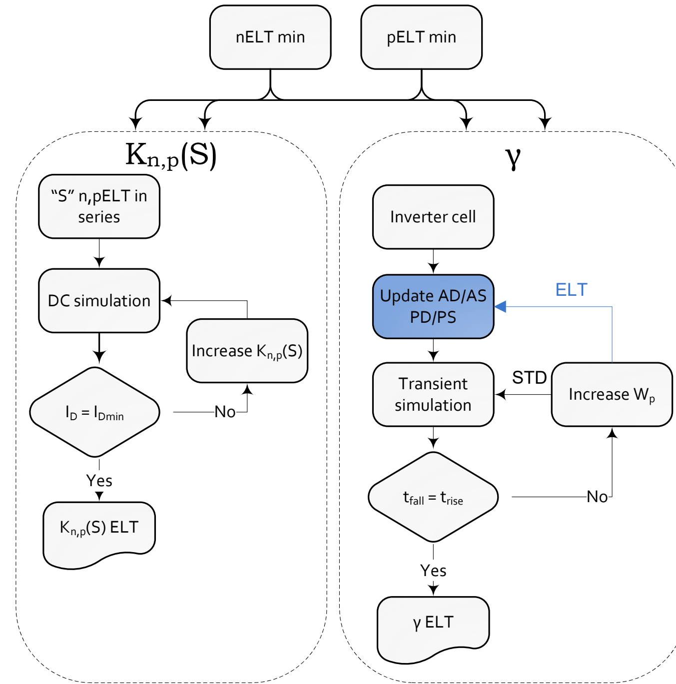
Figure 4.2 illustrates the proposed flow for the acquisition of $K_{n,p}$ and γ parameters in ELT devices. Notice that the primary difference between the standard (STD) and the ELT flow is the calculation of the source and drain areas and perimeters (highlighted blue box).

Finally, the skewing factor (r) is defined as how much an output transition is favored. In this case, for example, a HI-Skew gate $(r_{hi} > 1)$ favors the rising output transition (i.e., reduces t_{rise}), and a LO-Skew $(r_{lo} > 1)$ favors the falling transition (i.e., reduces t_{fall}).

Summarizing the previous concepts with defined variables, four inverter cell configurations are depicted in Fig. 4.1. The standard inverter cell (a); the skewed version (b); and the unskewed versions (c) and (d), where the variables (x_1) in (4.1) and (x_2) in (4.2) are calculated to result in an equal rise and fall resistances, respectively.

$$x_1 = \frac{W_n \cdot \gamma}{W_p \cdot r_{lo}} \tag{4.1}$$

Figure 4.2: Summary of the acquisition steps of the LE variables



Source: Author.

$$x_2 = \frac{W_p}{r_{hi}} \tag{4.2}$$

The total Logical Effort for the rising transition (i.e., *up* or g_u) and the falling transition (i.e., *down* or g_d) are defined as follows:

$$g_u = \frac{\left(\frac{K_n \cdot W_n}{r_{hi}} + \frac{K_p \cdot \gamma}{r_{lo}}\right)}{\left(\frac{\gamma}{r_{lo}} + \frac{W_n \cdot \gamma}{W_p \cdot r_{lo}}\right)}, \tag{4.3}$$

$$\text{and } g_d = \frac{\left(\frac{K_n \cdot W_n}{r_{hi}} + \frac{K_p \cdot \gamma}{r_{lo}}\right)}{\left(\frac{W_n}{r_{hi}} + \frac{W_p}{r_{hi}}\right)}. \tag{4.4}$$

The average value for Logical Effort, or the average between rising and falling transitions (g_{avg}), is expressed by (4.5) as the simple average between (4.3) and (4.4).

$$g_{avg} = \frac{1}{2} \cdot (g_u + g_d) \tag{4.5}$$

To explicit the theoretical fastest average delay, i.e., the least medium average delay,

(4.6) solves the partial derivative of g_{avg} respect to γ, and (4.7) equals it to zero. This facilitates the calculation of the ideal gamma (γ_{ideal}), where γ achieves the critical point (i.e., the local minimum of γ in a balanced inverter cell ($W_n = 1$ and W_p calculated for $t_{fall} = t_{rise}$)).

$$\frac{\partial g_{avg}}{\partial \gamma} = \frac{K_p}{2 \cdot r_{lo} \cdot \left(\frac{W_n}{r_{hi}} + \frac{W_p}{r_{hi}}\right)} + \frac{K_p}{2 \cdot r_{lo} \cdot \left(\frac{\gamma}{r_{lo}} + \frac{W_n \cdot \gamma}{W_p \cdot r_{lo}}\right)} - \frac{\left(\frac{K_n \cdot W_n}{r_{hi}} + \frac{K_p \cdot \gamma}{r_{lo}}\right) \cdot \left(\frac{1}{r_{lo}} + \frac{W_n}{W_p \cdot r_{lo}}\right)}{2 \cdot \left(\frac{\gamma}{r_{lo}} + \frac{W_n \cdot \gamma}{W_p \cdot r_{lo}}\right)^2} \tag{4.6}$$

$$\left.\frac{\partial g_{avg}}{\partial \gamma}\right|_{\gamma=0} = \gamma_{ideal} = \sqrt{\frac{r_{lo} \cdot \ (K_n \cdot K_p \cdot \ W_n \cdot W_p)}{K_p \cdot r_{hi}}} \tag{4.7}$$

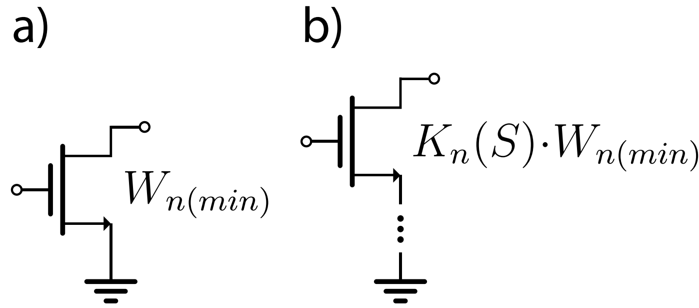
In an inverter cell designed with γ_{ideal}, only minor delay improvement is observed (around 3% when compared to the balanced configuration); the areas of the pMOS transistors, however, are significantly reduced. Consequently, not only the input capacitances are reduced, but also the power consumption (WESTE; HARRIS, 2010). Regarding these facts, the cells proposed in this work consider the optimized value γ_{ideal}. Additionally, to avoid excessive skewing, the maximum factor of two will be attributed for $r_{hi,lo}$.

Finally, The ratio of each n- and pMOS transistor is expressed as (4.8) and (4.9), respectively, where the variables W_n and W_p are the widths of the n- and pMOS devices when the distance between the inner and outer diffusion areas is minimal (i.e., equivalent to minimum L size).

$$W_n = \frac{K_n(S) \cdot W_{n(min)}}{r_{hi}} \tag{4.8}$$

$$W_p = \frac{K_p(S) \cdot \gamma}{r_{lo}} \tag{4.9}$$

Figure 4.3: $K_n(S)$ TB configurations for: a) Single nELT, and b) S nELT in series.



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4.2.1 Assigning input variables

To calculate the gate sizes according to LE-derived equations, the variables $K_{n,p}$ and μ should be known beforehand. These values can be first evaluated when running SPICE simulations. Nonetheless, these values should be further calibrated based on measurements.

The Test Benches (TBs) presented in Figs. 4.3 and 4.4 are proposed to acquire the parameters K and μ, respectively.

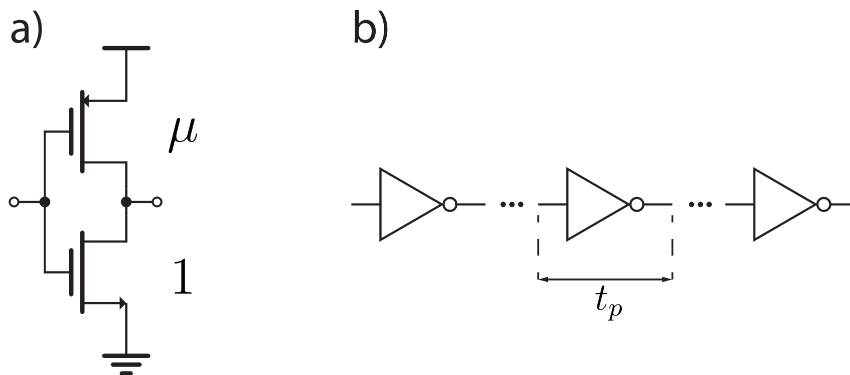
In order to acquire $K_n(S)$ though large-signal analysis, as shown in Fig. 4.3 (a), the first goal should be to simulate the $I_{D_{max}}$ of a single nELT (i.e., for $S = 1$). Then, as show in Fig. 4.3 (b), a parametric analysis can be performed to acquire the next S, which will result in the same output current $I_{D_{max}}$. Then, analogously, the simulation process should be repeated for pELT, i.e., to acquire the $K_p(S)$.

It is noteworthy that a digital cell usually stacks no more than four transistors in series. This procedure, also known by digital designers as fanout-of-four (FO4), avoids an excessive input capacitance. Following this criteria, the $K_{n,p}$ should only be simulated/characterized for $S = 2, 3$, and 4.

In a small-signal analysis, the extraction of parameter μ, as shown in Fig. 4.4 (a), is performed by sizing the pELT of an Inverter cell to produce equal rise and fall switching times (t_{rise} and t_{fall}). As a matter of fact, to avoid no-realistic IO signals, which are usually produced by ideal voltage sources during simulations, the analysis must be performed over the central inverter in a chain of at least five stages, as illustrated in Fig. 4.4 (b).

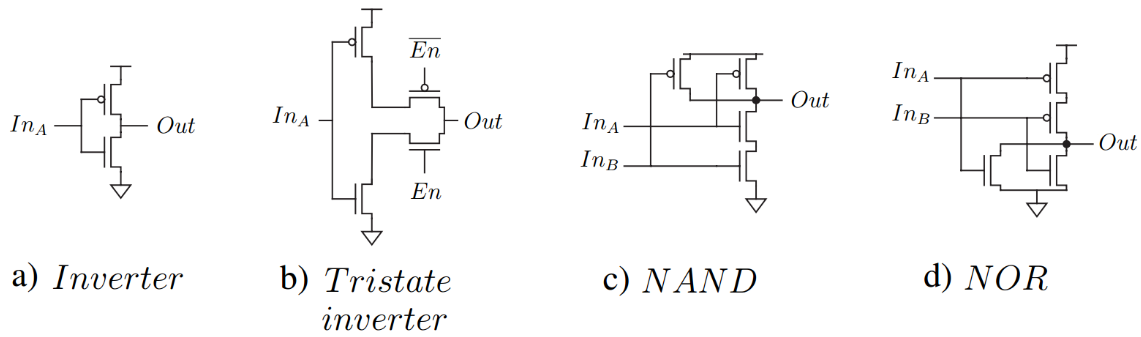
Once K and μ are known, it is possible to calculate γ_{ideal} trough (4.7), and the widths W_p and W_n trough (4.9) and (4.8), respectively. In the next Sections these equations will be implemented to size digital cells of any complexity.

Figure 4.4: TB configurations for simulate μ: a) In an inverter cell, and b) In a chain of at least five inverter cells over the central one.



Source: Author.

Figure 4.5: Schematic diagrams for combinational cells: (a) Basic inverter cell; (b) Tristate inverter; (c) 2-input NAND gate; and (d) 2-input NOR gate.



Source: Author.

4.3 Combinational logic cells

In the context of combinational logic cells, the Fig. 4.5 shows schematic configurations for: (a) Basic inverter cell; (b) Tristate inverter; (c) 2-input NAND gate; and (d) 2-input NOR gate.

Table 4.1 summarizes the values of K_n and K_p for n- and pMOS devices for different S indexes. That is to say, K_n and K_p are a function of the number of devices stacked in series in the logic cell.

Complementary, Table 4.2 displays the commonly used values for skew factors. This way, when using skewed cells, the proposal is to develop three versions of each logic cell; Standard, HI-, and LO-skewed.

Moreover, a robust cell library should contains multiples of each unit cell size current capability, i.e., various drive strengths (X) of each cell. Following the equations proposed in this work, this can be done by multiplying $K_{n,p}(S)$ by X (i.e., $X \cdot K_{n,p}(S)$).

Table 4.1: N,pMOS factors series.

Gate type	K_p	K_n
Inverter	1	1
Tristate	2	2
NAND	1	2
NOR	2	1
S MOS in series	$K_p(S)$	$K_n(S)$

Table 4.2: Proposed Skew factors for standard HI and LO-Skew gates.

Skew type	r_{lo}	r_{hi}
Standard	1	1
HI-Skew	1	2
LO-Skew	2	1

4.4 Multi-stage and best number of stages

At this point, to get the least overall delay of multi-stage cells, the method of LE introduces the concepts of branching effort (B); path electrical effort (H); path logical effort (G); and, finally the path effort (F).

The branching effort (B) accounts for the fanout within a network. The path electrical effort (H) refers to the input and output capacitances of the path as a whole. The path effort (G) multiplies the LE of all logic gates along the path. Therefore, the path effort (F) is given by:

$$F = G \cdot B \cdot H, \tag{4.10}$$

where, G, B, and H are given by:

$$G = \prod g_i, \tag{4.11}$$

$$B = \prod b_i \text{ ; with } b = \frac{(C_{on\ path} + C_{off\ path})}{C_{on\ path}}, \tag{4.12}$$

$$\text{and } H = \frac{C_L}{C_{in}}, \tag{4.13}$$

respectively.

Parameters C_L and C_{in} are the output capacitance, i.e., load capacitance and the input capacitance, respectively. For the designed ELTs, C_{in} is the sum of the gate oxide n and p capacitances $\left(C_{g_{n,p}}\right)$, following

$$C_{in} = C_{g_n} + C_{g_p}. \tag{4.14}$$

where $\left(C_{g_{n,p}}\right)$ is defined as the gate area over diffusion $\left(G_{area_{n,p}}\right)$ (in SI units of m^2) multiplied by the n- and pMOS gate oxide capacitance $\left(C_{gox_{n,p}}\right)$ (in units of $F/\mu m^2$), stated by:

$$C_{g_{n,p}} = G_{area_{n,p}} \cdot C_{gox_{n,p}}. \tag{4.15}$$

To determine the best number of stages, the calculation of N hat $\left(\hat{N}\right)$ is proposed, as shown in 4.16. For practical uses, the theoretical $\hat{N}$ value should be rounded to the nearest integer, then expressed only by variable N.

The LE method states that the minimum delay is achieved for stage effort $\left(\hat{f}\right)$ expressed as in 4.17.

$$\hat{N} \approx log_4\left(F\right) \tag{4.16}$$

$$\hat{f} = F^{\left(\frac{1}{N}\right)} \tag{4.17}$$

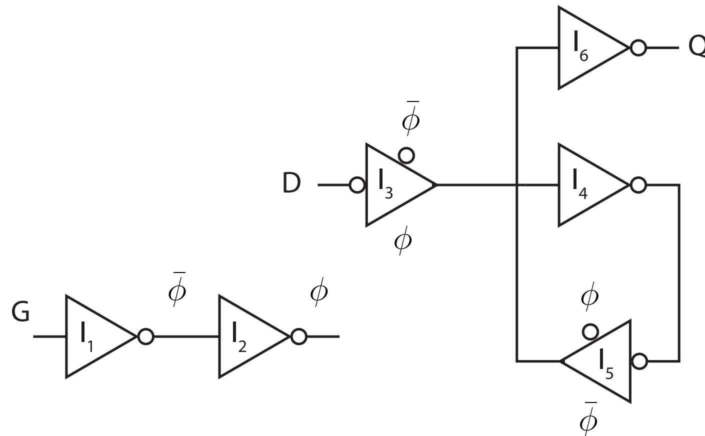
Finally, summarizing the discussed methodology in an *inline* example, (4.18) is proposed to size the stages of a buffer.

$$\left(\frac{W}{L}\right)_{(n,p)} (actual) = \hat{f}^{(stage\ n^o)} \cdot \left(\frac{W}{L}\right)_{(n,p)} (predecessor) \tag{4.18}$$

4.5 Sequential logic cells

To size sequential logic cells, this section introduces a *high active single Q transparent D-latch with active high enable*, which has its schematic diagram presented in Fig.

Figure 4.6: Schematic of a latch DLHQ.



Source: Author.

4.6. This configuration was chosen because it provides an output swing from rail-to-rail, static output, i.e., the output does not float when the latch is opaque, and also includes an output inverter (I_6) to reduce its noise at the output.

The main difference among the aforementioned procedures lies in the *weak* element, that is, the inverter (I_5). To staticize latches, a feedback element (e.g. I_5) is implemented to avoid a floating output when designing sequential cells.

However, to avoid excessive large devices when designing ELTs, the nELTs of I_5 are first designed with minimum DRC features, then their pMOS devices are designed according to γ_{ideal}.

Further, each input signal buffer (I_1, I_2) is designed for a drive strength equal to 2, and their pELTs have their sizes calculated for $X = 2$ and γ_{ideal}. The instance I_4 is equal to one of its input buffer.

Finally, the output buffer drive strength proposed with γ_{ideal} is equal to 4.

4.6 Summary and Discussion

Applying the method of Logical Effort, this Chapter derived equations to calculate the gate sizes of both n- and pMOS devices.

The method deals with series/parallel parameters, such as $K_{n,p}$ and γ. It should be noted that the methodology and the equations apply not only for standard Two-Edged devices but also for ELTs.

The analysis covered sequential and combinational cells by expliciting the related

Test Benches to characterize all necessary parameters, allowing for a complete sizing for any cell arrangement.

The next Chapter implements and discusses the proposed sizing methodology by running electrical level simulations in a commercial CAD tool.

5 ELECTRIC LEVEL SIMULATIONS PROPOSAL

5.1 Introduction

Aiming to evaluate the performance of the ELTs and to discuss the impacts of this design on circuit operation, this Chapter presents the electrical level simulation of the previously discussed logic cells. The purpose of these simulations is to compare how the figures of merit (FoMs) of ELT devices fare against those of STD devices. Additionally, aspects related to the source/drain asymmetry are also discussed.

Simulations were performed at the SPICE level, using a commercial CAD tool, licensed under R&D purposes by the Federal University of Rio Grande do Sul (UFRGS).

5.2 Simulation of assigned input variables

5.2.1 $K_{n,p}(S)$ and γ_{ideal}

Following the methodology presented in Chapter 4, the values for series factor $K_{n,p}(S)$ are shown in table 5.1. The presented values are for up to 4 series devices, for technology nodes of $180\ nm$ and $600\ nm$.

Table 5.1: Simulated values for series factor $K_{n,p}(S)$ up to 4 series devices.

	$K_n(S)$		$K_p(S)$	
S	$180\ nm$	$600\ nm$	$180\ nm$	$600\ nm$
2	1.537	1.555	1.877	1.868
3	2.069	2.104	2.761	2.744
4	2.601	2.653	3.648	3.622

With $K_{n,p}(S)$ and μ it is possible to acquire γ_{ideal}. In this case, the inverter cells are sized following the criteria presented in Section 4.2. The results obtained for $180\ nm$ and $600\ nm$ technology nodes are shown in Table 5.2 (it is noteworthy that this values can be calibrated based on measured values).

Table 5.2: Calculated γ_{ideal} value.

	$180\ nm$	$600\ nm$
γ_{ideal}	1.702	1.816

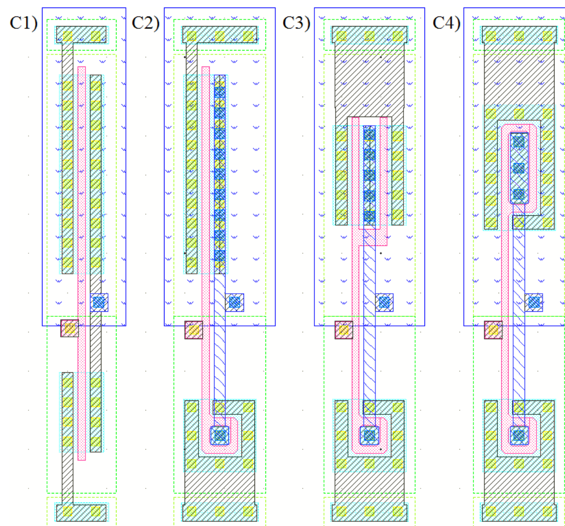
5.3 Core digital logic cells

5.3.1 Inverter cells

Based on minimum design rules, it is proposed a electrical level simulation of Inverter cells in both $600\ nm$ and $180\ nm$ CMOS technologies. Different arrangements were designed, combining both ELT and STD topologies with both n- and pMOS devices.

The configurations proposed are displayed in Fig. 5.1, numbered from one (C_1) to four (C_4). Each configuration was simulated for two drive strengths (the minimum size and its double current capacity, i.e., X_1 and X_2) and for two channel lengths (the minimum size and four times its minimum value, i.e, L_1 and L_4).

Figure 5.1: Inverter cell configurations combining: C_1) n,pSTD; C_2) nELT, pSTD; C_3) nELT, pSTD 2-fingered; and C_4) n,pELT.



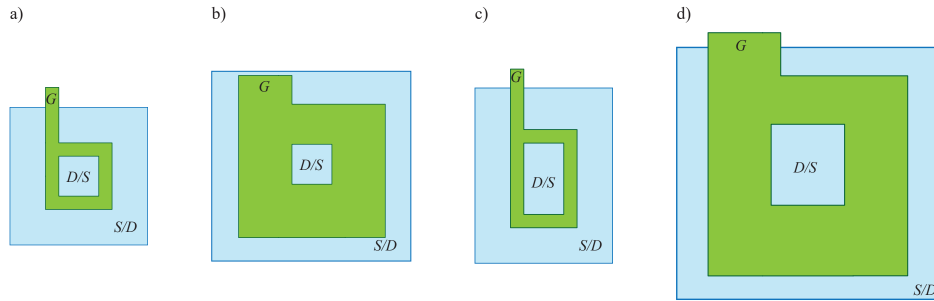
Source: Author.

Figure 5.2 shows the channel length variations, from (a) (minimum sized) to (d) (double capacity and four times the minimum channel length).

Following lithography requirements, the ELT proposal for $600\ nm$ comply with the Rectangular geometry, whereas the $180\ nm$ comply with Rectangular Broken Corners. The ratio between n- and pMOS devices was calculated to achieve the minimum average delay according to γ_{ideal}, expressed in (4.7). Finally, the calculated drain/source areas and perimeters were updated in the simulation netlist.

The performed test bench (TB) consists of a chain of five inverters. The input, output and current signals of the central inverter are analyzed over one inverting cycle.

Figure 5.2: ELT devices when varying X and L: a) X_1L_1 and X_1L_4, and b) X_2L_1 and X_2L_4.



Source: Author.

This test bench was adopted in order to reduce the non-realistic (ideal) simulation signals provided by the input voltage sources. The compendium of acquired FoMs are: propagation delay (t_p); fall and rise times (t_{fall} and t_{rise}); average power (P_{avg}); energy dissipation (E); and noise margins high and low (NM_H and NM_L). The necessary input parameters related to these TBs are shown in Table 5.3 for 600 nm and 180 nm technologies.

Table 5.3: Test Bench related variables for 180 nm and 600 nm.

Description	Variable	Val. for 600 nm	Val. for 180 nm	Unit
Input frequency	f_{in}	100 M	100 M	Hz
Rise and fall times	$t_{rise,fall}$	100 p	100 p	s
Supply voltage	V_{DD}	5	1.8	V

Tables 5.4 and 5.5 show the simulated results using Typical Conditions for 600 nm and 180 nm technologies, respectively. Similarly Tables 5.6 and 5.7 display the results obtained using Corners, whereas Tables 5.8 and 5.9 exhibit the results using Monte Carlo simulation. The values *Min.* and *Max.* expressed in the aforementioned Tables represent their absolute minimum and maximum simulated results, respectively.

The typical condition was set to nominal $T = 27°C$ and V_{DD} of 5 V and 1.8 V, respectively for 600 nm and 180 nm. The Corner simulations were set using a minimum temperature of $-40°C$, maximum temperature of $80°C$ and $\pm$ 10% of the nominal V_{DD} value. The Monte Carlo analysis was set in a Gaussian distribution in a confidence interval of 99.73% (3σ), varying both process and mismatch variables.

Table 5.4: Simulated results (Typical) of $X_{1,2}$ ELT-based inverter cells for channel lengths L and L_4 in 600 nm.

	C_1				C_2				C_3				C_4			
	X_1		X_2		X_1		X_2		X_1		X_2		X_1		X_2	
	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4
NM_H	1.707	1.868	1.728	1.879	1.704	1.868	1.726	1.879	1.747	1.885	1.745	1.888	1.706	1.868	1.727	1.879
NM_L	1.326	1.559	1.297	1.542	1.329	1.559	1.299	1.542	1.297	1.547	1.282	1.535	1.327	1.56	1.298	1.542
t_{fall}	78.67 p	477.3 p	77.25 p	473.5 p	78.77 p	477.3 p	77.29 p	473.4 p	72.05 p	459.7 p	71.15 p	457.3 p	78.72 p	477.3 p	77.27 p	473.5 p
t_{rise}	112.1 p	791 p	111.6p	791 p	112 p	791 p	111.6 p	791.1 p	105.5 p	771.9 p	104.9 p	771.6 p	112 p	791 p	111.6 p	791.1 p
t_{pHL}	89.87 p	604.9 p	87.8 p	596.5 p	90.02 p	604.9 p	87.87 p	596.4 p	81.54	580.1 p	80.34 p	574.3 p	89.95 p	605 p	87.83 p	596.5 p
t_{pLH}	90.4 p	644.8 p	89.74 p	644.3 p	90.35 p	644.8 p	89.71 p	644.3 p	85.27	630.3 p	84.28 p	628.3 p	90.38 p	644.7 p	89.73 p	644.3 p
t_p	90.14 p	624.9 p	88.77 p	620.4 p	90.19 p	624.9 p	88.79 p	620.3 p	83.4	605.2 p	82.31 p	601.3 p	90.16 p	624.9 p	88.78 p	620.4 p
P_{avg}	220.6 μ	745.1 μ	443.8 μ	1.505 m	220.4 μ	745.1 μ	443.5 μ	1.505 m	200.6 μ	713.6 μ	408.8 μ	1.45 m	220.2 μ	745.2 μ	443.3 μ	1.505 m
E	2.206 p	7.451 p	4.438 p	15.05 p	2.204 p	7.451 p	4.435	15.05 p	2.006	7.136 p	4.088 p	14.5 p	2.202 p	7.452 p	4.433 p	15.05 p

Table 5.5: Simulated results (Typical) of $X_{1,2}$ ELT-based inverter cells for channel lengths L and L_4 in 180 nm.

	C_1				C_2				C_3				C_4			
	X_1		X_2		X_1		X_2		X_1		X_2		X_1		X_2	
	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4	L	L_4
NM_H	0.7149	0.8065	0.7127	0.7959	0.7151	0.8064	0.7126	0.7959	0.7243	0.8073	0.7168	0.796	0.7151	0.8064	0.7127	0.7959
NM_L	0.6165	0.6098	0.6185	0.6202	0.6164	0.6098	0.6186	0.6202	0.6107	0.609	0.6159	0.62	0.6163	0.6098	0.6185	0.6202
t_{fall}	23.62 p	167.4 p	23.2 p	172.3 p	22.28 p	16.08 p	22.09 p	168.3 p	21.12 p	157 p	20.84 p	164 p	2045 p	153 p	21.39 p	165.6 p
t_{rise}	28.99 p	324.7 p	28.24 p	316.5 p	27.51 p	31.35 p	26.99 p	310.5 p	26.95 p	308.2 p	25.91 p	303.6 p	25.4 p	300.1 p	26.19 p	306.1 p
t_{pHL}	27.33 p	230.7 p	26.88 p	237.4 p	26.09 p	22.39 p	25.86 p	233.4 p	24.81 p	219.2 p	24.44 p	227.8 p	23.97 p	213.8 p	25.07 p	230 p
t_{pLH}	29.71 p	308.1 p	28.88 p	303.2 p	27.97 p	29.5 p	27.43 p	296 p	27.5 p	289.4 p	26.43 p	289 p	25.96 p	282 p	26.66 p	291.6 p
t_p	28.52 p	269.4 p	27.88 p	270.3 p	27.03 p	25.94 p	26.65 p	264.7 p	26.16 p	254.3 p	25.43 p	258.4 p	24.97 p	247.9 p	25.86 p	260.8 p
P_{avg}	7.732 μ	24.76 μ	15.25 μ	55.32 μ	7.345 μ	23.9 μ	14.59 μ	54.25 μ	6.952 μ	23.37 μ	13.8 μ	52.99 μ	6.795 μ	22.88 μ	14.17 μ	53.49 μ
E	77.32 f	247.6 f	152.5 f	553.2 f	73.45 f	239 f	145.9 f	542.5 f	69.52 f	233.7 f	138 f	529.9 f	67.95 f	228.8 f	141.7 f	534.9 f

Table 5.6: Simulated results (Corners) of X_1 ELT-based inverter cells for channel length L in 600 nm.

	$C_1 : X_1L_1$		$C_2 : X_1L_1$		$C_3 : X_1L_1$		$C_4 : X_1L_1$	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
NM_H	1.658	1.739	1.654	1.735	1.7	1.777	1.656	1.737
NM_L	1.259	1.433	1.262	1.435	1.231	1.408	1.261	1.434
t_{pHL}	64.5 p	118 p	64.7 p	119 p	58.4 p	108 p	64.6 p	118 p
t_{pLH}	62.8 p	121 p	62.7 p	121 p	59.4 p	114 p	62.8 p	121 p
t_{fall}	59.5 p	100 p	59.6 p	100 p	54.6 p	91.3 p	59.6 p	100 p
t_{rise}	73.4 p	170 p	73.3 p	170 p	69.1 p	161 p	73.4 p	170 p
P_{avg}	195 μ	247 μ	195 μ	247 μ	177 μ	224 μ	194 μ	246 μ
E	1.95 p	2.47 p	1.95 p	2.47 p	1.77 p	2.24 p	1.94 p	2.46 p

Table 5.7: Simulated results (Corners) of X_1 ELT-based inverter cells for channel length L in 180 nm.

	$C_1 : X_1L_1$		$C_2 : X_1L_1$		$C_3 : X_1L_1$		$C_4 : X_1L_1$	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
NM_H	662 m	768 m	662 m	768 m	679 m	775 m	663 m	768 m
NM_L	600 m	646 m	600 m	646 m	592 m	640 m	600 m	646 m
t_{pHL}	24.3 p	30.5 p	23.3 p	29.1 p	22.3 p	27.5 p	21.4 p	26.7 p
t_{pLH}	27.1 p	32.1 p	25.7 p	30 p	25.3 p	29.5 p	23.8 p	27.9 p
t_{fall}	20.4 p	27.2 p	19.4 p	25.6 p	18.4 p	24.2 p	17.8 p	23.5 p
t_{rise}	25.4 p	32.2 p	24.2 p	30.5 p	23.9 p	29.7 p	22.3 p	28.2 p
P_{avg}	7.55 μ	7.88 μ	7.2 μ	7.46 μ	6.82 μ	7.06 μ	6.66 μ	6.9 μ
E	75.5 f	78.8 f	72 f	74.6 f	68.2 f	70.6 f	66.6 f	69 f

In the context of ELTs, as already discussed in Section 3.3.4, the decision of placing the drain inside improves output conductance (channel length modulation) at the expense of frequency operation. The simulations performed in this section considered the drain inside for all configurations. When enclosing the drain, and consequently assigning the source to a more stable potential, such as V_{DD} or V_{SS}, the smaller area is assigned to the output, reducing the reffered output capacitance. Therefore, shorter switching times would be required to charge/discharge these capacitances.

By analyzing the simulated results, it is possible to verify the same behavior when increasing channel length or drive strength for all FoMs. Indeed, the four inverter cell configurations are equivalent in terms of their (W/L), except for different areas/perimeters - manually updated in SPICE simulations. Thus, the results are in agreement with the Two-Edged expected behavior.

Regarding noise margins, the simulated output values should, ideally, be the same, even with different S/D parameters. Therefore, the slight variations observed (in the second and third decimal place) are attributed to the analytical values calculated for (W/L) in

Table 5.8: Simulated results (Monte Carlo) of X_1 ELT-based inverter cells for channel length L in 600 nm.

	$C_1 : X_1L_1$		$C_2 : X_1L_1$		$C_3 : X_1L_1$		$C_4 : X_1L_1$	
	Avg.	σ	Avg.	σ	Avg.	σ	Avg.	σ
NM_H	1.71	51.2 m	1.70	51.5 m	1.747	51.1 m	1.70	50.7 m
NM_L	1.32	46.4 m	1.32	45.4 m	1.295	44.3 m	1.325	44.5 m
t_{pHL}	89.9 p	3.16 p	90 p	3.13 p	81.5 p	2.95 p	89.9 p	3.18 p
t_{pLH}	90.4 p	3.75 p	90.4 p	3.75 p	85.3 p	3.59 p	90.4 p	3.76 p
t_{fall}	78.7 p	2.52 p	78.8 p	2.51 p	72.1 p	2.38 p	78.7 p	2.52 p
t_{rise}	112 p	4.53 p	112 p	4.53 p	106 p	4.38 p	112 p	4.53 p
P_{avg}	221 μ	5.14 μ	221 μ	5.13 μ	201 μ	4.98 μ	220 μ	5.14 μ
E	2.21 p	51.4 f	2.21 p	51.3 f	2.01 p	49.8 f	2.20 p	51.4 f

Table 5.9: Simulated results (Monte Carlo) of X_1 ELT-based inverter cells for channel length L in 180 nm.

	$C_1 : X_1L_1$		$C_2 : X_1L_1$		$C_3 : X_1L_1$		$C_4 : X_1L_1$	
	Avg.	σ	Avg.	σ	Avg.	σ	Avg.	σ
NM_H	712.5 m	8.95 m	712.9 m	9.15 m	723.8 m	8.59 m	712.6 m	8.88m
NM_L	616.9 m	10.54 m	616.4 m	11.06 m	609.7 m	10.53 m	616.9 m	10.21 m
t_{pHL}	27.32 p	498.5 f	26.07 p	474.9 f	24.81 p	466.2 f	23.98 p	438.6 f
t_{pLH}	29.69 p	597.6 f	27.93 p	568.3 f	27.48 p	567.6 f	25.94 p	531.3 f
t_{fall}	23.61 p	294.1 f	22.26 p	274 f	21.12 p	264.8 f	20.45 p	252.5 f
t_{rise}	28.99 p	563.7 f	27.48 p	532.8 f	26.95 p	547.2 f	25.39 p	505.4 f
P_{avg}	7.72 μ	58.53 n	7.33 μ	58.37 n	6.95 μ	58.07 n	6.79 μ	55.84 n
E	77.3 f	617.4 a	73.4 f	615.7 a	69.5 f	612.6 a	67.9 f	589.1 a

ELTs, which differ from those from STD devices, in which the gate width (and length) are integers multiples of the minimum design pitch.

In FoMs related to transient simulations, the updated S/D areas cause slight variations, especially in the 180 nm technology. In this technology node, in an extreme comparison between C_1L_1 (Pull up and down Two-Edged) and C_4L_1 (Pull up and down Enclosed), it is possible to verify the reduction of almost 10% in t_p, P_{avg} and E. Moreover, even with transistor folding, which, in perspective of Radiation-Hardening, is undesirable (due to the multiplication of the LOCOS areas), a reduction of almost 3% of t_p, P_{avg} and E is observed.

As a matter of fact, for the 600 nm technology node, an even larger difference (better FoMs) is expected when progressing from C_1 to C_4. In this case, the differences were not so prominent because of the increased channel length (nonetheless, this behavior and statements are currently being under our analysis). Following this statement, reduced variations (smaller σ) were also expected in Monte Carlo simulations due to the increased area when employing ELTs.

These aforementioned assumptions are supported by the work of Anelli (ANELLI,

2000), that shows a similar and linear trend for $\sigma\Delta V_{th}$, which for channel lengths of $0.5\ \mu m$ and $0.28\ \mu m$, are $\approx 3\ mV$ and $\approx 4.3\ mV$; and $\approx 2.6\ mV$ and $\approx 4.7\ mV$ for ELT and STD devices, respectively. These values reinforce the validity of our simulation approach. Detailed experimental investigations of the V_{th} variability, however, is required.

5.3.2 Ring oscillators

The proposed simulations for Ring Oscillators (ROsc) addresses the same group of Inverter cells that were laid-out in this work (presented in the following Section for $600\ nm$). The two inverters' configurations are the same exhibited in Fig. 5.1 by C_1 and C_4.

The number of stages was calculated to result in an oscillation frequency in the order of some MHz, which is in the range required for the available measuring instruments. Thus, the number of stages of each ROsc is 99, and the disposal was set in three rows of 33 columns each one.

Table 5.10 summarizes the simulated oscillation frequency for each configuration. In Section 8.2.4, the simulated values are compared to practical measurements.

Table 5.10: Simulation frequency for Ring oscillators.

Conf.	Oscillator	Sim. freq.
C_1	n,pSTD	$54.97\ MHz$
C_4	n,pELT	$55.97\ MHz$

5.4 Summary and Discussion

This Chapter evaluated the performance of the ELTs by comparing their figures of merit to standard devices. The simulations covered configurations combining standard and enclosed devices for different drive strengths.

Based on the most emblematic digital cell (inverter cell), this Chapter has simulated and compared different layout topologies with enclosed devices regarding power, delay, and area consumption. In this sense, the simulated results showed better performances related to propagation delay, energy consumption and less variability when compared to standard devices.

The next Chapter implements the layout concepts of enclosed devices, guard rings, and a template proposal in order to present a physical RHBD design flow proposal.

6 PHYSICAL DESIGN FLOW PROPOSAL

6.1 Introduction

In this Chapter, the proposed methodology of RHBD ELT-based library cells design flow is discussed. It is vital to emphasize that the methodology proposed in this work does not significantly alter the classic and well-established custom standard cell library design flow. It actually proposes additional procedures to enable the CAD tool to properly recognize and account for the enclosed geometry, providing the equivalent $(W/L)_{eff}$ for the following procedures. These additional steps are included during the front-end phase and have a negligible increase in the computation design time.

6.2 Design flow diagram

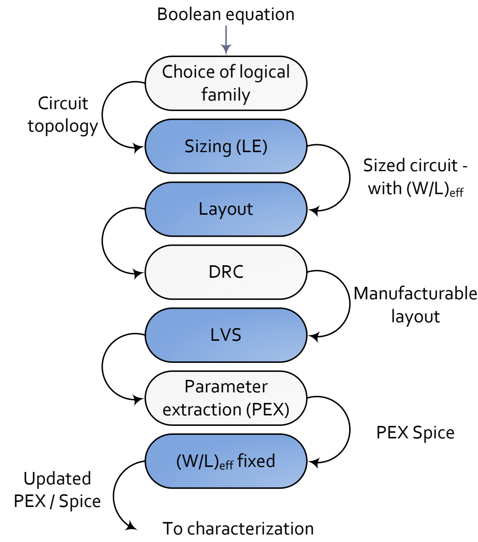
The proposed methodology aims to provide the necessary additional steps for RHBD design that can be fully included and automated into CAD tools, using the input files and design rules of standard commercial fabrication processes. There are four fundamental steps to the process: the first is to size the circuit topology according to LE equations; the second is to layout the devices using an ELT that satisfies the digital design requirements (such as cell pitch) and that is fully compatible with the Design Rule Checking (DRC); the third step is to verify the Layout Versus Schematic compatibility; and the fourth is to update the dimensions of each transistor based on its equivalent (W/L).

Figure 6.1 depicts the high level abstraction of the full-custom proposed design flow. The highlighted blue boxes represent the aforementioned steps — i.e., respectively, the sizing phase, proposed layout, LVS verification and the calculation of device's parameters (in which the (W/L), as well as the source and drain diffusion areas and perimeters, are updated in the SPICE netlist).

In the Algorithm (1), the *sizing* and *layout* phases are covered. The base equations are indicated through the addition of comments in the code and, to facilitate the code reading, function names were properly chosen. The code was implemented employing, MATLAB, C and SKILL programming languages. Nonetheless, other programming languages can be used in order to better conform to designer facilities or software/hardware constraints — the algorithm concept remains the same.

For the *Sizing* step, the LE equations are employed, according Section 4.2. For the

Figure 6.1: Bird's eye view of full-custom design flow.



Source: Author.

Algorithm 1: Sizing and layout phases of INV X2

```
   /* ----------------------------                              */
   /* IN: Struct related to basic input data                     */
   /* TPL: Struct related to template definitions                */
   /* ----------------------------                              */
1  TPL = read_template(IN); ;                          /* Fig. 6.2 */
2  X = 2; ;                                          /* Inverter X2 */
3  [d_{hor,ver_{min}}]= calc_distance(TPL); ;           /* Fig. 3.7 */
4  nELT = calc_param_nELT(IN, X); ;             /* (3.6) and (3.5) */
   /* Calculate number of devices in parallel using
      ratio between d_hor and d_ver equal to 3                   */
5  if (nELT.d_hor > (3 × nELT.d_{hor_{MIN}})) then
6      flag_ok = 0;
7      num_parallel = 2; ;                  /* Devices in parallel */
8      while (flag_ok == 0) do
9          nELT = calc_param_nELT(IN, X/num_paralell);
10         if (nELT.d_hor > (3 × nELT.d_{hor_{MIN}})) then
11             num_parallel + +;
12         else
13             flag_ok = 1;
14 nGEOM = draw_geometries(IN, TPL, nELT);
15 γ = calc_gamma(nELT, X); ;                              /* (4.7) */
16 pELT = calc_param_pELT(IN, nELT);
17 if (pELT.d_hor > (3 × pELT.d_{hor_{MIN}})) then
18     ... ;                               /* The same as for nELT */
19 pGEOM = draw_geometries(IN, TPL, pELT);
20 cellGEOM = draw_group_cell(IN, TPL, nELT, pELT);
```

Layout step, lithography constraints and design rules are the primary concerns. For the case studies presented in Chapter 7 the transistor geometries are defined using equations from Section 3.3.2 in which, for instance, due to angle requirements at the edge of the enclosed polysilicon gate, annular ELTs were implemented in the $180\ nm$ test chip, whereas the rectangular ELTs were implemented in the $600\ nm$ test chip.

Finally, both the *LVS* and the final $(W/L)_{eff}$, which reintroduces in the Parameter Extraction (PEX) Spice the effective transistor dimensions previously calculated in the sizing step. This fix (i.e., update the (W/L)) can be included into the CAD tool using, for example, a SKILL Language (SYSTEMS, 2012), allowing an automated calculation of such variables.

Algorithms (2) and (3) represent an example of the base SKILL codes, which introduce the calculation of device parameters into CAD tool (last blue box in Fig. 6.1). The code in the file *MOS_ELT.il* declares input variable(s) (e.g., *var1*) and the button (e.g., *Update W/L*) responsible to invoke the callback function(s) (e.g., *update_woverl()*), which, on its turn, should be implemented in the file *callbacks.il*.

Algorithm 2: Base MOS SKILL code example

```
   /* ----------------------------                */
   /* MOS_ELT.il                                  */
   /* ----------------------------                */
 1 elt_cell = ddGetObj("MOSELT_lib" "nmos_elt")
 2 baseCell = cdfGetBaseCellCDF(elt_cell)
 3 cdfParamId = cdfCreateParam(baseCell
 4 ?name "var1"
 5 ?prompt "var1"
 6 ?defValue "0"
 7 ?type "string"
 8 ?parseAsNumber "yes"
 9 ?parseAsCEL "yes"
10 ?units "lengthMetric"
11 )
12 ... ;     /* Include all Eq., (3.6), (3.5) variables */
13 cdfParamId = cdfCreateParam(baseCell
14 ?name "calc"
15 ?prompt "Update (W/L)"
16 ?type "button"
17 ?callback "update_woverl()"
18 )
```

Notice that the other steps of the design flow are not modified and no particular process modification was required. Once every cell is defined and the transistors geometries

Algorithm 3: Base callback SKILL code example

```
  /* ----------------------------                  */
  /* callbacks.il                                  */
  /* ----------------------------                  */
1 procedure( update_woverl()(@optional (cdf cdfgData))
2 var1 = cdfParseFloatString(cdf->var1->value)
3 ... ;                            /* Get all variables */
4 woverl = ... ;          /* Use var(s) to calculate W/L */
5 )
```

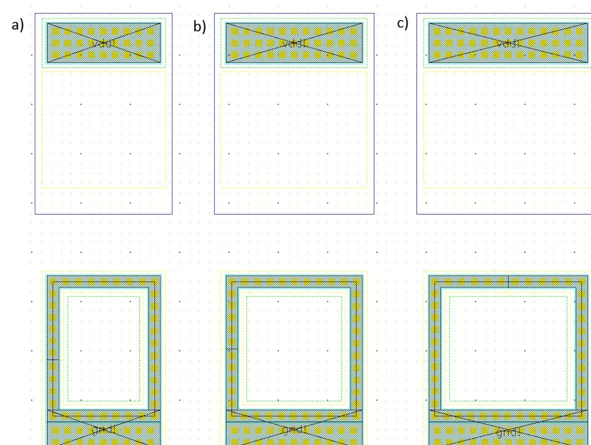
are calculated through LE, it is possible to fully automate the generation of the simulation netlist.

6.3 Template

The main criteria to incorporate any standard cell into automatic digital synthesis flow is the standardization of the cell's height and width. In this work, the adopted cell's height and width were defined as integer multiples of MET1 and MET2 pitches respectively.

Thus, the cell's height has a fixed value, whereas its width is variable. This approach is also implemented in popular CAD tools. For this reason, as presented in Fig. 6.2, the adopted cell's height was defined with the value of $43.2\ \mu m$ (distance multiple of MET1 pitch), and the widths are multiples of $1.3\ \mu m$ (distance multiple of MET2 pitch), as represented by (a), (b), and (c).

Figure 6.2: Template for digital cells: a) Minimum width of ELT device, b) $1.1\cdot$ min. width of ELT device and c) $1.2\cdot$ min. width of ELT device.

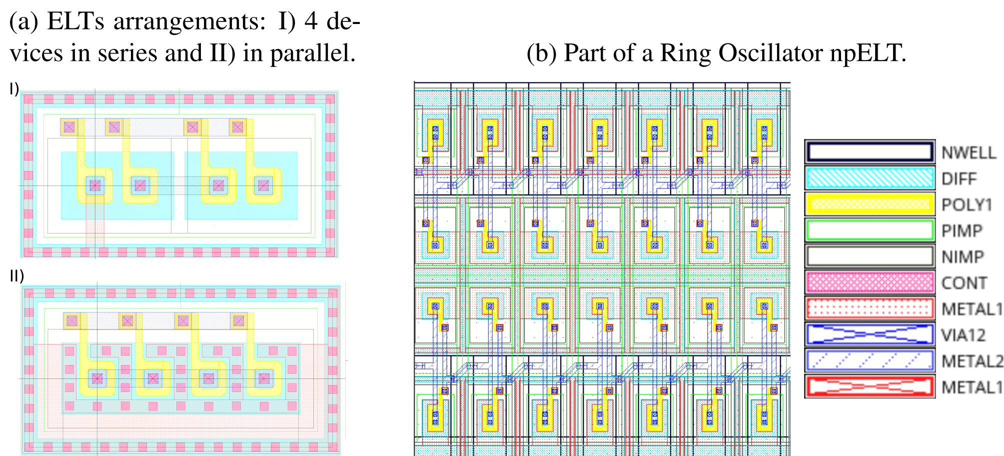


Source: Author.

Regarding RHBD aspects, the use of p^+ guard rings, enclosing pull-down networks are mandatory. Hence, the basic template embedded such structures, surrounding the nMOS devices to reduce the leakage path inter-device (through different n-well regions biased at different potentials).

The power lines V_{DD} or V_{SS} have, each one, the height of 2 times minimum MET1 pitch - approximately the same distance as the foundry-provided digital cells template. Moreover, the cells should maintain the abutment possibility (i.e., the superposition of power rails and lateral guard rings), where the area allocation is substantially reduced in automated digital layouts. A complete example of such template and design definitions can be seen in a part of the Ring Oscillator, in Fig. 6.3 (b), designed in 180 nm.

Figure 6.3: Template devices examples in 180 nm.



(a) ELTs arrangements: I) 4 devices in series and II) in parallel.

(b) Part of a Ring Oscillator npELT.

In order to avoid an excessive load (input) capacitance, digital designers usually stack no more than four devices in series (fanout-of 4, FO4) (WESTE; HARRIS, 2010). Thus, in this work, the maximum devices stacked in series or parallel will be 4. Layout examples of p^+ guard rings and series/parallel arrangements are shown in Fig. 6.3 (a) I and II, respectively.

It is important to notice that pMOS transistors, in principle, do not require an enclosed layout, since the accumulation of positive charge has a negative (decreasing) impact on leakage current. Nonetheless, since the nMOS transistors require enclosed geometry, they will be intrinsically wider than conventional standard MOS transistor; thus, in the context of fixed height with variable width, as is the case of digital cells, enclosing the pMOS transistors does not increase the area overhead in comparison to nELT only layouts. This is actually beneficial to the frequency response of the device, given that the output capacitance (i.e., drain capacitance) will be smaller.

In cases which higher aspect ratios are needed (i.e., long $d_{hor,ver}$), the devices are divided into parallel structures as shown in Fig. 6.3 (a) II.

6.4 Digital cells

The first group of digital cells designed is composed of a minimum set of instances. This decision aims to enable a faster implementation and the verification of necessary parameters to validate the design flow methodology, especially when employing ELTs, which is the core of this thesis.

This methodology, in order to ease the library maintenance, was also followed in other related works as (LIU et al., 2014b; KLOUKINAS et al., 1998; LIU et al., 2014a; STABILE; LIBERALI; CALLIGARO, 2008).

Table 6.1 summarize the selected and designed group of cells.

Table 6.1: RHBD core cells.

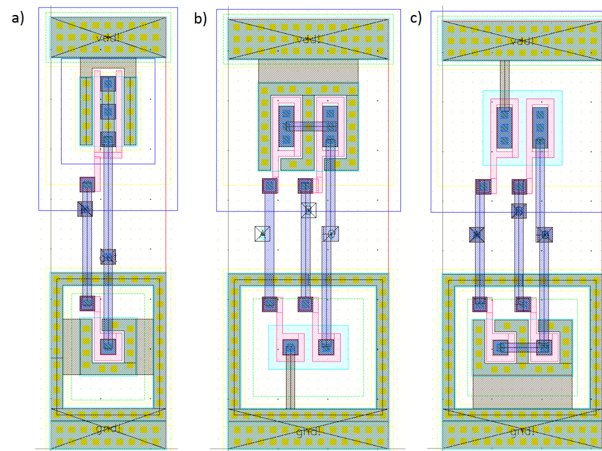
Cell type	Description	Drive strengths	Area penalty
INV	Inverter	$1; 2; 3$	4.09
BUFF	Buffer	$1; 2; 30\ pF$	> 4
NAND	2-input NAND gate	$1; 2$	3.81
NOR	2-input NOR gate	$1; 2$	2.86
DLHQ	Active-high D-type transparent latch	$1; 2$	8.59

The layout of the Inverter, NAND, and NOR gates are illustrated in Fig. 6.4. The layout of the sequential block Active-high D-type transparent latch is presented in Fig. 6.5. It is important to emphasize that in case of more complex cells, as for instance the latch illustrated in Fig. 6.5, a wider drain area may favor the occurrence of a SEE.

Hence, to reduce the probability of this undesirable effect occur, the drain area should be carefully sized. Throughout this work, the relation between drain and source areas is designed to better suit with template definitions and, where possible, aiming to maximize the frequency operation of the cell. The specific task of optimize the drain size focusing to reduce SEEs is proposed as a complementary future work.

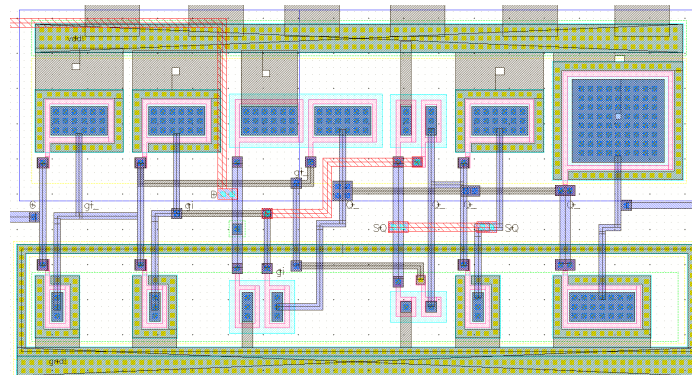
A final comparison between a ring oscillator standard and ELT is shown in Fig. 6.6, where in (a) is presented an oscillator employing both networks with ELT, and in (b) both networks with conventional (and foundry provided) library core.

Figure 6.4: Digital cells: a) INV, b) NAND, and c) NOR.



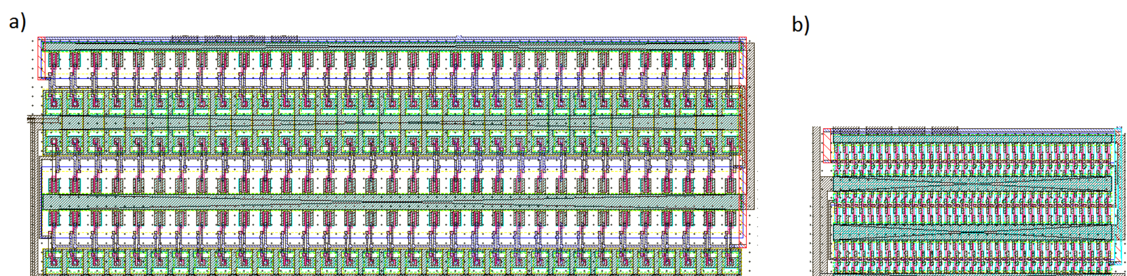
Source: Author.

Figure 6.5: Digital cell: Active-high D-type transparent latch (DLHQ).



Source: Author.

Figure 6.6: Scaled Ring Oscillators calibration test structures: a) n,pELT RHBD, and b) n,pSTD from foundry's library core.



Source: Author.

6.5 Summary and Discussion

This section proposed a RHBD ELT-based library cells design flow methodology. The proposed flow embeds a template proposal with guard rings. Moreover, the designed

cells respect the abutment lithography requirements aiming to be included in the automated digital synthesis flow.

Through four fundamental steps, it has been shown that is possible to incorporate RHBD designs into CAD tools. The aforementioned steps include the *sizing* phase, where the device's parameters are first calculated; the *layout* phase, where the cells are effectively draw; the *LVS* phase, where the verifications are performed and, finally, the (W/L) *fixed* phase, where parameters as, e.g., source and drain areas are updated in the SPICE netlist.

The expertise of automating RHBD ICs is an overwhelming majority of restricted availability (proprietary right). In most cases, the discussions within academic institutions cover aspects related to modeling and simulation of the equivalent (W/L). In this sense, a great effort was performed to face the challenge of incorporating the designed cells into CAD tools especially to meet the lithography requirements, where the only way to design some geometries was by their calculation and inclusion directly by *Layout Extend Format - LEF* data file.

As a final consideration, it is noteworthy that the technology nodes explored in this work ($600\ nm$ and $180\ nm$) have relatively large gate length if compared to cutting edge nanometer scale technologies. Nonetheless, the advance in the state-of-the-art aimed to introduce the possibility to fully automate the process of including ELT devices for a user with minimal or even negligible expertise in RHBD layouts.

The next Chapter presents the test structures to provide experimental data to characterize the RHBD cell library.

7 TEST STRUCTURES

7.1 Introduction

In order to fairly compare the standard gate topology provided by the commercial foundry's PDK against those of ELT and validate the proposed RHBD design flow, test structures were designed for both $600\ nm$ and $180\ nm$ technology nodes. Therefore, this Chapter introduces a group of cells selected to provide practical measurements to characterize the basic building blocks of the RHBD cell library and, thus, provide technical support to validate the proposed design flow. It is noteworthy that the structures were fabricated using standard commercial processes, without requiring any additional processing step.

In order to qualify the hardness degree of the ELTs and compare it to the standard gate topology provided by the commercial foundry's PDK, two main measurement setups were designed, each one counting with a specific IO PAD.

The first group, with its IO signals connecting directly to intra-chip μ-PADs (i.e., only available through μ-probes), was designed to provide large-signal measurements pre- and post-irradiation, as well as after annealing.

The second group has its IO signals connected to outer-chip PADs (i.e., ready to direct measurements trough packaging pins). This way, this group of cells includes Electrostatic Discharge protection (ESD) and an output buffer.

The μ-PADs area were laid-out with the minimum dimensions of $65\ \mu m \times 65\ \mu m$, in order to allow the manual placement of the testing probes. Thereby, even considering that each PAD shares the terminals of the device's source and drain, a huge area was needed for each instance.

For these aforementioned reasons, and taking into account a very limited area (of approximately $2\ mm \times 2\ mm$) for each test chip, the floorplanning decision was to prioritize the characterization of the devices through testing probes. Thus, in both test chips, only a few instances (n,pMOS ELT and STD minimum sized and its equivalent, respectively) were assigned to the IO PADs.

Finally, rectangular geometry was employed for transistors laid-out in the $600\ nm$ technology node due to design constraints (i.e., it does not withstand $45°$ angle corners). On the other hand, since such constraint is absent in the $180\ nm$ process, annular geometry was used.

7.2 Designed devices and cells

a) Individual enclosed transistors: The individual enclosed structures are composed of 12 ELTs in each fabricated chips. Of these, 8 are n-type and 4 are p-type. Five of the n-type transistors have a fixed X $(X1)$ and a varying length ($L1$, $L1.2$, $L2$, $L5$ and $L10$), whereas the remaining three have a fixed L $(L1)$ and a varying drive strength ($X1$, $X1.5$, $X2$ and $X3$). The 4 p-type transistors have a fixed length $(L1)$ and a varying drive strength ($X1$, $X1.5$, $X2$ and $X3$).

b) Individual standard transistors: For the standard structures, there are 4 transistors in each fabricated chip, being 2 n- and 2 p-type devices. Of these, two are the minimum-sized nSTD and pSTD, whereas the remaining two are equivalent to the minimum-sized nELT ($nELTX1L1$) and pELT ($pELTX1L1$).

c) n,pELT in series: There are six structures in the 600 nm technology, being three with 2 transistors in series $(Sr2)$, and three with 4 transistors in series $(Sr4)$. The three $Sr2$ configurations consist of two nELT configurations $(K_n(1)L1)$ and $(K_n(2)L1)$ and one pELT configuration $(K_p(1)L1)$; on the other hand, the three $Sr4$ configurations consist of two nELT ($K_n(1)L1$ and $K_n(4)L1$) and one pELT $(K_p(1)L1)$. For the 180 nm technology, there are 9 structures; 6 of them are equivalent to those previously discussed; the additional three are comprised of arrangements of 3 transistors, being two nELT ($K_n(1)L1$ and $K_n(3)L1$) and one pELT $(K_p(1)L1)$.

d) n,pELT in parallel: For both chips, there are three nELT and three pELT arrangements of two, three and four transistors in parallel ($Pr2$, $Pr3$ and $Pr4$, respectively), totaling six arrangements. For all the transistors in these structures, the sizing is $X1L1$.

e) Inverter-based Ring Oscillators: Two inverter-based ring oscillators were laid-out being one with standard transistors only and the other with ETLs only. The inverters were designed using the PN-ratio based on γ_{ideal} from (4.7).

f) Output Buffers: For each technology node, an output buffer was designed to load an output capacitance of 30 pF. The resulting number of stages for each buffer

is 3 and 5 for the $600\ nm$ and $180\ nm$ technologies, respectively. The number of gates in each stage (pMOS/nMOS) was equal to $(1/1,\ 4/4,\ 16/16)$ and $(1/1,\ 3/2,\ 9/6,\ 32/21,\ 142/84)$.

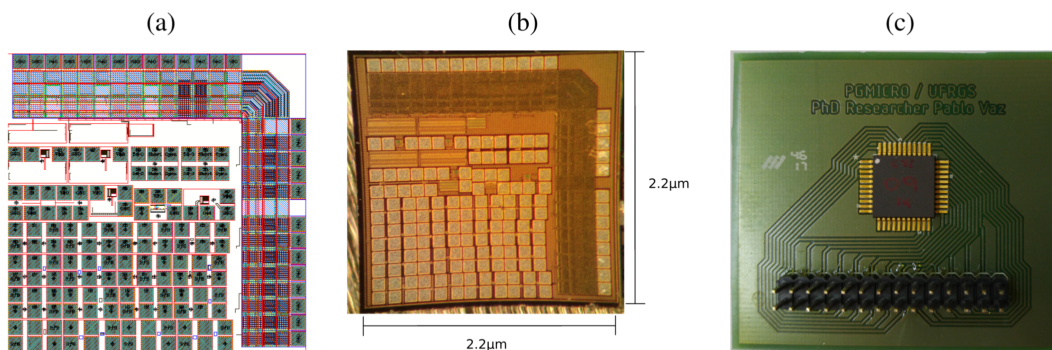
7.3 Tape-out

In the context of *process calibration test structures*, the documentation is often unavailable by silicon manufacturers. The design and inclusion of test structures are crucial for proper characterization. The work of (WESTE; HARRIS, 2010) also adds that these structures are particularly necessary in academic designs, which receive less support from foundries.

Thus, structures such as Ring Oscillators (combining ELTs and STDs devices), shown in Fig. 6.6; a group of IO contacts (open, short and $50\ \Omega$ resistance); and an output buffer (designed to drive μ-PADs, which do not have output buffer), were used to allow the evaluation of contact resistance and device parameters in silicon.

Figures 7.1 and 7.2 illustrate the top view of the three major design and fabrication process steps; in (a) the layout in CAD tool; (b) laid-out and naked die; and (c) the final prototype for test chip $600\ nm$ and $180\ nm$, respectively. The total dimensions of the test chip are, respectively, $(2.2\ \mu m \times 2.2\ \mu m)$ and $(1.6\ \mu m \times 1.6\ \mu m)$.

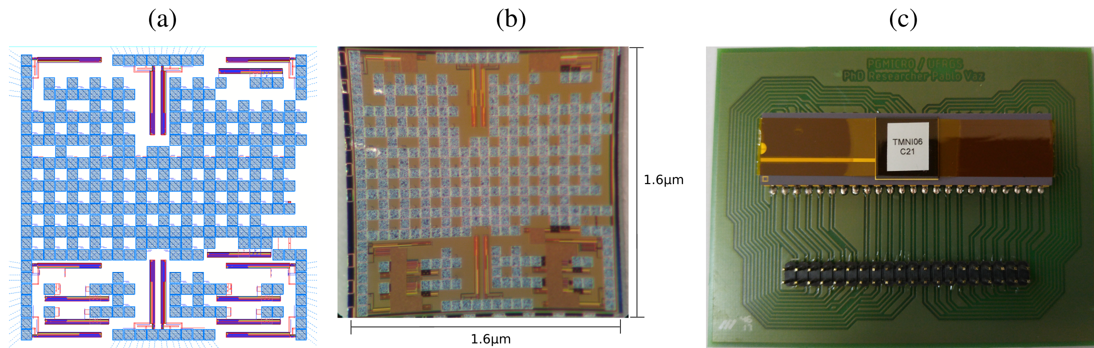
Figure 7.1: Top view of the three major design and fabrication process steps in $600\ nm$; in (a) the layout in CAD tool; (b) laid-out and naked die; and (c) the final prototype.



Despite the ELT devices, it is noteworthy that the entire fabrication process was performed using standard commercial process, without the need of any additional processing steps. In the same way, the wire bonding, Printed Circuit Board (PCB) and the weld followed the standard commercial methodology.

Figure 7.2: Top view of the three major design and fabrication process steps in $180\ nm$; in (a) the layout in CAD tool; (b) laid-out and naked die; and (c) the final prototype.

(a) (b) (c)



Source: Author.

7.4 Summary and Discussion

This Section presented the test chip to qualify the hardness degree of the ELTs and compare it the standard gate topology provided by the commercial PDK of the foundry.

The test chip consists of individual n- and pMOS transistors of enclosed and standard layouts; n,pELT connected in series and in parallel; ring oscillators combining ELT and STD devices; and an output buffer (designed to drive μ-PADs, which do not have output buffer).

Next Chapter presents and discusses the experimental measurement results from pre- and post-irradiation stress.

8 EXPERIMENTAL RESULTS

8.1 Introduction

The practical measurements were held in two phases, the pre-irradiation, and during and post-irradiation.

The pre-irradiation measurement experiment was held at the Electrical Characterization Laboratory (*Laboratório de Caraterização Elétrica - LCE*) of the Federal University of Rio Grande do Sul (*Universidade Federal do Rio Grande do Sul - UFRGS*), located at Porto Alegre - RS - Brazil.

The during and post irradiation experiment was held at the Ionizing Radiation Laboratory (*Laboratório de Radiação Ionizante - LRI*) of the Institute for Advanced Studies (*Instituto de Estudos Avançados - IEAv*), located at São José dos Campos - SP - Brazil.

The Sections 8.2 and 8.3 present and discuss in further detail the practical experiments for pre-irradiation, and during and post-irradiation, respectively.

8.2 Pre-irradiation

8.2.1 Introduction

In the pre-irradiation experimental phase, the large-signal characteristics were measured using a precision semiconductor parameter analyzer *Agilent 4156C* and a microprobe station *Cascade Microtech EP6* equipped with testing probes *Cascade Microtech PH110* composed of tungsten probes *Cascade Microtech PTT*-$120/4-25$*"* for the contact between the devices' PADs and the measurement equipment. The measurements were performed under ambient atmosphere in a dark environment with relative humidity in the range of $50-60\%$. The simulations used for comparison with practical results were performed in the SPICE level with BSIM3V3, using Cadence Virtuoso environment.

Next Subsections (i.e., 8.2.2, 8.2.3, and, 8.2.4) present and compare measurement and simulation results. The difference between them, expressed in $\%$, were determined using (8.1). Moreover, their differences were calculated where the device operates in the region of strong inversion and in saturation, i.e., $I_{D_{max}}$ for $V_{GS,DS} = V_{DD}$ (or V_{SS}), and

$V_{BS} = V_{SS}$ (or V_{DD}).

$$I_{D_{diff}} = \left(\frac{\left(\frac{W}{L}\right)_{eff}^{sim} - \left(\frac{W}{L}\right)_{eff}^{mea}}{\left(\frac{W}{L}\right)_{eff}^{sim}} \right) \quad (8.1)$$

8.2.2 Individual transistors

For each technology node, two aspect ratios were designed; the minimum sized (MIN); and the equivalent to $ELTX1L1$ (EQU), calculated with (3.5) for $600\ nm$, and with (3.6) for $180\ nm$. Results are shown in Table 8.1.

Table 8.1: Difference between simulated and measured drain current values for n,pSTD devices (in [%]).

	$600\ nm$		$180\ nm$	
Configuration	MIN	EQU	MIN	EQU
$nSTD$	4.85	3.44	0.94	3.59
$pSTD$	25.53	11.49	2.40	7.32

In ELT devices, to evaluate the output characteristic $(I_D\ vs.\ V_{DS})$ and transfer function $(I_D\ vs.\ V_{GS})$, the RMS calculation is adopted as shown in (8.2). In the same context, the RMS difference has been previously brought to bear by (GIRALDO; PACCAGNELLA; MINZONI, 2000). The refereed work uses the $I_{D_{diff}}$, analogously as defined in (8.1), to calculate the average difference (given in percentage) between simulated and measured values.

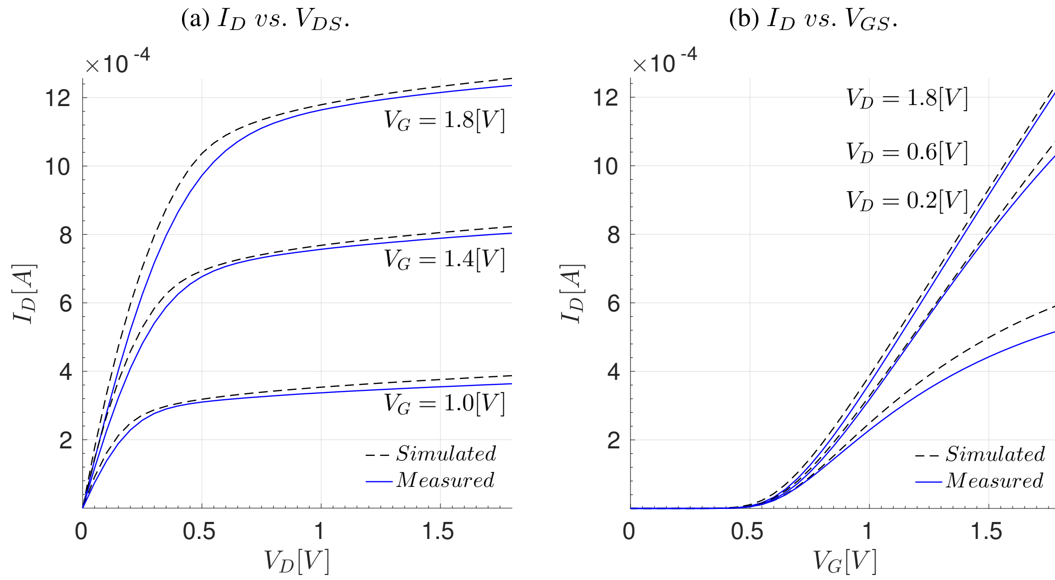
$$RMS_{diff} = \frac{100}{N} \sqrt{\sum_{i=1}^{N} \left(I_{D_{diff}}\right)^2} \quad (8.2)$$

Moreover, the related current differences are analyzed in the region in which their ratio is constant, i.e., in strong inversion and for small CLM (low V_{DS}). In this region the ratio $(W/L)_{eff}$ (or $I_{D_{diff}}$) should be constant, since it only depends on the aspect ratio of the two devices.

Figure 8.1 shows a comparison of the $I_D\ vs.\ V_{DS}$ and $I_D\ vs.\ V_{GS}$ between simulated versus measured values for an $nELTX1L1$ designed in $180\ nm$. In these behaviors, the parametric voltages are $V_{GS} = 1.8$, 1.4, and 1.0; and $V_{DS} = 1.8$, 0.6, and 0.2, respectively.

In the same manner, Table 8.2 shows the RMS numerical values for various different

Figure 8.1: Characteristics for $nELTX1L1$ in 180 nm: a) I_D $vs.$ V_{DS} and b) I_D $vs.$ V_{GS}.



Source: Author.

drive strengths (X) and channel lengths (L) for the two test chips fabricated.

Table 8.2: RMS Difference between simulated and measured drain current values for nELT devices (in $[\%]$).

Node	600 nm				180 nm			
$nX1$	$L1.2$	$L2$	$L5$	$L10$	$L1.2$	$L2$	$L5$	$L10$
	10.36	14.38	12.34	1.71	1.37	2.01	3.60	0.59
$nL1$	$X1$	$X1.5$	$X2$	$X3$	$X1$	$X1.5$	$X2$	$X3$
	8.51	9.21	9.18	8.36	1.27	0.32	0.33	0.28
$pL1$	$X1$	$X1.5$	$X2$	$X3$	$X1$	$X1.5$	$X2$	$X3$
	16.86	18.00	16.11	15.62	8.88	5.39	6.22	6.59

8.2.3 Series and parallel arrangements

Tables 8.3 and 8.4 display the root-mean-square difference between simulated and measured drain currents for a group of devices stacked in series and in parallel, respectively.

Table 8.3: RMS Difference between simulated and measured drain current values for n,pELT devices in series (in [%]).

	600 nm		180 nm		
	$Sr2$	$Sr4$	$Sr2$	$Sr3$	$Sr4$
$K_n(1)$	7.27	10.71	4.01	8.10	9.03
$K_n(x)$	10.98	33.27	3.15	2.85	6.61
$K_p(1)$	17.53	17.35	19.49	20.32	20.77

Table 8.4: RMS Difference between simulated and measured drain current values for nELT devices in parallel (in [%]).

	600 nm			180 nm		
	$Pr2$	$Pr3$	$Pr4$	$Pr2$	$Pr3$	$Pr4$
$nX1$	7.66	6.46	5.33	0.39	0.80	0.87
$pX1$	6.64	9.88	6.63	16.60	15.65	15.38

8.2.4 Ring Oscillator

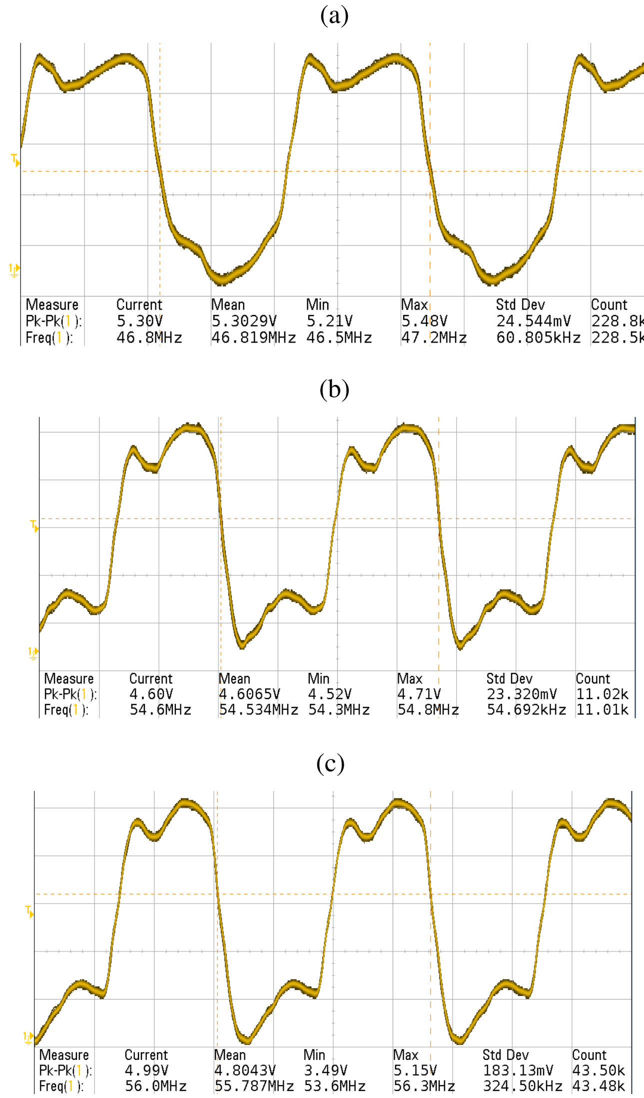
Figure 8.2 and Table 8.5 show the output oscillation frequency, graphically and numerically, respectively. The inverter-based ring oscillators in 600 nm are proposed in three configurations. The first configuration, $ROsc\, n, pSTD$, employed standard transistors in both pull-up and pull-down network. The second configuration, $ROsc\, n, pELT$, was laid-out with ELT devices in both networks. The third configuration, $ROsc\, nELT, pSTD-2F$, employed $nELT$ devices in pull-down network and $pSTD$ two fingered devices in pull-up network.

The oscillation frequency of the enclosed layout oscillator is roughly 15% above that of the standard layout, which was expected given the asymmetric characteristic of the ELT layout. Even though the better performance observed was from $n, pSTD$ to $nELT, pSTD - 2F$ by applying transistor folding, the FoMs is even better employing ELTs, when comparing $nELT, pSTD - 2F$ to $n, pELT$. Nevertheless, based on Monte Carlo's simulations, seen in Table 5.8, by introducing ELT structures into inverter cells, the device area is increased and, consequently, the standard deviations are reduced.

Table 8.5: Ring oscillators frequency comparison.

Conf.	FOsc. meas. $[Hz]$	FOsc. sim. $[Hz]$	Diff.
$n, pSTD$	46.81 M	54.97 M	148 m
$nELT, pSTD-2F$	54.53 M	60.49 M	98 m
$n, pELT$	55.78 M	55.97 M	3 m

Figure 8.2: Ring Oscillators' output characteristics for: a) $n, pSTD$, b) $nELTpSTD2F$ and c) $n, pELT$.



8.2.5 Summary and Discussion

Based on the measured and simulated standard devices, shown in Table 8.1, stronger deviations from the models were expected for the 600 nm technology node and for p-type devices. Despite the use of the enclosed geometry, the SPICE simulated individual devices with different aspect ratios and lengths showed good agreement with the measured data, as

presented in Table 8.2. This is in agreement with the works of (ANELLI et al., 1999) and (GIRALDO; PACCAGNELLA; MINZONI, 2000), who proposed the methodology for the equivalent (W/L) calculation.

The deviation from simulation observed for nELTs and pELTs of both technology nodes was similar to that of the standard devices. Overall, the best agreement was observed for long devices $(L10)$, while no direct dependence was observed in terms of the aspect ratio, X. Also, it is noteworthy that the relative difference was more significant for a lower gate and drain voltages, as observed in Fig. 8.1 (a) and 8.1 (b).

This is an important aspect of methodology validation; there was no need to fully characterize and model the ELTs in order to obtain adequate simulations. Simulation results were obtained using conventional commercial PDKs and CAD tools. Naturally, though, full characterization and modeling of ELTs may provide better and more reliable circuits.

For a series association of ELTs, the simulated and measured results showed good agreement with the minimum-sized transistors. While the introduction of the multiplicative factor K did not significantly affect the difference for most cases, when the K parameter was introduced for the 4-stacked series transistors in the $600\ nm$ technology, the difference increased significantly, as shown in Table 8.3. Further studies on the multiplicative K factor in ELTs for transistors in series are still required.

For the parallel association of ELTs, the difference between simulated and measured was roughly independent on the number of transistors in parallel. Interestingly, the observed relative difference was smaller than that of the individual minimum-sized transistor for the $600\ nm$ technology, and larger for the same individual device in the $180\ nm$ technology.

The increase in the oscillation frequency of the ring oscillator is attributed to the decision of placing the drain inside the enclosed gate. Comparatively to the ring oscillator designed with equivalent standard transistors, the ELT presents lower drain capacitance and, thus, a faster switching speed.

8.3 During and post irradiation

8.3.1 Introduction

Following the irradiation procedures, given by the European Space Agency (ESA) Basic Specification 22900 (AGENCY, 2016), the ICs were exposed to ionizing radiation

under a Cobalt-60 (^{60}Co) gamma radiation source ($\gamma - ray$). Moreover, the test circuit board was exposed to a maximum total ionizing dose of $500\ krad(Si)$ at a dose rate of $700\ rad(Si)/h$ within 29 intermediate TID measurement steps.

Large signal measurements were performed using a Parameter Analyzer ***Keithley 4200A-SCS*** with a test fixture ***Agilent 16442B***, at a room temperature of $25°C \pm 1°C$.

To maximize the TID effects, during the irradiation procedure, the devices were biased at worst case scenario, i.e., biased in order to provide the highest electric field at the transition between thin and thick oxide and the gate stack (i.e., Si/SiO_2 interface). Thus, the respective applied voltages for n,pMOS devices during irradiation were:

nMOS: $V_D = V_G = V_{DD}$ and $V_S = V_B = V_{SS}$ and,

pMOS: $V_D = V_G = V_{SS}$ and $V_S = V_B = V_{DD}$,

where the subscript letters $D,\ S,\ G,\ B,\ SS$, and DD, referee respectively to drain, source, gate, bulk, ground and the power supply.

These voltages maximize the formation of the inversion layer in the channel region. Thus, the accumulation of trapped charges in the insulating layers and reversely biased PN junctions maximize the TID effects as well.

After the irradiation procedure, the test circuits were maintained both at worst case situation for bias condition, and at room temperature of $25°C \pm 1°C$ during 24h. After this period, all terminals were biased at V_{SS} and the test circuits were annealed during 168h at $100°C$.

For characterization of the transistors during irradiation, the group of devices in the $600\ nm$ worked as expected. Unfortunately, due to a malfunction in the ESD protection for the $180\ nm$ instances, the electrical characterization was jeopardized. This issue forbid the access to the PAD-connected instances and the proper evaluation of this technological node during the irradiation experiments. Therefore, the irradiation experiments is only presented for $600\ nm$.

It is important to clarify that the ESD protection was embedded only with ELTs devices using the same automated geometry generation, which has been prior validated to the entire group of cells. Therefore, I claim that the problem it is not in the devices themselves. On the other hand, as ESD projects, at first sight, run out of the scope of this work they were not exhaustively analyzed. Hence, what I proposed was the use of a simple topology and sizing, following the same foundry-provided PAD-protection applied to ELTs. For some reason, either the gate sizing or the ESD chosen topology seemed to

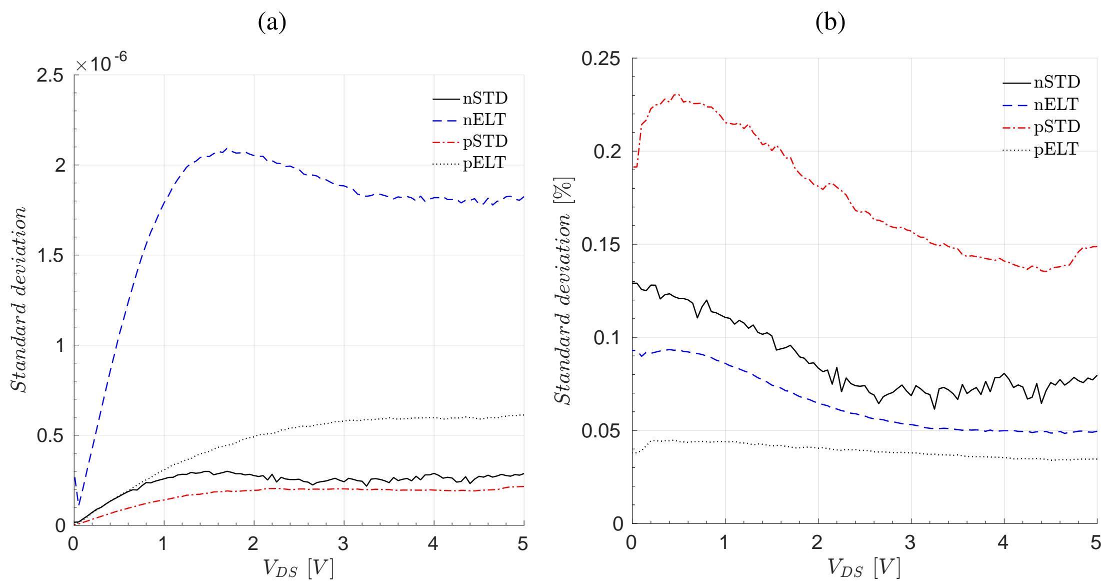
be unsuitable for ELTs. A proper ESD project design only with ELTs should be better investigated in future works.

8.3.2 Measured data $(600\ nm)$

Prior to irradiation, in order to estimate the measurement error, both the output characteristic $(I_D\ vs.\ V_{DS})$ and the transfer function $(I_D\ vs.\ V_{GS})$ of each individual standard and enclosed layout transistor were acquired five consecutive times. Based on the measured values, for each group of consecutive measures, the average $(\bar{x})$ and the standard deviation (σ) were calculated.

The calculated standard deviations are depicted in Figs. 8.3 and 8.4 for $(I_D\ vs.\ V_{DS})$ and $(I_D\ vs.\ V_{GS})$, respectively. Their values were calculated based on five consecutive measurements.

Figure 8.3: Standard deviation for output characteristic $(I_D\ vs.\ V_{DS})$ in a) absolute value, and b) expressed in percentage.



Source: Author.

The numerical values for σ of I-V characteristics are presented in Table 8.6. Their values, both absolute and in percentage, presented for output characteristic and transfer function, are explicit for the four devices (i.e., n,pMOS STD and ELT).

The measured output characteristics $(I_D\ vs.\ V_{DS})$ at different total doses for the n- and p-channel standard devices are presented in Figs. 8.5 (a) and 8.6 (a), respectively; the measured transfer functions $(I_D\ vs.\ V_{GS})$ at different total doses for these devices are

Figure 8.4: Standard deviation for transfer function ($I_D\ vs.\ V_{GS}$) in a) absolute value, and b) expressed in percentage.

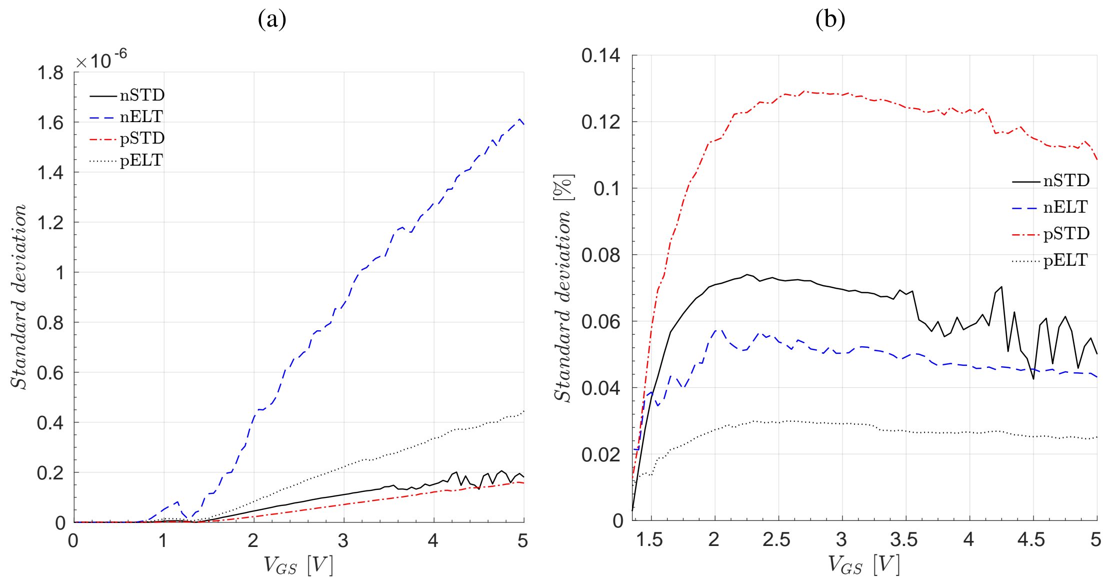


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Table 8.6: Values for standard deviation.

	$I_D\ vs.\ V_{DS}$		$I_D\ vs.\ V_{GS}$	
	$\sigma\ [A]$	$\sigma\ [\%]$	$\sigma\ [A]$	$\sigma\ [\%]$
$nSTD$	$299.51n$	0.13	$206.22n$	5.02
$nELT$	2.09μ	0.09	1.61μ	1.42
$pSTD$	$215.23n$	0.23	$159.98n$	0.12
$pELT$	$611.98n$	0.04	$445.15n$	0.02

presented in Figs. 8.5 (b) and 8.6 (b).

Figures 8.5 (c) and 8.6 (c) present the output characteristics at different total doses for the n- and p-channel ELTs, respectively; whereas, Figs. 8.5 (d) and 8.6 (d) depict the transfer functions at different total doses for these devices. In these cases, the devices were analyzed in strong inversion and saturation i.e., the parametric variable was biased at V_{DD} or V_{SS} for n and pMOS devices, respectively.

A compendium of some numerical values for I-V plots is given in Table 8.7. They cover some intermediate representative steps of ionizing exposure doses.

In all cases, the reference is considered as pre-incidence of radiation (i.e., $0\,rad(Si)$), where the deviation is calculated as defined in (8.3).

$$deviation = \left[\frac{(x)\,rad\,(Si) - (0)\,rad\,(Si)}{(0)\,rad\,(Si)}\right] \cdot 100[\%] \tag{8.3}$$

Figure 8.5: $I_D\ vs.\ V_{DS}$ and $I_D\ vs.\ V_{GS}$ nMOS characteristics, respectively for: STD devices (a) and (b); and ELT devices (c) and (d).

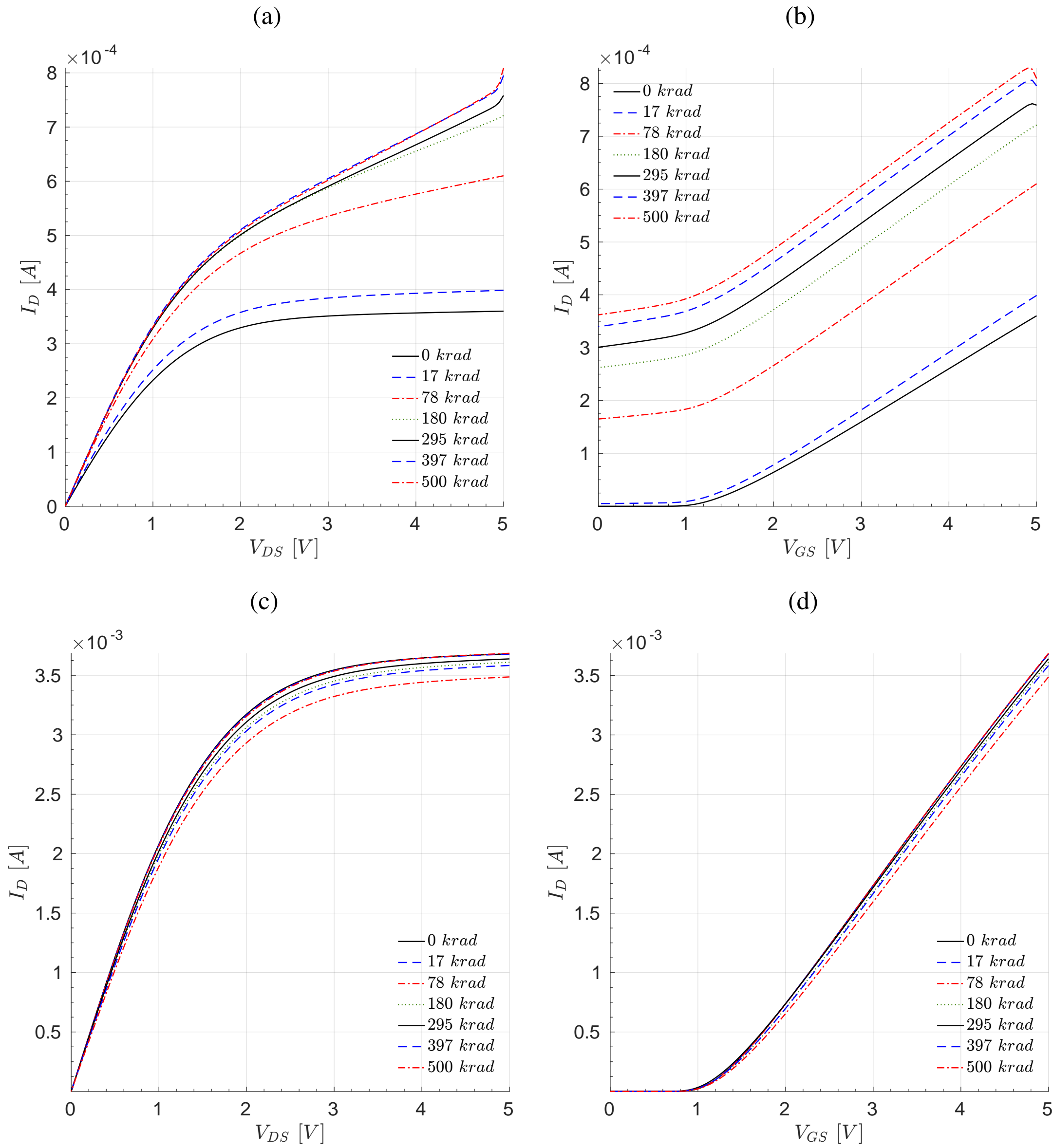

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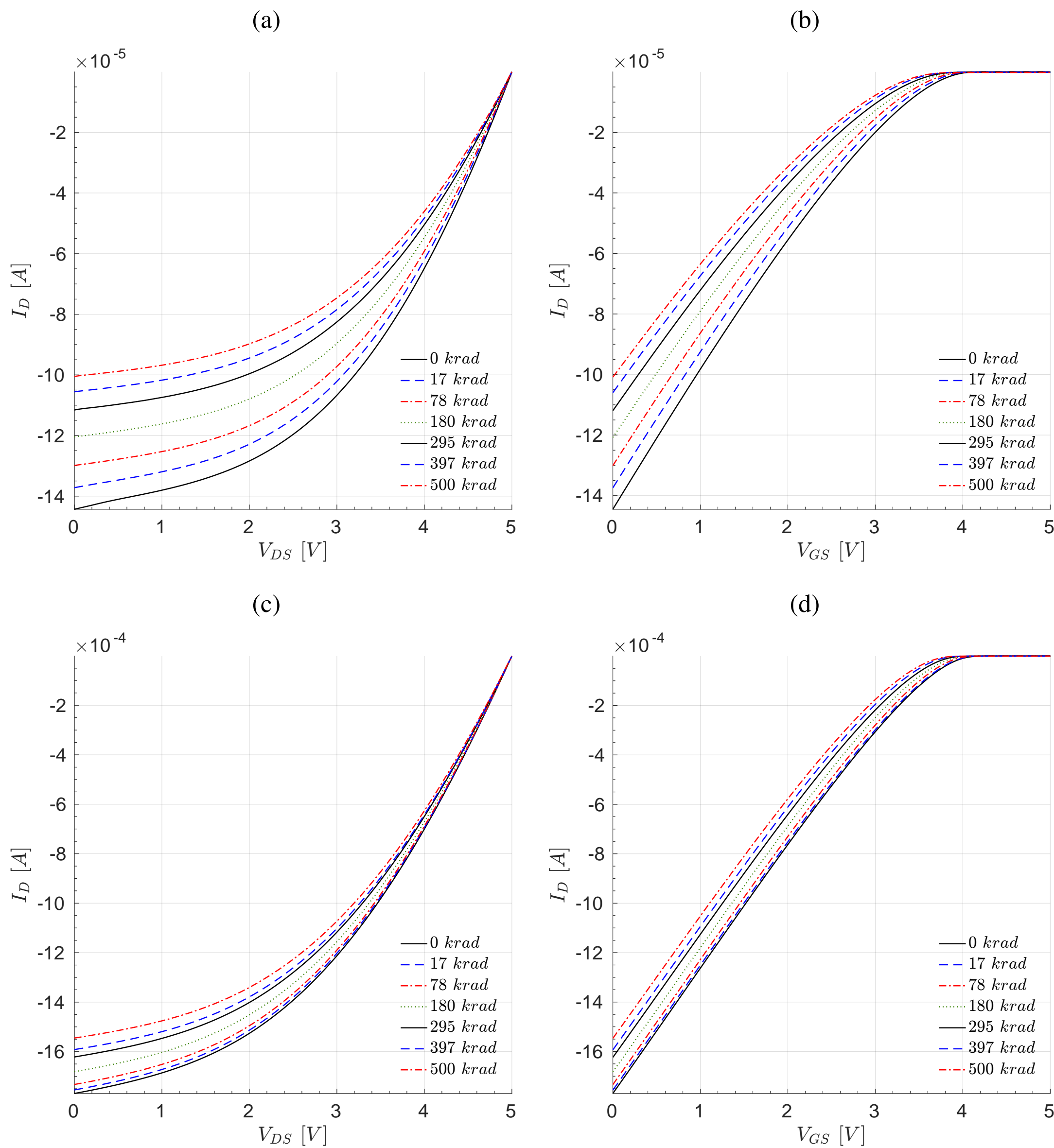
Table 8.7: Values for $I_D\ vs.\ V_{DS}$ and $I_D\ vs.\ V_{GS}$ for n,pMOS devices up to $500krad(Si)$.

	$(I_D\ vs.\ V_{DS})\ dev.\ in[\%]$				$(I_D\ vs.\ V_{GS})\ dev.\ in[\%]$			
	nMOS		pMOS		nMOS		pMOS	
$krad(Si)$	STD	ELT	STD	ELT	STD	ELT	STD	ELT
17	10.69	−0.05	−4.93	−0.80	10.66	0.00	−4.89	−0.75
78	69.41	0.12	−10.01	−2.05	69.32	0.14	−9.98	−2.02
180	100.28	−1.92	−16.53	−4.98	100.15	−1.89	−16.43	−4.92
295	110.57	−1.15	−22.69	−8.33	111.33	−1.10	−22.53	−8.25
397	120.82	−2.65	−26.84	−10.03	123.65	−2.65	−26.65	−9.96
500	124.61	−5.27	−30.36	−12.66	130.02	−5.26	−30.21	−12.60

Figure 8.6: I_D $vs.$ V_{DS} and I_D $vs.$ V_{GS} pMOS characteristics, respectively for: STD devices (a) and (b); and ELT devices (c) and (d).



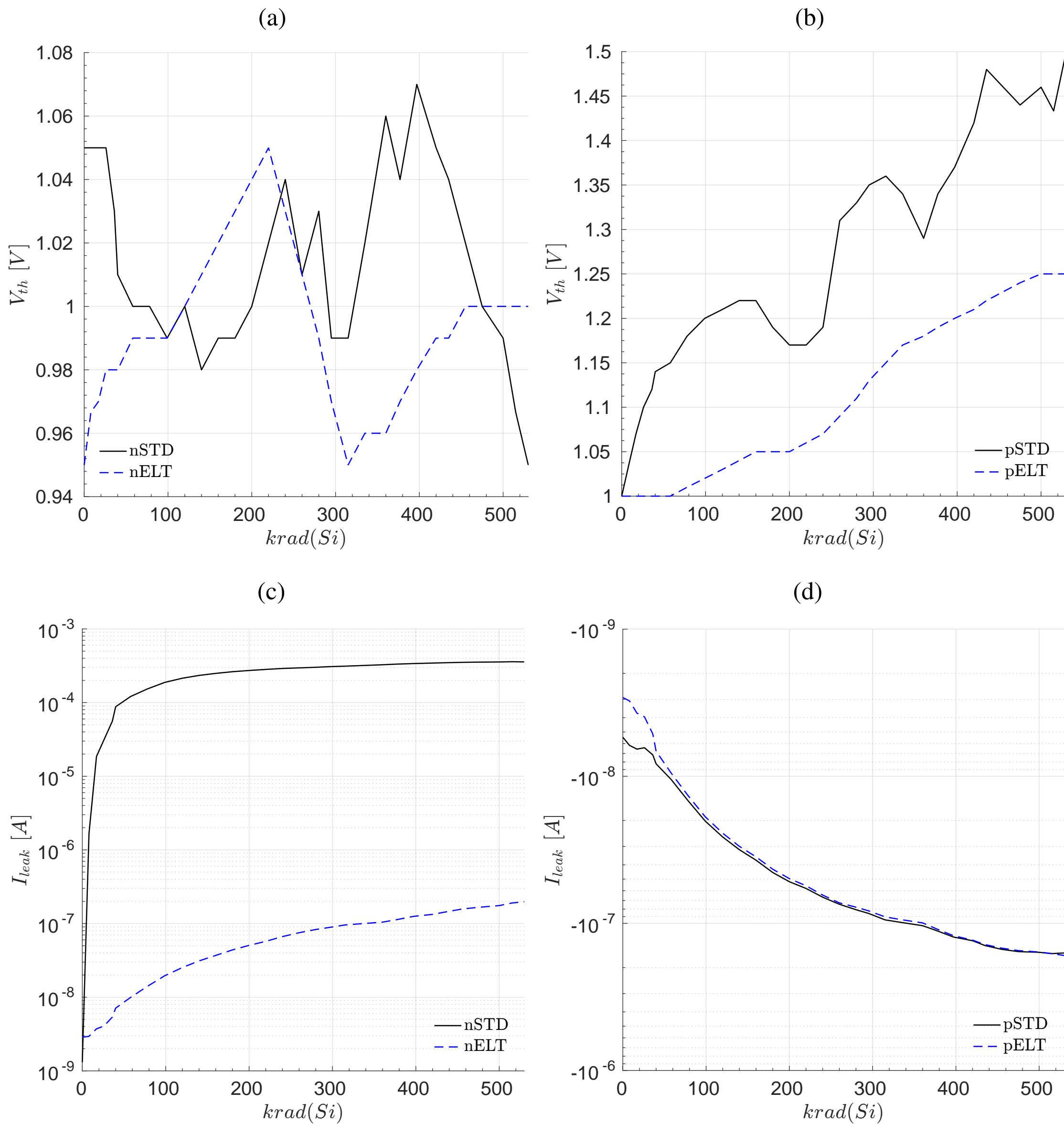
Source: Author.

Based on the values presented in Table 8.7, the transconductance g_m is calculated. Once the g_m is known, the threshold voltage (V_{th}) is calculated as the maximum absolute value of Δg_m. Following these preceding definitions, Figs. 8.7 (a) and 8.7 (b) show the V_{th} trends for n and pMOS devices, respectively. The plots include some radiation steps in order to compare the influence of radiation.

The leakage drain current (I_{leak}), as a function of total dose for both n- and p-channel standard and enclose layout devices, is presented in figures 8.7 (c) and 8.7 (d).

The I-V Annealing response is presented in Fig. 8.8, only for pMOS devices. The

Figure 8.7: Trends for V_{th} respectively for: (a) nMOS, and (b) pMOS devices; and I_{leak} respectively for: (c) nMOS and (d) pMOS devices.



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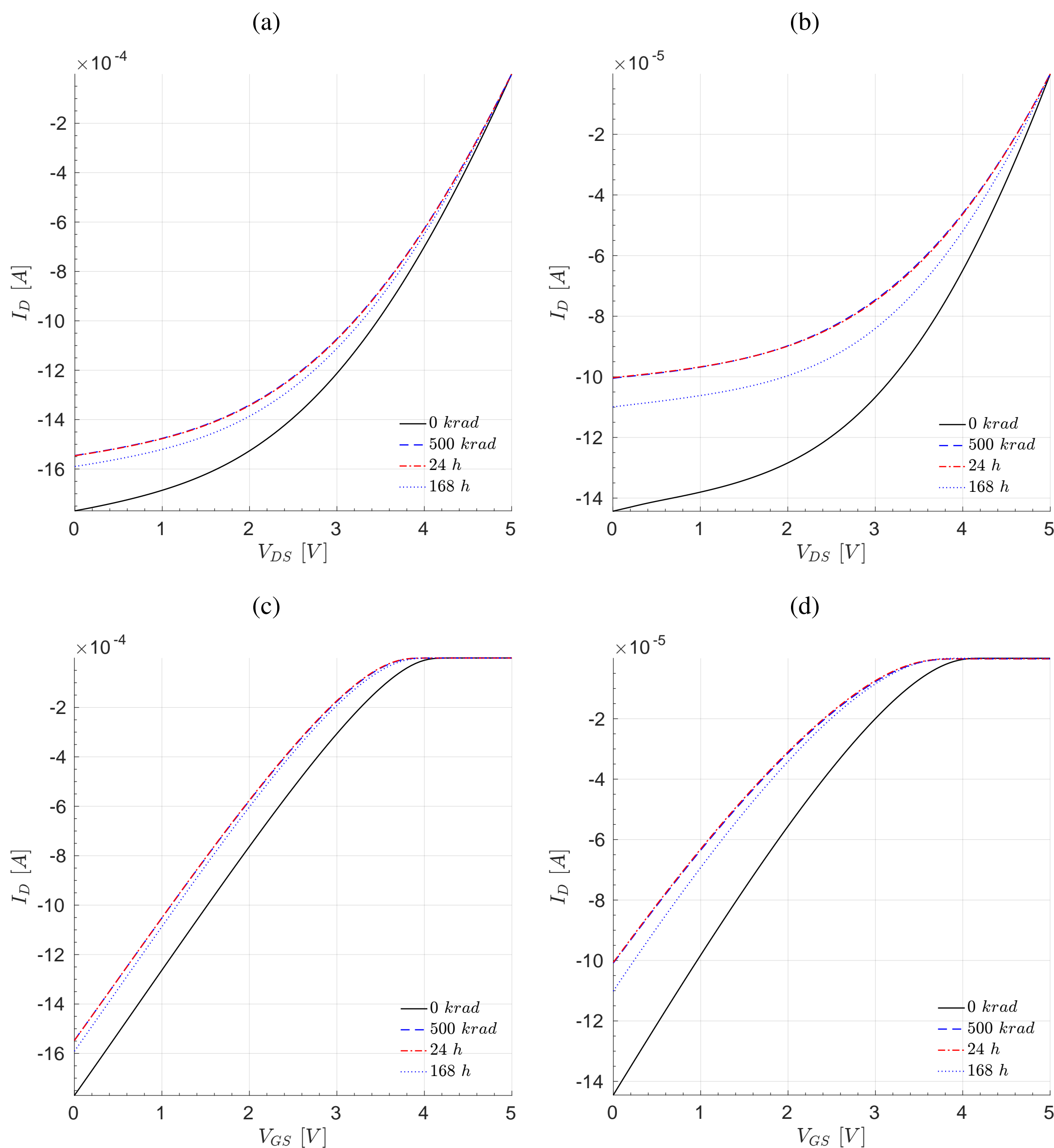
plots show the effects measured for $24h$ and $168h$ compared with base and final exposure (i.e., $0\ krad(Si)$ and $500\ krad(Si)$, respectively). The $I_D\ vs.\ V_{DS}$ and $I_D\ vs.\ V_{GS}$ behavior for pSTD and pELT are respectively organized in 8.8 (b) and 8.8 (d); 8.8 (a) and 8.8 (c).

8.3.3 Summary and Discussion

Considering the pre-irradiation measurements, it is possible to verify that absolute values for standard deviation are higher for ELT devices when compared to STD geometry.

Figure 8.8: Annealing effects measured for $24h$ and $168h$, respectively for: (a) and (c) pELT; and (b) and (d) pSTD.



Source: Author.

This behavior is expected because the effective currents are higher for ELTs. Also, it should be noted that nMOS currents (and, consequently the σ) should be higher when compared to pMOS.

The standard deviation, given in percentage, however, provides more valuable insight on radiation tolerance. The STD devices present a higher normalized standard deviation when compared to the ELT. Since the area increases, the variability should be reduced. Thus, the measured differences for enclosed devices should be small, taking into account the absolute current values.

Regarding the measurement error, the observed standard deviation was sufficiently small, so that it did not affect the reliability of the measured data.

It should be noted that data from irradiation and annealing experiments are scarce in the literature, especially when considering a specific node (as is the case of $600\ nm$ technology); thus, it is difficult to provide quantitative analysis and comparison to other works. Similar adversity was also reported by Gaillardin *et al.* (GAILLARDIN et al., 2013). Nonetheless, the qualitative behavior of the devices characterized in this study is in accordance with the literature (ANELLI, 2000; SNOEYS; GUTIERREZ; ANELLI, 2002; GREIG et al., 2013).

The leakage current, the most sensitive parameter for deep submicron technologies subjected to ionizing radiation, is primarily discussed. An increase of approximately 3 orders of magnitude has been observed when comparing nSTD vs. nELT devices irradiated up to $500\ krad(Si)$.

Works of Anelli (ANELLI, 2000) and Snoeys *et al.* (SNOEYS; GUTIERREZ; ANELLI, 2002) have reported similar trend; nonetheless, for a channel length of $280\ nm$, and up to 30 and $40\ Mrad(Si)$, respectively. In both works the leakage current increase was approximately 6 orders of magnitude. The data reported by Greig *et al.* (GREIG et al., 2013) for $180\ nm$ and $500\ krad(Si)$ also corroborates these findings, with an evidence of an increase of 3 orders of magnitude in I_{leak}.

Conventionally pMOS devices do not require enclosed geometry, because the accumulation of positive charges has a negative (decreasing) effect on the leakage current (ANELLI, 2000). To the best of our knowledge, practical results of ELTs with these devices are unavailable in the literature; hence, it is not possible to compare to other works. Nonetheless, it is reported, for the first time, results comparing pMOS devices with and without enclosed geometry. Indeed, it was observed a negligible difference in I_{leak} (less than 1%) when comparing STD against ELT irradiated up to $500\ krad(Si)$.

Taking into consideration the absolute value for V_{th} of nMOS (Fig. 8.7 (a)), I consider that it remains relatively stable over the irradiation steps and, thus, verified as a constant — varying between $0.96\ V$ to $1.06\ V$, which represents less than 2% off V_{DD}. In case of pMOS devices (Fig. 8.7 (b)), a slightly increment in the absolute value was observed; the V_{th} value for pSTD has increased approximately 9%, whereas the pELT 5%. Moreover, the greater variation identified in the behavior of pMOS devices is pointed out to be better investigated in future work.

The effect of the annealing phase on pMOS devices is depicted in Fig. 8.8. Consid-

ering the last radiation step, as expected, the annealing brings back both $I_D \ vs. \ V_{DS}$ and $I_D \ vs. \ V_{GS}$ to their original characteristics. The pSTD current was moved by 0.04% and 9.5%, respectively for $24h$ and $168h$ of annealing. These values are related to maximum absolute value of I_D, acquired in $I_D \ vs. \ V_{DS}$ for $500 \ krad(Si)$. Similarly, pELT returned 0.3% and 3.1%, respectively. Unfortunately, during this phase, the nMOS devices have malfunctioned (probably due to electrostatic discharge - ESD); so, the annealing data for nMOS devices is unavailable.

Finally, it is important to report to the reader that a delay of almost 9 months passed from the tape-out to the beginning of the irradiation experiment due to bureaucratic and minor technical issues. Moreover, the test chips may have experienced some “mechanical stress” during the land-based transport from Porto Alegre - RS to São José dos Campos - SP.

In addition, at the beginning of the experiment (approximately at $170 \ krad(Si)$), a power failure momentarily interrupted the irradiation procedure. Although the energy loss period was not significant (approximately $24h$) considering the whole irradiation experiment (approximately $740h$), a slightly unplanned recover should be expected. The effects of these mechanical stress, delay to measurements, and momentarily power failure are very difficult to predict and deviate from the scope of this work. Nonetheless, I consider very important to share these information with the reader.

9 CONCLUSION

9.1 Final discussion

In this thesis, the development of a complete Radiation-Hardening by Design (RHBD) flow methodology was proposed. The methodology embedded enclosed layout transistors (ELTs) and guard rings, two well effective hardening techniques. Moreover, the flow methodology, transparent to the designer, is fully compatible with commercial CAD tools and standard fabrication processes. In order to achieve these goals, some state-of-the-art improvements to key points of the ICs design flow such as the template proposal for digital cells, as well as their series and parallel arrangements were developed. Therefore, the automated calculation of the effective aspect ratio (W/L) of the ELTs; complete template proposals meeting lithography rules; the calculation of PN ratio and output buffers dimension using Logical Effort (LE) methodology; test structures and, finally, the irradiation test were performed in order to meet the design steps and their requirements.

Integrated Circuits (ICs) exposed to the incidence of ionizing radiation suffer undesirable effects such as upsets or damages in the devices' materials. In this manner, space and satellite (S&S) and, even on the ground level, High Energy Physics (HEP) applications are severely affected by ionizing radiation.

After the interaction of ionizing radiation, electron-hole pairs $(\bar{e}/h)$ are produced. The movement of these charges when occurs in reverse-biased PN junctions and in silicon dioxide may cause long term degradation in semiconductor device's materials. The most prominent observable effects of this charge movement are the shifting in the device threshold voltage and increase in the leakage current, in this last case considering both intra- and inter-device.

To harden a device against ionizing radiation, various techniques can be applied through entire IC design flow hierarchy, from the system architecture to the layout of a single transistor. Nonetheless, the decision of hardening the basic building block of any IC at the layout perspective, i.e., the single transistor, achieve highest levels of tolerance against long term exposure, maintaining the possibility to embed other system level mitigate proposals. In this perspective, two major design techniques are employed; the use of enclosed devices and guard rings.

The challenge of using enclosed devices is the prediction of the effective (W/L)

aspect ratio. This occurs because there is not a physical equivalent to the transistor's width in annular geometries. In this sense, this work performed a deep investigation and research in the literature among the main and largely adopted enclosed devices, choosing two proposals — in which, between them, there is only a minor difference in the gate's corner regions to satisfy the possibility to perform 45 or $90°$ angle in polysilicon layer. Additionally, was proposed the individualization of two internal model's variables to enable the use of a wider range of aspect ratios.

To calculate the gate sizes of digital cells, PN ratio and output buffers, the method of Logical Effort (LE) was adopted. The use of this method was employed for the first time, for the sake of our knowledge, in the Radiation-Hardening context with enclosed devices.

Therefore, to validate the methodology of RHBD ELT-based library cells design flow and to qualify the hardness degree of ELTs, two test chips were designed. Characterization at the electrical level were performed pre-, during and post-irradition. Prior radiation, the large signal measurements show that individual SPICE simulated devices with different aspect ratios and lengths displayed good agreement with the experimental data, which is a very important aspect of the proposed methodology — there was no need to fully characterize and model the ELT devices in order to achieve reasonable accurate simulation results.

Regarding during and post-irradiation and annealing results, it was difficult to provide comparative analysis due to the scarce reported data in $600\ nm$. Nonetheless, the qualitative insight was in accordance with findings in the literature. The hardening characteristics of proposed cells are meet. In a comparison between nSTD versus nELT devices (irradiated up to $500\ krad(Si)$), an increase of almost 3 orders of magnitude was observed in standard devices. In this sense, in addition to irradiation results for nELT devices, this work contributed to increment the scarce experimental data reported for pELTs — because they do not require enclosed geometry, since the effect on the leakage current has the opposite behavior. Finally, yet less than 10% but, as expected, the annealing phase brings back output and transfer characteristics to their original behavior.

Summing up, the main goal of this thesis was achieved; a complete RHBD design flow methodology was proposed having its steps transparent to the designer and complaining with commercial CAD tools. The fabricated test chips were useful to validate and consolidate the theoretical concepts, showing that the flow proposal is suitable for more complex cells. The automation of design geometries has been validated as a feasible and

elegant solution to be employed not only in the academic context but also to improve the Brazilian IC industry.

During the execution of this thesis, various technical challenges have been faced. Eventually, some difficulties have seemed unsolvable during the development this work as, for example, the automated generation of device's geometries in the "LEF" file, embed the (W/L) calculation into the CAD tool, DRC of new devices whose were outside of the commercial deck, the abutment proposal in series and parallel ELT arrangements and the test chip itself. Nonetheless, it is known that the complete path for the development of the complete flow methodology is extremely long and some further improvements in specific phases are opportune.

Therefore, in the upcoming Section, some future works are addressed.

9.2 Future works

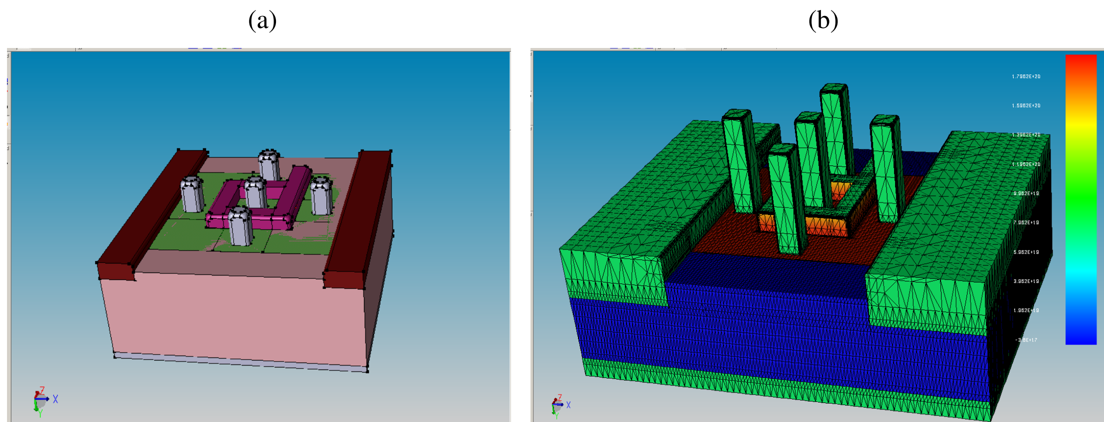
As a continuation of this work, I am very confident to propose the possibility of improving some clear, and advanced, research fields:

a) To improve TCAD simulations: To simulate a device through Technology Computer-Aided Design (TCAD) tool is necessary to describe either the entire fabrication process or device's geometries, doping profiles and diffusion regions. By calculating the device's geometries, analogously to the generation of ELT's GDSII output files, it is possible to design a device to TCAD context. In this sense, some work has been already initiated. As depicted in Fig. 9.1 (a) and (b), which represent an ELT geometries definitions and its diffusion profile, respectively. By improving some methods (coded in C language), it will be possible to analyze further TID hardened proposals as, for instance, reported by (XIE et al., 2019).

b) To extend analytic studies: To extend analytic studies: Some of the technical pillars of this thesis are the ability to simulate and analyze the device's IV characteristics. Hence, as future work, the improvements and expansion of simulated devices and topologies can be performed. To analyze and compare SPICE versus TCAD simulation results, depicted in Fig. 9.2 (a) and (b), are examples of output characteristic and transfer function, respectively for $L = 180\ nm$ and $L = 360\ nm$.

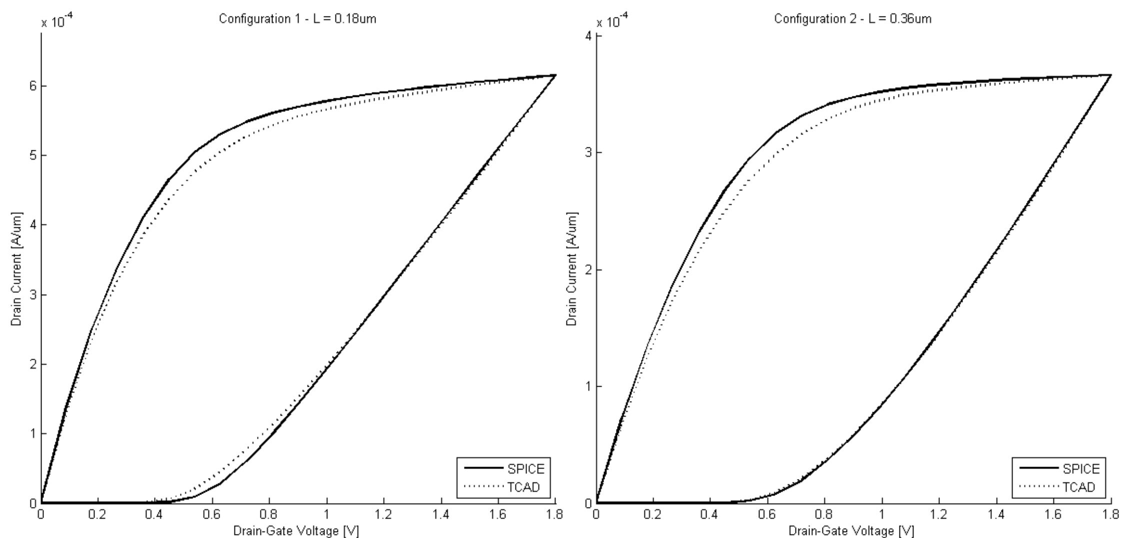
Figure 9.1: TCAD ELT doping profile: a) Geometries definition and b) Diffusion.

(a) (b)



Source: Author.

Figure 9.2: TCAD versus SPICE simulation results for an ELT device:Left side for $L = 180\ nm$ and right side $L = 360\ nm$ (in both cases: $I_D\ vs.\ V_{DS}$ with $V_{GS} = V_{DD}$ and $I_D\ vs.\ V_{GS}$ with $V_{DS} = V_{DD}$).



Source: Author.

c) <u>To investigate and debug ESD structures</u>: A proposal for ESD protection was laid-out and tested in the 180 nm test chip. Nonetheless, for an unknown reason, the structures presented functional failure. I suppose that the problem could be at the layout level. As future work, a deep investigation around these structures may be performed.

d) <u>To continue and improve CAD automation</u>: The core of this thesis is the automation of CAD tools. Thus, there are many MATLAB, C, SKILL, C#, and even some Perl developed/implemented codes. As future work, I conceive that the most substantial

research field is to expand and improve any of the developed codes for design geometries or to include some CAD functionalities.

e) <u>To continue irradiation tests</u>: The test chips can be characterized for higher TID levels.

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APPENDIX A — SUMMARY IN PORTUGUESE

A.1 Introdução

A.1.1 Motivação

Ao se observar o sucesso da tecnologia CMOS, é indispensável a referência ao contínuo progresso do escalamento tecnológico. O agressivo aumento no nível de integração tem conduzido a indústria semicondutora a um progresso vertiginoso, aprimorando recursos e funções de Circuitos Integrados (CIs) neste processo (PELLISH, 2012).

Para sintetizar circuitos complexos, os quais agregam um enorme número de funcionalidades e recursos (por exemplo, microprocessadores ou Circuitos Integrados de Aplicação Específica - ASICs), a utilização de um fluxo de projeto automatizado é inerentemente necessária, a fim de reduzir tempo de projeto e custos de produção. O cerne desse processo se constitui de um grupo de células digitais pré-projetadas e devidamente caracterizadas, nomeado de biblioteca digital. Estas células são o elo de ligação entre as ferramentas de CAD, as quais possibilitam a descrição em alto nível do sistema (descrito em linguagem de descrição de hardware como, por exemplo, VHDL ou Verilog) e a efetiva implementação física do sistema (SCHUCH et al., 2009).

No entanto, a incidência de radiação ionizante pode resultar em efeitos indesejados nos CIs, como perturbações transientes ou danos permanentes nos materiais dos dispositivos. Assim, aplicações sujeitas a ambientes radioativos podem operar de forma imprevisível, reduzindo sua confiabilidade e tempo de vida útil (LIU et al., 2014b; KNUDSEN; CLARK, 2006).

Dispositivos em aplicações operando ao nível do mar são naturalmente menos susceptíveis à incidência de radiação ionizante quando comparados aos de aplicações aeronáutica ou aeroespaciais (S&S); isto ocorre, sobretudo, devido à presença do campo magnético natural da Terra. O campo magnético aprisiona partículas ionizantes, especialmente as expelidas da Massa Coronal solar, dando origem aos cinturões de radiação conhecidos como Cinturões de Van Allen. Contudo, aplicações espaciais e, mesmo aquelas ao nível do mar, como aplicações para física de alta energia (HEP), são severamente afetadas pela radiação ionizante (VELAZCO et al., 2007, BOUDENOT in).

A proposta de implementação física mais robusta referenciada como *"Radiation-Hardening by Design"* (RHBD) provê a possibilidade de se elevar a tolerância à Dose

Total Ionizante (TID). Ao se utilizar técnicas de RHBD é possível atenuar tanto efeitos de TID quanto Efeitos de Eventos Únicos (SEE), devido à combinação de técnicas de tolerância tanto no nível de projeto quanto no nível de implementação física (KNUDSEN; CLARK, 2006). No contexto de automatização do fluxo de projeto, o maior desafio se encontra no fato de que bibliotecas de células com técnicas de tolerância não se encontram disponíveis comercialmente sendo, portanto, objeto de propriedade intelectual (IP) sujeitas às normas territoriais (CHANG et al., 2014).

Ao passo que HEP, S&S, sistemas de controle confiáveis e a exploração do espaço têm sido estudados e subsidiados em outros países (como EUA, China e França) (YIN et al., 2016), aqui no Brasil são objeto de estudos relativamente recentes. Em nosso contexto (indústria de pesquisa e desenvolvimento de circuitos integrados no Brasil), o conhecimento para o desenvolvimento de tais dispositivos tem se tornado um interesse crescente nos últimos anos. Isso ocorre mesmo nos casos em que não há embargos territoriais como, por exemplo, a regulamentação do governo dos EUA que proíbe ou dificulta a exportação de seus componentes eletrônicos tolerantes à radiação aos demais países impedidos pelo ITAR *("International Traffic in Arms Regulations")* (VAZ, 2015).

O Brasil compra estes IPs mas não os fabrica e, ao longo do tempo, a carência desta tecnologia não apenas suprime oportunidades de pesquisa e desenvolvimento, como também aumenta drasticamente os custos de compra de dispositivos tolerantes e confiáveis.

Assim, de modo a prover CIs tolerantes à radiação, esta tese apresenta uma metodologia para o desenvolvimento de biblioteca de células RHBD na tecnologia *bulk* CMOS, utilizando restrições reais de projeto. Deste modo, avanços ao estado-da-arte em pontos-chave do fluxo de projeto de CIs são propostos: a análise e implementação de modelos para o cálculo da estimativa da razão de aspecto (W/L); e o projeto de células integralmente otimizadas, baseadas em premissas analógicas, gerando os arquivos de caracterização necessários e compatíveis com o fluxo de projeto comercial. Estas contribuições são cruciais para fomentar a prática da indústria brasileira de semicondutores para a fabricação de circuitos RHBD.

No entanto, com relação às análises técnicas e ao desenvolvimento, nós entendemos que a maior contribuição desta tese, a qual exigiu um grande empenho (e alguma experiência), foi reunir todo o conhecimento desde os primeiros passos de projeto (isto é, desde o transistor) até os passos finais (isto é, implementação final das células).

Além disso, esta tese implementa todas as técnicas de RHBD para os nós tecnológicos disponíveis na indústria Brasileira de semicondutores, possibilitando que toda a cadeia

de produção do nível de transistores (RTL) para a dos arquivos gráficos (GDSII) seja incorporada ao fluxo de projeto de automatizado.

A.1.2 Estrutura da tese e contribuições

A Figura 1.1 ilustra a estrutura desta tese, destacando seus aspectos originais e análises apresentadas ao longo do trabalho.

Coloridas em verde claro, estão apresentadas as seções (ou subseções) nas quais o autor introduz algumas pequenas contribuições, como opiniões originais nas análises, novos dados ou pequenos ajustes em parâmetros de equações. Coloridos em verde escuro, encontram-se os pontos e contribuições principais da Tese, as áreas nas quais este trabalho tem um papel crucial ao avanço do estado-da-arte (considerando-se o que há disponível na literatura), estabelecendo uma sólida conexão com todas as etapas do fluxo de projeto.

Seguindo este critério, após a introdução, o Capítulo 2 apresenta os conceitos básicos relacionados à interação da radiação ionizante com a matéria. O Capítulo 3 discute algumas técnicas de tolerância, as quais podem ser aplicadas através dos diferentes níveis de abstração dos circuitos, considerando processos de fabricação convencionais disponíveis comercialmente, cobrindo os desafios usuais da aplicação das técnicas propostas. Além disso, uma pequena expansão com relação à equação de estimativa do $(W/L)_{eff}$ é proposta (e validada através de análises e simulações elétricas), de modo a possibilitar, da forma mais ampla, a aquisição de razões de aspecto para geometrias do tipo não retangulares.

O Capítulo 4 propõe uma generalização do já conhecido método do *"Logical Effort"* (LE), o qual leva em consideração todas as variáveis de projeto em uma mesma equação, permitindo uma automatização do cálculo do *"gate"* de transistores n,pMOS e, também, a razão de aspecto PN para o menor atraso médio. O Capítulo 5 explora simulações elétricas de células digitais baseadas na topologia de *"gate"* fechado através de análises de pequenos e grandes sinais.

O Capítulo 6 apresenta e explica o fluxo de projeto proposto. O Capítulo 7 apresenta as estruturas de teste nos nós tecnológicos de $600\ nm$ e $180\ nm$, com foco na validação da metodologia proposta. O Capítulo 8 apresenta os resultados pré e pós exposição à radiação e, finalmente, o Capítulo 9 apresenta as conclusões e considerações finais.

A.1.3 Informações importantes

Ao longo deste trabalho, termos relacionados à radiação ionizante, e projetos e aplicações espaciais seguem o padrão referenciado pela norma Europeia *"European Cooperation for Space Standardization"* (ECSS) (ECSS, 2004).

Os termos referenciados por *"qualified"* ou *"hardened"* inferem que o dispositivo é projetado de modo a operar dentro das margens aceitáveis de tolerância ou, em outras palavras, de modo a manter seu fluxo correto de funcionamento, dentro das suas especificações. Além disso, o termo *"mitigate"*, quando utilizado, refere-se à atenuação ou à redução dos impactos dos fenômenos relacionados, tornando-os menos severos.

Nesse contexto, um circuito eletrônico pode ser considerado tolerante à radiação quando seu desempenho e suas características elétricas possibilitem que seu funcionamento se mantenha dentro das margens de tolerância especificadas, a fim de garantir um processamento de dados válidos durante o tempo em que estiver submetido à incidência de radiação.

A síntese das propostas de mitigação e técnicas de tolerância, foco deste trabalho, são propostas de modo a reduzir substancialmente os efeitos da radiação ionizante em dispositivos CMOS do tipo *"bulk"*. Com isso, dando origem ao termo *"Radiation-Hardening by Design"* (RHBD).

A.2 Conclusão

A.2.1 Discussão final

Nesta tese, o desenvolvimento completo de uma metodologia para fluxo de projeto de biblioteca de células tolerante à radiação foi proposto. A metodologia utiliza dispositivos de *"gate"* fechado e *"guard rings"*, duas técnicas de tolerância à radiação consolidadas. Além disso, a metodologia, transparente ao projetista, é totalmente compatível com ferramentas de CAD comerciais e processos de fabricação convencionais. De modo a atingir estes objetivos, alguns avanços ao estado-da-arte em pontos críticos no fluxo de projeto, como a proposta de *"template"* para células digitais, assim como seus arranjos em série e paralelo foram desenvolvidos. Contudo, o cálculo automatizado da razão de aspecto efetiva (W/L) dos dispositivos de *"gate* fechado; propostas completas para o *"template"* respeitando as regras litográficas; o cálculo da razão PN e *"buffers"* de

saída dimensionados através do método do *"Logical Effort"* (LE); estruturas de teste e, finalmente, o teste de irradiação foram executados de modo a suprir os passos de projeto e seus requisitos.

Circuitos Integrados (CIs) sujeitos à incidência de radiação ionizante sofrem efeitos indesejados tais como *"upsets"* ou danos no material dos dispositivos. Entretanto, aplicações aeroespaciais e, mesmo aquelas ao nível do mar, como aplicações para física de alta energia (HEP) são severamente afetadas pela radiação ionizante.

Após a interação de radiação ionizante, pares elétron-lacuna $(\bar{e}/h)$ são produzidos. O movimento destas cargas quando ocorre em uma junção PN reversamente polarizada e no dióxido de silício pode causar degradações no material semicondutor do dispositivo. O efeito mais relevante em decorrência do movimento destas cargas são desvios na tensão de limiar e o incremento na corrente de fuga, neste último caso considerando tanto interno quanto externo do dispositivo.

De modo a proteger um dispositivo contra a radiação ionizante, várias tecnicas podem ser aplicadas ao longo de toda a hierarquia do fluxo de projeto dos CIs, desde a arquitetura de sistema ao layout de um único transistor. No entanto, a decisão de proteção do bloco básico de qualquer CI sob a perspectiva de *"layout"*, isto é, um único transistor, atinge os maiores níveis de tolerância contra degradações em decorrência à exposição de longa duração, mantendo a possibilidade de embarcar outras propostas de mitigação à nível de sistema. Sob esta perspectiva, duas técnicas principais foram aplicadas; o uso de dispositivos de *"gate"* fechado e *"guard rings"*.

O desafio da utilização de dispositivos de *"gate"* fechado está na predição do cálculo da razão de aspecto efetiva (W/L). Isto ocorre porque não há um equivalente físico à largura do transistor em geometrias anulares. Deste modo, este trabalho realizou uma pesquisa e investigação profunda na literatura dentre as principais e amplamente adotadas geometrias, escolhendo duas propostas — nas quais, dentre elas, há apenas uma pequena diferença na região dos ângulos do *"gate"* de modo a satisfazer a possibilidade de execução dos ângulos de 45 ou $90°$ graus na camada de poli silício. Adicionalmente, foi proposta a individualização de duas variáveis internas dos modelos de modo a promover uma variedade mais ampla de razões de aspecto.

Para calcular o tamanho do *"gate"* de células digitais, a razão PN de *"buffers"* de saída, o método do *"Logical Effort"* (LE) foi adotado. O uso deste método foi aplicado pela primeira vez, no melhor do nosso conhecimento, no contexto de tolerância à radiação com dispositivos de *"gate"* fechado.

Contudo, para validar a metodologia do fluxo de projeto tolerante à radiação baseada em dispositivos de *"gate"* fechado e para qualificar o nível de tolerância dos dispositivos, dois *test chips* foram projetados. As medidas práticas foram adquiridas pré, durante e pós incidência de radiação. Na preirradiação, as medidas de *"large signal"* mostram que as simulações SPICE de dispositivos individuais com diferentes razões de aspecto e comprimentos de canal apresentam boa correspondência com os dados experimentais, o que é um aspecto muito importante para a metodologia proposta — não há a necessidade de uma caracterização completa e modelagem dos dispositivos de modo a atingir resultados de simulação razoavelmente precisos.

Com relação aos resultados adquiridos durante e pós irradiação e *"annealing"*, é difícil fornecer uma análise quantitativa devido a escassez de dados reportados para o nó de $600\ nm$. No entanto, uma abordagem qualitativa está em acordo com os achados na literatura. As características de tolerância das células propostas foram supridas. Em uma comparação entre os dispositivos padrão (nSTD) versus os de *"gate"* fechado (nELT) (irradiados até $500\ krad(Si)$), um incremento de quase 3 ordens de magnitude foi observada em dispositivos padrão. Deste modo, além dos resultados de radiação para dispositivos do tipo nELT, este trabalho contribuiu enriquecendo os escassos resultados experimentais apresentados para pELTs — porque eles não necessitam de geometria fechada, uma vez que o efeito no incremento na corrente de fuga tem um efeito negativo. Finalmente, ainda que menos que 10% mas, como esperado, a fase de *"annealing"* trouxe de volta a função de saída e de transferência para seus valores originais.

Ademais, o objetivo primordial da tese foi atingido; o desenvolvimento completo de uma metodologia para fluxo de projeto de biblioteca de células tolerante à radiação foi proposto tendo seus passos transparente para o projetista e sendo compatíveis com as ferramentas de CAD comerciais. Os *"test chips"* fabricados foram úteis para a validação e consolidação dos conceitos teóricos, mostrando que o fluxo proposto é adequado para células mais complexas. A automatização do projeto das estruturas foi validada como possível e uma solução elegante a ser implementada não apenas em contexto acadêmico como também para o desenvolvimento da indústria Brasileira de circuitos integrados.

Durante a execução desta tese, vários desafios técnicos foram confrontados. Eventualmente, algumas dificuldades pareceram sem solução, como, por exemplo, a automatização da geração das geometrias do dispositivo no arquivo "LEF", implementar o cálculo da razão de aspecto (W/L) na ferramenta de CAD, o DRC de novos dispositivos os quais não pertenciam ao *"deck"* comercial, a proposta de *"abutment"* dos arranjos de gate

fechado em série e em paralelo e o *"test chip"* propriamente. O caminho completo para o desenvolvimento completo de um fluxo de projeto é extremamente longo e alguns futuros aperfeiçoamentos em fases específicas são oportunos.

Contudo, na Seção seguinte, alguns trabalhos futuros são apresentados.

A.2.2 Trabalhos futuros

Como continuação do trabalho apresentado nesta tese, sinto-me confiante em abrir claramente a possibilidade de aperfeiçoamento e a possibilidade direta, e já avançada, de pesquisa nas subáreas:

a) Aperfeiçoar simulações TCAD: Para simular dispositivos através de ferramentas *"Technology Computer-Aided Design"* (TCAD) é necessária ou a descrição do processo de fabricação completo do dispositivo, ou a sua disposição geométrica, perfil de dopantes e regiões de difusão. Pelo cálculo da geometria dos dispositivos, analogamente à geração dos arquivos de saída GDSII dos dispositivos ELTs, é possível o design de estruturas para o contexto TCAD. Neste sentido, algum trabalho já foi iniciado, como ilustrado na Fig. 9.1 (a) e (b), a qual representa, respectivamente, geometrias ELTs e seus perfis de difusão. Aperfeiçoando alguns métodos (codificados em linguagem C) será possível analisar futuras propostas de dispositivos tolerantes à TID como, por exemplo, no trabalho reportado por (XIE et al., 2019).

b) Expandir estudos analíticos: Um dos pilares técnicos desta tese é a habilidade em simular e analisar as características IV dos dispositivos. Com isso, como trabalho futuro, um aperfeiçoamento e expansão dos dispositivos e geometrias simulados podem ser desenvolvidos. De modo a analisar e comparar o resultado de simulações TCAD versus SPICE, a Fig. 9.2 (a) e (b) mostra exemplos da função de transferência e características de saída, respectivamente para $L = 180\ nm$ e $L = 360\ nm$.

c) Investigar e depurar estruturas ESD: Uma proposta de estrutura de proteção ESD foi desenvolvida e fabricada no *"test chip"* de $180\ nm$. No entanto, por um motivo desconhecido, as estruturas apresentaram algum defeito funcional. Eu suponho que o problema esteja relacionado a nível de *layout*. Como trabalho futuro, uma profunda investigação acerca destas estruturas pode ser realizada.

d) Continuar e aperfeiçoar a automatização de CAD: O cerne desta tese é a automatização de ferramentas de CAD. Com isso, durante o projeto, foram implementados e desenvolvidos uma série de códigos em MATLAB, C, SKILL, C#, and até mesmo Perl. Como trabalho futuro, eu julgo que o campo de pesquisa mais fértil seja o de expandir e aperfeiçoar qualquer um dos códigos desenvolvidos, sejam eles tanto para o *"design"* das geometrias quanto para incluir funcionalidades nas ferramentas de CAD.

e) Continuar os testes de irradiação: Os chips de teste podem ser caracterizados para doses mais altas de radiação.