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DESIGN OF CONTINUOUS-TIME SIGMA-DELTA MODULATORS WITH INVERTER-BASED AMPLIFIERS FOR SUB-1V APPLICATIONS

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DEDICATION

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ABSTRACT

Analog-to-digital converters (ADCs) are essential building blocks in applications ranging from electronic instrumentation to modern communication systems and devices for Internet-of-Things (IoT). These applications demand power-efficient and reliable circuits to extend battery life, and low-voltage operation capability to allow energy harvesting operated devices. One of the most suitable ADC topologies for low-voltage and low-power applications is the Sigma-Delta (SD) ADC, whose design bottleneck is the loop-filter low-voltage operational transconductance amplifiers (OTAs). This thesis presents the development of sub-1V continuous-time sigma-delta modulators (CT-SDMs) with inverter-based amplifiers. The state of the art of CT-SDMs with inverter-based amplifiers has been delimited, and two low-voltage CT-SDMs prototypes have been designed and experimentally characterized. The first prototype is a 0.6-V third-order single-bit CT-SDM with a single-amplifier resonator in the loop filter and a low-power structure to implement the feed forward coefficients and quantization to increase power efficiency. The proposed single-stage inverter-based OTA topology has a negative conductance cell for DC gain enhancement and uses an on-chip bulk-bias technique to control the output common-mode voltage and to mitigate PVT variations. A compensation technique to mitigate the effects of amplifier's finite DC gain in the resonator transfer function is presented enabling the use of low-gain amplifiers ($\leq$ 40 dB). The proposed modulator was fabricated in a 130-nm triple-well CMOS process with an active area of 0.232 mm^2 and presented a peak SNR/SNDR of 69.04/59.43 dB and a DR of 74.2 dB for a 100-kHz signal bandwidth while consuming 89.50 μW. The second prototype is a power-efficient third-order CT-SDM with three loop-filter integrators and a passive RC path to assist the first integrator amplifier. The proposed inverter-based OTA uses a bulk-based current mirror to provide its operating point and to reduce gain-bandwidth product (GBW) variations. The proposed modulator was fabricated in a 180-nm CMOS process with an active area of 0.36 mm^2. The modulator loop filter operates with a supply voltage as low as 0.45 V while the digital circuitry operates at 0.6 V. The modulator power consumption is 28.72 μW. For a 50-kHz signal bandwidth, the measured peak SNR/SNDR is 71.24/70.64 dB and the achieved DR is 78.3 dB, leading to a Schreier figure-of-merit of 170.70 dB.

Keywords: Sigma-Delta Modulation, AD conversion, Low-Voltage, Integrated Circuit Design.

RESUMO

Conversores analógico-digitais (ADCs) são essenciais em aplicações que vão desde instrumentação eletrônica a modernos sistemas de comunicação e dispositivos para Internet das Coisas (IoT). Essas aplicações exigem circuitos confiáveis e com baixo consumo de energia para prolongar a duração da bateria, e capacidade de operação em baixa tensão para permitir dispositivos acionados por colheita de energia. Uma das topologias de ADCs mais adequadas para aplicações de baixa tensão e baixo consumo de energia é o ADC Sigma-Delta, cujo principal desafio de projeto são os amplificadores operacionais de transcondutância (OTAs) de baixa tensão empregados no filtro de laço do modulador. Esta tese apresenta o desenvolvimento de moduladores sigma-delta em tempo contínuo (SDMs-CT) com amplificadores baseados em inversores CMOS para aplicações sub-1V. O estado da arte de SDMs-CT com amplificadores baseados em inversores foi delimitado, e dois protótipos de SDMs-CT de baixa tensão foram projetados e caracterizados experimentalmente. O primeiro protótipo é um SDM-CT com tensão de alimentação de 0,6 V que utiliza no filtro de laço um ressonador projetado com apenas um OTA, e adota uma estrutura de baixa potência para implementar os coeficientes em avanço e quantização. O OTA baseado em inversores CMOS utilizado é de um estágio e utiliza uma célula de condutância negativa para aumento de ganho DC. O controle da tensão de modo comum de saída e a mitigação dos efeitos devido a variações de processo, tensão e temperatura (PVT) é efetuada por uma técnica de polarização do terminal de corpo dos transistores dos inversores. Uma técnica para mitigar os efeitos do ganho DC finito do amplificador na função de transferência do ressonador também é apresentada, permitindo o uso de amplificadores de baixo ganho ($\leq$ 40 dB). O modulador proposto foi fabricado em tecnologia CMOS de 130 nm com uma área ativa de 0,232 mm^2 e apresentou SNR/SNDR de pico de 69,04/59,43 dB e um DR de 74,2 dB para sinais de até 100 kHz, enquanto o consumo de energia é de 89,50 µW. O segundo protótipo é um SDM-CT de terceira ordem, com três integradores no filtro de laço, e uma rede RC para auxiliar o amplificador do primeiro integrador. O OTA baseado em inversor proposto utiliza um espelho de corrente baseado na tensão de corpo do transistor para fornecer seu ponto de operação e reduzir as variações do produto ganho-faixa (GBW). O modulador proposto foi fabricado em tecnologia CMOS de 180 nm com uma área ativa de 0.36 mm^2. O filtro de laço modulador opera com uma tensão de alimentação de 0,45 V, enquanto o circuito digital opera com tensão de 0,6 V. O consumo de energia é do modulador é 28,72 µW. Para uma largura de banda de sinal de 50 kHz, o SNR/SNDR de pico é 71,24/70,64 dB e o DR obtido é de 78,3 dB, proporcionando uma figura de mérito de Schreier de 170,70 dB.

Palavras-chave: Modulação Sigma-Delta, Conversão AD, Baixa-Tensão, Projeto de Circuitos Integrados.

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LIST OF ABBREVIATIONS

1P6M	Single-Poly Six-Metal
1P8M	Single-Poly Eight-Metal
AAF	Anti-Alias Filter
AD	Analog-to-Digital
ADC	Analog-to-Digital Converter
BW	Bandwidth
CIFB	Cascade of Integrators in Feedback
CIFF	Cascade of Integrators in Feed-Forward
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
CS	Common Source
CT	Continuous-Time
CT-SDM	Continuous-Time Sigma-Delta Modulator
DAC	Digital-to-Analog Converter
DC	Direct Current
DR	Dynamic Range
DT	Discrete-Time
DT-SDM	Discrete-Time Sigma-Delta Modulator
ELD	Excess Loop Delay
ENOB	Effective Number of Bits
EVB	Evaluation Board
FIR	Finite-Impulse Response
FoM	Figure of Merit
FS	Full Scale
GBW	Gain Bandwidth Product
IBN	In-Band Noise
IC	Integrated Circuit
IF	Intermediate Frequency
IIT	Impulse-Invariant Transformation

IM3	Third-order Intermodulation Distortion
IoT	Internet-of-Things
ISI	Inter-Symbol Interference
LDO	Low-Dropout
LHP	Left Half-Plane
LV	Low-Voltage
MASH	Multi-Stage Noise-Shaping
MC	Monte Carlo
MiM	Metal-insulator-Metal
MPW	Multi-project Wafer
NRZ	Non Return-to-Zero
NTF	Noise Transfer Function
OBG	Out-of-Band Gain
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PSD	Power Spectrum Density
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage and Temperature
Q	Quality Factor
RMS	Root Mean Square
RTO	Return-To-Open
RZ	Return-To-Zero
SAB	Single-Amplifier Biquad
SAR	Successive Approximation Register
SC	Switched-Capacitor
SCR	Switched-Capacitor-Resistor
SD	Sigma-Delta
SDM	Sigma-Delta Modulator
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip

SQNR	Signal-to-Quantization-Noise Ratio
SR	Slew-Rate
SSCB	Semi-Constant Current Bias
STF	Signal Transfer Function
TAT	Trapezoidal Association of Transistors

LIST OF SYMBOLS

$Adder(s)$	Adder transfer function taking into account a real amplifier
A_V	Amplifier DC gain
C_{ox}	Oxide capacitance
dBFS	Decibels relative to the Full Scale
δ	Clock period uncertainty
Δ	Difference between two quantization levels
ε_o	Vacuum permittivity
ε_r	Relative permittivity
$e(n)$	Quantization noise
$e(z)$	Processed quantization noise
$E(z)$	Z transformation of the quantization noise
f_{in}	Input signal frequency
f_N	Nyquist frequency
$\mathrm{FoM_W}$	Walden figure-of-merit
$\mathrm{FoM_S}$	Schreier figure-of-merit
Fs, f_s	Sampling frequency
gds	Transistor output conductance
gds_N	NMOS transistor output conductance
gds_P	PMOS transistor output conductance
gm	Transconductance
gm_N	Transconductance of NMOS transistor
gm_P	Transconductance of PMOS transistor
gm_{OTA}	OTA transconductance
γ	Channel length modulation coefficient
$H(s)$	Continuous-time loop filter transfer function
$H(z)$	Discrete-time loop filter transfer function
$\bar{I}^2$	Current spectral density
$\mathrm{I_D}$	Drain current
k	Boltzmann constant
k_f	Technology dependent flicker noise parameter

L	MOS transistor channel length
μ	Mobility
N	Number of bits
n_f	Flicker noise excess factor
$NTF(z)$	Discrete-time noise transfer function
$n_{thermal}$	Thermal noise excess factor
ω_a	Amplifier cut-off frequency expressed in rad/s
ω_u	Amplifier unity gain frequency expressed in rad/s
P_E	In-band quantization noise power
P_{noise}	Noise power at the integrator input
P_Q	In-band quantization noise value in an oversampling ADC
P_W	Circuit power consumption
R_{DAC}	DAC resistor
$R_{DAC}(s)$	DAC transfer function
$\rho_q(e)$	Quantization error probability density function
$S_E(f)$	Quantization error power spectral density
σ	Standard deviation
σ^2	Variance
$\sigma^2(e)$	Total quantization noise power
$STF(z)$	Signal transfer function
t_{ox}	Oxide width
T_s	Sampling period
$u(n)$	Quantizer input signal
$\bar{v}^2_{DAC}$	DAC noise density
$\bar{v}^2_{flicker}$	Flicker noise density
$\bar{v}^2_{in-thermal}$	Thermal noise density at the inverter input
$\bar{v}^2_R$	Resistor noise density
$\bar{v}^2_{R_{IN}}$	Input resistor noise density
$\bar{v}^2_{out-thermal}$	Thermal noise density at the inverter output
$\bar{v}^2_{vin-OTA}$	OTA noise density
$\bar{v}^2_{total}$	Total noise density at the the integrator input
Vbctrl	Control voltage of the bulk terminal
VCM	Common-Mode Voltage

VDD	Supply Voltage
V_{DS}	Drain-Source Voltage
V_{GS}	Gate-Source Voltage
VREF+	Positive voltage reference
VREF-	Negative voltage reference
V_{SB}	Source-bulk voltage
V_T	Threshold Voltage
V_{T0}	Threshold voltage for V_{BS} = 0 V
V_{TN}	NMOS Transistor Threshold Voltage
V_{TP}	PMOS Transistor Threshold Voltage
V_{trip}	CMOS Inverter Trip-Point
W	MOS transistor channel width
X_{FS}	Quantizer full scale input amplitude
$X(z)$	Sigma-delta modulator input
Y_{FS}	Quantizer output full-scale
$y(n)$	Quantizer output signal
$Y(z)$	Sigma-delta modulator digital output

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1 INTRODUCTION

The technological advancement in the semiconductor industry combines the transistors scaling with the supply voltage reduction for the development of digital circuits with low power consumption. To integrate low-voltage digital and analog circuits without the need for on-chip step-down converters, it is necessary to develop low-voltage analog circuits (CHEN; PUN, 2012).

Low-power circuits operating with low supply voltages are essential for portable devices and Internet of Things (IoT) applications where Web connectivity is mandatory. Among the IoT applications can be highlighted mobile devices such as cell phones, biomedical circuits, sensor network nodes, and autonomous devices whose power source comes from energy harvesting (MALOBERTI; BONIZZONI; BASYURT, 2016).

Analog-to-Digital Converters (ADCs) are essential building blocks in IoT systems that, in addition to Web connectivity, require electronic instrumentation combined with digital signal processing. These applications use medium and high-resolution ADCs (9-14 bits) with signal bandwidths up to 1 MHz (MALOBERTI; BONIZZONI; BASYURT, 2016). The most employed ADC architectures that achieve these requirements are Successive Approximation Registers (SAR) and Sigma-Delta (SD).

SD ADCs are composed of an anti-alias filter (AAF), a sigma-delta modulator (SDM), and a digital decimation filter. The fundamental block of an SD ADC is the SDM since it limits the bandwidth and accuracy of the ADC (SCHREIER; TEMES, 2005).

One of the SDMs main characteristics is its robustness against analog circuits imperfections, which makes them an excellent choice for the design of ADCs in nanometer-scale CMOS integrated circuits and modern System-on-Chip (SoCs) (DE LA ROSA; DEL RIO, 2013). Also, they provide high resolution with low precision components due to the benefits of both noise shaping and oversampling while presenting a good compromise between input signal bandwidth and accuracy. Thus, the design of low-power sub-1V SDMs for IoT applications despite challenging is very attractive.

There are two main approaches to the development of SDMs: discrete-time (DT) and continuous-time (CT) design. Both approaches have proven to be effective for the development of SDMs for sub-1V applications with typical bandwidths in the audio track

(PUN; CHATTERJEE; KINGET, 2007) (CHAE; HAN, 2009). However, few works in the recent literature address the design of low-voltage continuous-time sigma-delta modulators (CT-SDMs) using amplifiers based on CMOS inverters. Thus, this thesis proposes the study and design of low-power CT-SDMs with inverter-based amplifiers for sub-1V applications.

1.1 Motivation

The energy consumption of SDMs is given mainly by the modulator loop filter. In recent years, one of the strategies employed to reduce the energy consumption of SDMs is the replacement of the traditional differential-pair operational amplifiers for operational transconductance amplifiers (OTAs) based on CMOS inverters, which is considered one of most energy and area efficient OTA topologies (DE LA ROSA *et al.*, 2015).

The first SDM employing CMOS inverter-based amplifiers was presented in (CHAE; HAN, 2009). Currently, it is a promising strategy for the development of low-power and high-performance SDMs (BREEMS *et al.*, 2016).

However, inverter-based OTAs are susceptible to process, voltage and temperature (PVT) variations that affect the inverter trip point and impact the DC gain, the Gain-Bandwidth Product (GBW) and the output swing of the inverter if no PVT compensation strategies are used. Existing strategies to compensate PVT variations increase the OTAs design complexity (HARJANI; PALANI, 2015), and the development of new compensation strategies is an open research field.

An extensive bibliographical review at the initial phase of this work revealed, to the author's best knowledge, that there were no sub-1V CT-SDMs with inverter-based amplifiers designed and experimentally characterized. At that time, only a few studies based on schematic or post-layout simulation results were available on the literature. Meanwhile, different silicon-proven low-voltage discrete-time SDMs with inverter-based amplifiers in the loop filter are reported.

Thus, this thesis work main motivation is to explore, design, and experimentally characterize low-power CT-SDMs with inverter-based amplifiers for sub-1V applications.

1.2 Objectives

The main objective of this work is to investigate, analyze, and design low-power sub-1V CT-SDMs with inverter-based amplifiers for portable devices and IoT applications.

Existing techniques for the design of inverter-based amplifiers are analyzed and used as a starting point to develop novel amplifier topologies. Different PVT compensation strategies to mitigate the effects of PVT variations in the amplifier characteristics are used, minimizing the DC gain and GBW variations.

The amplifiers analyzed and developed in this thesis work were used in the design of different low-voltage CT-SDMs, aiming, in particular, to reduce the energy consumption of these modulators without deteriorating their performance.

1.3 Contributions

This work presents a review on the main design techniques of inverter-based amplifiers for application in SD modulators operating at nominal and low supply voltages.

Two CT-SDMs are designed and experimentally characterized in this thesis work. The first modulator is designed in a 130-nm CMOS process and operates with a supply-voltage of 0.6 V. This CT-SDM is based on single-stage inverter-based amplifiers. The designed amplifier uses an on-chip bulk-bias technique to control the output common-mode voltage and to mitigate the effects of PVT variations. Also, a negative conductance cell connected at the amplifier output enhances its DC gain providing DC gain values up to 40 dB for a single-stage amplifier. To increase the modulator power efficiency, by reducing the number of OTAs, the loop filter uses a single-amplifier biquad (SAB) resonator. To enable the implementation of this SAB with low-gain amplifiers, a compensation technique to mitigate the effects of amplifier's finite DC gain in the resonator transfer function (TF) is presented. The proposed solution provides a resonator TF similar to the one provided by an amplifier with DC gain of 80 dB. This proposed CT-SDM has an active area of 0.232 mm^2 and achieves a dynamic range (DR) of 74.2 dB, a signal-to-noise ratio (SNR) of 69.04 dB and signal-to-noise and distortion ratio (SNDR) of 59.43 dB for a 100 kHz signal bandwidth while consuming 89.50 μW. To the author's best knowledge, this thesis introduced for the first time a low-voltage silicon proven CT-SDM with inverter-based amplifiers operating at 0.6 V. Also, the use of a SAB resonator in the loop filter is explored in the context of low-voltage CT-SDMs.

The second contribution is a PVT compensated single-stage inverter-based OTA topology for low-voltage CT-SDMs. The OTA operating point is controlled by a bulk-based current mirror, providing a robust operation and significantly reducing the unity gain-bandwidth variation across PVT corners while presenting a DC gain of 41.9 dB at nominal conditions when operated at 0.6 V. The effectiveness of the proposed circuit was initially verified in a 180-nm CMOS process by transistor-level simulations including PVT variations and mismatch. A 0.6-V third-order CT-SDM was also designed with this OTA to verify the robustness against voltage and temperature variations. Then, this OTA topology was used to design the second silicon-proven CT-SDM presented in this thesis.

The second CT-SDM presented in this thesis runs at 10 MHz and was characterized for a 50-kHz signal bandwidth. The inverter-based amplifiers operate in weak-inversion enabling the analog loop filter to operate at supply voltages as low as 0.45 V while the digital circuit operates at 0.6 V. The inverter-based modulator was fabricated in a 180-nm

CMOS process and occupies an area of 0.36 mm^2. Measurement results show that the designed modulator achieves a DR of 78.30 dB over a 50-kHz bandwidth while consuming only 28.72 µW leading to a Schreier figure-of-merit (FoM) of 170.70 dB.

1.4 Publications

1.4.1 Publications Included in This Thesis

- P. C. C. de Aguirre and A. A. Susin, "A 0.6-V 74.2-dB DR Continuous-Time Sigma-Delta Modulator With Inverter-Based Amplifiers," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 10, pp. 1310-1314, Oct. 2018.

- P. C. C. de Aguirre and A. A. Susin, "PVT compensated inverter-based OTA for low-voltage CT sigma-delta modulators," in Electronics Letters, vol. 54, no. 22, pp. 1264-1266, Nov. 1 2018.

- P. C. C. de Aguirre, E. Bonizzoni, F. Maloberti and A. A. Susin, "A 170.7 dB FoM-DR 0.45/0.6-V Inverter-Based Continuous-Time Sigma-Delta Modulator," **Accepted for publication** in IEEE Transactions on Circuits and Systems II: Express Briefs.

1.4.2 Publications not Included in This Thesis

The subject of the following papers is not related to this thesis scope.

- R. A. Domanski, L. A. da Silva Jr., P. C. C. de Aguirre and A. G. Girardi, "A Hybrid Sampling Method for In-the-Loop Yield Estimation of Analog ICs in an Optimization Process," in IEEE Latin America Transactions, vol. 15, no. 5, pp. 779-785, May 2017.

- A. L. Chinazzo, P. C. C. de Aguirre and T. R. Balen, "Low cost automatic test vector generation for structural analog testing," 2017 18th IEEE Latin American Test Symposium (LATS), Bogota, 2017, pp. 1-4.

- M. S. Oliveira, P. C. C. de Aguirre, L. C. Severo, A. G. Girardi and A. A. Susin, "A digitally tunable 4th-order Gm-C low-pass filter for multi-standards receivers," 2016 29th Symposium on Integrated Circuits and Systems Design (SBCCI), Belo Horizonte, 2016, pp. 1-6.

- A. C. de Oliveira, P. C. C. de Aguirre, L. C. Severo and A. G. Girardi. "An optimization-based methodology for efficient design of fully differential amplifiers," in Analog Integrated Circuits and Signal Processing, v. 88, p. 1-15, 2016.

1.5 Organization of This Thesis

This work is organized in 7 Chapters. The following Chapter presents the main concepts about Sigma-Delta Modulation and addresses the characteristics of SDMs for low-voltage operation. Chapter 3 presents a review on the design techniques of inverter-based amplifiers and the state of the art regarding SDMs with inverter-based amplifiers. The high-level synthesis of the designed modulators and the modeling of the non-idealities present in this modulator architecture are presented in Chapter 4. Chapter 5 introduces the first amplifier topology designed in this work and presents in detail the circuit-level implementation of a 0.6-V CT-SDM with inverter-based amplifiers in a 130-nm CMOS technology. The second inverter-based amplifier topology proposed in this work and the second CT-SDM prototype are analyzed in detail in Chapter 6, along with a comparison with recent related works present in the literature. Finally, the main conclusions of this thesis and future works are given in Chapter 7.

2 SIGMA-DELTA MODULATION: THEORETICAL REVIEW

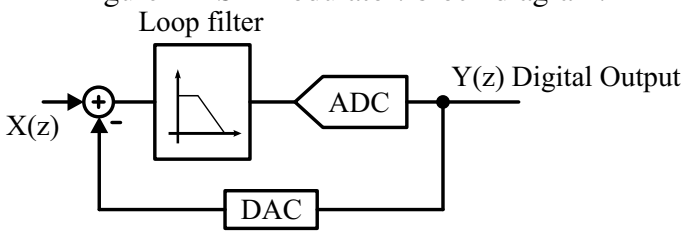
This Chapter presents the basics of SD modulation and a review of the SD modulators main characteristics. Sigma-delta modulators in continuous-time mode are introduced and a review on SD modulators architectures for sub-1V applications is also presented.

Finally, the performance metrics used to evaluate SD modulators are provided to support the state-of-the-art review of CT-SDMs with inverter-based amplifiers for sub-1V applications.

2.1 Sigma-Delta Modulators: Principle of Operation

Figure 1 presents the basic architecture of an SD modulator. The input signal X(z) is applied in an adder block at the input of the SD modulator, and passes through a filter, known as the loop filter. The loop filter is usually composed of integrators, and in its simplest version consists of only one integrator. After passing through the filter, the signal is quantized by an ADC, also known as quantizer. The output signal from the quantizer is applied to the input of a Digital-to-Analog Converter (DAC) which feeds the SD modulator through the summing block present at the modulator input closing the feedback loop.

Figure 1 – SD modulator: block diagram.



Source: The author

The ADC and DAC employed in an SD modulator are designed with N bits, with N usually ranging from 1 to 4 (DE LA ROSA, 2011). Due to the quantization process, the ADC inserts an error e(n), which is the difference between the input signal of the ADC and the digital output signal Y(z). The quantization error within the signal band

is reduced by the use of oversampling and noise shaping (SCHREIER; TEMES, 2005). Thus, a high-resolution digital output signal can be obtained using a low-resolution ADC.

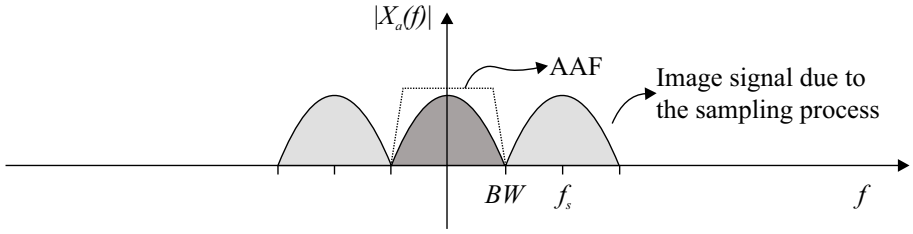
2.1.1 Oversampling

The oversampling process consists of sampling signals with a sampling frequency f_s higher than the Nyquist frequency f_N, where $f_N = 2 \times \text{BW}$ (HAYKIN; MOHER, 2006). The oversampling ratio (OSR) is then calculated by: $\text{OSR} = f_s/(2 \times BW)$.

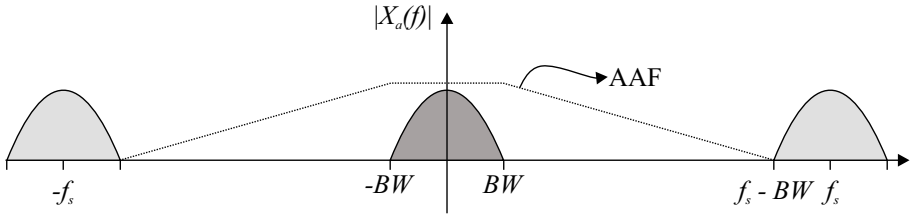
If f_s is greater than f_N, the input signal images created by the sampling process become more spaced in the frequency domain than in a Nyquist-rate ADC ($f_s = f_N$), as shown in Figure 2.

Thus, the input signal spectral components in the bandwidth [BW, f_s - BW] do not overlap with the signal bandwidth, reducing the requirements of the AAF.

Figure 2 – Input signal and AFF.



(a) Nyquist-rate ADC.



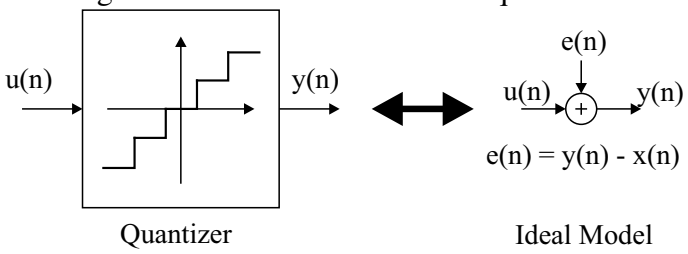
(b) Oversampled ADC.

Source: The author

The second effect is related to the uniform distribution of quantization noise within the range [$-\frac{f_s}{2}$, $\frac{f_s}{2}$], where only a fraction of quantization noise is located within the ADC signal band. It is necessary to perform a mathematical analysis of the quantization process to understand this effect. The quantization error can be strongly correlated to the input signal of the quantizer (JOHNS; MARTIN, 1997). However, if it is considered that there is no correlation, the behavior of the quantization error can be approximated by the addition of a white noise source to the input signal, as shown in Figure 3.

The quantization error is the difference between the input signal and the output signal of the quantizer. In this model, it is approximated as an independent random number evenly distributed between $\pm\Delta/2$, where Δ is the difference between two adjacent quantization levels (JOHNS; MARTIN, 1997). However, this model is valid only when the input signal changes rapidly and has an amplitude lower than or equal to the quantizer full-scale

Figure 3 – The linear model of a quantizer.



Source: The author

(FS) input amplitude, $\pm X_{FS}/2$. If the amplitude of the input signal is outside the limit $\pm X_{FS}/2$, the quantization error exceeds $\pm\Delta/2$ and grows monotonically (DE LA ROSA, 2011).

For an N-bit quantizer, the quantization step Δ is defined by Equation 1.

$$\Delta = \frac{\mathrm{Y_{FS}}}{2^{\mathrm{N}} - 1} \tag{1}$$

Where $\mathrm{Y_{FS}}$ is the quantizer full-scale output range and N is the quantizer number of bits.

The probability density function of the quantization error, $\rho_q(e)$, is uniform in the range of $[-\Delta/2\ ,\ +\Delta/2]$. The total quantization noise power, $\sigma^2(e)$, is equal to $\Delta^2/12$ and is independent of the sampling frequency f_s (JOHNS; MARTIN, 1997), being evenly distributed in the band [-$\frac{f_s}{2}$, $\frac{f_s}{2}$]. Thus, the power spectral density of the quantization error, $S_E(f)$, is constant with amplitude $k = \frac{\Delta}{\sqrt{12}}\sqrt{\frac{1}{f_s}}$ and is concentrated in the frequency interval [-$\frac{f_s}{2}$, $\frac{f_s}{2}$], being calculated by Equation 2.

$$S_E(f) = \frac{\sigma^2(e)}{f_s} = \frac{\Delta^2}{12 \times f_s} \tag{2}$$

Consequently, the in-band quantization noise power due to the quantization process (P_E) is calculated by Equation 3.

$$P_E = \int_{-BW}^{+BW} S_E(f)\mathrm{d}f = \int_{-BW}^{+BW} k^2 \mathrm{d}f = \frac{\Delta^2}{12 \times OSR} \tag{3}$$

If the signal is sampled at the Nyquist rate, all the quantization noise falls inside the signal bandwidth and $P_E = \Delta^2/12$. Based on Equation 3 one may realize that it is possible to decrease the power of the quantization noise inside the signal bandwidth by increasing the OSR.

In an N-bit Nyquist-rate ADC, the signal-to-quantization-noise ratio (SQNR) is expressed by Equation 4 (JOHNS; MARTIN, 1997).

$$\mathrm{SQNR} = 6.02 \times \mathrm{N} + 1.76\ \mathrm{dB} \tag{4}$$

In oversampling ADCs, the SQNR is calculated taking into account the OSR, according to Equation 5.

$$\text{SQNR} = 6.02 \times \text{N} + 1.76 + 10 \times \log(\text{OSR}) \text{ dB} \tag{5}$$

It can be seen from Equations 3 and 5 that doubling the sampling frequency, i.e the OSR, reduces the in-band quantization noise power by half, increasing the SQNR by approximately 3 dB (3 dB/octave). It provides a 0.5 bit increment in the maximum ENOB achieved by the modulator, since the ENOB is calculated according to Equation 6.

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \text{ bits} \tag{6}$$

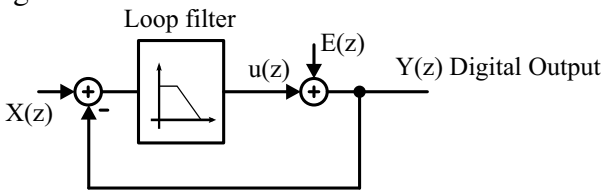
The SNDR is defined as the ratio between the signal power (usually a sinusoidal signal) and the power of the total noise produced by the circuit and the quantization process, also considering the distortions caused by the modulator circuit (ORTMANNS; GERFERS, 2006). In an ideal SD modulator, the SNDR is equal to the SQNR.

The oversampling ratio also impacts the modulator dynamic range (DR). The modulator DR is the input signal amplitude that provides an SNDR equal to zero (MALOBERTI, 2007), and its value is approximately equal to the peak SNDR (JOHNS; MARTIN, 1997).

2.1.2 *Noise Shaping*

The noise shaping is responsible for reducing the in-band quantization noise power at the cost of increasing the quantization noise out of the signal bandwidth. Thus, the flat spectrum of the quantization noise is modified resulting in a shaped spectrum (SCHREIER; TEMES, 2005) (MALOBERTI, 2007). To understand the noise shaping effect, one should consider the linear model of an SD modulator, illustrated in Figure 4, where the quantization error is represented as the addition of white noise to the quantizer.

Figure 4 – The linear model of an SD modulator.



Source: The author

The SD modulator loop filter is represented by a transfer function H(z) while the modulator feedback has a unit gain. Consequently, the SD modulator can be analyzed as a two-input system whose output, Y(z), is represented by Equation 7.

$$Y(z) = STF(z) \times X(z) + NTF(z) \times E(z) \tag{7}$$

Where $X(z)$, $Y(z)$ and $E(z)$ are, respectively, the representations of the input, output and quantization error of the SD modulator in the Z domain, and $STF(z)$ is the signal transfer function, given by Equation 8:

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{8}$$

and $NTF(z)$ is the quantization noise transfer function, calculated by Equation 9.

$$NTF(z) = \frac{1}{1+H(z)} \tag{9}$$

The SDM loop filter transfer function is chosen in order to not affect the input signal magnitude and to filter the in-band quantization noise. Therefore, H(z) must be chosen in such a way that the STF(z) behaves like a low-pass filter for the input signal and the NTF(z) behaves as a high-pass filter for the quantization. Thus, H(z) is usually chosen as a low-pass filter with high DC gain. A known transfer function with these characteristics is the integrator transfer function.

The in-band quantization noise power of an oversampling ADC with noise shaping, P_Q, is calculated according to Equation 10.

$$P_Q = \frac{\Delta^2}{12} \times \frac{\pi^{(2L)}}{(2L+1) \times OSR^{(2L+1)}} \tag{10}$$

Where L is the order of the loop filter. It should be noted that the increase of the quantization noise at high frequencies is not a critical issue since a digital decimation filter is used after the SDM, which decimates the modulator digital output and removes unwanted quantization noise at high frequencies.

The ideal DR of an L-order SDM is calculated by Equation 11 (MORGADO; DEL RÍO; DE LA ROSA, 2011).

$$\text{DR} \approx \text{SNDR} \approx 10 \times \log_{10}\left(\frac{3}{2} \times (2^{\text{N}}-1)^2 \times \frac{(2\text{L}+1) \times \text{OSR}^{(2\text{L}+1)}}{\pi^{(2\text{L})}}\right) \tag{11}$$

From Equation 11 it is possible to see that the SNDR is dependent on the OSR, the loop filter order (L) and the quantizer number of bits. Thus, strategies for increasing the performance of SD modulators are based on the change of these parameters, as described in Section 2.2.

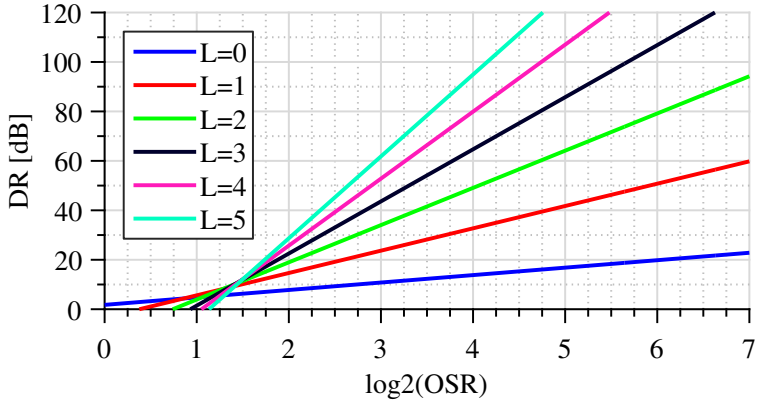
2.2 Performance of Sigma-Delta Modulators

The performance of SD modulators ir usually related to power consumption and the achieved DR for a given signal bandwidth. This section addresses the increase of modulator DR throughout changes in the modulator's high-level architecture.

2.2.1 Loop-Filter Order Increase

The increase of the loop-filter order enhances the noise shaping and more quantization noise is shaped out of the signal band. According to Equation 11, increasing the order of the modulator loop filter improves the DR. This is best evidenced in Figure 5.

Figure 5 – DR versus the OSR for different loop-filter orders. Results for a 1-bit quantizer.



Source: The author

2.2.2 Oversampling Increase

The increase in the oversampling ratio improves the DR, and these increase amount is dependent on the loop-filter order. In a first order SDM, the DR is increased by 1.5 bit/octave of OSR. In general, increasing the oversampling provides a DR increase of $(2 \times L + 0.5)$ bits/octave in an SDM with L-order loop filter.

2.2.3 Quantizer Number of Bits Increase

Increasing the quantizer number of bits reduces the quantization step and thus the quantization noise power. Each extra quantizer bit provides a DR increment of approximately 6 dB. A multi-bit quantizer requires a multi-bit DAC in the feedback loop. However, multi-bit DACs are not intrinsically linear as 1-bit DACs.

The non-linearities generated by multi-bit DACs are added directly to the input of the modulator and are not attenuated by noise shaping. Thus, the multi-bit DACs in the feedback loop must have linearity greater than or equal to the desired linearity of the SDM, which increases the design complexity of multi-bit DACs and the power consumption of the modulator. Hence, the quantizer number of bits is usually limited to four or five bits.

2.3 Classification of Sigma-Delta Modulators

Different SDMs architectures have been and continue to be reported in the literature (SCHREIER; TEMES, 2005) (DE LA ROSA, 2011). Such architectures were developed for different signal characteristics and, especially, increased DR. Thus, the main classifications of SDMs are presented below.

2.3.1 Signal Bandwidth

SDMs may be employed for the processing of low-frequency signals or signals centered at an intermediate frequency (IF) other than zero. The low-pass SDMs type are employed in the processing of low frequency signals as such as audio signals or baseband signals in zero-IF receivers. On the other hand, band-pass SDMs type are used to process non-zero IF signals, usually present in radio frequency receivers.

2.3.2 Modulator Order

An L order SD modulator is designed with an L-order loop filter. Increasing the loop-filter order causes the DR increment as previously stated. However, high-order modulators are conditionally stable and instability problems can arise in modulators with no proper coefficient scaling (DE LA ROSA; DEL RIO, 2013). Thus, in most practical implementations the loop-filter order is equal to or lower than four due to these stability issues (SCHREIER; TEMES, 2005).

2.3.3 Number of Quantizer Bits

SDMs are also classified according to the quantizer number of bits as single-bit or multi-bit (DE LA ROSA; DEL RIO, 2013). The feedback DACs have the same number of bits as the quantizer.

2.3.4 Number of Quantizers

SDMs that have only one quantizer are classified as single-loop structures. SDMs that have more than one quantizer, and therefore more than one loop, are classified as cascade SDMs. Loop filters of single-loop structures of order greater than two are subject to instability (SCHREIER; TEMES, 2005). Thus, cascade SDMs are used to generate high-order noise shaping employing more than one loop-filter with order generally lower than or equal to two (ORTMANNS; GERFERS, 2006).

2.3.5 Loop-Filter Implementation

The SDMs are also classified according to the nature of the loop filter in two main groups: discrete-time SDMs and continuous-time SDMs, focus of this work. Other classifications arose in the last years, as such as the hybrid SDMs, that combines the characteristics of both DT-SDMs and CT-SDMs (MORGADO; DE LA ROSA; DEL RÍO, 2009).

2.3.6 Sampling Technique

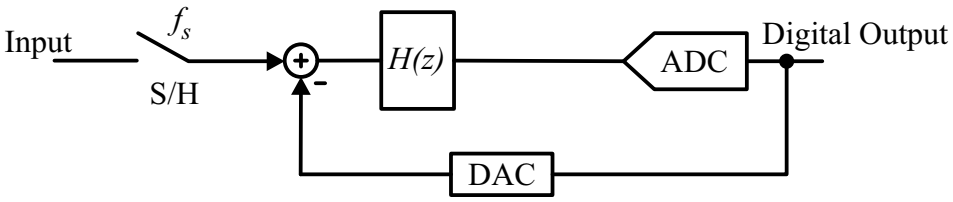
The sampling process in traditional SDMs is synchronous and the sampling frequency is constant. Synchronous SDMs are widely employed in a variety of applications and thus are the focus of this thesis. However, there are ADCs based on asynchronous SDMs where

the analog input signal is translated to an asynchronous duty-cycle square wave. It can be stated that asynchronous SDMs are a special type of continuous-time SDMs where the sampled quantizer is replaced by a continuous-time comparator with hysteresis (ROZA, 1997) and currently designs are mainly focused on low-voltage applications (KULEJ; KHATEB; FERREIRA, 2019).

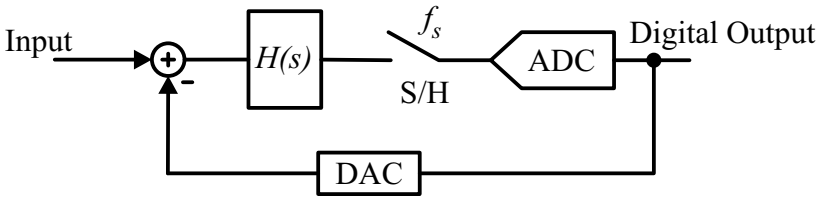
2.4 Discrete-Time versus Continuous-Time

An SD modulator can be implemented using a discrete-time or continuous-time topology. Figure 6 (a) illustrates the block diagram of a typical DT-SDM, while Figure 6 (b) represents a CT-SDM. The main difference between CT-SDMs and DT-SDMs is that in the first one the sampling operation takes place within the modulator loop and in the second one the sampling operation usually occurs in a sample-and-hold circuit at the SD modulator input (ORTMANNS; GERFERS, 2006).

Figure 6 – SD Modulators: DT versus CT.



(a) Discrete-time SD modulator.



(b) Continuous-time SD modulator.

Source: The author

Errors in the sampled signal due to the sample-and-hold limitations are present at the DT-SDM input. These errors are treated as an input signal and are not attenuated by the noise shaping, increasing the modulator noise floor. The sampling operation of a CT-SDM is at the quantizer input. Thus, the errors due to the non-ideal sampling process is attenuated by the noise shaping and does not affect the modulator performance as in their DT counterparts. (CHERRY; SNELGROVE, 2000).

Another feature of the location of the sampling process is the implicit AAF present in many CT-SDM. As the sampling occurs in front of the quantizer, the high-frequency alias components reflected for the signal bandwidth are inserted into the quantizer input. Therefore, they suffer the effect of noise shaping, being attenuated by the loop filter. However, it is necessary to analyze the modulator topology and its construction at an electric

level since the intrinsic AAF may have its characteristics degraded (PAVAN, 2011a), or even not exist when using the topology described in (SILVA *et al.*, 2001).

Regarding energy consumption, it can be stated that CT-SDMs generally present lower energy consumption than their discrete-time counterparts, making them more advantageous to high-speed and low-power applications. It is possible because the DT-SDM loop filter is implemented with switched-capacitor integrators, which require operational amplifiers with a GBW between eight and ten times the sampling frequency and a DC gain typically above 80 dB. On the other hand, CT-SDMs are usually designed with active-RC integrators whose amplifiers require a GBW in the range of one to two times the sampling frequency and a DC gain commonly in the range of 40 to 60 dB, drastically reducing the modulator power consumption (ORTMANNS; GERFERS, 2006).

However, CT-SDMs present less linearity due to the use of active-RC integrators or Gm-C integrators in the loop filter. In addition, they still suffer from the clock jitter effects, and the excess-loop delay (ELD).

2.5 Continuous-Time Sigma-Delta Modulators

This section briefly describes the main strategies to design CT-SDMs and the source of its main non-idealities.

2.5.1 Synthesis of CT-SDMs Loop Filter

The synthesis of a CT-SDM begins by defining the characteristics of the modulator, such as order, OSR and quantizer number of bits. After that, one must determine the NTF of the modulator and map the NTF to one of the existing SDM architectures. There are two main strategies to design the CT loop filter: DT/CT transformation and direct synthesis of CT loop filter (ORTMANNS; GERFERS, 2006). The first strategy is the most used since it is based on an observed equivalence between DT-SDMs and CT-SDMs.

In the last years, several modulator architectures, tools and techniques focused in DT implementations were developed. Thus, it is easier to design and analyze sigma-delta modulators in discrete-time operation to verify the achieved performance, and then to convert the discrete-time loop to a continuous-time loop (OLIAEI, 2003). After the DT/CT conversion, a CT-SDM with the same characteristics as its discrete-time counterpart is obtained (BELOTTI; BONIZZONI; MALOBERTI, 2012). The main DT/CT conversion methodologies are: impulse-invariant transformation (IIT) (SHOAEI, 1995) and modified z-transform (BENABES; KERAMAT; KIELBASA, 1997).

In this work, the IIT method is used for the DT/CT transformation for the CT-SDMs high-level design since it accurately models the effect of excess loop delay (ORTMANNS; GERFERS, 2006). The DT-SDM design is done using the Matlab Toolbox called Delta Sigma Toolbox (SCHREIER, 2016). More details will be presented in Chapter 04.

2.5.2 Clock Jitter Effects

Unlike DT-SDMs, the CT-SDMs are sensitive to the clock jitter and a modulator performance degradation is evidenced even for a jitter of 0.1% of the clock period.

The clock jitter impacts on the sampling process in front of the quantizer and during the generation of the DAC feedback signal (CHERRY; SNELGROVE, 1999a). The modulator noise shaping attenuates the sampling error due to the clock jitter. However, the induced errors in the DAC output waveform due to jitter are not attenuated by the noise shaping and limit the modulator performance. This occurs because the waveform generated by the DAC is integrated over time and the statistical variations of this waveform propagate through the modulator. Consequently, this increases the modulator output noise, reducing the SNDR. However, CT-SDMs for low-voltage applications typically operate with sampling frequencies in the range of tens of MHz, reducing the clock jitter requirements.

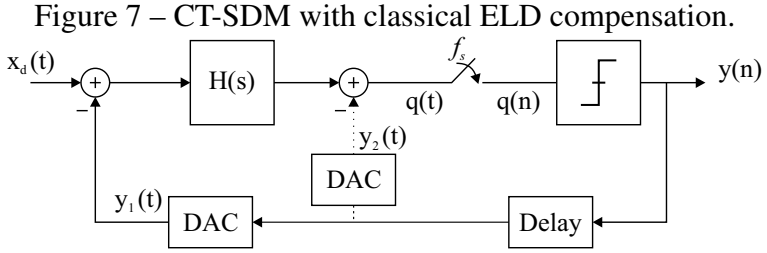
2.5.3 Excess-Loop Delay Effects

The ELD is the delay between the CT-SDM ideal feedback signal waveform and the waveform generated by the DAC in its circuit-level implementation. This delay occurs in the chain composed of the sampling process, signal quantization and digital-to-analog conversion in the feedback loop (CHERRY; SNELGROVE, 1999b).

Thus, there is a delay between the rising edge of the clock signal and the actual feedback DAC output signal change, modifying the modulator ideal transfer function H(s) and hence the equivalence between the continuous-time modulator and its discrete-time counterpart. Furthermore, the modulator can became unstable according to the ELD amount.

However, different techniques to compensate the ELD effects are present in the literature (ALAMDARI; EL-SANKARY; EL-MASRY, 2009) (SINGH; KRISHNAPURA; PAVAN, 2010) (PAVAN, 2008). In this work, the technique proposed by (PAVAN, 2008) was used, as it will be presented in Chapter 4. This technique consists in the addition of a short feedback loop around the quantizer, as illustrated in Figure 7, combined with an adjustment of the modulator coefficients. Usually, a fixed delay of half or a full clock period is used. Additionally, this fixed delay avoids possible errors due to the quantizer metastability (CHERRY; SNELGROVE, 1999a).

Figure 7 – CT-SDM with classical ELD compensation.



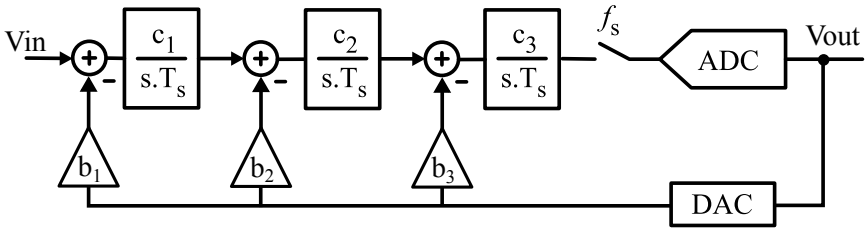
Source: The author

2.6 SDM Architectures for Sub-1V Applications

Usually, CT-SDMs for sub-1V applications present in the literature are of the low-pass type, with the exception of the work presented by (HE *et al.*, 2011). Thus, only the main architectures of low-pass CT-SDMs are discussed in this Section (SCHREIER; TEMES, 2005): Cascade of Integrators Feedback (CIFB) and Cascade of Integrators in Feed-Forward (CIFF).

The CIFB architecture has multiple feedback paths into the loop filter. The required number of feedback DACs is equal to the loop-filter order. Figure 8 shows the block diagram of a generic third-order SDM implemented with the CIFB architecture. Also, the input signal component is present at the output of each integrator. Thus, the integrators output swing is larger when compared to the output swing of the integrators of a CIFF architecture. Another characteristic is the GBW requirement of the loop-filter amplifiers: the closer the amplifier is to the quantizer, higher is the required GBW.

Figure 8 – Third-order generic CIFB architecture.



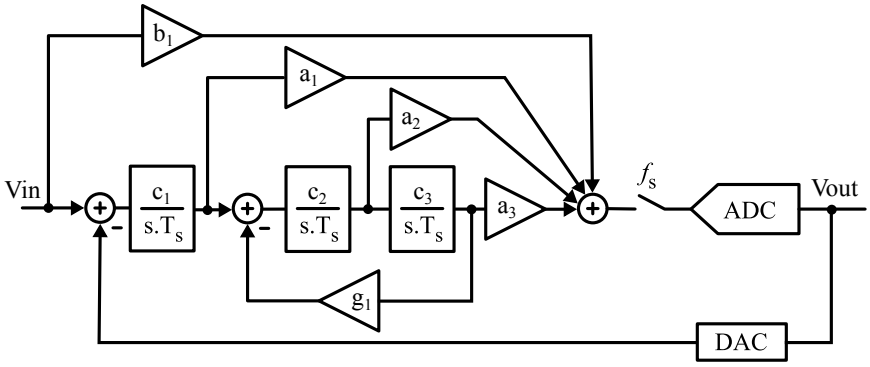
Source: The author

The CIFF architecture, shown in Figure 9, uses only one DAC in the feedback loop and an adder in front of the quantizer to sum the output signals of each integrator. This architecture presents integrators with low output swing, being a good choice for low-voltage applications.

In this topology, the amplifier of the first integrator requires high GBW and linearity, and these requirements are reduced for the subsequent amplifiers. The coefficient b_1 can be defined as 0 or 1. The input signal component is present at the integrator outputs when b_1 is equal to 0. However, when $b_1 = 1$, the input signal is applied to the quantizer input and the modulator provides an STF equal to 1 (SILVA *et al.*, 2001). In this case, the integrators output swing is low since the loop filter processes only the quantization noise. Also, the CT-SDMs intrinsic anti-alias filter ceases to exist because the input signal is applied directly to the input of the quantizer and is not filtered by the low-pass filter of the modulator (LV; LI, 2015).

As a common feature, both architectures can be adapted for inclusion of resonators in the loop filter, which are responsible for implementing a NTF with optimized zeros, and therefore increasing the modulator SQNR (SCHREIER; TEMES, 2005). The CIFF architecture presented in Figure 9 has a resonator composed of the last two integrators

Figure 9 – Third-order generic CIFF architecture.



Source: The author

and a feedback path with the coefficient g_1 around these two integrators.

Suitable modulator architectures for low-voltage operation should present integrators with low output swing due to limitations imposed by the reduced power supply. Therefore, the CIFF architecture is employed in this thesis work. However, it should be noted that some sub-1V CT-SDMs were designed with the CIFB topology (PUN; CHATTERJEE; KINGET, 2007) (CHEN; PUN; KINGET, 2011). Additionally, single-bit quantizers are the best candidates for sub-1V applications due to their intrinsic linearity (MALOBERTI, 2007).

2.7 Figures of Merit

The comparison between SD modulators reported in the literature is done with the aid of figures of merit (FoM) (DE LA ROSA; DEL RIO, 2013) based on the main SD modulator specifications. In this work, two FoMs widely accepted by the community of SDM developers are used: Walden FoM (FoM_W) and the Schreier FoM (FoM_S).

The FoM_W was proposed by (WALDEN, 1999) and is expressed in Equation 12:

$$FoM_W = \frac{P_W(W)}{2^{ENOB(bits)} \times 2 \times BW} \times 10^{15} \ [fJ/conv] \tag{12}$$

where P_W is the circuit power consumption, ENOB is the modulator effective number of bits and BW is the modulator bandwidth. This FoM is expressed in Joules and gives the amount of energy used for one conversion step. It is the most used FoM for ADCs comparison and emphasizes energy consumption. The lower its value, more power-efficient is the modulator.

The Schreier FoM was initially introduced in (RABII; WOOLEY, 1997) and presented in a modified form in (SCHREIER; TEMES, 2005). This FoM is calculated according to Equation 13. It emphasizes the modulator DR and the larger the value of this FoM, more power-efficient is the modulator.

$$\mathrm{FoM_S} = \mathrm{DR} + 10\log\left(\frac{\mathrm{BW}}{\mathrm{P_W}}\right)\ [\mathrm{dB}] \tag{13}$$

When the modulator exhibits a strong non-linear behavior, the SNDR is limited, reducing the ENOB. Then, the Schreier FoM could be used replacing the DR by the SNDR to a better evaluation of circuits under analysis, as shown by Equation 14.

$$\mathrm{FoM_{SNDR}} = \mathrm{SNDR} + 10\log\left(\frac{\mathrm{BW}}{\mathrm{P_W}}\right)\ [\mathrm{dB}] \tag{14}$$

2.8 Final Considerations

This Chapter provided the background of sigma-delta modulation and the main characteristics of CT-SDMs. Since the focus of this work is the design of inverter-based CT-SDMs for sub-1V applications, the main design strategies and the appropriate architectures for sub-1V operation are provided.

In the next Chapter, the operation principle of CMOS inverters as analog amplifiers and a deep bibliographic review on CT-SDMs with inverter-based amplifiers are given.

3 SIGMA-DELTA MODULATORS WITH INVERTER-BASED AMPLIFIERS

The design of CT-SDM for sub-1V applications requires the development of low-voltage operational transconductance amplifiers since these are essential elements of the SDM loop filter (ORTMANNS; GERFERS, 2006). Usually, CT-SDMs are designed using fully differential amplifiers, from now on called as differential amplifiers. Differential amplifiers are used in AD conversion applications since they provide common-mode noise suppression (RAZAVI, 1998). However, these amplifiers need an additional circuit to control the output common-mode voltage: the common-mode feedback circuit (CMFB).

The first CT-SDMs reported on the literature capable of 0.5 V operation usually uses two-stage differential OTAs with bulk-input (PUN; CHATTERJEE; KINGET, 2007). The circuits reported by (HE *et al.*, 2011) and (CHEN; PUN; KINGET, 2011) uses a two-stage gate-input differential amplifier previously reported in (HE; PUN; KINGET, 2009).

It should be noted that high-performance or high-resolution circuits are designed for their MOS transistors to operate in the strong inversion region ($V_{GS} - V_T > 0.2$ V) (Gate-Source Voltage - V_{GS}; Threshold Voltage - V_T) (CHATTERJEE; TSIVIDIS; KINGET, 2005). This requires the voltage between drain and source terminals (V_{DS}) to be higher than 0.2 V, and the minimum V_{DS} voltage, for both weak inversion and moderate inversion, is in the range of 150 mV (TSIVIDIS; MCANDREW, 2010). Thus, the development of amplifier topologies with the reduced number of stacked transistors is sought. An excellent alternative for low voltage applications is the use of CMOS inverters as in the loop filter of sigma-delta (DE LA ROSA *et al.*, 2015).

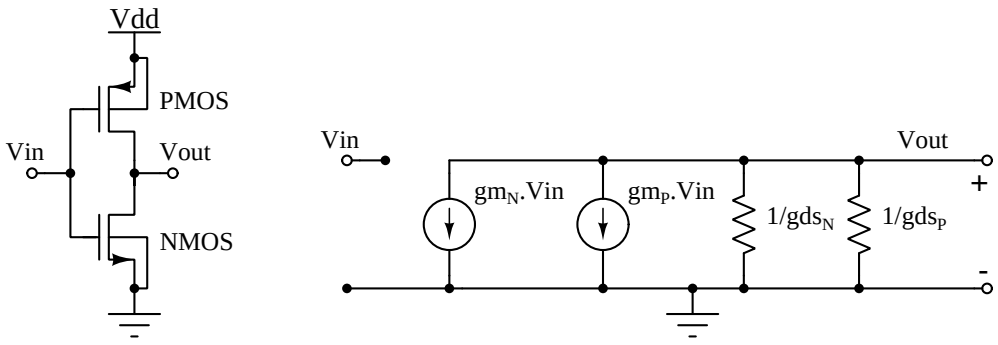
Hereafter, this Chapter provides a review of CMOS inverters operating as analog voltage amplifiers and later a review on SD modulators with CMOS inverters in the loop filter is provided.

3.1 CMOS inverters as analog voltage amplifiers

The following analysis demonstrates the main features of the CMOS inverter operating as an amplifier. Consider the schematic of a CMOS inverter and its respective small-

signal AC model, without the parasitic capacitances, shown in Figure 10. The AC gain of a CMOS inverter calculated according to Equation 15.

Figure 10 – CMOS inverter and its small-signal model.



(a) Schematic. (b) Small-signal model.

Source: The author

$$\mathrm{Av} = -(\mathrm{gm_N} + \mathrm{gm_P}) \times \frac{1}{\mathrm{gds_N} + \mathrm{gds_P}} \tag{15}$$

Where $\mathrm{gm_N}$, $\mathrm{gm_P}$, $\mathrm{gds_N}$ and $\mathrm{gds_P}$ are, respectively: NMOS transistor transconductance, PMOS transistor transconductance, NMOS transistor output conductance and PMOS transistor output conductance. These parameters, calculated by using the MOS transistor square model, are expressed by Equations 16 and 17 (GRAY *et al.*, 2009).

$$\mathrm{gm} = \mu \mathrm{C_{ox}} \left(\frac{\mathrm{W}}{\mathrm{L}}\right)(\mathrm{V_{GS}} - \mathrm{V_T}) = \frac{2\mathrm{I_D}}{(\mathrm{V_{GS}} - \mathrm{V_T})} \tag{16}$$

$$\mathrm{gds} = \lambda \left(\frac{\mu \mathrm{C_{ox}}}{2}\right)\left(\frac{\mathrm{W}}{\mathrm{L}}\right)(\mathrm{V_{GS}} - \mathrm{V_T})^2 = \approx \lambda \mathrm{I_D} \tag{17}$$

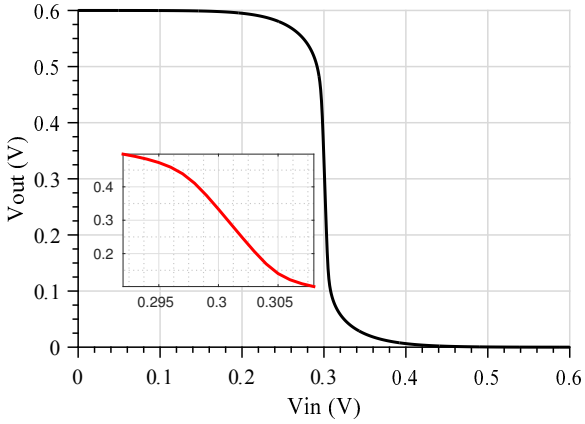
Where λ is the channel length modulation effect, W is the channel width, L is the channel length, Cox is the oxide capacitance and $\mathrm{I_D}$ is the drain current (RAZAVI, 1998).

According to Equation 15, the gain is dependent on the sum of NMOS and PMOS transistors transconductances instead of only one of these transconductances as in classic differential amplifiers (RAZAVI, 1998). Thus, it can be concluded that CMOS inverters have high transconductance efficiency.

The channel width increase of both PMOS and NMOS transistors generates the increase of transistors transconductance and output conductance (*gds*). Consequently, the inverter gain-bandwidth product increases. Hence, the CMOS inverter gain is controlled by the transistors length. It is directly related to the transistors intrinsic gain. A good approach to set the L of the transistors is to perform a full technology characterization as proposed by (JESPERS; MURMANN, 2017).

Figure 11 presents the DC transfer function of a CMOS inverter. Usually, the inverted is designed for a trip-point voltage (V_{trip}) equal to half of the supply voltage (NAUTA, 1992). The maximum inverter gain is achieved for input common-mode voltages equal or near to the inverter trip-point voltage.

Figure 11 – CMOS inverter transfer function. VDD=0.6 V.



Source: The author

The V_{trip} is calculated considering that the drain current of the NMOS and PMOS transistors are equal. By using the drain current square model, the V_{trip} value is calculated by Equation 18 (NAUTA, 1992).

$$V_{trip} = \frac{VDD - |V_{TP}| + V_{TN} \times \sqrt{\frac{\beta_N}{\beta_P}}}{1 + \sqrt{\frac{\beta_N}{\beta_P}}} \tag{18}$$

Where $\beta = \mu C_{ox} \frac{W}{L}$, V_{TP} and V_{TN} are the PMOS and NMOS transistors *threshold* voltage, respectively. Based on what has been presented, one may conclude that V_{trip} is sensitive to PVT variations. Thus, the operating point of CMOS inverters is dependent on PVT changes, which affects the inverter's DC gain and GBW.

Ideally, it is intended to bias the inverter-based amplifier with an input common-mode voltage equal to V_{trip}, enabling maximum voltage gain, and an output common-mode voltage equal to V_{trip}. However, this is not possible without the use of some technique to mitigate the effects of PVT variations on the studied inverter.

In (NAUTA, 1992), the proposed compensation strategy is to use a CMOS inverter replica with its input connected to its output to bias the main amplifier. However, transconductance variations of up to 50 % are evidenced. Thus, it can be stated that the biggest challenge for the design of amplifiers based on CMOS inverters is the increase of their robustness against PVT variations (HARJANI; PALANI, 2015).

3.1.1 Effects of PVT Variation in Inverter-Based Amplifiers

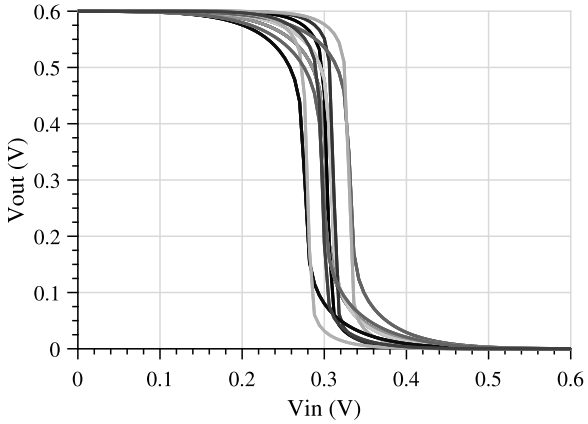
Process variations can be classified into global variations and local variations (WIRNSHOFER, 2013). For global variations such as oxide thickness and dopants concentration, the parameters of all devices are equally varied. These effects can be visualized using process corners simulations. Local variations, known as mismatch, are randomly uncorrelated variations and each device is affected differently. These effects can be verified through Monte Carlo simulations.

The process variations are represented by the variation of the mobility (μ) of the devices and V_T variations. The value of V_T is affected by variations of dopants and also temperature variations (TSIVIDIS; MCANDREW, 2010). The impacts of PVT variations on the performance of a CMOS inverter are illustrated by means of schematic level simulations using an inverter designed with a 130 nm CMOS process and powered by a 0.6 V power supply.

Take into account a CMOS inverter with transistors size equal to: $W_{PMOS} = 5.7\ \mu$m, $L_{PMOS} = 1.0\ \mu$m, $W_{NMOS} = 1.4\ \mu$m and $L_{NMOS} = 1.0\ \mu$m. In addition, a 300 mV DC voltage is applied at the PMOS body terminal. Results from process corners simulations for different temperatures ($-25°$C, 25°C and 85°C) indicate a V_{trip} voltage ranging from 276.8 to 330.5 mV whereas the typical value is around VDD/2 (302.4 mV).

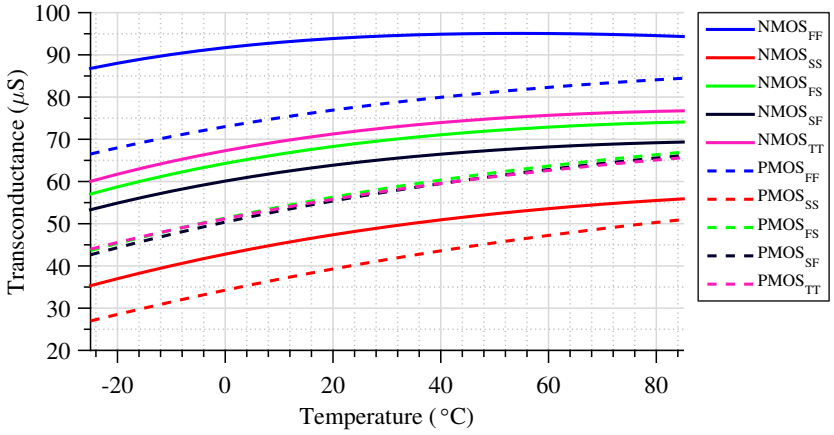
Figure 12 shows different simulated DC transfer functions of the above-mentioned inverter. One can concluded that this inverter can not have a fixed DC bias voltage, because when subjected to PVT variations the inverter will not be operating in the linear range. Thus, it is imperative to develop CMOS inverters bias techniques that are tolerant to PVT variations. The DC gain of the inverter and the GBW are also quite susceptible to variations in the supply voltage and temperature. It is explained by the transconductance variation of the transistors of the CMOS inverter, whose behavior versus temperature and voltage are presented, respectively, in Figures 13 and 14.

Figure 12 – CMOS inverter DC transfer function for different process corners.



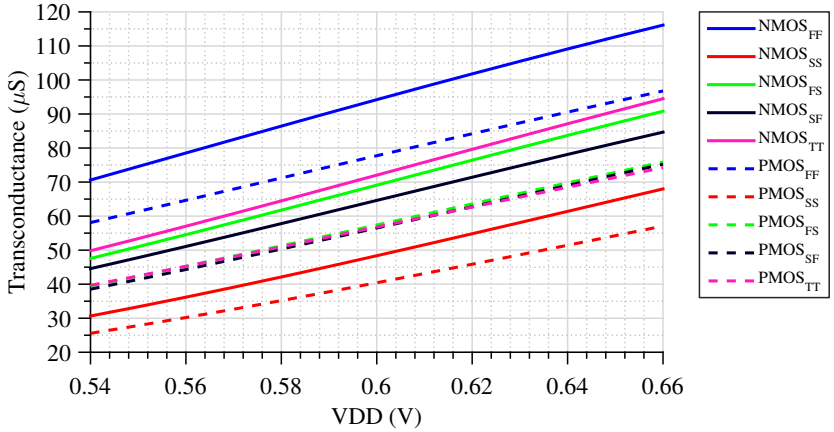
Source: The author

Figure 13 – Transconductance versus temperature.



Source: The author

Figure 14 – Transconductance versus power supply.



Source: The author

Using the replica approach to bias this inverter at V_{trip} it is possible to achieve DC gains from 29.88 dB to 33.88 dB and GBW ranging from 9.78 to 28.02 MHz for different process corners and temperature ranging from -25°C to 85°C. However, this bias strategy is dependent on transistors matching and requires a CMFB circuitry for the design of pseudo-differential amplifiers since a CMOS inverter does not provide rejection of the input common mode voltage. Possible solutions to mitigate the effects of PVT variations are presented in Section 3.2.

3.2 Inverter-Based Amplifiers with PVT Compensation

The strategies to mitigate the effects of PVT variations in inverter-based amplifiers include: input common mode voltage control, supply voltage control (CHRISTEN, 2013), body-bias to control the V_T of the transistors (LUO *et al.*, 2013) and the control of the current flowing through the inverter transistors (ISMAIL; MOSTAFA, 2016) (HARJANI; PALANI, 2015). It should be noted that these strategies aim to restore the inverter V_{trip},

previously described in Equation 18.

3.2.1 Supply Voltage Control

The V_{trip} is proportional to the inverter supply voltage. Thereby, the inverter operating point can be controlled by monitoring V_{trip} and correcting the supply voltage. It can be done using a low-dropout voltage regulator (LDO).

3.2.2 Body-Bias Control

This strategy aims to change the transistors threshold voltage through body-bias to restore the V_{trip}, as can be seen in Equation 19 (GRAY *et al.*, 2009).

$$V_T = V_{T0} + \gamma \times (\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}) \tag{19}$$

Where V_{T0} is threshold voltage for $V_{SB} = 0$ V, V_{SB} is the voltage between source and bulk, $2\phi_F$ is the surface potential and γ is the parameter that defines the MOS transistor body effect. The change of V_T could be performed by forward bulk-bias ($V_{SB} < 0$ V) to decrease V_T or by reverse bulk-bias ($V_{SB} > 0$ V) to increase V_T.

This is exemplified by considering an NMOS transistor with source terminal connected at 0 V and the bulk terminal connected at a voltage V_B = 0 V. If V_B increases, a V_{SB} reduction occurs, and consequently the reduction of V_{TN} due to the forward bulk biasing, generating the reduction of V_{trip}. In the case of a PMOS transistor, consider the source terminal connected at 0.6 V and the bulk terminal connected at a voltage VB = 0.3 V. This generates a voltage $V_{SB} > 0$ V, increasing the V_T of the PMOS transistor, and reducing V_{trip}.

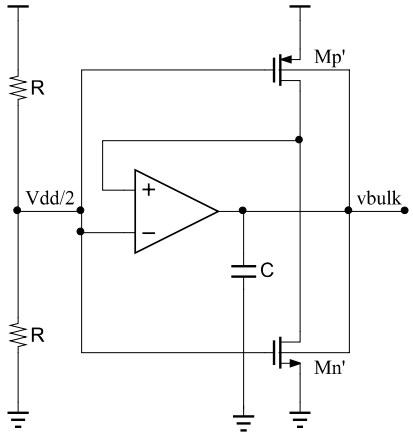
An example of this strategy, proposed in (VIERU; GHINEA, 2011), is presented in Figure 15. This circuit generates the bulk voltage of the transistors of a CMOS inverter to mitigate the effects of PVT variations. Applying this strategy to bias only the bulk terminal of the PMOS transistor of the example of the previous section, it is possible to reduce the V_{trip} variation from 276.8-330.5 mV to 298.8-308.2 mV.

3.2.3 Current Bias Control

This control technique aims to change the current flowing through both NMOS or PMOS transistors or keep the current of one of these transistors fixed while the other changes according to PVT variations. This method usually generates a bias voltage to bias replicas of the same controlled inverter. Thus it is possible to reduce the transconductance variations of the transistors due to PVT variations (HARJANI; PALANI, 2015).

The current change of the NMOS and PMOS transistors is performed to keep a constant transconductance or to keep the current drawn by inverters constant (PALANI; HARJANI, 2014).

Figure 15 – Circuit to generate the transistors bulk voltage of a CMOS inverter.



Source: (VIERU; GHINEA, 2011)

3.3 Input-Referred Noise in Inverter-Based Amplifiers

Among the design stages of CT-SDM, one can cite the calculation of the maximum noise level referred to the modulator input. This noise is composed of the sum of the noise of the passive components, the noise from the DAC and the input-referred noise of the first integrator amplifier. In this work, amplifiers based on CMOS inverters are used in all the integrators of the modulator. Thus, the noise analysis of a CMOS inverter is necessary.

The amplifier input-referred noise analysis is easily performed in the Cadence simulation environment (*Noise Analysis*), which was used in this work. However, analytical noise analysis is suggested to evaluate the relationship between the design variables and the resulting noise. For this, it is necessary to calculate the noise contribution of each transistor of the inverter.

MOS transistors have two major noise sources: *flicker* noise, also known as $1/f$ noise, and thermal noise. Flicker noise is dominant at low frequencies and is modeled as a voltage source in series with the gate of the transistor, whose voltage density per unit of bandwidth is expressed by:

$$\bar{v}_{in-flicker}^2 = \frac{K}{C_{ox}WL} \times \frac{1}{f} \, [V^2/Hz] \tag{20}$$

where K is a process dependent constant (RAZAVI, 1998) and C_{ox} is the oxide capacitance that is defined by 21, where t_{ox} is the oxide thickness, ε_o is the vacuum permittivity and ε_r is the relative permittivity.

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \tag{21}$$

The total thermal noise main source is the noise generated inside the MOS transistor channel. This noise is modeled as a current source in parallel with the drain and source

terminals of the transistor. The current spectral density per unit of bandwidth is defined in Equation 22 (RAZAVI, 1998):

$$\bar{I^2} = 4kT\gamma gm \tag{22}$$

where γ is equal to 2/3 for long channel transistors, which may have a higher value for short channel devices. The total output thermal noise due to the noise contribution of PMOS and NMOS transistors is calculated according to Equation 23.

$$\bar{v}^2_{out-thermal} = \frac{(4kT\gamma gm_N + 4kT\gamma gm_P)}{(gds_N + gds_P)^2} \tag{23}$$

Thus, the output thermal noise referred to the input is calculated by dividing Equation 23 by the squared inverter gain (BAKER, 2010), as expressed in Equation 24.

$$\bar{v}^2_{in-thermal} = \frac{(4kT\gamma)}{gm_N + gmP} \tag{24}$$

Considering what has been presented, one can calculate the total noise density per unit of bandwidth referred to the input of a CMOS inverter according to Equation 25.

$$\bar{v}^2_{in-total} = \frac{(4kT\gamma)}{gm_N + gmP} + \frac{K_N}{C_{oxN}W_N L_N} \times \frac{1}{f} + \frac{K_P}{C_{oxP}W_P L_P} \times \frac{1}{f} \; [V^2/Hz] \tag{25}$$

This analysis could be extended to calculate the input-referred noise of differential and pseudo-differential inverter-based amplifiers.

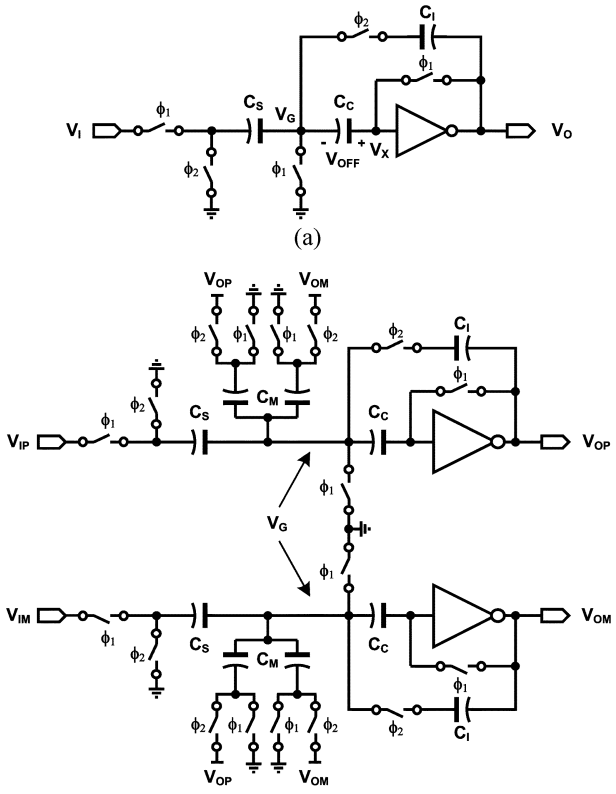
3.4 Sigma-Delta Modulators with Inverter-Based Amplifiers: State-of-the-Art Review

This section will present a review of the state-of-the-art on SDMs with inverter-based amplifiers. The main figure-of-merit used for comparison is the FoM_W (DE LA ROSA *et al.*, 2015). It depends on the circuit power consumption, the bandwidth of the input signal (BW) and the signal-to-noise and distortion ratio (SNDR). The smaller the value of this FOM the more efficient is the modulator.

The first sigma-delta modulator with inverters based-amplifiers was introduced in 2009 by (CHAE; HAN, 2009) and it is a discrete-time implementation using switched-capacitor (SC) integrators. The SC integrator implementation uses the auto-zeroing technique to mitigate the effects of the inverter input-referred offset, as depicted in Figure 16. A study of the impact of the inverter supply voltage (VDD) in the inverter operation mode is presented as well: class AB operation if $\text{VDD} > \text{V}_\text{TN} + |\text{V}_\text{TP}|$ or class C operation if $\text{VDD} < \text{V}_\text{TN} + |\text{V}_\text{TP}|$.

The supply voltage value also impacts on the DC gain and GBW of the inverter. The inverter DC gain is maximized in the weak inversion region while the GBW increases

Figure 16 – Inverter-based switched capacitor integrator.



Source: (CHAE; HAN, 2009)

proportionally with the supply voltage until the transistors start their operation in the saturation region. (CHAE; HAN, 2009) suggests that the inverter power supply should be equal to $V_{TN} + |V_{TP}|$ for the inverter to present high DC gain and high GBW. Thus, the inverter transistors operate between the weak inversion and strong inversion region. Three DT-SDMs were developed in (CHAE; HAN, 2009), one of them operating at 0.7 V with a sampling frequency of 4 MHz for a signal bandwidth of 20 kHz. The peak SNDR of this modulator is 81 dB, its FoM_W is 98 fJ/step, and is considered, to this date, one of the best FoMs for SDMs designed with inverter-based integrators.

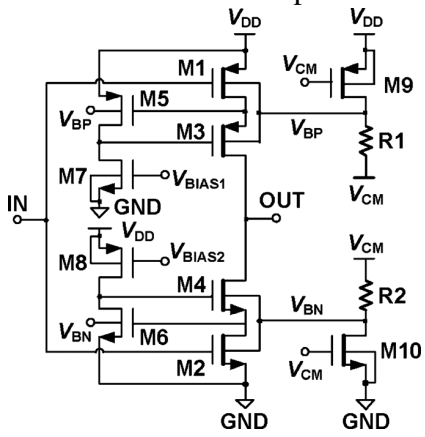
In (WANG; MATSUOKA; TANIGUCHI, 2009) the authors presented the design and measurement results of a fourth-order discrete-time SDM based on CMOS inverters. This modulator operates with a 0.5 V supply voltage providing an SNDR of 71 dB for a signal bandwidth of 78 kHz (Fs = 10 MHz) while its FoM_W is 1,900 fJ/step.

A SC SDM operating with a supply voltage of 250 mV is presented by (MICHEL; STEYAERT, 2012). In this work, integrators based on CMOS inverters operating in sub-threshold are used. The biasing approach for the inverters is accomplished by using a switched capacitor in series with the sampling capacitor present at the integrator input, increasing the circuit operation complexity. Due to the low power supply, a clock booster circuitry is used to increase the clock signal voltage for faster switching. This work uses inverters with 30 dB of DC gain, which reduces the SNDR of the modulator. However,

this work still presents an SNDR of 61 dB for a signal bandwidth of 10 kHz providing a FoM_W of 410 fJ/step.

In 2013, a SC SDM for audio applications operating at 0.8 V is introduced by (LUO *et al.*, 2013). This circuit also uses the auto-zeroing technique and the same CMFB strategy used in (CHAE; HAN, 2009). The integrators are pseudo-differential ones and are designed with cascode class-C inverters ($VDD < V_{TN} + |V_{TP}|$). Additionally, a gain-boosting technique (SACKINGER; GUGGENBUHL, 1990) is used providing DC gains higher than 80 dB. The schematic of the proposed inverter is shown in Figure 17. A body-bias technique is used to mitigate the effects of PVT variation. This technique uses forward bulk bias to change the V_T of the transistors of the inverter, reducing the GBW variation for different process corners. However, resistors R1 and R2 are off-chip components and also a manual trimming is required. This modulator provides an SNDR of 91 dB for a signal bandwidth of 20 kHz when operated with a 0.8 V power supply, and provides a FoM_W of 198.25 fJ/step.

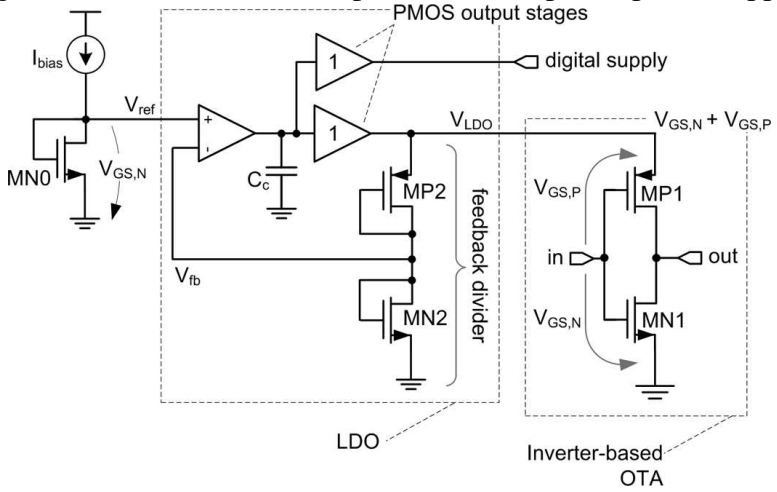
Figure 17 – Gain-boosted inverter-based amplifier with PVT compensation.



Source: (LUO *et al.*, 2013)

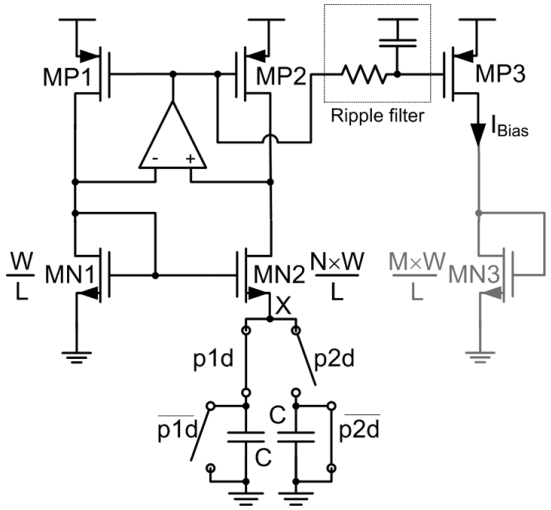
Another SC SDM with inverter-based amplifiers was introduced by (CHRISTEN, 2013), but for operation with a supply voltage of 1.4 V ($VDD = V_{TN} + |V_{TP}| + 200mV$), that is with the transistors operating in moderate inversion. The operating point of the inverters is controlled by changing the supply voltage, as shown in Figure 18. A low-dropout voltage regulator (LDO) is used to generate a supply voltage that keeps the inverters' V_{trip} equal to $V_{GS,N}$, mitigating the effects of PVT variations on the inverter operating point. The current source I_{bias} is generated by a constant Gm-C current reference as shown in Figure 19. This current reference was initially presented in (GREGOIRE; MOON, 2007), and allows to generate a transconductance proportional to the switching frequency of the capacitors. This modulator provides an SNDR of 87.9 dB for a signal bandwidth of 20 kHz bandwidth while featuring a FoM_W of 173 fJ/step. However, it should be noted that this modulator is reconfigurable, and can be used for signal bandwidths up to 100 kHz.

Figure 18 – Inverter-based amplifier with adaptable power supply.



Source: (CHRISTEN, 2013)

Figure 19 – Constant Gm-C current reference.

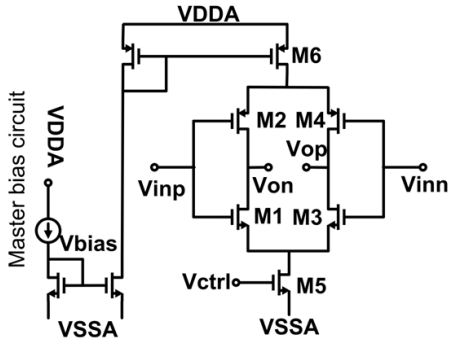


Source: (CHRISTEN, 2013)

A fully differential CMOS inverter OTA is used in the circuit proposed by (HONARPARVAR; SAFI-HARB; SAWAN, 2016), as shown in Figure 20. The transistors of the amplifier operate in weak-inversion, allowing DC gains of up to 50 dB. This work presents the design of a fourth order multi-stage noise-shaping (MASH) composed of two second-order SC SDMs. This work was designed in a 180 nm CMOS technology operating at 0.9 V. Post-layout simulation results indicate an SNDR of 89 dB for a signal bandwidth of 20 kHz and a FoM_W of 58 fJ/step.

In the same year, the work presented in (FAZLI YEKNAMI, 2016) introduces an SC SDM operating at 0.3 V. This modulator is designed with a new inverter-based amplifier topology, depicted in Figure 21, and is suitable to implantable medical devices. This amplifier consists of a CMOS inverter followed by a single current mirror output stage (GRAY *et al.*, 2009). It enables the increase of DC gain and GBW. The gain of this

Figure 20 – Fully-differential inverter-based amplifier.

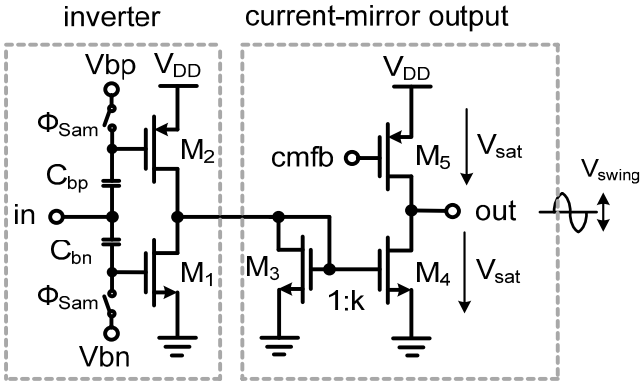


Source: (HONARPARVAR; SAFI-HARB; SAWAN, 2016)

amplifier is calculated according to Equation 26. This circuit uses an internal clock signal generator with low-V_T devices and auxiliary circuits such as charge-pumps and level shifters to increase the clock signal voltage. This circuit has an SNDR of 60.7 dB for a signal bandwidth of 1 kHz and provides a FoM_W of 464 fJ/step. However, these results are based on schematic-level simulations, and the impact of mismatch and different process corners is not addressed.

$$Av = \frac{gm_1 + gm_2}{gm_3 + gds_1 + gds_2 + gds_3} \times \frac{gm_4}{gds_4 + gds_5} \tag{26}$$

Figure 21 – Inverter-based amplifier with current mirror output stage for gain enhancement.

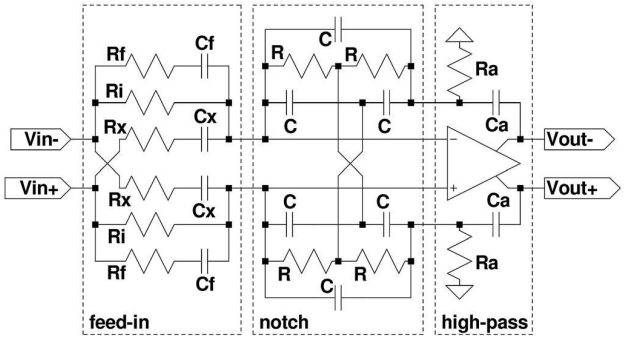


Source: (FAZLI YEKNAMI, 2016)

3.4.0.1 CT-SDMs with Inverter-Based Amplifiers

The first CT-SDM with inverter-based amplifiers is presented in (ZELLER *et al.*, 2014). This work introduces a pseudo-differential CT-SDM, composed of two single-ended modulators. It presents for the first time a third-order CT-SDM using only one amplifier (loop filter with a third-order resonator). Figure 22 presents this third-order resonator, which is derived from the second-order one proposed in (ZELLER; MUENKER; WEIGEL, 2011).

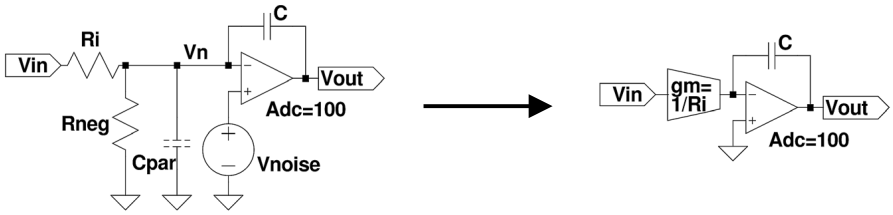
Figure 22 – Third-order resonator.



Source: (ZELLER *et al.*, 2014)

However, the transfer function of this resonator is affected by the finite DC gain and finite GBW of the amplifier (ZANBAGHI; HANUMOLU; FIEZ, 2013). Thus, this work uses different techniques to mitigate these two effects. These techniques can be used in integrators or resonators, and are explained below. For this, an active RC integrator, shown in Figure 23, will be used for explanation purposes.

Figure 23 – Integrator with negative resistance at the input.



Source: (ZELLER *et al.*, 2014)

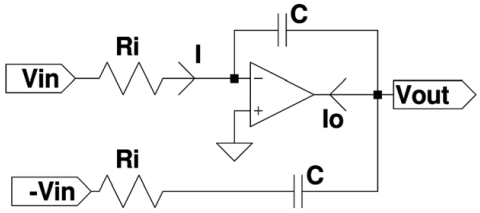
The finite amplifier DC gain generates oscillations on the circuit virtual ground, deteriorating the input current through the resistor Ri. A possible solution to this problem is the use of a high output impedance transconductor, with $\mathrm{gm} = 1/\mathrm{Ri}$, instead of resistor Ri. However, a negative resistance at the amplifier input can be used to reduce or even nulling the effects of amplifier finite DC gain when ($|\mathrm{R_{neg}}| = \mathrm{Ri}$). The transfer function of an active RC integrator with a negative resistance at its input is presented in Equation 27. Thus, the transfer function of the integrator can be restored using a negative resistance Rneg equal to Ri. Cross-coupled inverters at the amplifier inputs are used to implement negative resistances in the circuit proposed in (ZELLER *et al.*, 2014).

$$\frac{\mathrm{Vout(s)}}{\mathrm{Vin(s)}} = -\frac{1}{\left(1+\frac{1+\mathrm{Cpar/C}}{\mathrm{A(s)}}\right)\mathrm{sRiC}+\frac{1+\mathrm{Ri/Rneg}}{\mathrm{A(s)}}} \tag{27}$$

This work also uses a technique to aid amplifiers with low GBW, similar to the technique known as Assisted OpAmp (PAVAN; SANKAR, 2010). The first integrator of most sigma-delta modulators has at the input both the input signal and the high-speed DAC feedback. Thus, the integrator amplifier should provide an output current Io containing

high-frequency components. It is possible to use an auxiliary circuit responsible for providing part of this output current, thereby reducing virtual ground oscillations, and consequently, the distortion at the integrator output. Figure 24 presents an amplifier assistance technique based on an RC path.

Figure 24 – RC path to assist the integrator amplifier.



Source: (ZELLER *et al.*, 2014)

Thereby, it is possible to reduce the ratio of the current supplied by the amplifier according to the equation 28. Further, the bias current of the amplifier can be reduced by reducing the energy consumption of the first integrator. The second CT-SDM prototype designed in this thesis uses this technique to allow the loop-filter operation at 500 mV and below.

$$\frac{\mathrm{Io(s)}}{\mathrm{I(s)}} = -\frac{2}{\mathrm{sRC}+1} \tag{28}$$

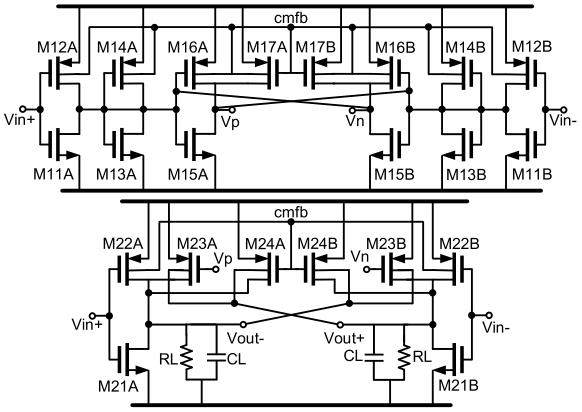
The CMOS inverter used in this work is a cascode one with low-V_T cascode transistors. The pseudo-differential modulator output common-mode voltage is controlled through an adaptive bulk bias circuit which generates different NMOS and PMOS bulk voltages. This work still remains among state-of-the-art sigma-delta modulators due to its small $\mathrm{FoM_W}$.

A third-order CT-SDM composed of active-RC integrators is proposed in (ESSAWY; ISMAIL, 2014). The amplifiers of the integrators are implemented with Nauta transconductors (NAUTA, 1992). This modulator operates with a power supply voltage of 0.75 V and a clock frequency of 100 MHz, enabling an SNDR of 50 dB for 2 MHz signal bandwidth. These results are based on schematic level simulations and achieved $\mathrm{FoM_W}$ is 581 fJ/step.

In 2015, a fourth-order inverter-based CT-SDM operating with a 300 mV supply voltage was reported in (LV; LI, 2015). This work uses two-stage amplifiers with feedforward compensation (THANDRI; SILVA-MARTINEZ, 2003), as shown in Figure 25. Transistors M11x and M12x compose the first stage. The second stage consists of transistors M23x, while the compensation stage is composed of the transistors M21x and M22x. The transistors M15 and M16 implement negative resistances to increase the gain of the first stage. The gain of the second stage is increased through the use of a negative resistance implemented through the bulk transconductance, gmb, of the transistors M23 and M24. The output common-mode voltage control is performed through the bulk terminal of the PMOS transistors and the auxiliary transistors M17 and M24. The common-mode

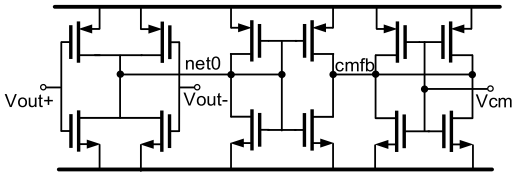
feedback circuit, shown in Figure 26, is performed based on the differential difference amplifier proposed in (CZARNUL; TAKAGI; FUJII, 1994). This work presents post-layout simulation results. The peak SNDR is 75.9 dB for a 50 kHz BW with Fs of 6.4 MHz. The achieved FoM_W is only 57 fJ/step. However, it should be noted that no analysis regarding process variations and mismatch is presented.

Figure 25 – Two-stage inverter-based amplifier with feedforward compensation.



Source: (LV; LI, 2015)

Figure 26 – Common-mode feedback circuitry.

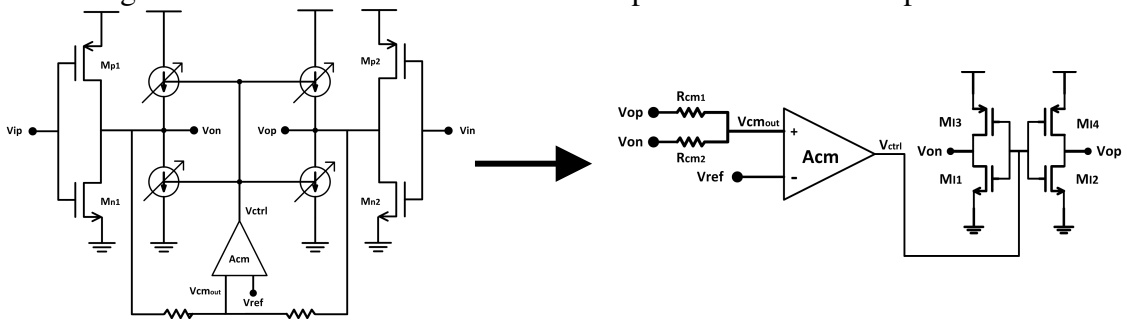


Source: (LV; LI, 2015)

A third-order CT-SDM using CMOS inverters with PVT compensation by changing the drain current of the PMOS and NMOS transistors was introduced in (ISMAIL; MOSTAFA, 2016). The proposed amplifier is shown in Figure 27. Resistors are used to sense the output common-mode voltage and an error amplifier compares this voltage to the reference voltage generating a control voltage. This control voltage controls the current of the auxiliary current sources, which are also implemented with CMOS inverters. This technique is an optimization of the semi-constant current bias (SSCB) technique presented in (HARJANI; PALANI, 2015). The amplifier is characterized in different process corners, but no variability analysis is presented. The modulator operates at 0.8 V and schematic-level simulation results indicate a peak SNDR of 74 dB for a 64 kHz BW with Fs of 6.4 MHz, while the achieved FoM_W is 610 fJ/step.

A high-performance fourth-order CT-SDM with pseudo-differential inverter-base amplifiers is introduced in (BREEMS *et al.*, 2016). These amplifiers have three stages with output common-mode feedback circuitry acting at the input common-mode voltage, as

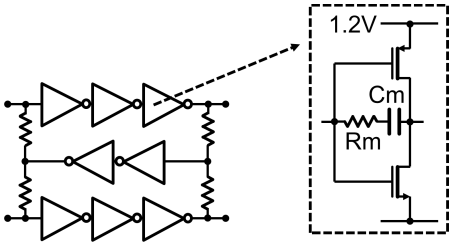
Figure 27 – Differential inverter-based amplifier with PVT compensation.



Source: (ISMAIL; MOSTAFA, 2016)

shown in Figure 28. A resistive network is used to measure the output common-mode level that is amplified and applied as the amplifier input common-mode voltage.

Figure 28 – Three-Stage Inverter-based amplifier.



Source: (BREEMS *et al.*, 2016)

The supply voltage of these inverters is adjusted to mitigate the effects of process and temperature variation. This CT-SDM uses only two amplifiers due to the use of single-amplifier resonators (CHAE *et al.*, 2014). The modulator operates with a 1.2-V supply voltage providing a peak SNDR of 77 dB for 25 MHz signal bandwidth with Fs of 2.2 GHz while achieving a FoM_W of 143 fJ/step.

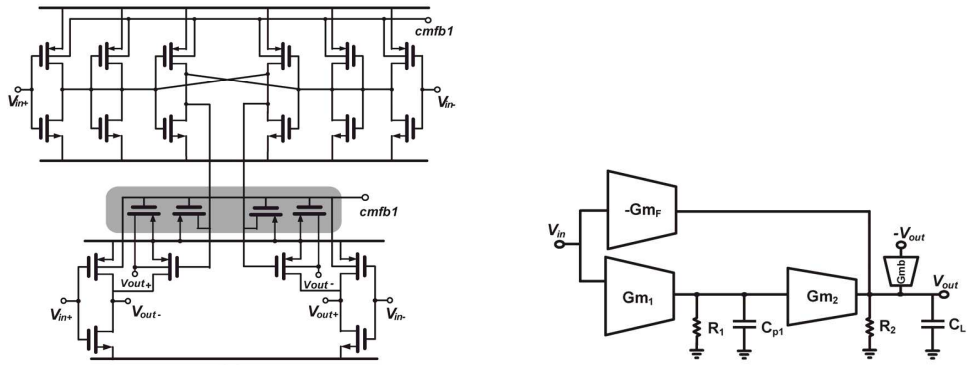
It is noteworthy that only the works of (ESSAWY; ISMAIL, 2014), (LV; LI, 2015) and (ISMAIL; MOSTAFA, 2016) presented CT-SDMs with inverter-based amplifiers for sub-1V operation until the middle of 2018. Their lack of silicon measurement results, to show the effectivity of these circuits, motivated the development of this thesis. Therefore, this work aims to extend these previous studies providing silicon implementation and measurement results of novel CT-SDMs with inverter-based amplifiers for sub-1V applications. At the end of the development of this thesis, two very interesting inverter-based CT-SDMs were published in the literature (LV *et al.*, 2018) (LV *et al.*, 2019).

By the end of 2018, a 0.4-V CT-SDM is proposed by (LV *et al.*, 2018) whereas the loop-filter is implemented with Gm-C proportional integrators using a modified Nauta transcondutor topology that includes a replica body-bias and the CMFB circuit introduced in (LV; LI, 2015). The main idea of this amplifier is to use a replica bias to control the supply voltage of the Nauta transcondutor. Also, the CMFB circuit controls the bulk bias of PMOS and NMOS transistor used in the modified Nauta cell. This modulator was

fabricated in a 90 nm CMOS process and achieves a peak SNDR of 74.40 dB and a DR of 78.50 dB within a 50 kHz bandwidth. This modulator operates at near-threshold supply voltages and achieves a FoM_W of 61.2 fJ/step and a FoM_S of 167 dB.

In (LV *et al.*, 2019) a fourth-order CT-SDM with active-RC integrators is implemented using two-stage feedforward compensated subthreshold amplifiers with the same CMFB introduced in (LV; LI, 2015). The amplifier schematic is illustrated in Figure 29. The first stage is a classic Nauta transconductor while the second and feedforward stages shares the same NMOS transistor. The output common-mode circuit acts at the body terminal of the PMOS transistors used in the amplifier. A negative output conductance is also generated to improve the DC gain by a cross-coupled connection of the bulk of some PMOS transistors. This CT-SDM achieved a peak SNDR of 68.50 dB for a 50-kHz bandwidth and a DR of 72.20 dB, leading to a Schreier FoM of 164.99 dB.

Figure 29 – Two-stage subthreshold amplifier.



(a) Amplifier schematic (b) Simplified small-signal model

Source: (LV *et al.*, 2019)

3.5 Considerations

This Chapter addressed the basic concepts regarding the design of inverter-based amplifiers. Also, a state-of-the-art review of SDMs with inverter-based amplifiers is presented. The main characteristics and drawbacks of the use of these amplifiers in CT-SDMs are given, providing an insight into the design details that should be taken into account.

4 SYSTEM-LEVEL DESIGN AND SIMULATIONS

This Chapter presents the system-level synthesis and analysis approach used in the design of the CT-SDMs introduced in this work. It includes an overview of architecture selection, loop filter implementation, and analysis of non-idealities. This Chapter focuses on the first CT-SDM prototype developed in this work. This modulator is suitable for IoT applications and has a signal bandwidth of 100 kHz. The target SNDR is set to 74 dB.

4.1 System-Level Design

The system-level design of CT-SDMs includes the NTF design and architecture selection for its implementation. The architecture selection is made regarding a low-voltage circuit implementation while the proper NTF is obtained to achieve the desired specifications.

4.1.1 Architecture Selection

The choice of proper CT-SDM loop filter architecture depends on numerous factors, such as input signal bandwidth, targeted SNDR, loop stability, linearity, etc. Among reported low-voltage (and also nominal-supply modulators) there are two main loop filter architectures: Cascade of Integrators in FeedBack (CIFB) and Cascade of Integrators in Feed Forward (CIFF). The CIFB architecture presents a flat STF and does not suffer from the STF peaking effect present in CIFF architectures (PAVAN; SCHREIER; TEMES, 2017). However, the CIFB architecture requires a higher number of feedback DACs: an Lth order CIFB modulator needs L feedback DACs while the CIFF loop-filter requires only one feedback DAC. In addition, the CIFB topology has a high input signal component at the integrators output, leading to the increase of integrators output swing when compared to the CIFF topology (DE LA ROSA; DEL RIO, 2013).

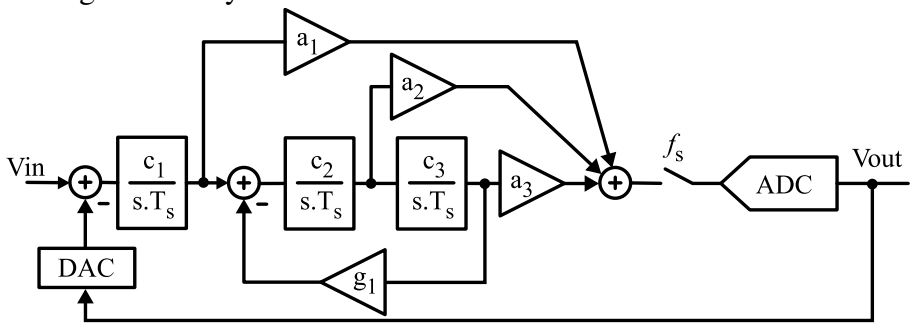
For low voltage applications, the loop filter integrators should present reduced output swing to minimize linearity issues. A good approach is to implement the modulator with unity STF since only the quantization noise is processed by the loop filter (SILVA *et al.*, 2001). However, the modulator misses its inherent anti-alias filter property since the input

signal is fed directly to the quantizer input (JESPERS, 2001) (DE LA ROSA; DEL RIO, 2013).

The CIFF topology was chosen in this work to provide AAF capability, and the coefficients scaling was carefully performed to provide integrators differential output swing limited to $\pm$100 mV for a 0.6-V power supply. Thus, the slew-rate, GBW and linearity requirements on the amplifiers is reduced due to the modulator smaller internal signal swings. In addition, it has been chosen to employ a single-bit quantizer due to its intrinsic linear behavior and power-efficiency since it is composed of a single comparator and does not affect the design complexity of the feedback DAC.

In order to achieve the design requirements, and to obtain a safety factor, a third-order loop filter with an OSR of 50 was used, leading to a 10-MHz sampling frequency. Then, the chosen modulator architecture is a traditional single-loop, single-bit, third-order CIFF one. It is known that SDMs of order equal to or greater than three are conditionally stable (SCHREIER; TEMES, 2005). Thus, the modulator is designed to maintain stability for a wide range of input signals whose maximum amplitude limits are close to the modulator reference voltage. In order to further increase the modulator SQNR, a local feedback path from the third integrator output to the second integrator input was used to form a resonator (SCHREIER; TEMES, 2005). This resonator generates optimized zeros in the NTF, reducing the in-band quantization noise. The coefficient g1 sets the location of the optimized zeros. The 3rd-order CT-SDM system-level architecture is shown in Figure 30.

Figure 30 – System-level architecture of the 3rd-order CT-SDM.



Source: The author

4.1.2 Continuous-Time Loop-Filter Design

The design of the CT loop filter was performed with the DT-to-CT conversion to speed-up the system-level design procedure. Initially, a DT-SDM that achieves the required performance is designed and simulated in discrete-time domain. Then, the DT loop filter is converted to its CT counterpart. The CT coefficients are calculated based on the DT ones and on the feedback DAC waveform. The DT-to-CT conversion was done using the Impulse-Invariant Transformation (IIT) (ORTMANNS; GERFERS, 2006).

4.1.2.1 Discrete-Time Loop-Filter Design

The discrete-time modulator coefficients c_1, c_2, c_3, a_1, a_2 and a_3 were calculated to provide a third-order optimal NTF with out-of-band gain (OBG) of 1.5 for an OSR equal to 50, as presented in Equation 29. In this design stage, the optimized zeros were not taken into account.

$$NTF(z) = \frac{(z-1)^3}{(z-0.6694)(z^2-1.531z+0.6639)} \tag{29}$$

This NTF was obtained with the *synthesizeNTF* Matlab function available in the well-known Delta-Sigma Toolbox (SCHREIER, 2016). The coefficient g_1 was defined to set the optimum zeros location and to achieve the highest SNDR. It occurs when the zeros location is at 0, $\pm\sqrt{3/5}$ times the signal bandwidth, i.e the optimized zeros are located at the frequency of 0 and $\pm$77.46 kHz in this design, providing and SQNR improvement of 8 dB (SCHREIER; TEMES, 2005). Thus, the complete set of discrete-time coefficients without scaling are given by: [c_1, c_2, c_3, a_1, a_2, a_3, g_1] = [1, 1, 1, 0.8, 0.3, 0.056, 0.0022].

4.1.2.2 DT-to-CT Conversion

Different DAC transfer functions could be used to synthesize the CT loop filter that matches the noise-shaping behavior of its DT counterpart previously designed. The main DAC transfer functions used in low-voltage CT-SDMs are: Return-to-Zero (RZ) and its enhanced version Return-to-Open (RTO) (PUN; CHATTERJEE; KINGET, 2007), Non-return-to-Zero (NRZ) (ZHANG *et al.*, 2011) and Switched-Capacitor Resistor (SCR) (CHEN; PUN; KINGET, 2011).

The output signal of NRZ DACs is suitable to data-dependent transients that could generate inter-symbol interference (ISI) jeopardizing the modulator linearity. Despite RZ and RTO DACs being used to avoid inter-symbol interference (ISI), they still are more sensitive to noise-floor increase regarding jitter effects (CHERRY; SNELGROVE, 1999a). Also, RZ and RTO DACs require first integrator amplifiers with higher GBW and slew-rate when compared to NRZ DACs. Another solution to reduce jitter-related effects is to use an SCR DAC that provides an exponential DAC output and is less sensitive to clock jitter when compared to an NRZ DAC (ORTMANNS; GERFERS; MANOLI, 2005). However, it will increase the slew-rate and GBW specifications of the first integrator amplifier and also could degrade the anti-aliasing property of CT-SDMs (PAVAN, 2011b). RZ, RTO and SCR DACs could be designed to operate in half clock period only. Thus, they are less tolerant to ELD effects.

In this work, the NRZ DAC waveform allied to an ELD compensation strategy, as shown later on, is chosen providing a power-efficient solution. The CT-SDM coefficients obtained after the DT-to-CT conversion are: [c_1, c_2, c_3, a_1, a_2, a_3, g_1] = [1, 1, 1, 0.668, 0.244, 0.056, 0.00236].

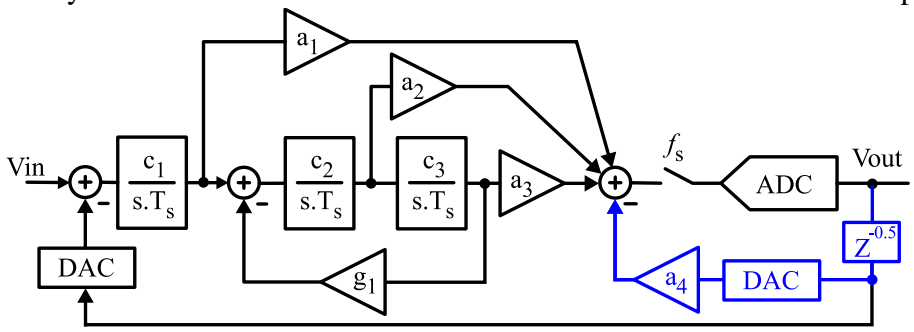
4.1.3 ELD Compensation

To provide stability against excess loop delay and to eliminate distortion effects due to quantizer metastability, the ELD compensation technique presented in (PAVAN, 2008) is adopted in this work.

This technique consists in the addition of a direct feedback path around the quantizer (known as "*fast path*") followed by the recalculation of the modulator coefficients. This compensation must be made for a specific time delay, usually half clock period. In this work, a fixed delay compensation of $0.5Ts$ ($\tau = 0.5$) is chosen. With this strategy the quantizer is synchronized with the rising edge of the clock signal while the DAC control is synchronized with the falling edge.

Figure 31 presents the system-level architecture of the 3rd-order CT-SDM designed in this work, including the ELD compensation.

Figure 31 – System-level architecture of the 3rd-order CT-SDM with ELD compensation.



Source: The author

The modulator coefficients are recalculated from the previous ones (a'_x) according to Equation 30.

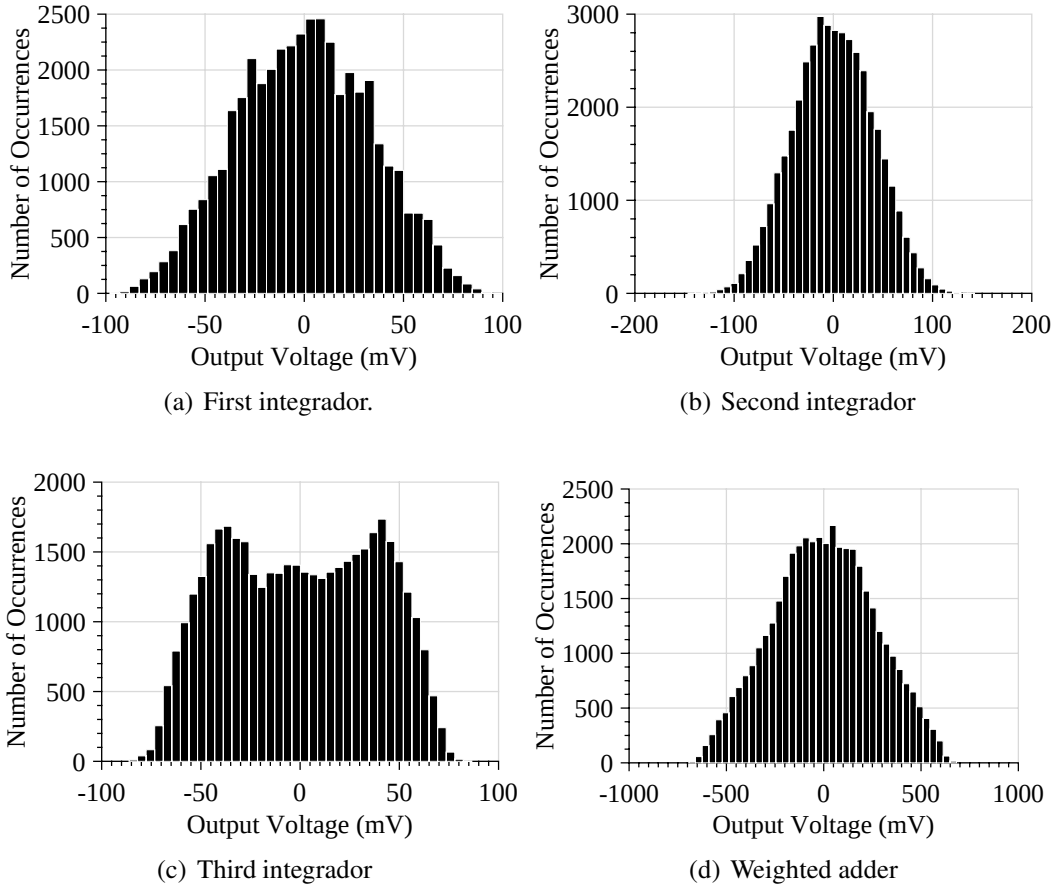
$$
\begin{aligned}
a_1 &= a'_1 + a'_2\tau + a'_3\frac{\tau^2}{2} \\
a_2 &= a'_2 + a'_3\tau \\
a_3 &= a'_3 \\
a_4 &= a'_1\tau + a'_2\frac{\tau^2}{2} + a'_3\frac{\tau^3}{6}
\end{aligned}
\tag{30}
$$

Once the new loop-filter coefficients were calculated, they were scaled to reduce the integrators output swing. It avoids nonlinearities in the modulator circuit-level implementation and downgrades the amplifiers GBW and slew-rate requirements. After scaling, the new loop filter coefficients are: [c_1, c_2, c_3, a_1, a_2, a_3, a_4, g_1] = [0.1, 1, 0.1, 7.97, 2.72, 5.6, 0.3657, 0.0236].

Figure 32 depicts the histogram of the loop-filter integrators and adder output swings for an input signal with amplitude of 300 mV (-6.02 dBFS). One can observe that the first integrator output swing is limited to $\pm$ 100 mV. This is essential to minimize distortions

originated by the first integrator. The output swing of the adder circuit does not need to be scaled down since it is connected directly to the quantizer input.

Figure 32 – Histogram of the loop-filter integrators and weighted adder output swings.



(a) First integrador. (b) Second integrador

(c) Third integrador (d) Weighted adder

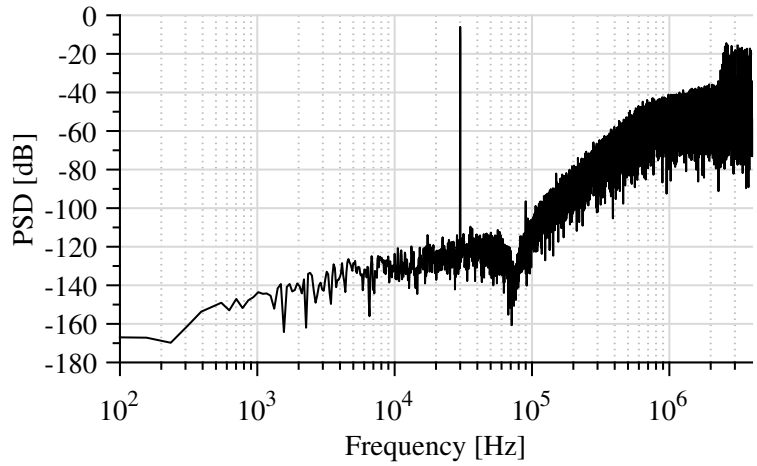
Source: The author

4.1.4 System-Level Simulations

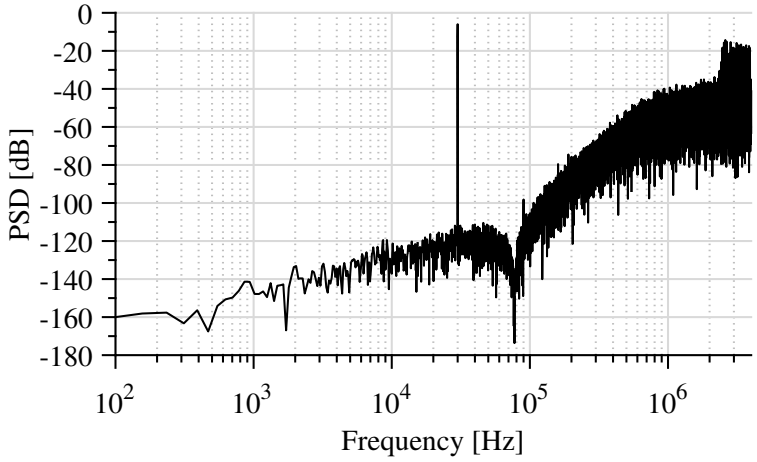
System-level simulations of the proposed CT-SDM and its DT counterpart are provided in this subsection to verify the effectiveness of the DT-to-CT conversion. This simulations were performed in Matlab/Simulink environment including a 30-kHz input signal. The modulators output Power Spectrum Density (PSD) for an input signal with amplitude of -6.02 dBFS, calculated with 128k points, are shown in Figure 33. The SQNR achieved by the CT-SDM and its DT counterpart are 82.97 dB and 83.03 dB, respectively.

The resulting NTF of the proposed CT-SDM is also evaluated. Figure 34 depicts the NTF behavior on dB scale. It is possible to verify that the achieved OBG is 1.5 (3.5 dB), as expected.

Figure 33 – Simulated PSD for a -6.02-dBFS 30-kHz input signal: DT versus CT.



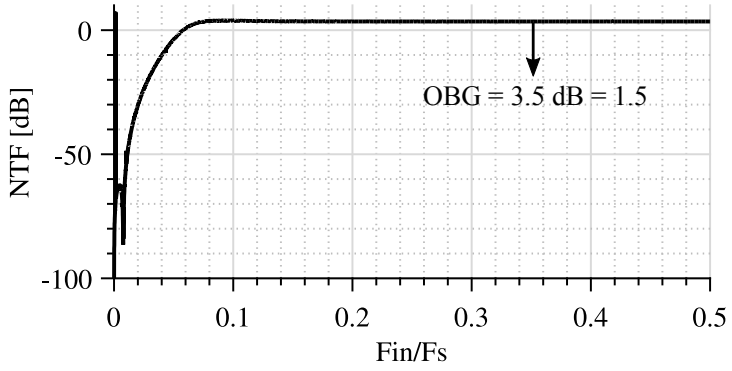
(a) DT-SDM.



(b) CT-SDM.

Source: The author

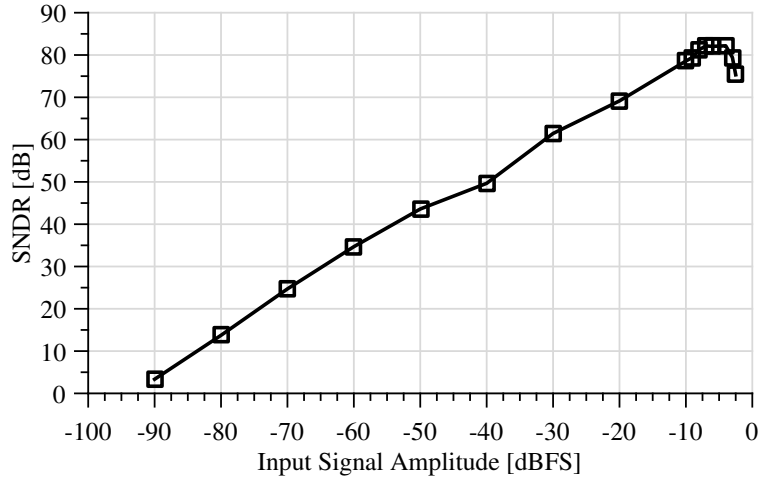
Figure 34 – Simulated NTF of the proposed modulator.



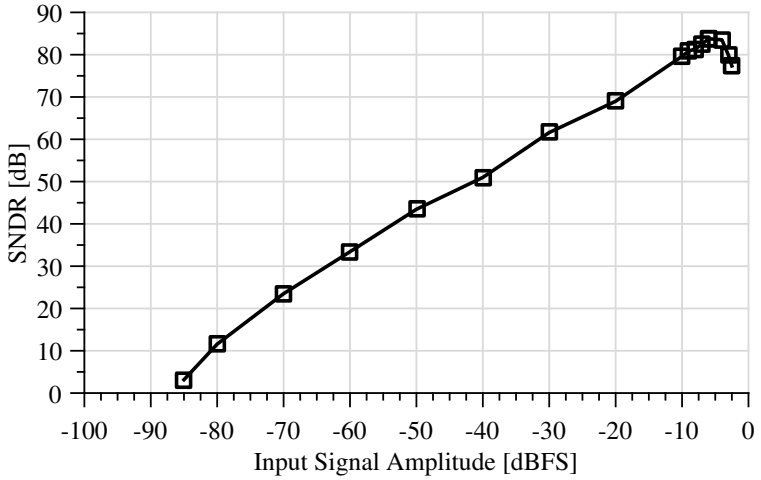
Source: The author

Figure 35 shows the measured SNDR as a function of the 30-kHz input signal amplitude. The DR of the CT-SDM is approximately 88 dB, presenting a slight reduction in comparison to its DT counterpart that presents a DR of 93.80 dB. This difference could be explained due to the time-step used in the transient simulation in Matlab.

Figure 35 – Simulated SNDR versus input signal amplitude (Fin=30 kHz): DT versus CT.



(a) DT-SDM.



(b) CT-SDM.

Source: The author

4.2 System-Level Simulations Including Non-Ideal Effects

System-level simulations were carried out to analyze the impact of non-idealities on the performance of designed modulator. These simulations evaluate the effects of the following non-idealities: clock jitter, ELD and amplifiers' finite DC gain, GBW and slew-rate. The modeling of those effects was performed using the modeling approach previously developed by the author (DE AGUIRRE, 2014) (DE AGUIRRE *et al.*, 2013). Initially, the effects of clock jitter and the modulator ELD were individually analyzed taking into account ideal integrators as follows.

4.2.1 Clock Jitter Effect

The clock jitter is a timing error that changes the width and position of the feedback DAC waveform. It is originated by time uncertainty in the clock signal and generates a statistical variation on the output waveform of the DAC. It is one of the main sources of

performance degradation in CT-SDMs (CHERRY; SNELGROVE, 1999a). The accuracy of traditional methods to simulate clock jitter effects in continuous-time simulations is dependent of the simulation time step. This type of simulation in the Matlab/Simulink environment should be done using a fixed simulation time step that is much smaller than the clock jitter effective value (RMS), which makes the simulation very slow.

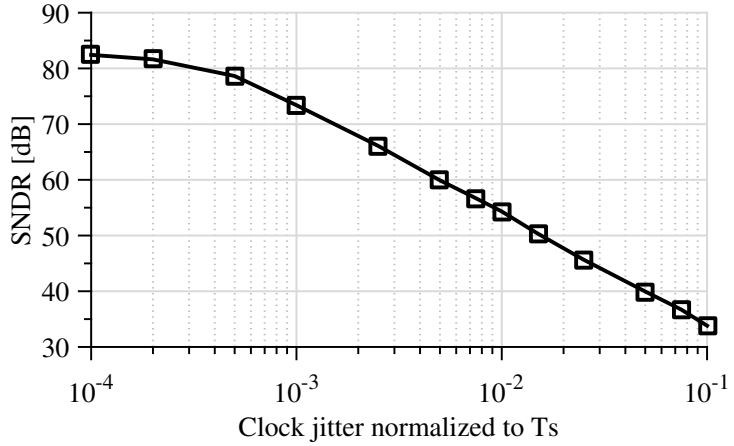
In this work, the clock jitter effect was simulated using the modeling approach introduced in (ASHRY; ABOUSHADY, 2009) to avoid timing-consuming simulations. The clock jitter effect is modeled as an additive noise at the input of the modulator whose amplitude is described in Equation 31.

$$J(t) = T_j \frac{d}{dt} DAC(t) \tag{31}$$

Where $J(t)$ is a random signal applied at the input of the modulator, $DAC(t)$ is the DAC output voltage and T_j is modeled as a Gaussian distribution with zero mean and standard deviation equal to the RMS jitter.

Figure 36 shows the relationship between the modulator SNDR and the clock jitter value, normalized to the clock period (0.1 µs). The impact of clock jitter on the modulator performance is significant, and from this simulation one can extract the requirements of clock signal used during the modulator testing. Based on the simulation results depicted in Figure 36, there is no SNDR degradation for clock jitter whose effective value is equal to or lower than 0.01% of the clock period (10 ps). These requirements are easily satisfied for the 10-MHz clock frequency.

Figure 36 – Simulated SNDR versus the clock jitter normalized to Ts.



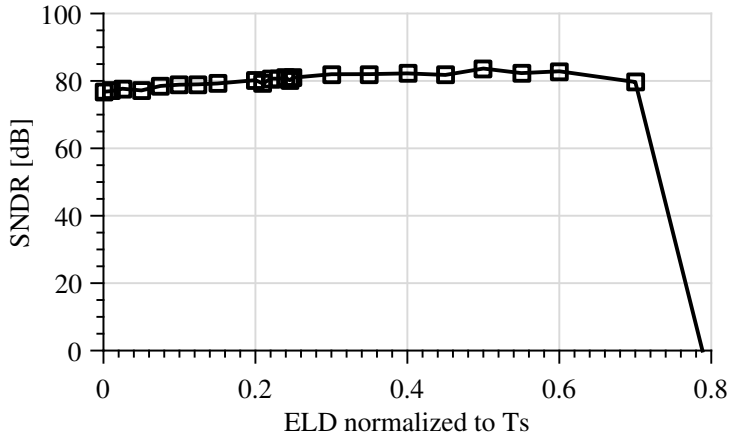
Source: The author

4.2.2 ELD Effect

Figure 37 depicts the modulator SNDR behavior against the ELD value. The modulator presents a stable behavior for ELD up to 70% of the clock period (T_s) due to the adopted ELD compensation strategy. In general, the effects of ELD up to 70% of T_s on

modulator SNDR is negligible. However, the quantizer should be designed to provide a conversion time lower than 50% of T_s to ensure a safe operation margin.

Figure 37 – Simulated SNDR versus ELD normalized to Ts.



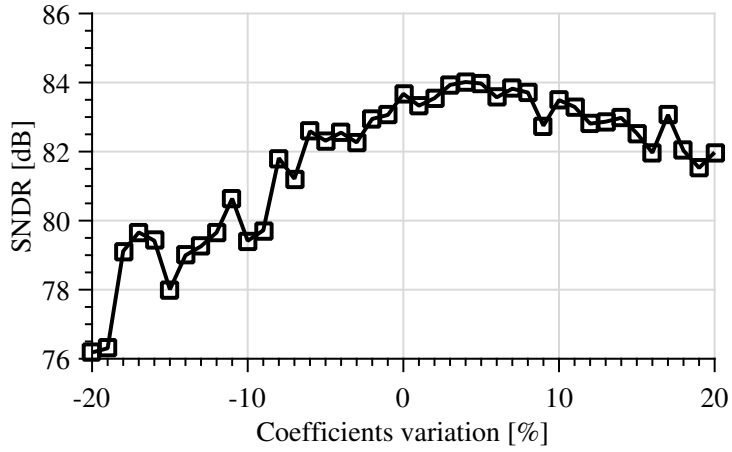
Source: The author

4.2.3 Coefficients Variation

The variation of the passive components values due to the circuit manufacturing process affects the value of the modulator coefficients. These variations can affect the modulator stability and performance. Therefore, it is necessary to evaluate the robustness of the modulator against the coefficients variation, and take it into account during the design stage of the integrators.

Initially, all the coefficients are varied by the same amount to emulate different process corners. Figure 38 shows modulator SNDR versus a coefficients variation in the range of $\pm$ 20%. It can be observed that the modulator is stable for process variations up to $\pm$ 20%. According to Figure 38, a more pronounced reduction of the modulator SNDR occurs when the value of the coefficients are simultaneously reduced below -10%.

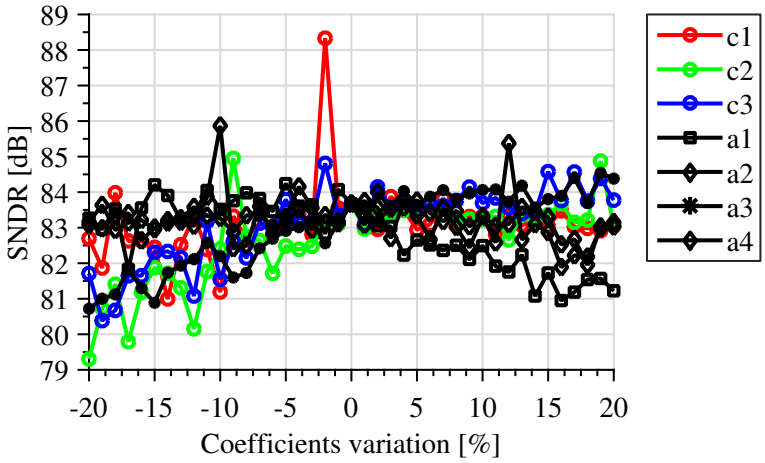
Figure 38 – SNDR versus coefficients variation: same variation for all coefficients.



Source: The author

Also, all coefficients were individually varied. Figure 39 depicts the effect of each coefficient variation in the modulator SNDR, that remains above 80 dB for variations of up to ± 15%.

Figure 39 – SNDR versus individual coefficient variation.

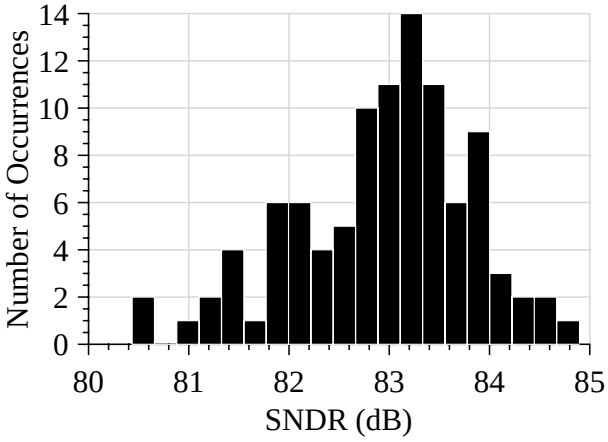


Source: The author

The circuit-level implementation of the feed forward coefficients will only be presented in the next Chapter. However, it is necessary to evaluate the effect of mismatch between the modulator feed-forward coefficients a_x on the SNDR.

System-level simulations including a random variation of ±10% for each of the four a_x coefficients were performed. Figure 40 shows the achieved modulator SNDR taking into account 100 simulation runs.

Figure 40 – Histogram of the modulator SNDR taking into account a random variation of feed forward coefficients a_x.



Source: The author

4.2.4 Non-Idealities of Loop-Filter Amplifiers

The modulator performance depends on the specifications of the loop filter amplifiers. The following analysis consider a classic circuit implementation with three active-RC integrators and one inverter summing amplifier. The effect of each amplifier non-ideality on the modulator SNDR is individually analyzed while considering other non-idealities with optimal values: GBW = 10×Fs, DC gain of 80 dB and slew-rate of 250 V/μs.

These analysis take into account the one pole model for all amplifiers. The amplifier one pole model is given by:

$$A(s) = \frac{Ao}{1 + s\frac{Ao}{\omega_u}} \tag{32}$$

where A_o is the amplifier DC gain and ω_u is the GBW. Based on this model it is possible to find the transfer function of the integrators, $I(s)$, described in Equation 33, where the RC constant is dependent on the modulator coefficients c_i and the sampling frequency.

$$I(s) = \frac{1}{s^2(\frac{RC}{\omega_u}) + s(\frac{1}{\omega_u} + \frac{RC}{A_o} + RC) + \frac{1}{A_o}} \tag{33}$$

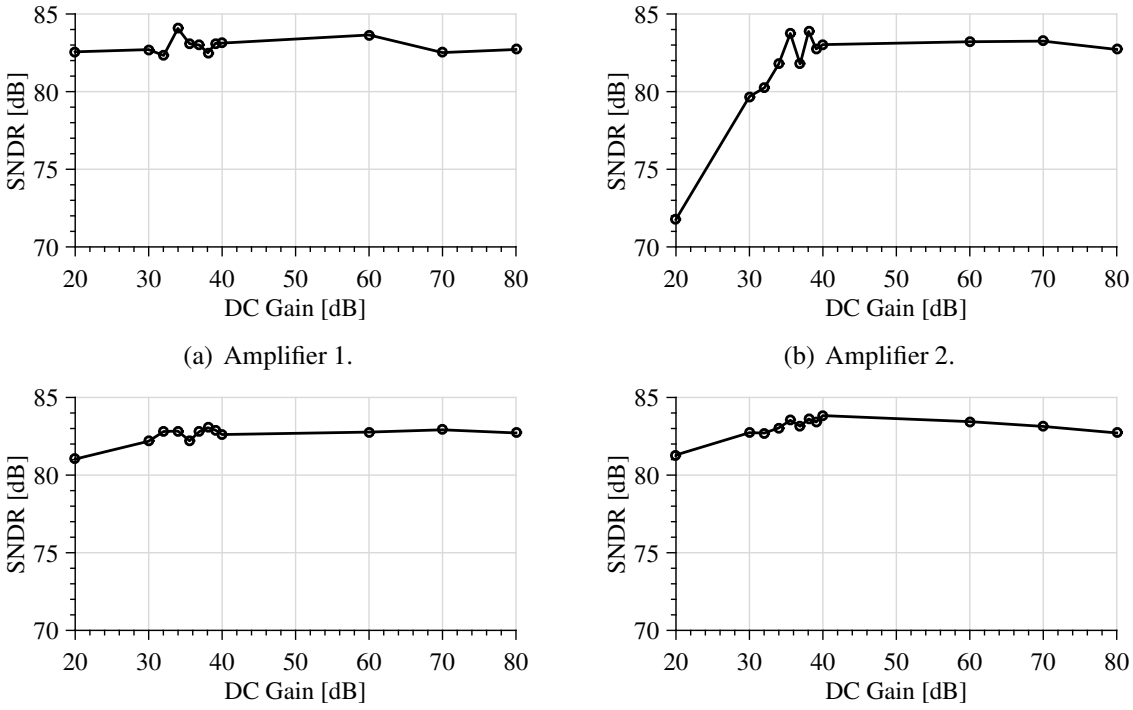
The adder model is performed by the ideal sum of the input signals whose gain is defined by an actual inverting amplifier. Thus, the transfer function of the adder, $Adder(s)$, is described in Equation 34. In this simulation a $Rf = 100$ kΩ and resistors Ri were calculated according to the coefficients g_1.

$$Adder(s) = \sum_{i=1}^{4} \frac{Rf}{s\left(\frac{Ri}{\omega_u} + \frac{Rf}{\omega_u}\right) + Ri + \frac{Ri+Rf}{A_o}} \tag{34}$$

The impact of the DC gain of the amplifiers on the SNDR of the modulator is shown in Figure 41. It is possible to observe that for gains greater than 40 dB there is practically no performance reduction. However, the second amplifier requires DC gains above 30 dB. This features is related to the use of a resonator in the modulator filter.

Regarding the GBW of the amplifiers it is possible to state that each amplifier has a distinct GBW requirement, as observed in Figure 42. The amplifiers of the first and second integrators require amplifiers with GBW equal to or greater than the sampling frequency while the amplifier of the third integrator can be designed with minimum GBW 10% of the sampling frequency. The inverter adder amplifier requires at least four times the sampling frequency, which results in high power consumption. This notion of GBW values avoids oversizing of the amplifiers, allowing a reduction in the power consumption of the modulator.

Figure 41 – Impact of the amplifiers' DC gain on the designed CT-SDM.



(a) Amplifier 1.

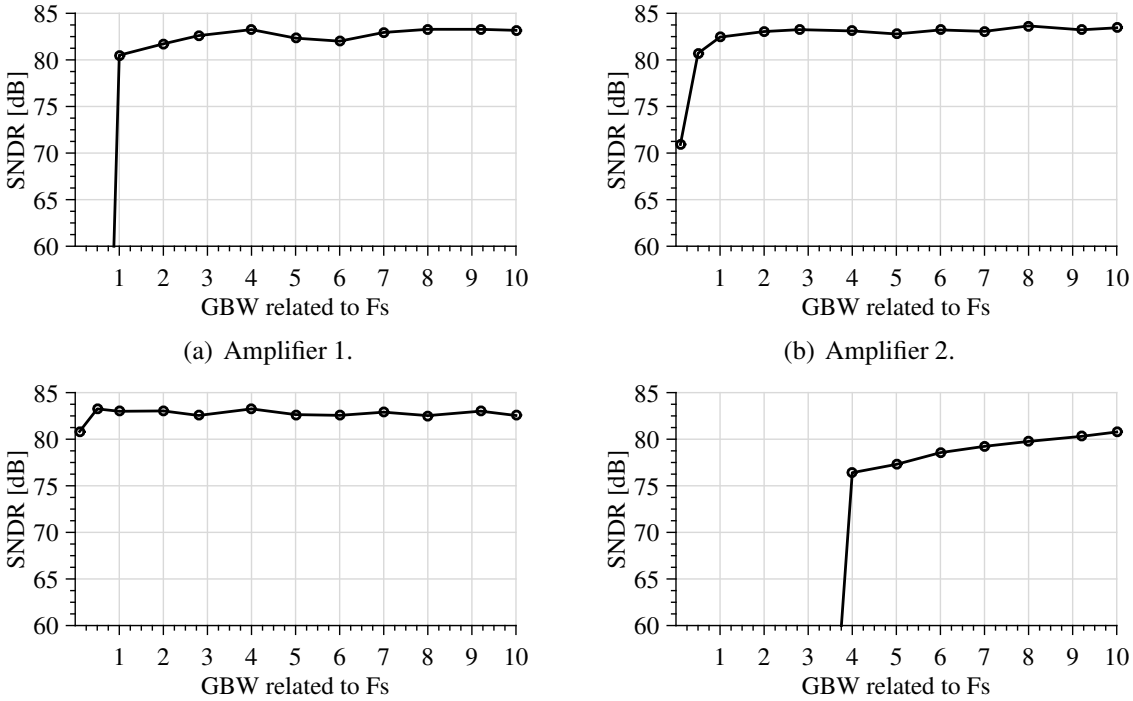
(b) Amplifier 2.

(c) Amplifier 3.

(d) Amplifier 4.

Source: The author

Figure 42 – Impact of the amplifiers' GBW on the designed CT-SDM



(a) Amplifier 1.

(b) Amplifier 2.

(c) Amplifier 3.

(d) Amplifier 4.

Source: The author

4.3 Discussions

This Chapter introduced the proposed CT-SDM architecture, including the loop-filter design and ELD compensation. System-level simulation results that evaluate the modulator performance are given. The main non-idealities present in CT-SDMs were taken into account, and their impact in the modulator performance was evidenced by system-level simulations. These analyses enable the correct sizing of the amplifiers that are used in the modulator loop filter to save power. Also, it is possible to verify the effect of coefficients spread and its impact on the modulator SNDR.

5 A LOW-VOLTAGE CONTINUOUS-TIME SIGMA-DELTA MODULATOR WITH SINGLE-AMPLIFIER BIQUAD

This Chapter presents the electrical implementation of the CT-SDM previously analyzed in system level. Initially, general definitions and details for the modulator electrical implementations are given. Then, the first inverter-based amplifier topology developed in this work is introduced and a 0.6-V transistor-level CT-SDM with three loop-filter amplifiers is presented and characterized by schematic-level simulations to demonstrate the possibility to use the proposed amplifier in the loop filter of low-voltage CT-SDMs with active-RC integrators. Later on, this Chapter describes the design and experimental measurement results of an improved 0.6-V power-efficient third-order CT-SDM with a single-amplifier resonator in the loop filter. This modulator was designed on the IBM CMOS 8RF-DM 130-nm CMOS process (MOSIS, 2017a). This process was chosen because it is suitable for the design of low-voltage and low-power integrated circuits, and also because it was available through the MOSIS multi-project wafer (MPW) program (MOSIS, 2017b).

5.1 General Definitions

The designed modulator uses the inverter-based pseudo-differential amplifier topology already introduced. The differential operation mode provides higher immunity to noise and common-mode disturbances from neighboring circuits and power supplies (RAZAVI, 1998), at the cost of increasing design complexity. Thus, the following considerations and explanations will be performed considering differential analog blocks.

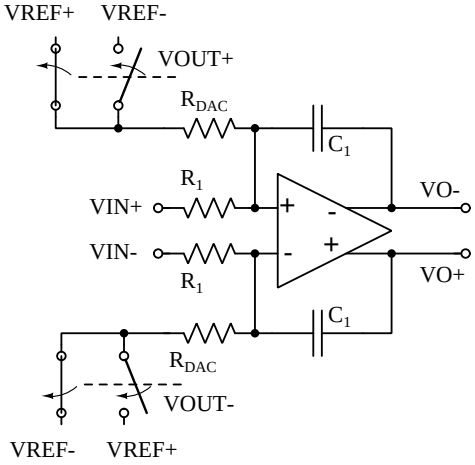
5.1.1 Implementation of the Loop-Filter Integrators

There are three main integrator topologies commonly used to design the loop filter of CT-SDMs: active-RC, Gm/C and MOSFET-C. Active-RC integrators provide higher linearity than other topologies due to the input resistor, and are chosen in this work. The loop-filter coefficients c_1, c_2 and c_3 are implemented by these integrators.

5.1.2 Definition of the DAC Topology

Single-bit NRZ DACs used in CT-SDMs with active-RC integrators are usually implemented by using reference voltages and resistors, or by using a current-steering DAC. This work uses a resistive DAC, composed of two resistors R_{DAC} connected at the input of the first integrator amplifier and two voltage references VREF+ and VREF-, as depicted in Figure 43. Resistors R_{DAC} are equal to the modulator input resistors, and the positive and negative voltage references are equal to VDD (0.6 V) and ground (0 V), respectively.

Figure 43 – Implementation of a 1-bit resistive DAC.

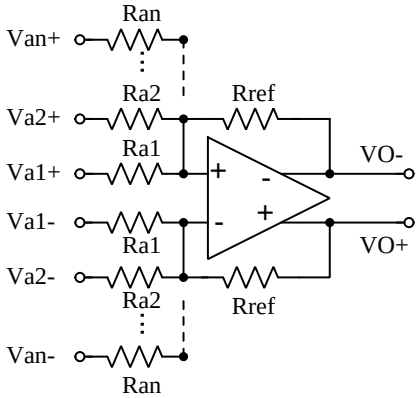


Source: The author

5.1.3 Electric Implementation of the Feed-Forward and Feedback Coefficients

Traditional CIFF SDM topologies use a power-hungry inverter summing amplifier in front of the quantizer to implement the feed-forward coefficients ax (RAZAVI, 1998), as shown in Figure 44.

Figure 44 – Implementation of the feed-forward coefficients with an inverter summing amplifier.



Source: The author

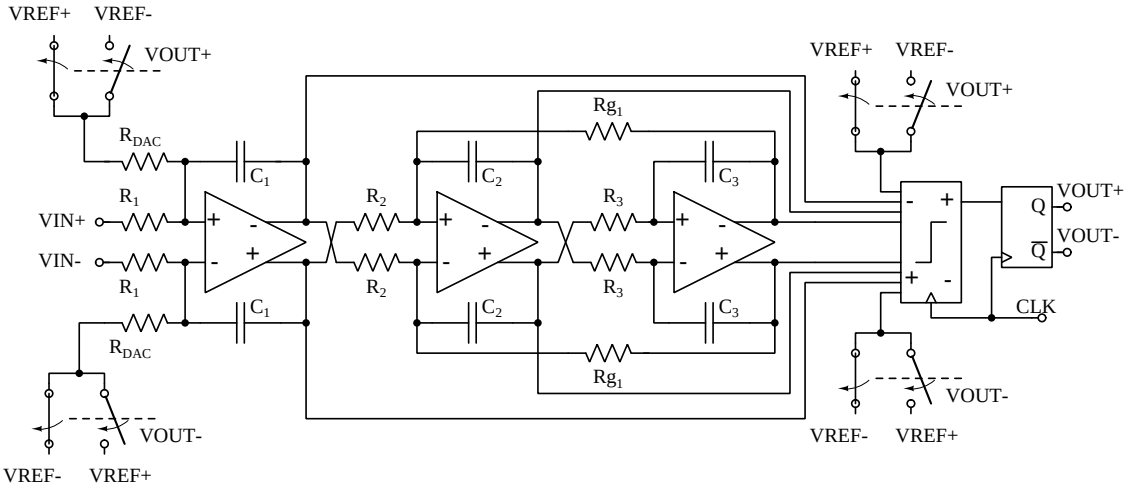
In this case, the coefficients are given by the relation between the feedback resistor Rref and the input resistors Rax: ax = Rref/Rax. This strategy requires amplifiers

with high GBW, increasing the modulator total power consumption (ORTMANNS; GERFERS, 2006).

In the last years, different strategies to implement the feed-forward coefficients avoiding the use of a power-hungry amplifier in front of the quantizer have been introduced. The use of capacitors to implement the feed-forward coefficients was proposed by (SCHIMPER *et al.*, 2004) while the use of passive resistor adders is adopted in (MATSUKAWA *et al.*, 2010). Both strategies reduce the loop-filter power consumption at the cost of loading the integrators and resonators of the loop filter. However, this work adopts the power-efficient structure presented in (ZHANG *et al.*, 2011) to implement the feed-forward coefficients. This power-efficient structure embeds the feed-forward coefficients and the sum operation in the comparator, reducing silicon area and power consumption, as explained later on in this Chapter.

On the other hand, the feedback coefficient g1 is implemented in a straightforward way by a feedback resistor Rg1 from the third integrator output to the input of the second integrator amplifier. The simplified schematic diagram of the proposed low-voltage CT-SDM is introduced in Figure 45 taking into account the definitions previously presented.

Figure 45 – Schematic diagram of the proposed CT-SDM.



Source: The author

5.2 Schematic-Level Implementation Details

This section gives the main electric details of the modulator schematic-level implementation. The supply voltage is set to 0.6 V and the input and output common-mode voltage of the analog circuits is set to 0.3 V. The sampling frequency is 10 MHz leading to an oversampling ratio of 50 for 100-kHz input signals, as already defined in Chapter 4.

In this implementation, the positive and negative voltage references are equal to the supply voltage: VREF+ = 0.6 V and VREF- = 0 V. The modulator voltage reference limits

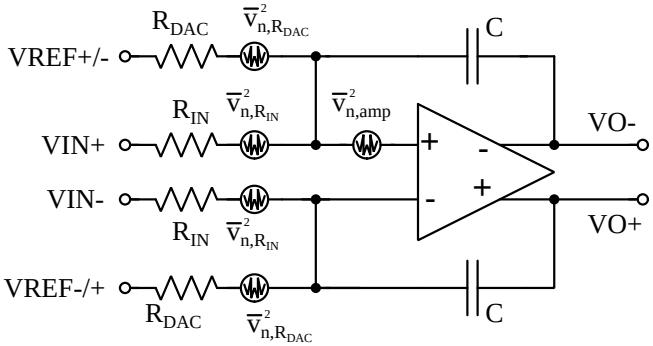
the maximum differential input signal at modulator input. In this case, the maximum SNDR is achieved for input signals amplitudes near to -6.02 dBFS (300 mV).

5.2.1 Input-Referred Noise at the Modulator Input

An important aspect regarding sigma-delta modulators design is the noise analysis to calculate the noise referred to the modulator input, which bases the sizing of the first integrator and the DAC resistors. In a CIFF architecture, the first integrator amplifier is the one that requires the largest GBW. The GBW of this amplifier must be minimized to reduce the modulator power consumption. Reducing the value of the integration capacitor achieves this goal. However, the integrator resistor should be increased to keep the same integrator coefficient, which causes an increase in the thermal noise present at the modulator input.

The noise present at modulator input does not suffer from the noise-shaping effect. Thus, any noise present at the modulator input will be present at the output, limiting the maximum SNDR that the modulator can achieve. Hence, it is necessary to analyze the total modulator input-referred noise to maximize the input resistors, thereby reducing the power consumption of the modulator. The main noise sources that affect the modulator performance are thermal noise of the input and DAC resistors, and amplifier input-referred noise. Figure 46 illustrates these noise sources.

Figure 46 – Noise sources present in active-RC integrators.



Source: The author

The total input-referred noise power density at the modulator input is calculated considering the noise contribution of each noise source depicted in Figure 46. This analysis regards uncorrelated noise sources in agreement with the study presented in (GERFERS; ORTMANNS; MANOLI, 2003).

The noise power density referred to the modulator input per bandwidth unit, $\bar{v}^2_{in-total}$, is expressed by Equation 35:

$$\bar{v}^2_{in-total} \approx 2 \times \left(\bar{v}^2_{R_{IN}} + \bar{v}^2_{DAC} \times \left(\frac{R_{IN}}{R_{DAC}} \right)^2 \right) + \bar{v}^2_{in-OTA} \times \left(1 + \frac{R_{IN}}{R_{DAC}} \right)^2 \qquad (35)$$

where $\bar{v}^2_{R_{IN}}$, $\bar{v}^2_{DAC}$ e $\bar{v}^2_{in-OTA}$ are the noise power densities of the input and DAC resistors, and the OTA input-referred noise density, respectively. In this work, $R_{IN} = R_{DAC}$ and one can simplify Equation 35, which results in Equation 36.

$$\bar{v}^2_{in-total} \approx 2 \times (\bar{v}^2_{R_{IN}} + \bar{v}^2_{DAC}) + 4 \times \bar{v}^2_{in-OTA} \; [V^2/Hz] \tag{36}$$

The noise power spectral density from a resistor is given by Equation 37:

$$\bar{v}^2_R = 4kTR \; [V^2/Hz] \tag{37}$$

where k = 1.3810^{-23} J/K is the Boltzmann constant, T is the temperature in Kelvin, and R is the resistor resistance. The value of $\bar{v}^2_{in-OTA}$ was already derived in Equation 25.

The input-referred noise power at the modulator input at a fixed bandwidth, P_{noise}, is obtained by integrating the noise power density from zero to the modulator signal bandwidth (BW) as expressed by Equation 38.

$$P_{noise} = \int_0^{BW} \bar{v}^2_{in-total} \; df \tag{38}$$

The maximum modulator input-referred noise allowed to achieve the desired SNDR should be known to enable the input resistor maximization. The same strategy used by the author in (DE AGUIRRE, 2014) is adopted in this thesis. It assumes that the three previously mentioned noise sources have the same weight in defining the modulator input-referred noise.

The calculation of R considers a target peak SNDR of 74 dB (12 bits). The reference voltage is 0.6 V, the modulator SQNR is 86 dB, and the peak SNDR occurs for input signals with an amplitude near to -6.02 dBFS. The total allowed in-band RMS noise is 42.33 µV. In the employed methodology, the performed calculations consider uncorrelated noise sources with the same weight. Thus, each input and DAC resistors contribute with an RMS noise of 14.96 µV. Thus, the calculated values for the first integrator and DAC input resistors are 134.92 kΩ. However, they are set to 125 kΩ to provide a safe margin.

5.2.2 Passive Components Calculation

The active-RC integrator passive components are calculated to accurately implement the loop-filter integrator coefficients. The integrator passive components are given by Equation 39:

$$a_k \times Fs = \frac{1}{R_k \times C_k} \tag{39}$$

where a_k are the integrators coefficients, Fs is the sampling frequency, R_k and C_k are the integrator resistors and capacitors, respectively. Thus, the more relaxed the noise specifications at the first integrator input, the larger the first integrator resistors and the smaller

the capacitors for implementing the same coefficient, reducing the modulator power consumption. Table 1 presents the calculated active-RC passive components of each loop-filter integrator.

Table 1 – Integrators resistor and capacitor values.

	Coefficient C_k	Resistor R_k (kΩ)	Capacitor C_k(pF)
Integrator_1	0.1	125	8.0
Integrator_2	1.0	100	1.0
Integrator_3	0.1	500	2.0

The g1 feedback coefficient is given by the relation between Rg1 and the second integrator input resistor R_2. Hence, the feedback resistor Rg_1 value is 4.24 MΩ.

5.2.2.1 Resistors and Capacitors Type Definition

The 130-nm CMOS process used to design the modulator provides eight different resistor types. The modulator loop filter is fully-differential. Thus, the resistors absolute value should present low variation due to the fabrication process, and resistors matching is also highly desired. Therefore, the loop-filter uses precision polysilicon resistors with a sheet resistance of $228\Omega/\square$ and a precision of $\pm 8\%$ (MOSIS, 2017a).

The process design kit (PDK) supported in the MOSIS multi-project wafer (MPW) allows the use of metal-insulator-metal (MiM) and dual-MiM capacitors. This work uses dual-MiM capacitors since they are more area-efficient than MiM capacitors. The used dual-MiM capacitors have a capacitance per area of 4.1 ± 0.41 fF/μm^2 and a temperature coefficient of 21 ppm/°C.

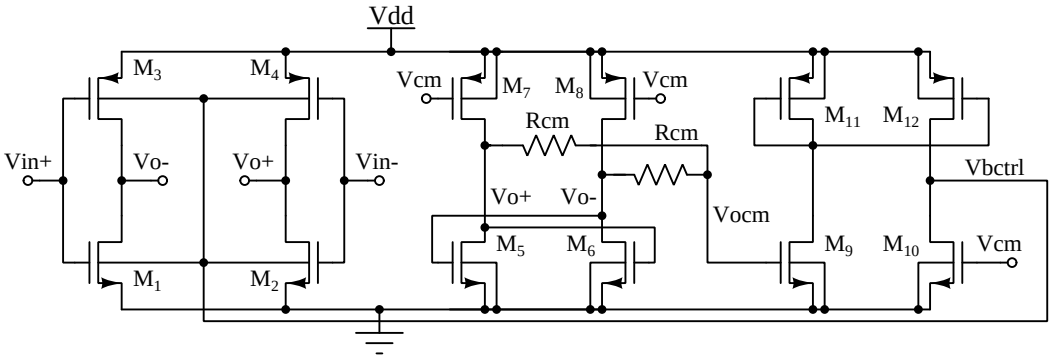
5.3 Proposed Inverter-Based Amplifier with Body Bias and DC Gain Enhancement

To improve power efficiency and operate at low supply voltages, we focused in the exploration of single-stage pseudo-differential amplifiers with a continuous-time CMFB. Based on the previously reported data in Chapter 3, the use of techniques to bias the bulk terminal of the inverter transistors is adopted. In this thesis, we come up with two inverter-based amplifiers topologies. The first one is explored hereafter.

Figure 47 introduces the schematic of the amplifier used in the design of first CT-SDM of this thesis. It is composed of two CMOS inverters comprising the main amplifier (transistors M_{1-4}), a CMFB network that consists of two resistors (R_{CM}) for output common-mode voltage sensing and an error amplifier composed of transistors M_{9-12}.

This circuit is designed with standard PMOS transistors and triple-well NMOS transistors. The body voltage of both PMOS and NMOS transistors are equal and controlled

Figure 47 – Pseudo-differential inverter-based amplifier.



Source: The author

by the CMFB loop for PVT compensation. According to (VIERU; GHINEA, 2011), this bias approach achieves better trip-point control. Thus, in a pseudo-differential inverter-based amplifier, it provides a stable common-mode output voltage against PVT variations. This bulk-bias approach reduces the bulk voltage amplitude variation when compared to a similar control applied only at the bulk of PMOS or NMOS transistors as in (LV *et al.*, 2019). This strategy is inspired by the amplifiers presented in (ISMAIL; MOSTAFA, 2016) and (LV; LI, 2015). However, instead of adding and control current sources in parallel with the transistors of the inverter, we control the bulk voltage of these transistors.

Also, a cross-coupled pair composed of transistors M_5 and M_6 is connected to the main amplifier output for gain enhancement purposes. The negative transconductance cell (M_{5-8}) produces a negative resistance at the amplifier output and is determined to cancel the output common-mode sensing resistors R_{CM} and the resistive amplifier output load R_L, typical in CT-SDMs implemented with active-RC integrators.

The amplifier was designed to operate in moderate inversion. The supply voltage is defined to be around $V_{TN} + V_{TP} + 200$ mV. Then, the amplifier supply voltage is set to 0.60 V and the input and output common-mode voltages are designed to be equal to VDD/2. The transistor sizing should be optimized to also provide a bulk control voltage (Vbctrl) equal to VDD/2 for the transistors M_{1-4} at nominal conditions, i.e, typical corner (TT, 25 °C).

The probability of latch-ups due to the forward bias applied across source-bulk junctions is minimized since the circuit is designed to operate at 0.6 V.

The amplifier DC gain is calculated by Equation (40).

$$\mathrm{Av} = \frac{\mathrm{gm}_1 + \mathrm{gm}_3}{\mathrm{gds}_1 + \mathrm{gds}_3 + \frac{1}{\mathrm{R}_{\mathrm{cm}}} + \frac{1}{\mathrm{R}_{\mathrm{L}}} + \mathrm{gds}_6 + \mathrm{gds}_8 - \mathrm{gm}_5} \tag{40}$$

The amplifier dominant pole frequency, Wp1, is given by Equation 41.

$$\mathrm{Wp1} = \frac{\mathrm{gds}_{\mathrm{P}} + \mathrm{gds}_{\mathrm{N}} + \frac{1}{\mathrm{R}_{\mathrm{CM}}} + \frac{1}{\mathrm{R}_{\mathrm{L}}} - \mathrm{gm}_5 + \mathrm{gds}_6 + \mathrm{gds}_8}{\mathrm{Co}} \tag{41}$$

Wp1 depends on the total equivalent capacitance load connected at the amplifier output node, Co, that is calculated according to Equation 42.

$$Co \approx C_L + Cdg_1 + Cdb_1 + Cds_1 + Cdg_3 + Cdb_3 + Cds_3 + Cgs_5 \quad (42)$$

Where C_L is the capacitive load at the amplifier output, usually the active-RC integrator capacitor.

5.3.1 Simulation Results

The amplifier topology was validated in a 130-nm CMOS process and the simulation results provided in this subsection take into account a supply voltage of 0.6 V (50% lower than the standard core supply) and an output load composed of a resistive load of 500kΩ and $C_L = 8$ pF. The circuit sizing is performed to achieve a nominal GBW higher than 12 MHz and a DC gain near 40 dB. Thus, the inverters were biased with a current of 30 µA and the negative transconductance cell was carefully designed to provide reliable operation across PVT.

Table 2 presents the transistors sizing. The transistors length is set to 1.00 µm in order to provide a good trade-off between intrinsic gain and short channel effects. The resistors R_{CM} are equal to 250 kΩ.

Table 2 – Transistors size of the proposed OTA.

Transistors	W/L (µm)
M_1 and M_2	$3 \times 1.55/1.0$
M_3 and M_4	$9 \times 4.50/1.0$
M_5 and M_6	$2 \times 1.04/4.0$
M_7 and M_8	$2 \times 11.89/4.0$
M_9 and M_{10}	$1 \times 1.94/10.0$
M_{11} and M_{12}	$1 \times 23/10.0$

Table 3 presents the amplifier simulation results at typical corner under voltage and temperature variations. The simulated Common Mode Rejection Ratio (CMRR) and the Power Supply Rejection Ratio (PSRR) decreases with the increase of temperature and are directly affected by the amplifier topology. Thus, both are lower than a differential input pair based amplifier with current tail. The bias current of the inverters also changes according temperature and voltage variations influencing the variation of the amplifier's power consumption. Nevertheless, the amplifier GBW is stable under temperature variations taking into account the same supply voltage. Regarding stability, the amplifier phase margin (PM) is approximately 90° since it is a single-stage amplifier. The proposed amplifier presents a limited CMRR, higher than 50 dB at the typical 0.6-V power supply. On the other hand, the PSRR is in agreement with other low-voltage amplifier topologies.

Table 3 – Amplifier Simulation Results.

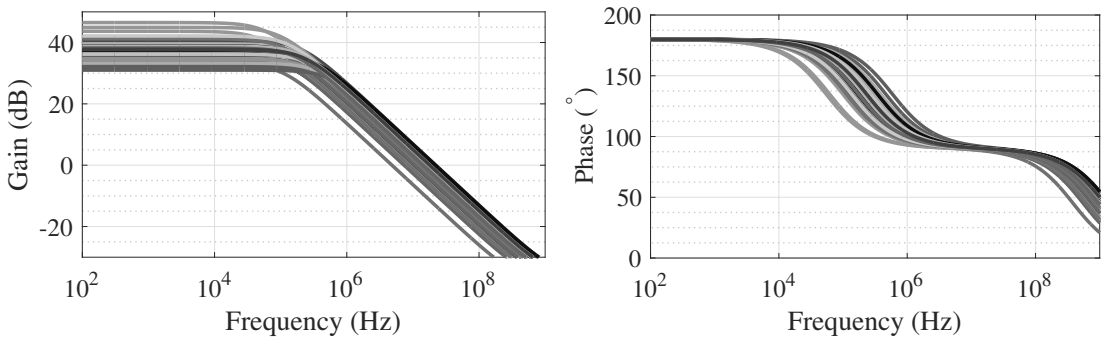
Supply (V)	0.54			0.60			0.66		
Temp. (° C)	-25	25	85	-25	25	85	-25	25	85
Av (dB)	38.14	37.73	34.55	41.60	38.41	34.16	42.14	37.80	33.31
GBW (MHz)	7.91	10.51	12.09	12.6	14.36	15.03	17.34	17.95	17.76
PM (degrees)	90.00	90.03	90.36	89.74	89.96	90.39	89.70	90.00	90.50
CMRR (dB)	52.41	51.21	46.58	55.79	51.59	45.61	53.89	50.43	43.63
PSRR+ (dB)	59.59	57.71	52.48	62.57	57.76	51.20	62.33	56.26	48.83
PSRR- (dB)	60.28	59.12	54.83	63.74	59.75	54.30	64.08	59.01	52.87
Power (µW)	12.11	21.74	32.76	26.52	40.13	54.00	50.32	67.06	82.83

The amplifier frequency response for a 500 kΩ||8 pF load across process (TT, FF, SS, FS, SF), voltage (0.54, 0.60, 0.66 V) and temperature ($-25°$C, 25°C, 85°C) corners is presented in Figure 48. The DC gain is higher than 31 dB in all corners while a GBW reduction higher than 50% is verified at the worst case corner.

A 1,000-runs Monte Carlo (MC) simulation including process and mismatch variations under nominal conditions (T = 25°C and VDD = 0.6 V) was carried out to examine the robustness of the proposed amplifier. The MC simulation results are shown in Figure 49. The amplifier average DC gain is 36.68 dB with a standard deviation (σ) of 2.17 dB. Values of DC gain below 30 dB are evidenced due to the variation of the negative conductance connected at the amplifier output. The average GBW is 14.36 MHz with $\sigma = 1.42$ MHz. The output common-mode voltage remains set around VDD/2 and the amplifier input offset is kept lower than ± 5 mV.

It is possible to avoid the need of a triple-well CMOS process by applying the Vbctrl control signal only at the PMOS transistors bulk terminal, as demonstrated in (LV; LI, 2015), at the cost of reduced robustness against PVT variations and higher swing of the Vbctrl signal.

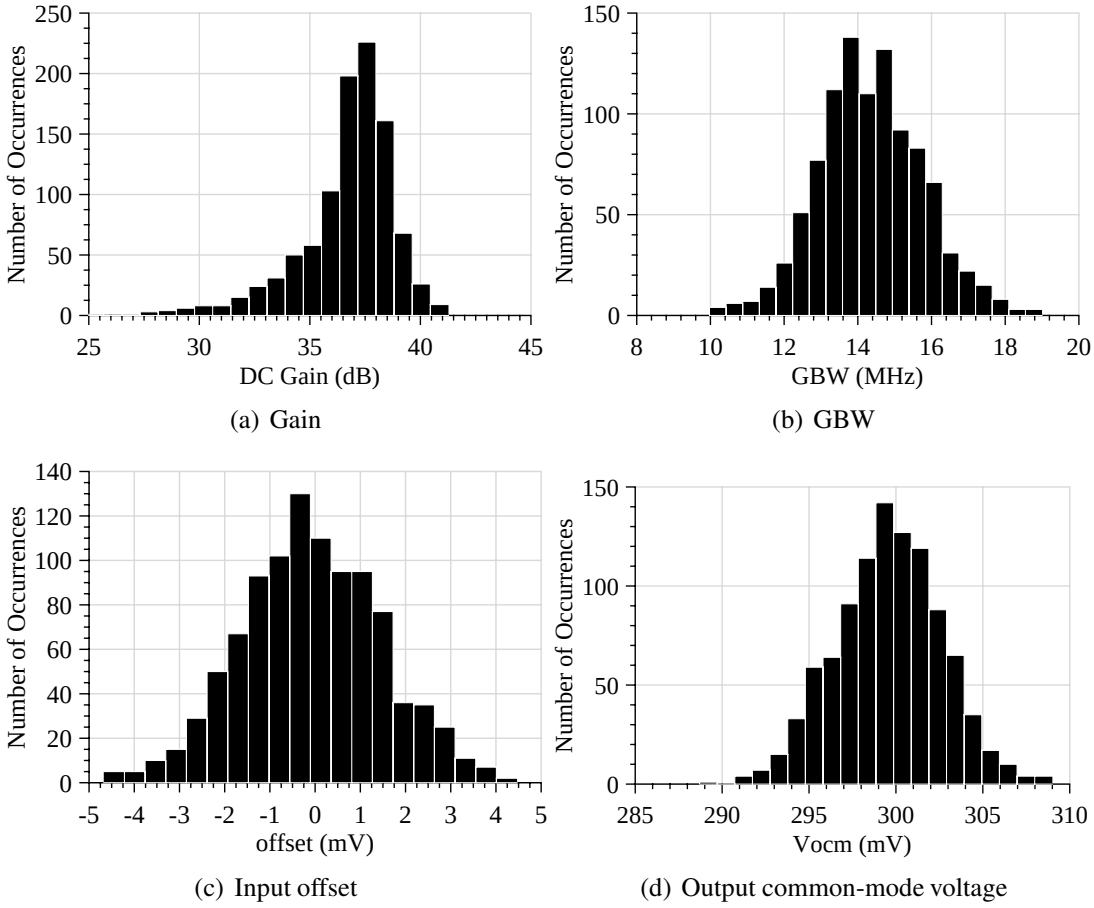
Figure 48 – AC response of the amplifier over PVT corners.



(a) Gain (b) Phase Margin

Source: The author

Figure 49 – Monte Carlo Simulation Results at VDD=0.6 V and T=25°C.



(a) Gain (b) GBW

(c) Input offset (d) Output common-mode voltage

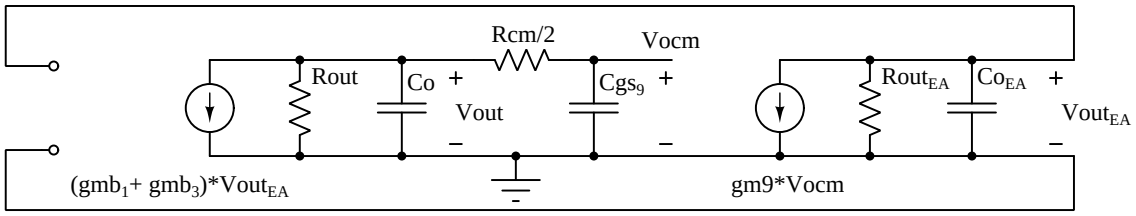
Source: The author

5.3.2 Considerations for Amplifier Stability and Robustness

The designed circuit has a negative conductance cell connected at the output nodes. It provides an increase of the DC gain at the cost of the increase in the DC gain variation for different process corners, especially when mismatch is taken into account (24.86-46.45 dB). A smaller variation of the amplifier gain is verified when no negative conductance cell is used. Thus, the impact of the negative resistance on the amplifier DC gain should be carefully analyzed.

Additionally, this circuit may present instability due to the CMFB loop for output common-mode control (HE; PUN; KINGET, 2009). The small-signal model of the amplifier CMFB loop is shown in Figure 50. There are 3 poles, which depending on their location may make the CMFB loop unstable. Based on extensive transient simulations it was found that the amplifier is stable when used inside a feedback network, and it is not necessary to perform the amplifier open loop compensation. Stability simulations were also performed with the stability analysis, stb, available in Cadence ADE-XL.

Figure 50 – CMFB loop small-signal model.



Source: The author

5.3.3 Alternatives to Enhance the Inverter-Based Amplifier DC Gain

The amplifier DC gain variation is originated by the variations in the negative conductance cell. Thus, alternative techniques to increase the amplifier output impedance without the need for a negative conductance cell were studied. A feasible approach is the use of the trapezoidal association of transistors (TAT) technique to design the inverters with increased output impedance. A parallel association of transistors to increase the gain of a Nauta transconductor (based on CMOS inverters) operating at 0.25 V was demonstrated by (BRAGA *et al.*, 2017). Despite the gain increase due to the increase of the transistors output impedance, the use of a rectangular association provides lower gain DC variation when mismatch is considered.

In (GIRARDI; BAMPI, 2004), the use of TAT to design inverter amplifiers is investigated, but no evaluation of the mismatch impact on the circuit performance is addressed. During this work, the use of TAT to design inverter-based amplifiers was explored. Preliminary results, based on MC simulations considering different process corners and mismatch, indicate that it is possible to achieve DC gains similar to those of the proposed amplifier topology. Also, the DC gain standard deviation is lower since no negative conductance cell connected at the amplifier output is required.

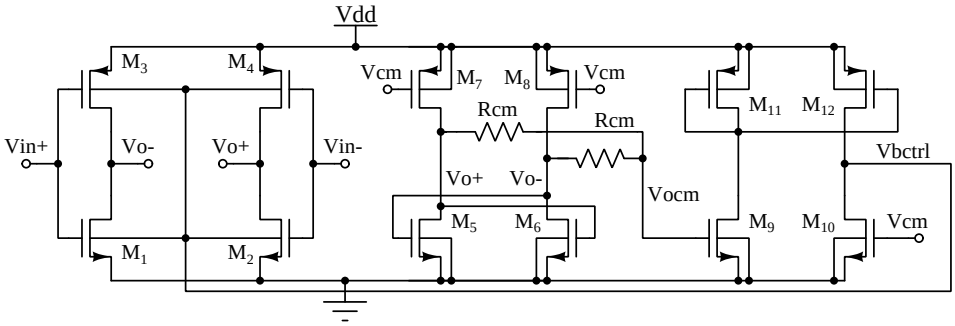
Since the project was carried out with an optimization tool that employs several parametric analyzes, and that no mathematical analysis to explain the results were performed until the present moment, these techniques will not be addressed in this thesis.

5.4 OTAs Design

The inverter-based OTA used in the modulator loop filter was already presented and is illustrated again in Figure 51. Each loop-filter integrator was individually scaled and optimized to reduce modulator power consumption. The first and second amplifiers use a negative conductance cell at the output to increase the DC gain. On the other hand, the third integrator amplifier does not require high gain. Therefore, the negative conductance cell at the amplifier output was removed.

To properly design each amplifier, one must determine its output load. The total amplifier output load is given by the parallel connection of a capacitance C_L and the subsequent

Figure 51 – First and second integrators amplifier topology.



Source: The author

integrator input resistance. The capacitance load C_L of an active-RC integrator is the sum of capacitances C_1 and C_{PAR}, where C_{PAR} is the equivalent parasitic capacitance at the amplifier output node and C_1 is the integrator capacitor. Table 4 presents the transistors size of the integrator OTAs.

Table 4 – Transistors size of the integrators OTAs.

Transistors	W/L (µm/µm)		
	OTA1	OTA 2	OTA 3
M_1 and M_2	$4 \times 1.55/1.0$	$3 \times 1.55/1.0$	$1 \times 1.26/2.0$
M_3 and M_4	$12 \times 4.50/1.0$	$9 \times 4.50/1.0$	$3 \times 4.05/2.0$
M_5 and M_6	$2 \times 1.04/4.0$	$2 \times 1.04/4.0$	$4 \times 1.04/4.0$
M_7 and M_8	$2 \times 11.89/4.0$	$2 \times 11.89/4.0$	$4 \times 11.89/4.0$
M_9 and M_{10}	$1\times 1.94/10.0$	$1\times 1.94/10.0$	N/A
M_{11} and M_{12}	$1\times 24.1/10.0$	$1\times 24.1/10.0$	N/A

5.4.1 Schematic-Level Simulation Results of the Loop-Filter Amplifiers

Table 5 presents the schematic-level simulation results of the designed OTAs at typical corner. The power consumption of each amplifier is scaled so that the first amplifier is the most energy-consuming while the third one is the lowest.

Table 5 – OTAs simulation results at typical corner.

Parameter	OTA 1	OTA 2	OTA 3
Load (F‖Ω)	8p‖100k	1p‖500k	2p
GBW(MHz)	19.38	93.99	9.43
DC gain (dB)	32.93	38.55	25.15
Phase Margin (degrees)	90.16	85.2	91.12
Total static current (µA)	87.73	66.2	19.78
Power (µW)	52.64	39.72	11.87
In-band Input-Referred Noise (µV)	8.86	-	-

Schematic-level simulations of the designed amplifiers for different process (TT, FF, SS, SF, and FS) and temperature (-25 °C, 25 °C and 85 °C) corners at the nominal supply voltage of 0.6 V were carried out to verify their robustness. Also, a Monte Carlo simulation with 1,000 runs was performed under nominal conditions, taking into account process variations and mismatch.

Tables 6, 7 and 8 summarizes the amplifiers main parameters achieved in these simulations. The amplifiers phase margin presents a low variation in all cases and is kept close to 90 degrees, as expected since the amplifiers are single-stage. The amplifiers GBW changes according to different process corners. The GBW of first OTA suffers a reduction of 40 % at the SS corner (T = -25 °C), and the maximum GBW of the amplifiers in corner analysis is approximate twice the minimum GBW. It occurs due to the variation of the amplifiers' bias current since there is no bias current control in this topology. The amplifiers DC gain also showed low variation. Thus, it can be stated that the designed amplifiers remain in operation even with a significant process and operating temperature variation.

Table 6 – OTA 1 main parameters: Monte Carlo and PVT corners simulation results.

Parameter	Monte Carlo		Corners	
	Average	Std. deviation	Minimum	Maximum
GBW(MHz)	19.45	1.992	11.69 (SS@-25°C)	24.71
DC gain (dB)	32.66	0.536	29.44 (FF@85°C)	35.17
Phase Margin (degrees)	90.2	0.096	89.85	90.77

Table 7 – OTA 2 main parameters: Monte Carlo and PVT corners simulation results.

Parameter	Monte Carlo		Corners	
	Average	Std. deviation	Minimum	Maximum
GBW(MHz)	93.43	9.461	57.11 (SS@-25°C)	119.65
DC gain (dB)	36.78	2.192	32.1 (FF@85°C)	46.6
Phase Margin (degrees)	85.41	0.315	84.72	85.88

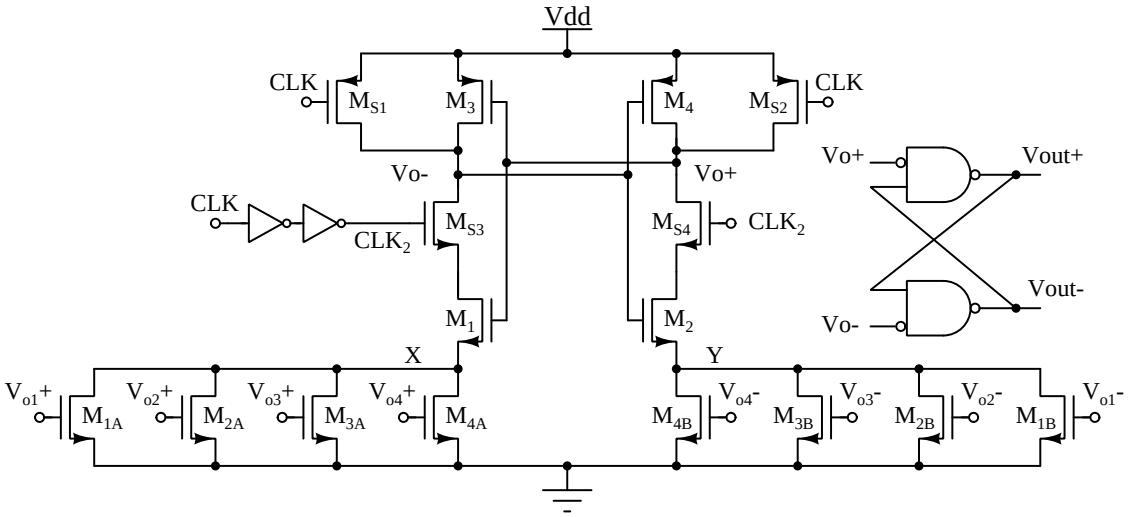
Table 8 – OTA 3 main parameters: Monte Carlo and PVT corners simulation results.

Parameter	Monte Carlo		Corners	
	Average	Std. deviation	Minimum	Maximum
GBW(MHz)	9.5	0.896	6.04 (SS@-25°C)	11.9
DC gain (dB)	25.1	0.365	23.15 (FF@85°C)	26.39
Phase Margin (degrees)	91.4	0.175	90.6	92.07

5.5 Feed-Forward Coefficients and Quantizer Design

The power-efficient multi-input weighted comparator introduced in (ZHANG *et al.*, 2011) is adopted in this thesis to implement the feed-forward coefficients. This single structure embeds the feed-forward coefficients a_x and the summing of these coefficients a_x into the comparator. This circuit is a dynamic latch, similar to the so-called strongARM latch (RAZAVI, 2015). Figure 52 depicts the single-bit quantizer schematic.

Figure 52 – Schematic of the single-bit quantizer.



Source: The author

Transistors M_{1A-4A} and M_{1B-4B} perform the differential signals sum operation and transistors M_1, M_2, M_3 and M_4 perform the signal comparison. This circuit uses a latch comparator, which is composed of a positive feedback circuit responsible for transforming the analog input signal into a digital output signal with two logic levels (GND or VDD) (RAZAVI, 1995). Two inverters with gain $-A_v$ ($A_v > 0$) and composed of transistors M_1, M_2, M_3 and M_4 implements the positive feedback. In this circuit, the voltage difference between nodes X and Y, $V_X - V_Y$, will be amplified to a digital voltage level.

The circuit operation is as follows. At the reset phase, the clock signal (CLK) is at low logic level (0V), closing transistors M_{S1} and M_{S2}. Then, the output nodes V_{o-} and V_{o+} are set at a high logic level. Besides, transistors M_{S3} and M_{S4} are open, and the voltage at nodes X and Y is zero. When the CLK signal goes to a high logic level (0.6 V), transistors M_{1A-4A} and M_{1B-4B} operate in the linear region, and the currents at nodes X and Y are derived according to equations 43 and 44.

$$I_X = \sum_{i=1}^{4} I_i = \mu_n C_{ox} \sum_{i=1}^{4} \frac{W_i}{L}(V_{oi+} - V_T - \frac{V_X}{2})V_X \tag{43}$$

$$I_Y = \sum_{i=1}^{4} I_i = \mu_n C_{ox} \sum_{i=1}^{4} \frac{W_i}{L}(V_{oi-} - V_T - \frac{V_Y}{2})V_Y \tag{44}$$

Approximating $V_Y = V_X$ (since both are close to zero) gives the difference between the currents I_X and I_Y, as described in Equation 45:

$$I_X - I_Y = \frac{\mu_n C_{ox} V_X}{L} \sum_{i=1}^{4} W_i V_{oi} \tag{45}$$

where $V_{oi} = V_{oi+} - V_{oi-}$ is the multi-input comparator differential input voltage (from the output of the integrators and from the ELD compensation feedback DAC), and W_i is the channel width of transistors M_{iA} and M_{iB}. Thus, this comparator implements the feed-forward coefficients through the W relation between these transistors and still performs the sum of these signals.

Equation 46 gives the W relation used to implement the modulator feed-forward coefficients a_x. Table 9 provides the transistors size of the four-input comparator.

$$a_1 : a_2 : a_3 : a4 \rightarrow 7.97 : 2.72 : 5.60 : 0.3657 \rightarrow W_1 : W_2 : W_3 : W_4 \tag{46}$$

Table 9 – Transistors size of the four-input quantizer.

Transistors	W/L (μm/μm)
M_{S1}, M_{S2}, M_{S3}, M_{S4}	$4 \times 10.0/0.12$
M_1, M_2, M_3, M_4	$4 \times 10.0/0.60$
M_{1A}, M_{1B}	$44 \times 4.0/0.50$
M_{2A}, M_{2B}	$15 \times 4.0/0.50$
M_{3A}, M_{3B}	$31 \times 4.0/0.50$
M_{4A}, M_{4B}	$2 \times 4.0/0.50$

Figure 52 also presents an SR latch after the dynamic latch whose function is to generate the modulator output bitstream and the NRZ DAC control signals. CMOS inverters have also been added to the dynamic latch output to drive the SR latch and reduce the quantizer decision time. The SR latch schematic is not shown since it is a basic digital block.

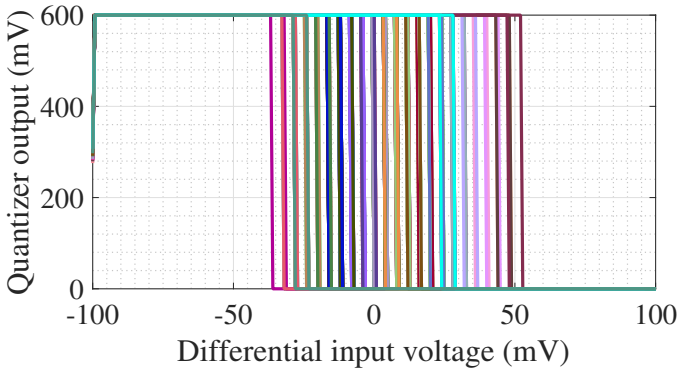
5.5.1 Quantizer Simulation Results

The comparator errors, namely offset and hysteresis, are not critical in CT-SDMs since the modulator loop-filter gain attenuates the impact of these errors. Nevertheless, the designed quantizer is simulated with the standard input-ramp method to verify its offset (DE LA ROSA; DEL RIO, 2013) and a triangular waveform is used to verify its hysteresis. In this simulation, the four differential inputs received the same input signal.

Figure 53 presents the 100-runs Monte Carlo simulation results. The comparator has a worst-case hysteresis of 4 mV and a worst-case input offset voltage of 50 mV. Extensive simulations in the Matlab/Simulink environment shows that this offset does not reduce

the modulator performance. It is noteworthy that the quantizer capacitive load used in the simulations is 250 fF. This load represents the input capacitance of the register used to provide the half clock cycle delay for ELD compensation. The simulated comparator decision time is approximately 7.1 ns for the falling time and 5.65 ns for the rising time, well below the half-clock period.

Figure 53 – Hysteresis electric characterization of the four-input comparator. Monte Carlo simulation with 100 runs.

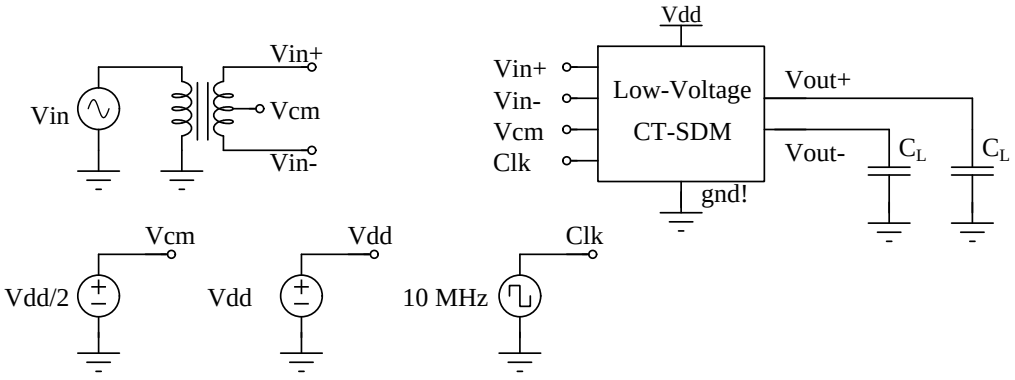


Source: The author

5.6 Schematic-Level Simulation Results of the Proposed CT-SDM

The complete modulator design used all the circuit blocks previously presented. The modulator electric simulations were carried out with the Spectre simulator using the test-bench depicted in Figure 54. The differential input signal is provided by a balun while the capacitive load of 1.5 pF at the modulator output simulates the output buffers input capacitance.

Figure 54 – Modulator testbench used in the schematic-level simulations.



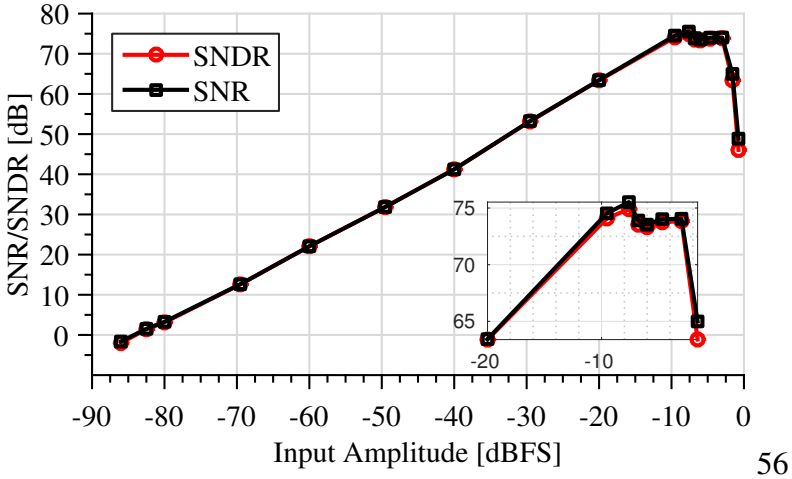
Source: The author

The modulator draws a current of 174.7 µA when powered by a 0.6-V power supply, leading to a power consumption of 104.7 µW. The modulator power consumption is dominated by the loop-filter amplifiers.

The modulator input signal used in the simulations has a frequency of 20 kHz and a DC level of 0.3 V. This frequency is chosen since its second and third-order harmonics falls inside the modulator signal bandwidth. The modulator output power spectrum density is calculated with a 64k-points FFT using a hanning window.

Figure 55 shows the simulated SNR and SNDR as a function of a 20-kHz input signal amplitude. The simulated DR is approximately 83 dB and the peak SNDR is 74.91 dB and occurs for input signals with amplitude of 250 mV (-7.6 dBFS). The ENOB is 12.15 bits and the SFDR is 81.86 dB, limited by the input signal fifth-order harmonic. The modulator does not show a significant SNDR reduction even for input signals with an amplitude of up to -3 dBFS. Additionally, the modulator presents a low distortion since the SNR and SNDR values are very close.

Figure 55 – SNR and SNDR versus the 20-kHz input signal amplitude: Schematic-level simulation.



Source: The author

Figure 56 presents the modulator output PSD for a 20-kHz input signal with amplitude of -6.02 dBFS. No significant harmonics are present in the signal bandwidth. Table 10 summarizes the modulator performance achieved by schematic-level simulation results.

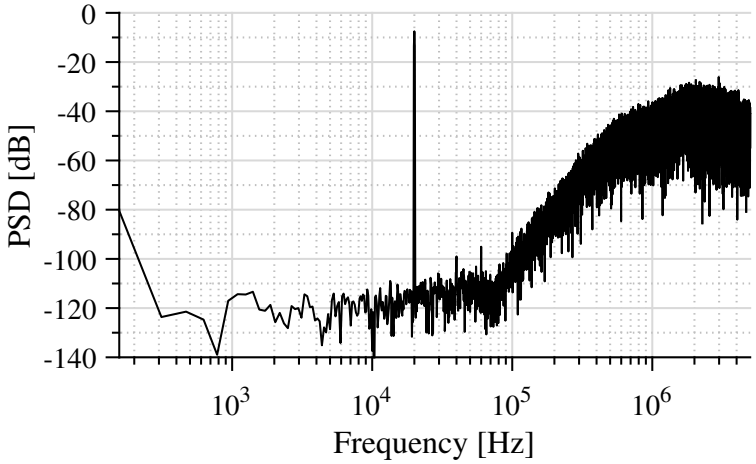
5.6.1 PVT Corners and Monte Carlo Simulation Results

The modulator was simulated against PVT corners to evaluate its robustness despite timing-consuming simulations. Figure 57 presents the modulator SNDR for a 20-kHz input signal with an amplitude of -6.02 dBFS considering process corners variations at 25°C, and also against temperature and power supply variations at the typical corner. The modulator presented an SNDR higher than 71.8 dB in all cases and a maximum SNDR of 75.68 dB.

Table 10 – Schematic-level simulation results of the designed modulator.

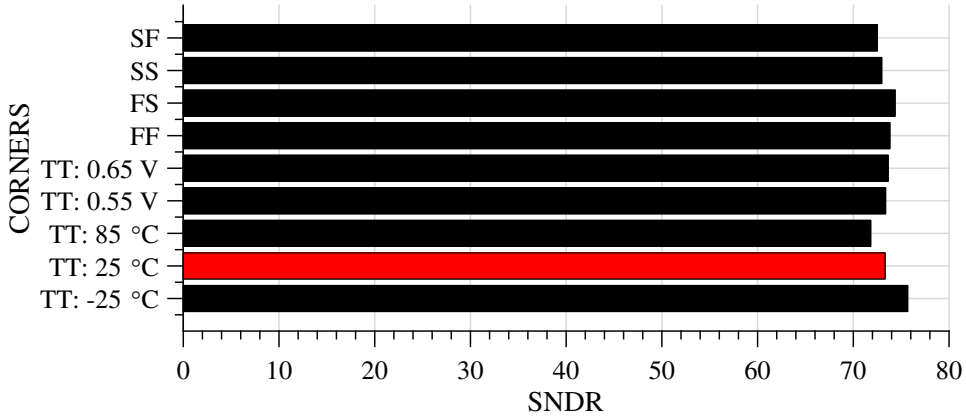
Parameters	Results
Supply voltage (V)	0.60
Fs (MHz)	10
BW (kHz)	100
OSR	50
Peak SNR (dB)	75.51
Peak SNDR (dB)	74.91
SFDR (dB)	81.86
ENOB (bits)	12.15
DR (dB)	83 dB
Power (µW)	104.82
FoM_W (fJ/conv.)	115.25
FoM_S (dB)	172.80

Figure 56 – Output PSD for a -6.02-dBFS input signal: schematic-level simulation.



Source: The author

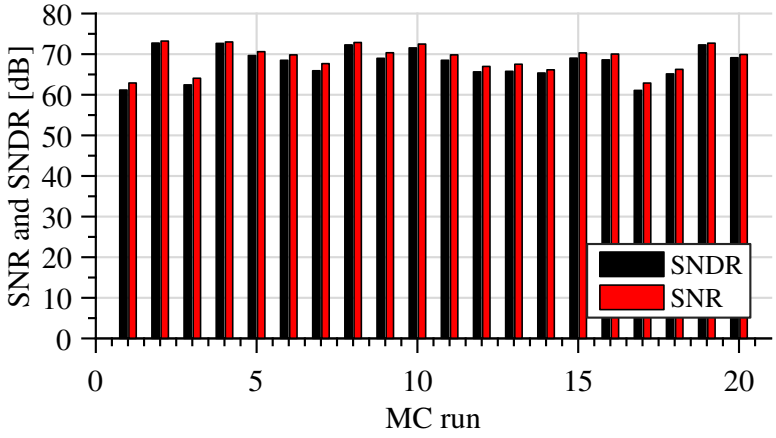
Figure 57 – Modulator SNDR for different PVT corners.



Source: The author

Monte Carlo simulation for 20 samples evaluates the modulator SNDR against process variations and mismatch. The number of Monte Carlo simulation runs is limited to 20 due to the high computational time required to finish the transient simulations. A 64k-point FFT requires a transient simulation of 6.6 ms. Figure 58 presents this simulation results. The SNDR varies from 62 dB to 73 dB. This variation should be further evaluated to accurately verify its origin. However, it is believed to be related to the amplifiers DC gain variation due to the negative conductance cell mismatch.

Figure 58 – Modulator SNDR with process and mismatch variations.



Source: The author

5.6.2 Discussions

This low-voltage third-order CT-SDM has three loop-filter integrators and uses three inverter-based amplifiers. Despite highlighting the possibility to design low-voltage and power-efficient CT-SDMs, this modulator was not fabricated due to the lack of available pins on the first manufactured multi-project chip. On the other hand, it is used as a basis to design a more power-efficient modulator designed with a single-amplifier resonator in the loop filter, reducing the number of loop-filter amplifiers as presented hereafter. This improved version was fabricated, and it is referred to as the first prototype (CT-SDM I).

5.7 CT-SDMs with Single-Amplifier Biquads

Generally, an n-order sigma-delta modulator requires n integrators in the loop filter, and depending on the topology, an adder in front of the quantizer is also needed. Thus, the loop filter implementation of an n order modulator needs n or n +1 amplifiers.

A large number of cascade integrators in a high-order modulator loop filter increases the total loop delay due to the amplifiers finite GBW (ORTMANNS; GERFERS, 2006). The increase of the amplifiers GBW reduces this delay at the cost of increasing the circuit power consumption. Thus, a strategy to minimize the loop filter delay, improve stability, and also save power, is to reduce the number of amplifiers in the modulator loop filter.

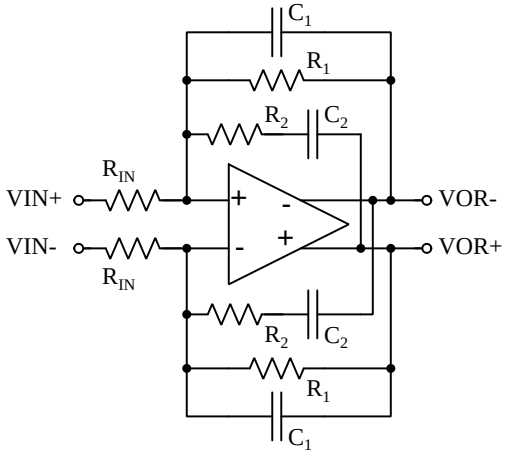
A commonly used strategy to reduce the power consumption of CT-SDMs is to design the loop-filter resonators with a single amplifier biquad (SAB). However, to the best knowledge of the author after an extensive bibliographical review, this approach has not been used yet to design CT-SDMs for low voltage applications. Thus, this led to the investigation of low-voltage CT-SDMs with SAB resonators in the loop filter.

The use of SABs to design the loop-filter resonators of CT-SDMs was introduced by (ZANBAGHI; FIEZ, 2009). This technique has been popularized as a strategy to reduce the energy consumption of CT-SDMs after the works presented by (MATSUKAWA *et al.*, 2010) and (ZANBAGHI; HANUMOLU; FIEZ, 2013), and it is explored in this thesis.

5.8 SAB Resonators with High Quality Factor

The SAB topology introduced by (CHAE *et al.*, 2014) to implement the loop-filter resonators of CT-SDMs was originally applied on the design of band-pass modulators. However, it has been employed in state-of-the-art low-pass CT-SDMs for high-frequency (BREEMS *et al.*, 2016) and audio (BERTI *et al.*, 2016) applications. Figure 59 shows the schematic diagram of this SAB resonator topology.

Figure 59 – Single-amplifier biquadratic resonator introduced by (CHAE *et al.*, 2014).



Source: The author

Its transfer function is given by Equation 47.

$$T(s) = \frac{R_1}{R_{IN}} \times \frac{sR_2C_2 + 1}{s^2(R_1R_2C_1C_2) + s(R_1C_1 + R_2C_2 - R_1C_2) + 1} \tag{47}$$

This circuit behaves as a resonator when Equation 48 is satisfied. Then, the resulting transfer function is equal to the one of an ideal resonator, as described by Equation 49 and the circuit resonance frequency is given by Equation 50.

$$R_1C_1 + R_2C_2 = R_1C_2 \rightarrow \frac{C_1}{C_2} = \frac{R_1 - R_2}{R_1} \tag{48}$$

$$T(s) = \frac{R_1}{R_{IN}} \times \frac{sR_2C_2 + 1}{s^2(R_1R_2C_1C_2) + 1} \tag{49}$$

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{50}$$

5.8.1 Finite Amplifier DC Gain Effect on the Resonator Transfer Function

Previously reported designs used high-gain amplifiers with two or more stages in the circuit-level implementation of this resonator. According to (CHAE *et al.*, 2014), this resonator topology requires high-gain amplifiers to achieve a high quality factor and low resonance frequency error. The transfer function of the resonator was calculated taking into account the amplifier finite DC gain. The resulting transfer function is given by Equation 51:

$$T(s) = \frac{sR_2C_2 + 1}{\text{DEN1} + \text{DEN2}} \tag{51}$$

where DEN1 and DEN2 expressed by equations 52 and 53.

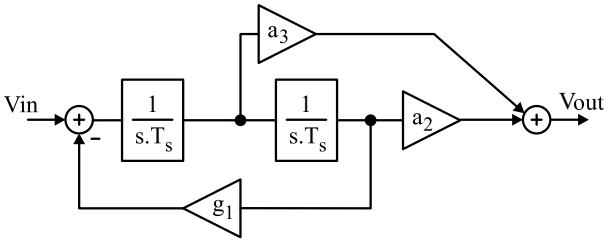
$$\text{DEN1} = \frac{R_{IN}}{R_1} \times (s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_1C_2) + 1) \tag{52}$$

$$\text{DEN2} = \frac{1}{AR_1} \times ((sR_2C_2 + 1) \times (R_1 + R_{IN}) + sC_1R_{IN}R_1 \times (sR_2C_2 + 1) + sR_1R_{IN}C_2) \tag{53}$$

The loop-filter resonator of the proposed CT-SDM is implemented with the presented single-amplifier resonator topology, and the following analysis shows the effects of amplifier finite DC gain on the resonator transfer function.

The resonator block diagram is depicted in Figure 60. Its transfer function is given by Equation 54 while the resonance frequency and resonator DC gain are given by Equation 55 and Equation 56, respectively.

Figure 60 – Block diagram of proposed CT-SDM loop-filter resonator.



Source: The author

$$Hres(s) = \frac{a_2sT_s + a_3}{s^2T_s^2 + g_1} \tag{54}$$

$$\omega_0 = \frac{\sqrt{g_1}}{T_s} \tag{55}$$

$$G_{DC} = \frac{a_3}{g_1} \tag{56}$$

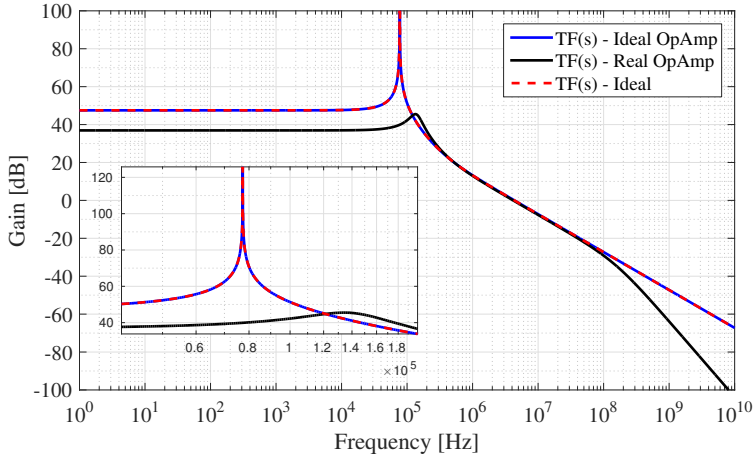
The passive components used in the resonator circuit-level implementation are calculated to satisfy the following equations: 48, 49 and 54. The input resistor (R_{IN}) is set to $R_{IN} = 50\ k\Omega$ to solve these equations. The resonator passive components are shown in Table 11.

Table 11 – Resonator passive components.

Component	R_{IN}	R_1	R_2	C_1	C_2
Value	50 kΩ	11.864 MΩ	625.73 kΩ	735.29 fF	776.23 fF

The frequency response of the ideal loop-filter resonator (Equation 54) and the transfer functions presented in equations 47 and 51 are shown in figures 61 and 62 taking into account an ideal amplifier and a real amplifier with DC gain of 40 dB and GBW equal to 15×Fs. This analysis considered the one pole amplifier model presented in Equation 57.

Figure 61 – Frequency response of the SAB resonator: Magnitude.

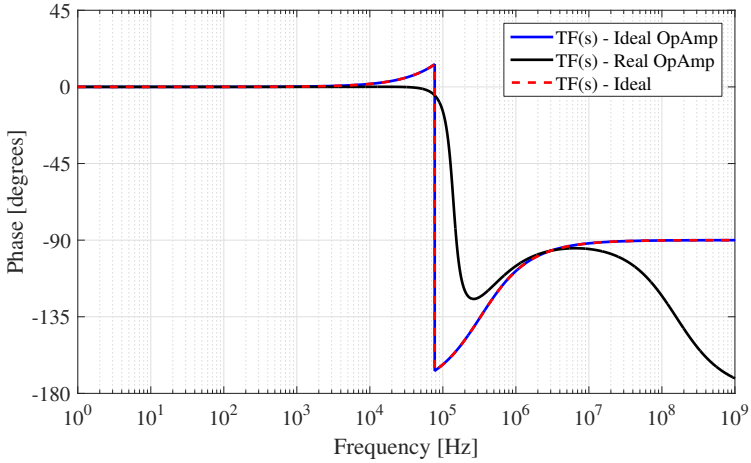


Source: The author

$$A(s) = \frac{A_v}{1 + s \times \frac{A_v}{\omega_u}} \tag{57}$$

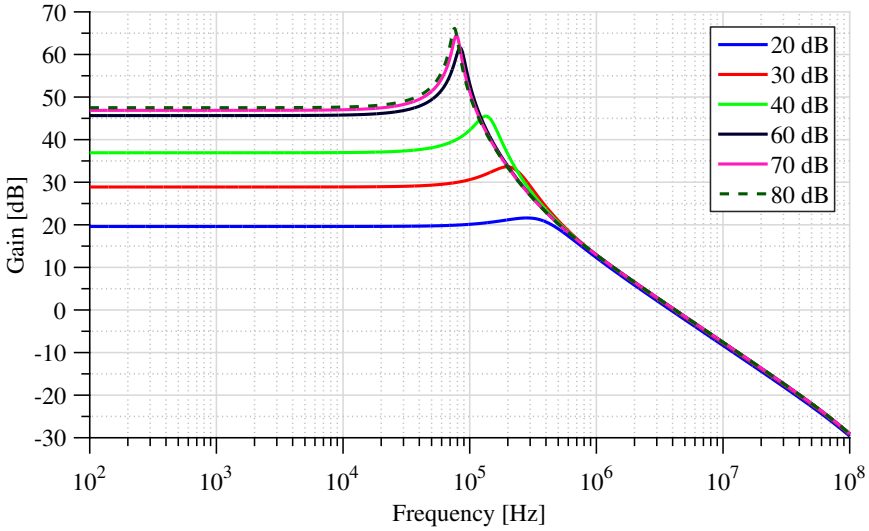
The use of amplifiers with finite DC gain (Av) generates the following effects: reduction of the resonator quality factor (Q), error in the TF DC gain, T(0), and increasing of the resonant frequency, ideally 77 kHz in this work. Figure 63 depicts those effects.

Figure 62 – Frequency response of the SAB resonator: Phase Margin.



Source: The author

Figure 63 – Resonator transfer function for amplifiers with different DC gains.



Source: The author

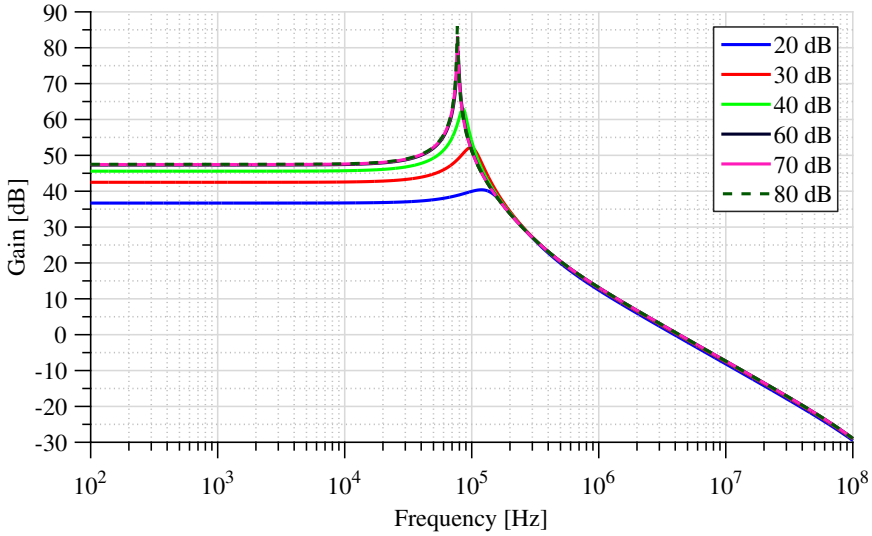
5.8.2 Compensated SAB Resonators with Low Gain Amplifiers

A scaling technique that improves the resonator quality factor was proposed by (BERTI *et al.*, 2016). It consists in reducing the resonator DC gain by a factor K (K=2) and multiplying the transfer function of the following block by the same factor K. This technique is effective for high-gain amplifiers (>60 dB) and is implemented reducing resistors R_1 and R_2, and increasing capacitors C_1 and C_2 after initial calculation.

This technique is extended in this work to properly restore the resonator TF even for amplifiers with finite DC gain as low as 40 dB. Initially, the passive components are calculated, considering resistor $R_{IN} = 50\,k\Omega$. Then, the resonator DC gain is reduced by a factor of K=10 by increasing resistor R_{IN} by 10, since $T(0) = R_1/R_{IN}$. It improves the quality factor, but the errors in the TF DC gain and in the resonant frequency persist, as shown in Figure 64. It should be noted that the higher the value of K, the lower

the resonance frequency error. It occurs because the unwanted term DEN2 present in Equation 51 tends to zero as K tends to infinity. However, the increase in K directly impacts the increase of the resistor R_{IN}, and consequently in the noise present at the first integrator output, which is not desired. Thus, an optimum value of K should be defined.

Figure 64 – Resonator transfer function for amplifiers with different DC gains and K=10.



Source: The author

After the definition of K, the value of the coefficient g1 must be changed before mapping the resonator coefficients to the electrical level implementation with the circuit shown in Figure 60.

The resonance frequency is given by Equation 55. The resonance frequency is corrected by iteratively reducing the g1 coefficient followed by the recalculation of passive components, keeping $R_{IN} = 50$ kΩ and scaling coefficient K=10, until the correct resonance frequency is restored. The reduction of g_1 from the value of 0.0236 to 0.018 leads to an increase in R1 with minor changes in other passive components while restoring the resonant frequency. Table 12 lists the new set of passive components.

Table 12 – Passive components used in the compensated resonator.

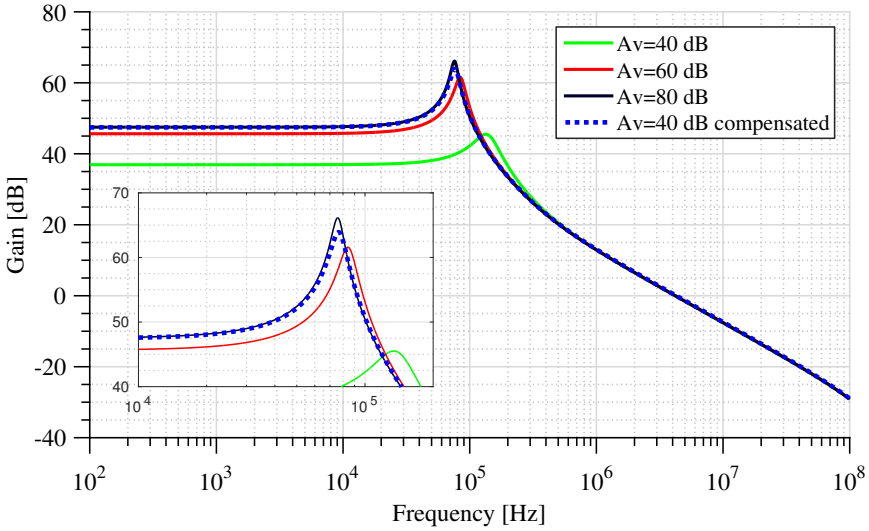
Component	R_{IN}	R_1	R_2	C_1	C_2
Value	500 kΩ	15.55 MΩ	633.66 kΩ	735.29 fF	766.51 fF

Besides, a block with gain K' must be added to the output of the resonator. Its gain may be greater than or equal to K, to leave the resonator DC gain identical to the DC gain of the ideal resonator transfer function. In this work K=K'=10.

Figure 65 presents the resonator TF response considering amplifiers with different finite DC gains without compensation and the compensated TF for an amplifier with $A_v = 40$ dB. This simulation considers a single-pole amplifier model with a fixed gain-bandwidth product of 150 MHz, i.e., $15 \times$ Fs. One can observe that the proposed solution

provides a resonator TF similar to the one provided by an amplifier with $A_v = 80$ dB and a DC gain error lower than 1%.

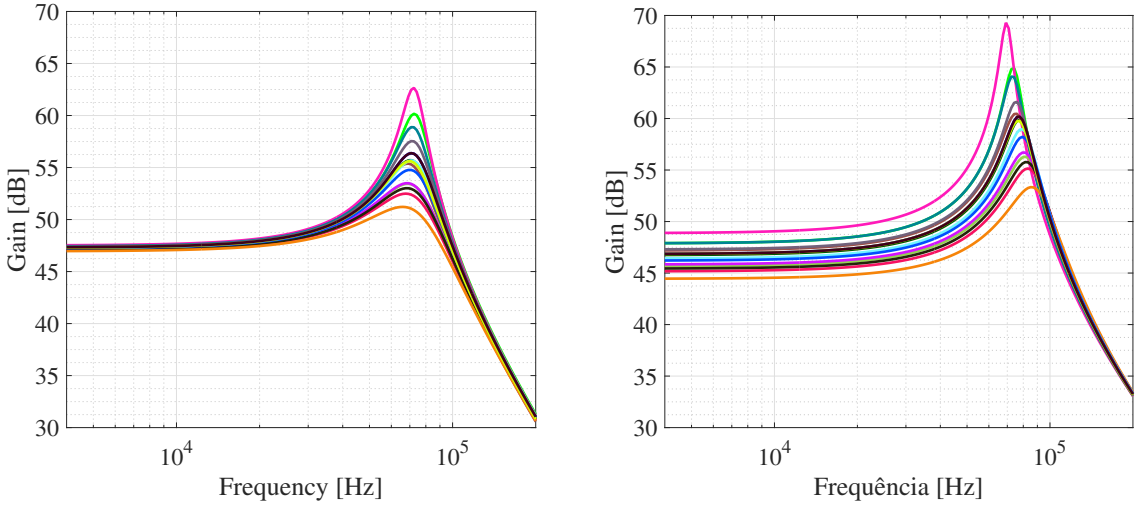
Figure 65 – Resonator TF for different Av without compensation and for Av=40 dB with compensation (GBW=15×Fs).



Source: The author

This resonator was designed with the proposed inverter-based amplifier already presented, and the compensation strategy is verified using schematic-level simulations. The traditional resonator implementation with two amplifiers is also designed and simulated for comparison purposes. Figure 66 presents the resonators frequency response across process (TT, FF, SS, SF and FS), voltage (0.55 V, 0.60 V and 0.65 V) and temperature (-25, 25 and 85 degrees) corners.

Figure 66 – Resonators frequency response for different PVT corners.



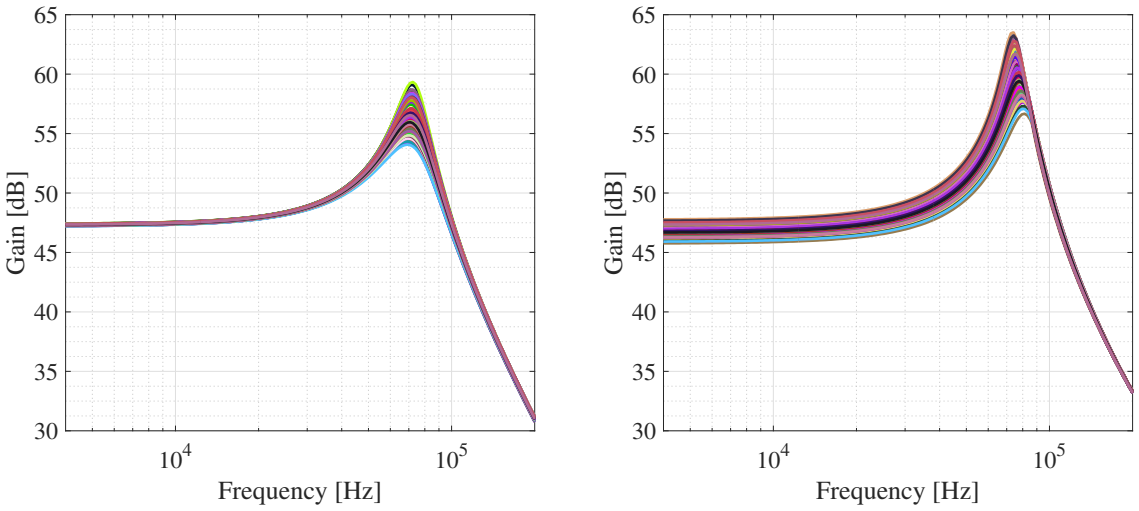
(a) Traditional resonator. (b) Compensated single-amplifier resonator.

Source: The author

According to Figure 66, the SAB resonator presents a resonance frequency between 70 kHz and 83 kHz across PVT corners while the classical resonator, with two amplifiers, has a more stable resonance frequency, between 70 and 75 kHz. This frequency shift in the SAB resonator occurs because of the amplifier DC gain and GBW variations. The SAB resonator presents a slightly higher quality factor in a traditional resonator, which favors the noise attenuation in the bandwidth of SDMs.

The resonators behavior against process variability and mismatch have also been evaluated at schematic-level. Figure 67 shows the Monte Carlo simulation results (1,000 runs) of traditional and single-amplifier resonators. The resonators behavior is similar to the one verified by corner simulations.

Figure 67 – Resonators frequency response: Monte Carlo simulation with 1,000 runs.



(a) Traditional resonator. (b) Compensated single-amplifier resonator.

Source: The author

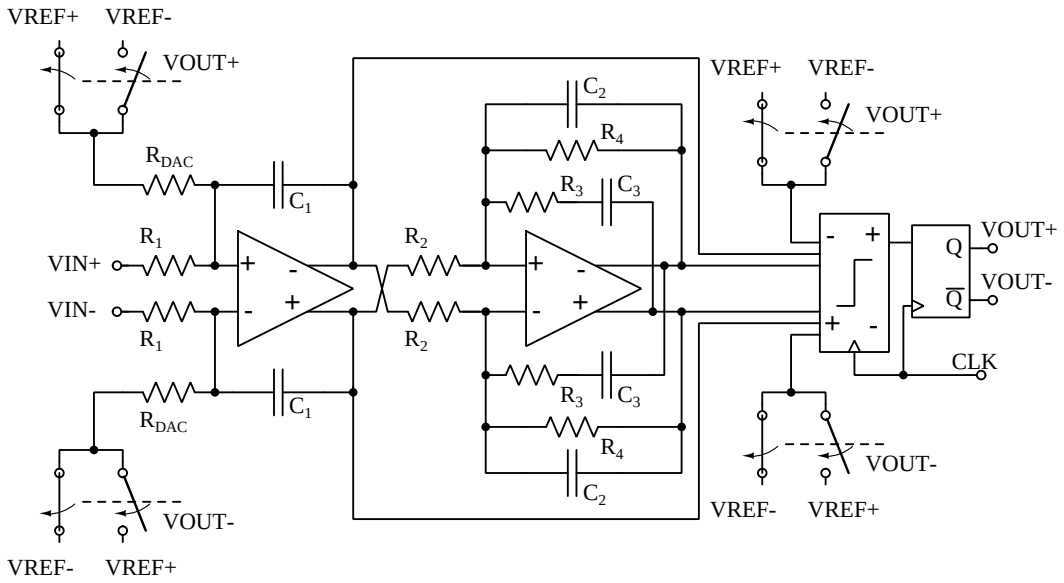
5.9 CT-SDM with Single-Amplifier Biquad Resonator

This section presents the implementation of the CT-SDM described in the previous Chapter, employing the proposed compensated SAB resonator in the modulator loop filter.

5.9.1 Schematic-Level Implementation

Figure 68 illustrates the schematic-level diagram of the proposed low-voltage CT-SDM in which the positive and negative voltage references of the resistive NRZ DAC are VDD and ground (0 V), respectively. The loop filter was implemented with active-RC structures using only two amplifiers: one for the first integrator and the other for the SAB resonator.

Figure 68 – Schematic of a CT-SDM with SAB resonator.



Source: The author

5.9.1.1 Integrator and Thermal Noise

To reduce the power consumption of the integrator amplifier, the resistors R_{IN} and R_{DAC} should be maximized in order to minimize the integrating capacitance. Notice, however, that the extent of which R_{IN} and R_{DAC} can be maximized is limited by the input thermal noise floor, since the input-referred noise at the modulator input is not attenuated by noise-shaping. The total input-referred noise density at the input of the modulator, $\bar{v}_{ir}^2$, is expressed by:

$$\bar{v}_{ir}^2 \approx 2 \times (\bar{v}_{R_{IN}}^2 + \bar{v}_{DAC}^2) + 4 \times \bar{v}_{in-OTA}^2 \; [V^2/Hz] \tag{58}$$

where $\bar{v}_{R_{IN}}^2$ and $\bar{v}_{DAC}^2$ are the noise from input and DAC resistors, respectively, and $\bar{v}_{in-OTA}^2$ is the input-referred noise of the first OTA. Thus, resistors R_{IN} and R_{DAC} were maximized for minimizing the integrating capacitance while keeping the input thermal noise floor at an acceptable level. In this work, an analysis considering uncorrelated noise sources was performed and the input resistors were defined as 125 kΩ (calculated equal to 134.92 kΩ) to keep the input-referred integrated noise in the 100-kHz bandwidth below 14.96 μV.

5.9.1.2 Loop-Filter Coefficients and RC Variation

The RC constant of active-RC integrators is susceptible to process variations and usually a RC tuning scheme is employed to cope with these variations. The RC time constant is implemented with high resistance poly resistor with 228 Ω/□ (maximum variation of ±8%) and dual-MiM capacitors with 4.1 fF/μm^2 (maximum variation of ±10%). Monte Carlo simulations (1,000 runs) indicate a resistor standard deviation of 4.38% while the

capacitors standard deviation is 2.79%. Based on these results, non-correlated and correlated statistical analysis were carried out providing a RC time-constant variation, in the 3σ range, of 15.27% and 20.22%, respectively. Thus, a RC tuning is not required and was not used in this prototype. Table 13 provides the passive component values used in the loop-filter design.

Table 13 – CT-SDM passive components value.

Resistors (kΩ)					Capacitors (pF)		
R_1	R_{DAC}	R_2	R_3	R_4	C_1	C_2	C_3
125	125	500	633.66	15,500	8.0	0.73529	0.77651

5.9.2 OTAs Design

The proposed modulator uses the same OTA topology already presented and all amplifiers are properly scaled to save power while providing the required GBW and DC gain. The sizing of the first integrator took into account a load composed of the resonator input resistor in parallel with the integrator capacitor C_1. Table 14 presents the amplifier main parameters achieved by schematic-level simulation results. The total power consumption is 36.77 µW where 2.96 µW is consumed by the CMFB circuit. The SAB resonator uses exactly the same amplifier since it achieves a GBW of 140 MHz for a 1-pF load. Table 15 summarizes the Monte Carlo (1,000 runs) and PVT corners simulation results.

Table 14 – OTA performance for a load of 8 pF||500 kΩ: schematic-level simulation results.

Parameter	Value
Supply voltage (V)	0.6
GBW(MHz)	14.5
DC Gain (dB)	38.54
Phase Margin (°)	89.83
Total static current (µA)	66.2
Power (µW)	39.72
In-Band Input-Referred Noise (µV)	10.39

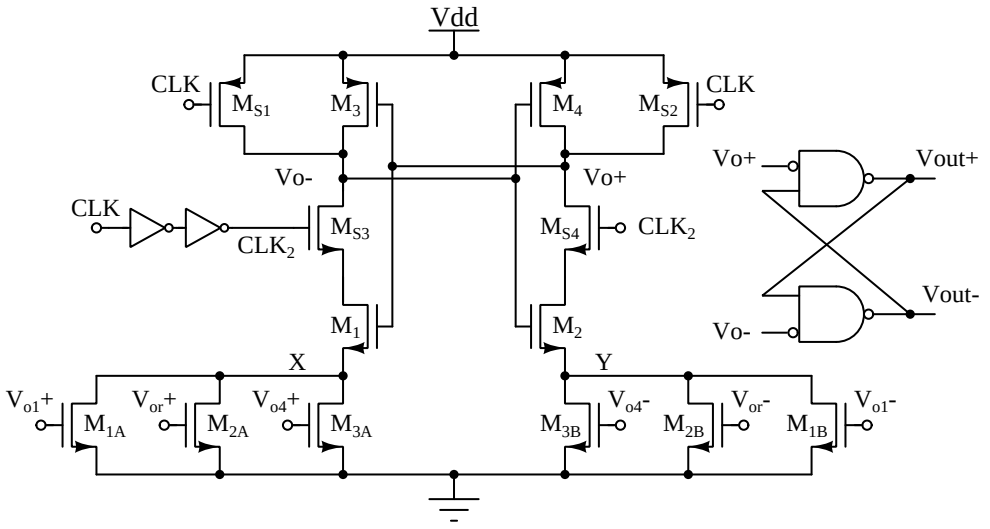
Table 15 – Main OTA parameters: Monte Carlo and PVT corners simulation results.

Parameter	Monte Carlo		Corners	
	Average	Standard Deviation	Minimum	Maximum
GBW(MHz)	14.52	1.50	8.71 (SS@-25deg)	18.52
DC gain (dB)	36.78	2.19	32.1 (FF@85deg)	46.6
Phase Margin (°)	90.01	0.266	89.41	90.55

5.9.3 Quantizer and Feed-Forward Coefficients

The multi-input comparator topology presented in previous the Chapter was maintained since it allows the implementation of summation and quantization functions with low energy consumption. A three-input comparator, depicted in Figure 69, is required since a SAB resonator is used in the loop filter. A careful transistors sizing provided the feed-forward coefficients implementation and a precise SAB resonator gain (K). Table 16 presents the quantizer transistors size.

Figure 69 – Quantizer schematic.



Source: The author

Table 16 – Quantizer transistors size.

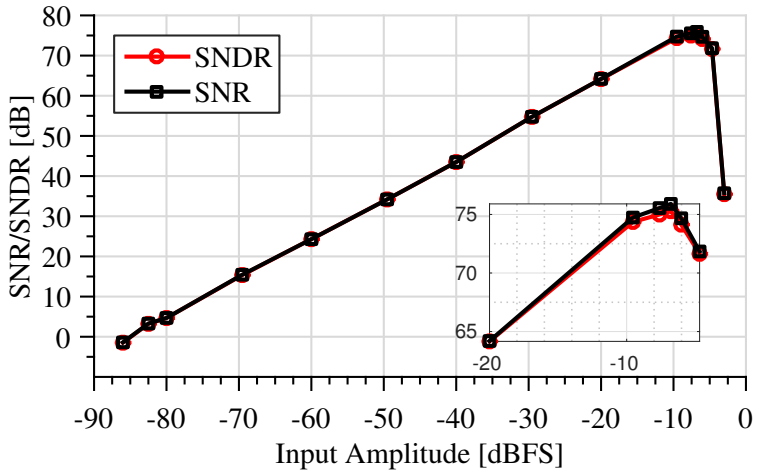
Transistors	W/L (μm/μm)
M_{S1}, M_{S2}, M_{S3}, M_{S4}	$4 \times 10.0/0.12$
M_1, M_2, M_3, M_4	$4 \times 10.0/0.60$
M_{1A}, M_{1B}	$44 \times 4.0/0.50$
M_{2A}, M_{2B}	$56 \times 4.0/0.50$
M_{3A}, M_{3B}	$2 \times 4.0/0.50$

5.10 Schematic-Level Simulations

Schematic-level simulations of the designed modulator at typical corner are given in this section. The modulator clock signal is generated by applying a 10-MHz sinusoidal signal, with amplitude of 600 mV and DC level of 300 mV, to a chain of inverters. The modulator draws an average current of 138.5 μA at 0.6 V leading to a power consumption of 82.83 μW. Figure 70 shows the simulated SNR and SNDR as a function of the 20-kHz input signal amplitude. The simulated DR is 85 dB and the peak SNDR is 75.28 dB

(ENOB=12.21 bits) and occurs for input signals with amplitude of 275 mVp. In general, the difference between SNR and SNDR is low, indicating a low-distortion modulator. However, a significant SNDR reduction occurs for input signals higher than -4.7 dBFS.

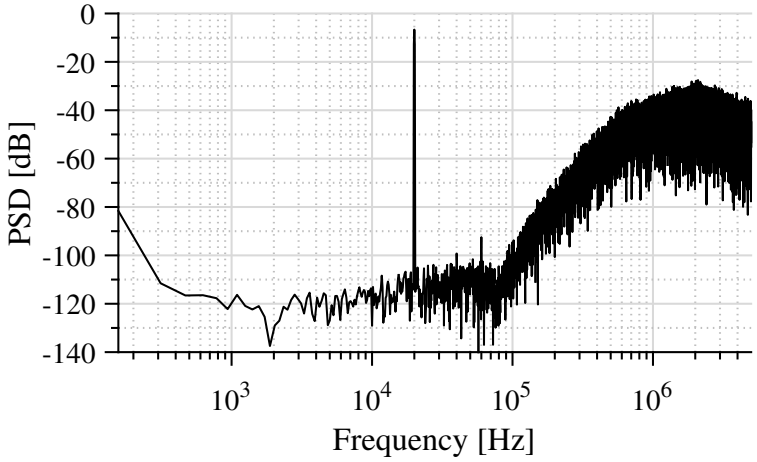
Figure 70 – SNR and SNDR versus the 20-kHz input signal amplitude: Schematic-level simulation.



Source: The author

Figure 71 presents the modulator output PSD for a 20-kHz input signal with amplitude of 275 mVp (-6.78 dBFS). The spurious-free dynamic range (SFDR) is 85.80 dB. It is limited by the input signal third-order harmonic. Table 17 summarizes the schematic-level simulation results of the designed modulator.

Figure 71 – Output PSD for a -6.02-dBFS input signal. FFT with 64k points.



Source: The author

5.10.1 PVT Corners Simulation Results

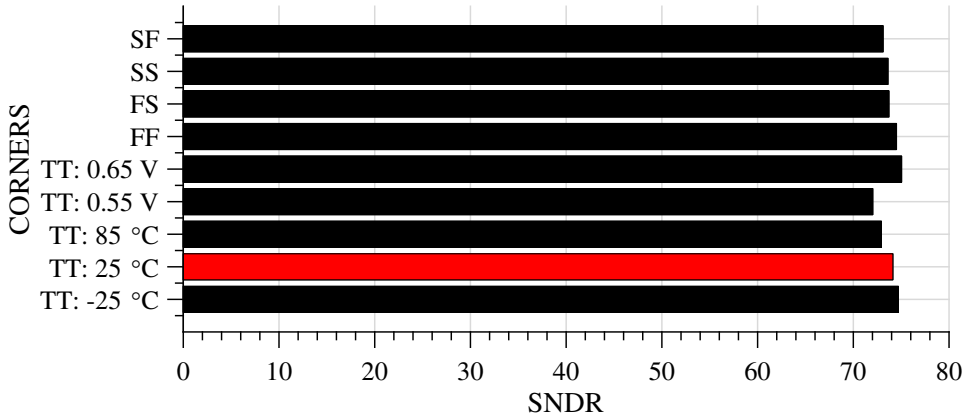
The modulator was simulated against PVT corners to evaluate its robustness despite timing-consuming simulations. Figure 72 presents the modulator SNDR for a 20-kHz input signal with an amplitude of -6.02 dBFS considering process corners variations at

Table 17 – Schematic-level simulation results of the designed modulator.

Parameters	Results
Technology (nm)	130
Supply voltage (V)	0.60
Fs (MHz)	10
BW (kHz)	100
OSR	50
Peak SNDR (dB)	75.28
Peak SNR (dB)	75.90
SFDR (dB)	85.80
ENOB (bits)	12.21
DR (dB)	85
Power (µW)	81.12
FoM_W (fJ/conv.)	86.38
FoM_S (dB)	175.86

25°C, and also against temperature and power supply variations at the typical corner. The modulator presented an SNDR higher than 72 dB in all cases.

Figure 72 – Modulator SNDR for different PVT corners.



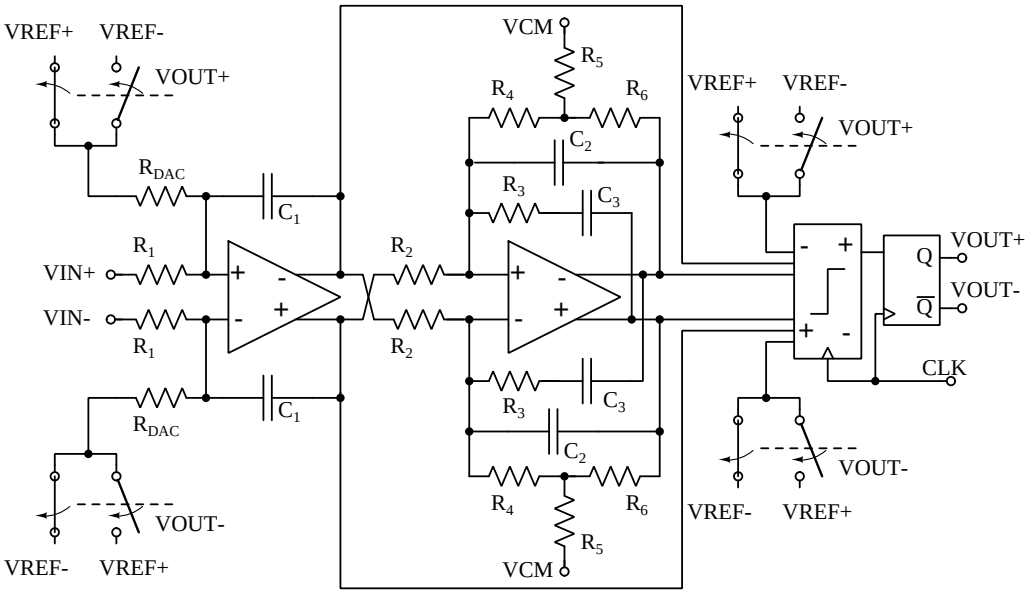
Source: The author

5.11 Layout

To reduce silicon area, the resistor R_3 present in Figure 68 is replaced by an equivalent T resistive network as illustrated in Figure 73.

This strategy is commonly used to implement high resistance resistors in CT-SDMs with single-amplifier resonators in the loop filter (KAALD; EGGEN; YTTERDAL, 2017). This resistive T network was calculated by defining resistors R_4 and R_6 equal to 500 kΩ and finding the value of R5 (17.18 kΩ) according to Equation 59, where Rf is the resistive T network equivalent resistance. Thus, the 15.50-MΩ resistor is replaced by resistors R_4, R_5 and R_6.

Figure 73 – Schematic diagram of proposed low-voltage CT-SDM.



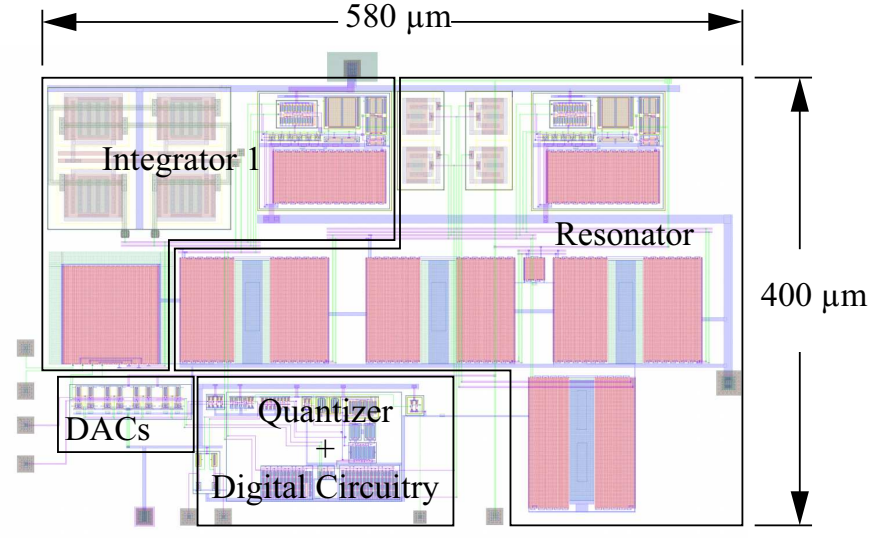
Source: The author

$$R_5 = \frac{R_4}{\frac{Rf}{R_4} - 2} \tag{59}$$

The presented CT-SDM was designed and fabricated in a 130-nm CMOS single-poly eight-metal (1PM8) process with triple-well and dual MiM capacitors option. The layout of this modulator was carefully performed using the main layout techniques as common-centroid and interdigitation for the amplifiers and passive components. However, due to the minimum dual MiM capacitors value (≈680 fF), no special layout technique was used for capacitors C3 and C4. The complete layout of the 3rd-order SAB CT-SDM is depicted in Figure 74. The modulator's total active area is 0.232 mm^2.

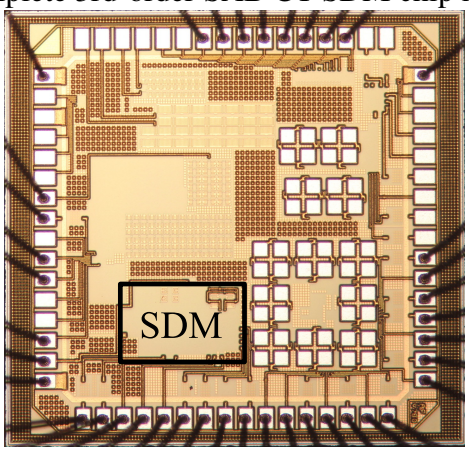
The circuit was included in a multi-design integrated circuit. Then, only two power supply pads were used due to the limited number of pins in the IC, one to power the analog circuits and other for the digital circuitry, including the output buffers. It limited the direct measure of the modulator digital circuitry power consumption. However, this strategy still reduces de probability of digital noise coupling into the analog circuits through the power supply pin. Also, the analog and digital ground are provided by the same pad. Electrostatic discharge (ESD) protection was also included in the IOs to protect the IC of undesired events. The chip microphotograph is shown in Figure 75. The amplifier of the first integrator was also independently fabricated in the same IC to allow the topology validation.

Figure 74 – Complete 3rd-order SAB CT-SDM layout.



Source: The author

Figure 75 – Complete 3rd-order SAB CT-SDM chip microphotograph.



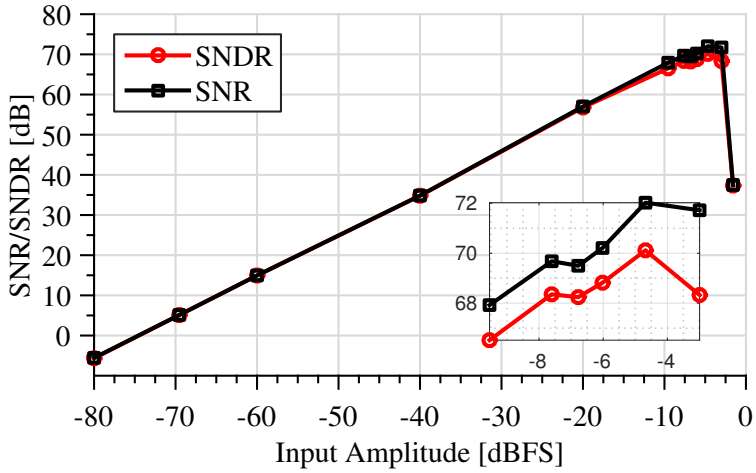
Source: The author

5.12 Post-Layout Simulation Results

The post-layout simulations of the proposed circuit are time consuming. They were carried out with the *Spectre* simulator in conservative mode and with the APS++ option active with 8 threads. The average simulation time for a 6.6 ms transient simulation was reduced from 52 hours (using native spectre) to 14.40 hours (APS++). A test simulation was performed, and the results from traditional and APS ++ *Spectre* simulations do no present discrepancies. To save simulation time, all output PSDs shown in this Section are calculated with a 32k-point FFT.

Figure 76 shows the simulated SNR and SNDR as a function of the 20-kHz input signal amplitude. The simulated DR is 74.50 dB and the peak SNDR is 70.12 dB (ENOB=11.33 bits) and occurs for input signals with amplitude of 350 mVp.

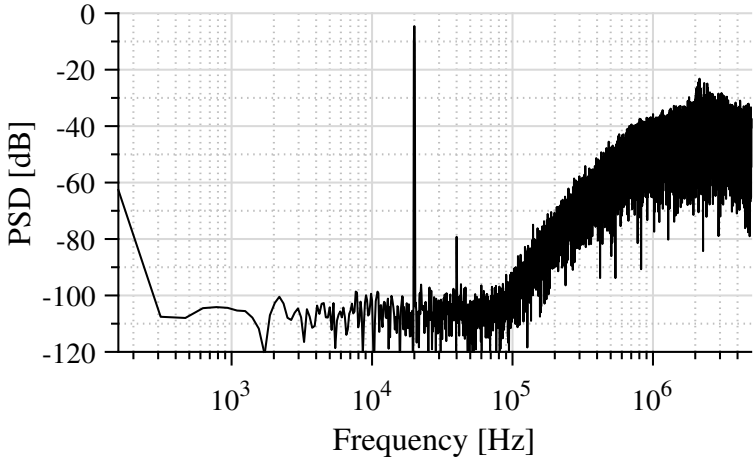
Figure 76 – SNR and SNDR versus the 20-kHz input signal amplitude: Post-layout simulation.



Source: The author

Figure 77 presents the modulator output PSD for a 20-kHz input signal with amplitude of 350 mVp. A second-order harmonic (HD2) arose at the modulator output spectrum. It was verified by simulation that this HD2 is due to the modulator top-level routing since it did not appear in simulations that took into account the extracted layout of all the elements, without the top routing. Thus, this HD2 is due to the asymmetric routing in the top-level layout and can be eliminated by an optimized layout. Despite the reduction of the achieved SFDR (76.65 dB), this HD2 is not significant to reduce the SNDR.

Figure 77 – Output PSD for a 20-kHz input signal with amplitude of 350 mVp: Post-layout simulation.



Source: The author

The simulated total power consumption of the proposed modulator, including the power consumption of clock generator and output buffers, is 109.80 µW. The loop-filter amplifiers dissipates 73.80 µW. The achieved Walden figure-of-merit (FoM_W) is 209.17 fJ/conversion. It is lower than the achieved one at schematic-level simulations due to the SNDR decrease.

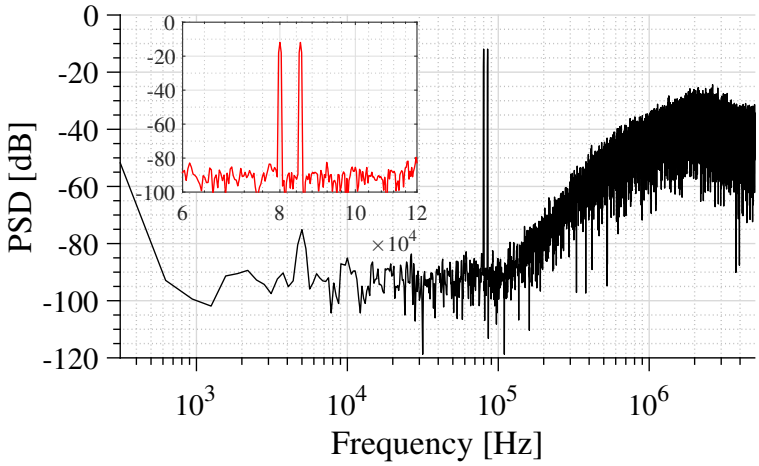
Table 18 presents the modulator SNDR against the power supply variation, considering a 20-kHz input signal with an amplitude of 275 mV. Decreasing the supply voltage reduces the amplifiers GBW and thus the modulator SNDR.

Table 18 – CT-SDM performance versus the power supply voltage.

Parameter	VDD (V)			
	0.50	0.54	0.60	0.66
SNR (dB)	61.65	64.89	69.50	73.09
SNDR (dB)	59.46	63.22	68.30	71.91
ENOB (bits)	9.585	10.21	11.06	11.65

Figure 78 shows the simulated output PSD plot obtained for the two-tone test to verify the third-order intermodulation distortion (IM3). The inputs signals have an amplitude of -12.04 dBFS (150 mVpeak) and frequencies of 80 kHz and 85 kHz (near the band-edge). This two-tone simulation resulted in IM3 components lower than -80 dB and IM2 of -75.11 dB at 5 kHz.

Figure 78 – Simulated output PSD for a two-tone test for signals near the band-edge.



Source: The author

5.13 Measurement Setup

The fabricated IC was packaged in a DIP40 package. In order to measure the fabricated CT-SDM, a customized evaluation board (EVB) was designed. The printed board circuit (PCB) was fabricated at the university using a standard two layer FR-4 board. Both layers were used for routing and the remained copper area in the EVB was used as ground.

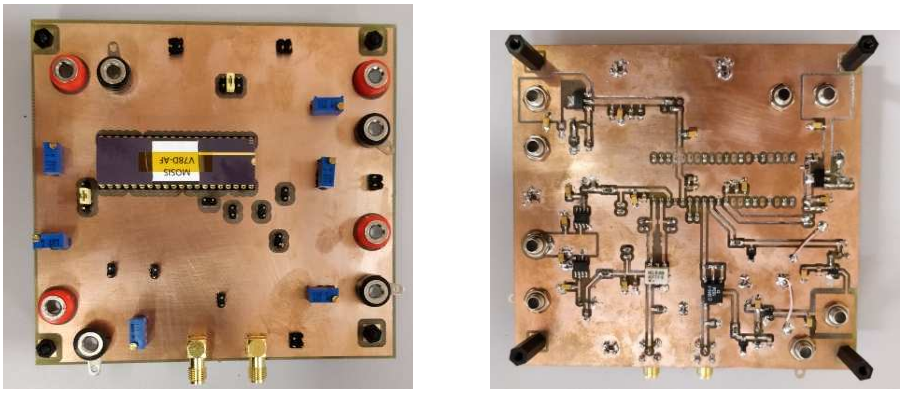
The modulator analog and digital power supplies of 0.6 V were generated by two on-board low-dropout regulators (LDOs) LT3080. Bypass capacitors of 10 µF and 100 nF were used at the regulator output and also as close as possible of the chip power supply pins to provide clean DC supply voltages. The amplifiers common-mode voltage of 0.3 V and the positive reference voltage were generated by a low-noise TI5020 voltage reference

followed by a resistor divider and a first-order RC filter. Also, bypass capacitors of 10 µF and 100 nF are used as close as possible of the chip pins.

The modulator input differential signal is provided by a ADTT1-6 balun that performs single-ended to fully-differential conversion. The balun output common-mode voltage is equal to 0.3 V, however, it is generated by a ADR3412 voltage reference. The clock signal is provided by a PWB3010 balun with a DC level equal to 0.3 V. This DC voltage is generated on board by a ADR3412 voltage reference in order do avoid noise coupling from the clock signal to the input common-mode voltage nodes.

The complete final version EVB is depicted in Figure 79. Only one EVB was built and the measured chips were connected to the PCB by a DIP40 socket.

Figure 79 – EVB used to characterize the 3rd-order SAB CT-SDM.



(a) Top. (b) Bottom.

Source: The author

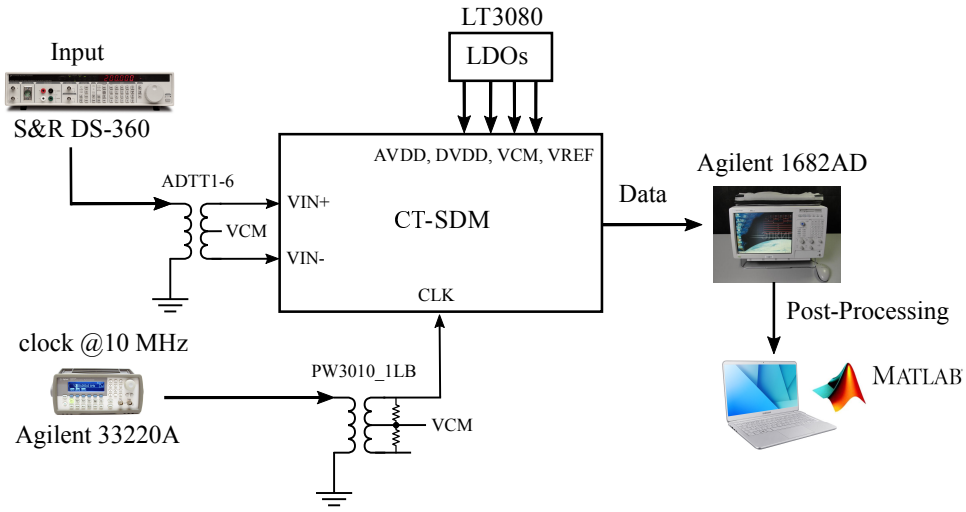
The measurement of this modulator took place at the Microelectronics Group of the Federal University of Santa Maria due to the need of a low-distortion signal generator. Figure 80 illustrates the measurement setup diagram while Figure 81 illustrates experimental setup.

The input signal was provided by a low-distortion DS-360 signal generator and an ADTT1-6 balun performs the single-ended to fully differential conversion. The clock signal was provided by an Agilent 33220A signal generator. The power consumption was measured with an Agilent 34401A digital multimeter. The output bitstream was captured by an Agilent 1682AD logic analyzer and post-processed on Matlab using a 32k-point FFT with periodic Hanning window for spectral leakage suppression.

5.14 Measurement Results

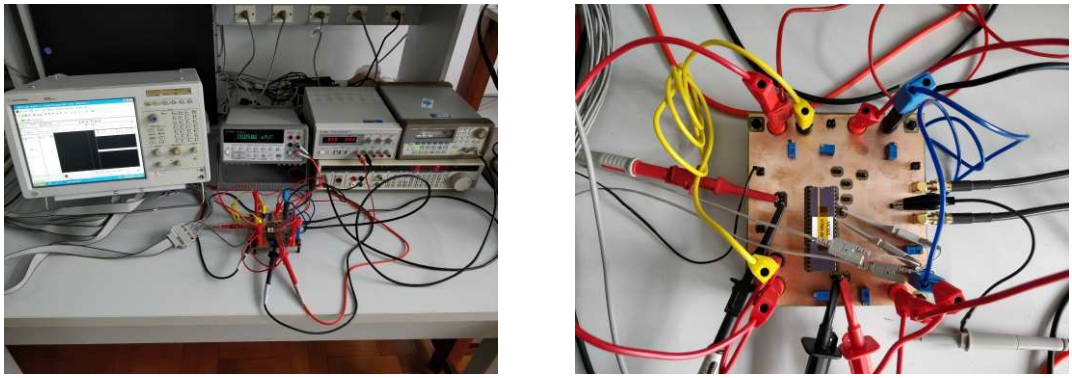
This section presents the measurement results of the 3rd-order SAB CT-SDM. Two samples were measured in this work and both presented very similar results. The provided measurement results and plots in this section are from the sample I unless otherwise

Figure 80 – Measurement setup diagram of the 3rd-order SAB CT-SDM.



Source: The author

Figure 81 – Measurement setup of the 3rd-order SAB CT-SDM.



(a) Measurement setup. (b) Zoom in the EVB.

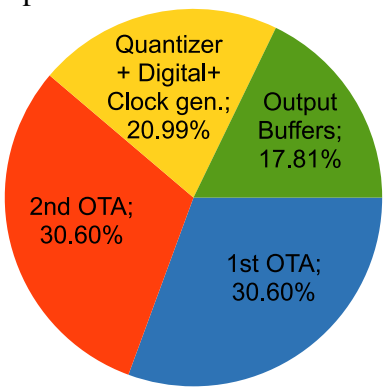
Source: The author

specified. The measurement process was conducted at room temperature and no temperature characterization was performed due to the unavailability of a thermal chamber and low-distortion signal generator in the same University.

The main characterization was performed using an input signal frequency of 30 kHz in order to include the second-order (HD2) and third-order (HD3) harmonic distortions.

The CT-SDM operates with a clock frequency of 10 MHz and the measured total power consumption is 89.50 µW, from which 54.78 µW is for the analog part and 34.72 µW is for the digital circuitry, including clock generation and output buffers (45.90% of the total digital power). The measured power consumption of the analog part, i.e. amplifiers, is less than the 73.80 µW obtained by post-layout simulation results. However, MC simulations of the loop filter indicate an average power consumption of 74.40 µW with $\sigma = 12.45$ µW. Figure 82 shows the modulator estimated power breakdown.

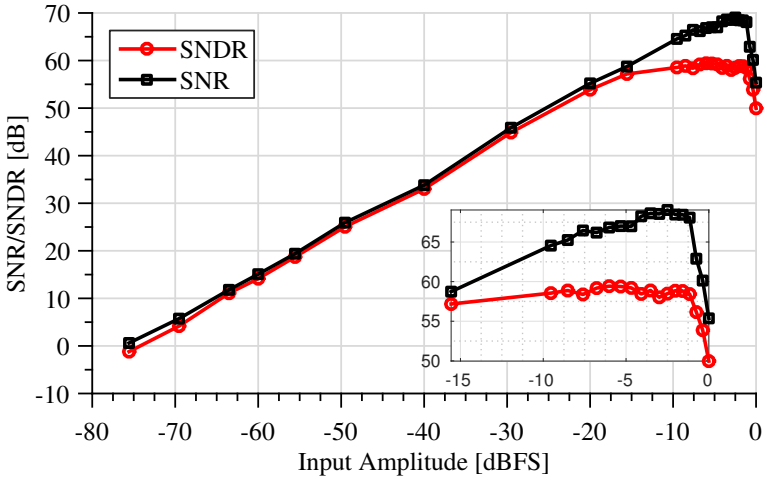
Figure 82 – Estimated power breakdown of the 3rd-order SAB CT-SDM.



Source: The author

Figure 83 presents the SNDR and SNR versus the input signal amplitude of sample II. The obtained dynamic range (DR) is 74.2 dB and one can observe a stable modulator for large input signals. The measured peak SNR, peak SNDR and peak SFDR are 69.04 dB, 59.43 dB, and 60.51 dB, respectively.

Figure 83 – Measured SNR/SNDR versus input power (Fin=30 kHz) at VDD = 0.60 V (Sample II).

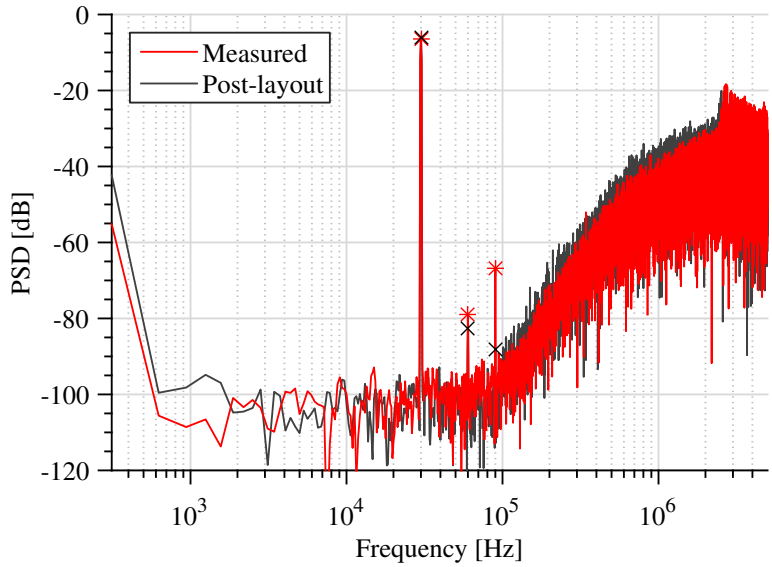


Source: The author

The measured and simulated (post-layout at typical corner) power spectrum density (PSD) for a -6.02-dBFS (300 mVpeak) input signal is presented in Figure 84.

As can be seen, HD2 and HD3 degrade the measured SNDR. After extensive simulations, it is possible to conclude that the former origin of HD2 is due to device and layout path mismatch since it appeared in post-layout simulation results. It produced a mismatch between rise and fall times of the output DAC current, generating inter-symbol interference (ISI). Also, after some post-layout simulations, it was verified that increasing the clock buffer capability it was possible to reduce the second-order harmonic. However, HD3 was evidenced only by measurement results. Post-layout simulations at different corners and 50 MC runs at schematic level were performed and no HD3 higher than HD2

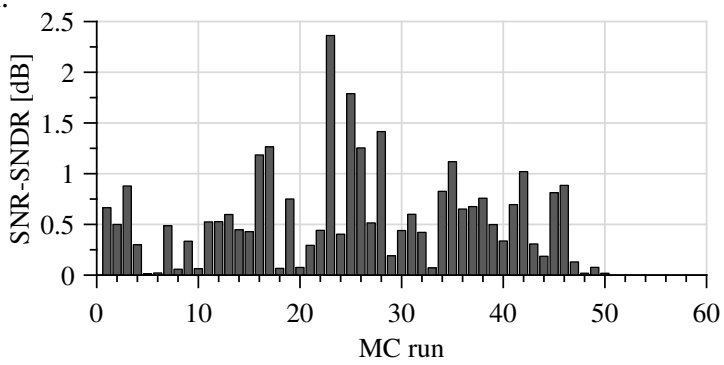
Figure 84 – Measured and simulated PSD for a -6.02-dBFS 30-kHz input signal (Sample II).



Source: The author

was obtained and no significant difference between SNR and SNDR was verified. Figure 85 presents difference between the modulator SNR and SNDR for a 50-runs Monte Carlo simulation at schematic level. In one of these simulation runs, the modulator presented an SNDR of only 42.69 dB, possibly originated by the reduction of maximum input signal amplitude for which the modulator is stable. Until now, the source of HD3 based on simulation results was not possible to identify.

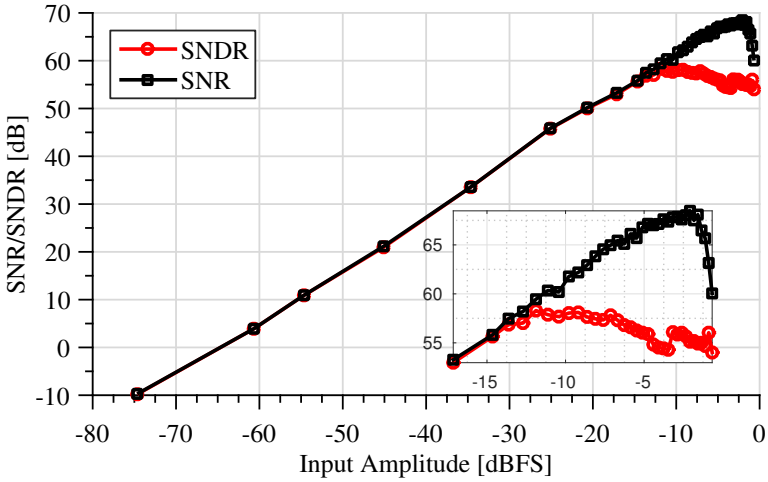
Figure 85 – Difference between SNR and SNDR: Monte Carlo simulation results at schematic-level.



Source: The author

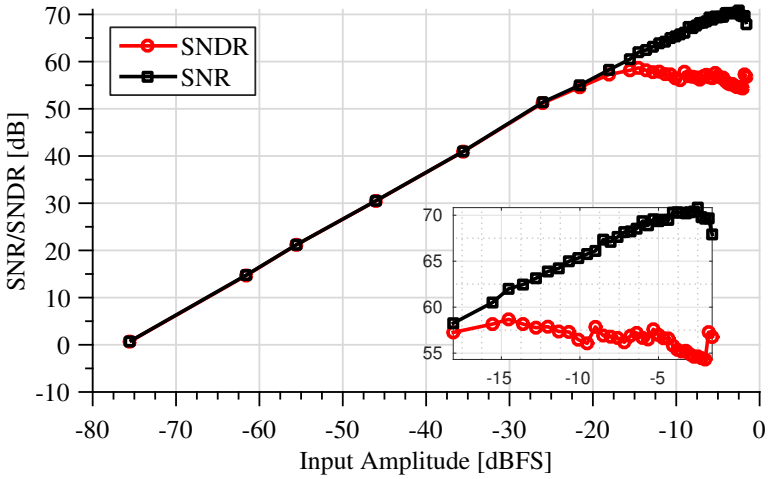
The modulator was also measured for a VDD variation of ±10%. At 0.54 V the achieved SNDR for sample II is 64.73 dB while the SNDR at 0.66 V is 60.30 dB. Figures 86, 87 and 88 present the modulator DR of sample I for VDD equal to 0.54 V, 0.60 and 0.66 V, respectively. One can see an SNDR degradation starting for amplitude signals as high as -10 dBFS. This behavior is equal in both samples.

Figure 86 – Measured SNDR/SNR versus input power (Fin=30 kHz) at VDD = 0.54 V (Sample I).



Source: The author

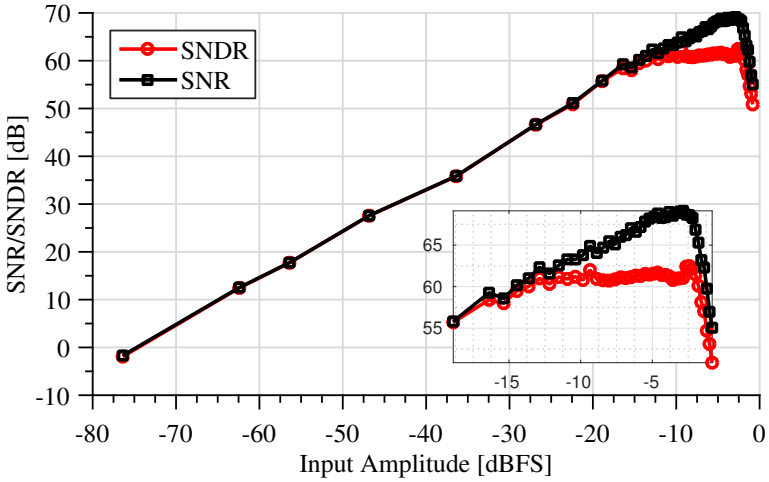
Figure 87 – Measured SNDR/SNR versus input power (Fin=30 kHz) at VDD = 0.60 V (Sample I).



Source: The author

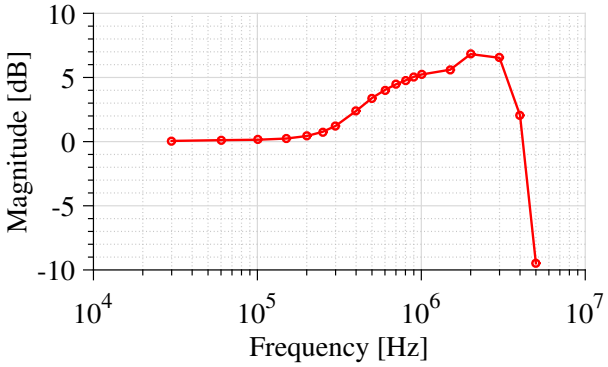
The evaluation of the STF peak was performed in sample II. A input signal with amplitude of -18.06 dBFS was applied by a standard signal generator (Rigol DG1022A) and the signal frequency was varied from 30 kHz to 5 MHz. Figure 89 presents the normalized input signal amplitude versus the signal frequency. An STF gain of 4.75 dB is verified for an input frequency of 800 kHz while the STF peak is 6.82 dB at 2 MHz (calculated with a 64k-point FFT). Thus, an input filter to suppress out-of-band interferes might be required if this modulator is used in an environment with high out-of-band (OOB) blockers. It should be pointed out that the measured STF gain at 800 kHz is lower than the STF gain of 5.77 verified in schematic-level simulations.

Figure 88 – Measured SNDR/SNR versus input power (Fin=30 kHz) at VDD = 0.66 V (Sample I).



Source: The author

Figure 89 – Measured STF for an input signal of -18.06 dBFS (Sample II).



Source: The author

5.15 Performance Summary and Comparison with Related Works

Table 19 summarizes the measured samples performance, including the output buffers power consumption. The main figure-of-merits (FoMs) are also calculated. The measured performance is lower than the achieved by post-layout simulations at typical corner. Table 20 presents the main parameters of the modulator regarding different design stages. It provides a straightforward insight about performance reduction across the design process.

A comparison with related works are summarized in Table 21 regarding sample II measured results. Only sub-1V silicon-proven inverter-based designs are taken into account in this comparison. It worth mention that the output buffers power consumption is considered in the modulator digital power consumption in this work. The achieved results of this modulator are aligned with recent reporter inverter-based sigma-delta modulators. However, the measured figures of merit are lower than the simulated ones due to the SNDR reduction and high digital power consumption.

Table 19 – Performance summary of the proposed modulator: measurement results at room temperature and post-layout results at 25°.

	Measured (sample II and sample I)			Post-layout
VDD (V)	0.54	0.60	0.66	0.60
peak SNDR (dB)	58.29/64.73	58.68/59.43	62.48/60.30	70.14
peak SNR (dB)	68.48/69.84	70.83/69.04	69.12/69.57	71.58
SFDR (dB)	62.14/66.79	63.87/60.51	64.21/62.30	76.65
DR (dB)	65.20/73.00	76.00/74.20	74.50/68.2	74.5
Power (μW)	55.83/55.93	88.08/89.50	130.21/130.41	93.33
FoM_W (fJ/step)	415.96/198.51	627.42/584.79	598.84/770.88	177.58
FoM_S (dB)	157.73/165.52	166.55/164.68	163.35/157.04	164.80
FoM_{SNDR} (dB)	150.82/157.25	149.23/149.91	151.33/149.14	160.43

Table 20 – Parameters degradation in the CT-SDM design flow (32k-point FFT).

CT-SDM design phase	peak SNR/SNDR (dB)	DR (dB)
Ideal model with ELD compensation	85.54/83.53	≈88
Schematic-level simulation	75.90/75.28	85
Post-layout simulation	71.58/70.14	74.50
Measurement results (sample II)	69.04/59.43	74.20

5.16 Summary

This Chapter presented the design and measurement results of a 0.6-V third-order inverter-based CT-SDM using only two amplifiers. It was achieved by using a single-amplifier resonator in the loop filter and a power-efficient structure to implement the feed forward coefficients and quantization. The loop-filter amplifiers are single-stage inverter-based amplifiers with gain enhancement through negative resistance. Furthermore, on-chip body bias is used to compensate PVT variations and to provide output common-mode control. The resonator transfer function was implemented by a single-amplifier biquad employing the proposed compensation technique for low-gain amplifiers ($\leq$ 40 dB). It provides a resonator transfer function similar to the one achieved by using amplifiers with 80 dB of DC gain. The inverter-based modulator was fabricated in a 130 nm triple-well CMOS process and presents a peak SNDR/SNR of 59.43/69.04 dB and a DR of 74.2 dB for a signal bandwidth of 100 kHz while consuming 89.50 μW. To the author's best knowledge, the presented circuit is one of the first low-voltage silicon-proven CT-SDM with inverter-based amplifiers operating at 0.6 V. Also, the use of a SAB resonator in the loop filter is explored in the context of low-voltage CT-SDMs.

Table 21 – Performance comparison with sub-1V SDMs with inverter-based amplifiers reported until the first quarter of 2018.

Parameters	This work - CT-SDM I (sample 1/sample 2) Measurement results at room temperature			[1] JSSC'13	[2] JSSC'09	[3] TCASII'17	[4] ESSCIRC'09	[5] ESSCIRC'14
Type	CT	CT	CT	DT	DT	DT	DT	DT
CMOS (nm)	130	130	130	65	180	65	180	130
VDD (V)	0.54	0.60	0.66	0.7	0.7	0.5	0.5	0.25
Fs (MHz)	10	10	10	5	4	2	10	1.28
BW (kHz)	100	100	100	20	20	20	78	10
peak SNR (dB)	68.48/69.84	70.83/69.04	69.12/69.57	92	84	65.3	N/A	73.7
peak SNDR (dB)	58.29/64.73	58.68/59.43	62.48/60.30	89	81	60.8	71	73.3
SFDR (dB)	62.14/66.79	63.87/60.51	64.21/62.30	N/A	N/A	N/A	N/A	85
DR (dB)	65.20/73.00	76.00/74.20	74.50/68.2	94	85	70.1	N/A	77
Power (μW)	55.83/55.93	88.08/89.50	130.21/130.41	152	36	43.4	860	35.6
FoM_W (fJ/step)	415.96/198.51	627.42/584.79	598.84/770.88	164.95	98	1210	1.900	471
FoM_S (dB)	157.73/165.52	166.55/164.68	163.35/157.04	175	172.44	156.73	N/A	161.49
FoM_{SNDR} (dB)	150.82/157.25	149.23/149.91	151.33/149.14	169.91	168.44	147.43	150.57	157.78

[1] - (LUO *et al.*, 2013) - *IEEE Journal of Solid State Circuits*.
[2] - (CHAE; HAN, 2009) - *IEEE Journal of Solid State Circuits*.
[3] - (PARK; HWANG; JEONG, 2017) - *IEEE Transactions on Circuits and Systems II: Express Briefs*.
[4] - (WANG; MATSUOKA; TANIGUCHI, 2009) - *IEEE European Solid State Circuits Conference (ESSCIRC)*.
[5] - (QIAO; ZHOU; LI, 2014) - *IEEE European Solid State Circuits Conference (ESSCIRC)*.

6 A LOW-VOLTAGE CONTINUOUS-TIME SIGMA-DELTA MODULATOR WITH AMPLIFIER ASSISTANCE

This Chapter presents an improved PVT compensated inverter-based OTA for low-voltage CT sigma-delta modulators that significantly reduces the GBW variation across PVT corners. The effectiveness of the proposed circuit was initially verified in a 180-nm CMOS process by transistor-level simulations including PVT variations and mismatch. A 0.6-V third-order CT-SDM designed at schematic level confirms the robustness of the proposed OTA against voltage and temperature variations. Later on, the same amplifier operates at a supply voltage as low as 0.45 V, and an amplifier assistance technique is used in the first integrator amplifier to enable the implementation of a power-efficient 50-kHz BW CT-SDM. This modulator was fabricated in a TSMC 180-nm process, and experimental measurement results are given to support the design approach.

6.1 Inverter-Based OTA with Reduced GBW Variation

The loop-filter amplifiers mainly determine the power efficiency of sigma-delta modulators. These amplifiers have a GBW specification that should be achieved across PVT, and usually, its design is oversized as a safety margin. It is known that inverter-based OTAs are susceptible to PVT variations that affect the inverter trip point and impacts the DC gain, GBW and output swing of the inverter if no PVT compensation strategy is used (HARJANI; PALANI, 2015).

The variation of amplifiers' GBW values across supply voltage and temperature variations can significantly reduce the modulator SNDR (HE; PUN; KINGET, 2009). Chapter 3 presented the main strategies reported in the literature to control the bias point of CMOS the inverters. Among them, it is worth highlighting the ones introduced in (LUO *et al.*, 2013), (LV; LI, 2015) and (ISMAIL; MOSTAFA, 2016). Also, Chapter 5 presented a 0.6-V CT-SDM with single-stage inverter-based OTAs in which the operating point is controlled by a CMFB loop that changes the bulk voltage shared by PMOS and NMOS transistors.

However, no mitigation strategy to reduce GBW variations are addressed in (LV; LI,

2015), (ISMAIL; MOSTAFA, 2016) and in the previously proposed OTA already published in (DE AGUIRRE; SUSIN, 2018). The reduction of GBW variation proposed in (CHRISTEN, 2013) is accomplished by changing the inverters supply voltage at the cost of a voltage regulator while in (LUO *et al.*, 2013) the proposed bulk bias technique provides a GBW reduction of the cascode inverter from 54% to 11% for the slow process corner at the typical 0.6-V power supply.

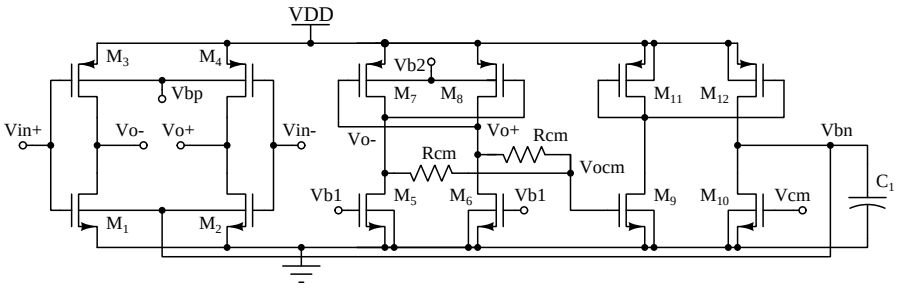
To overcome the aforementioned drawbacks, a PVT compensated low-voltage inverter-based OTA with reduced GBW variation for power-efficient low-voltage CT-SDMs is addressed here. It uses an auxiliary circuit to generate the bulk voltage of the PMOS transistors of the inverters to mitigate PVT variations. Also, the control of the output common-mode voltage is performed by controlling the bulk voltage of NMOS transistors, providing a GBW variation of only $\pm 3.9\%$ across process and temperature corners at typical power supply.

6.1.1 Proposed PVT Compensated Inverter-Based OTA Topology

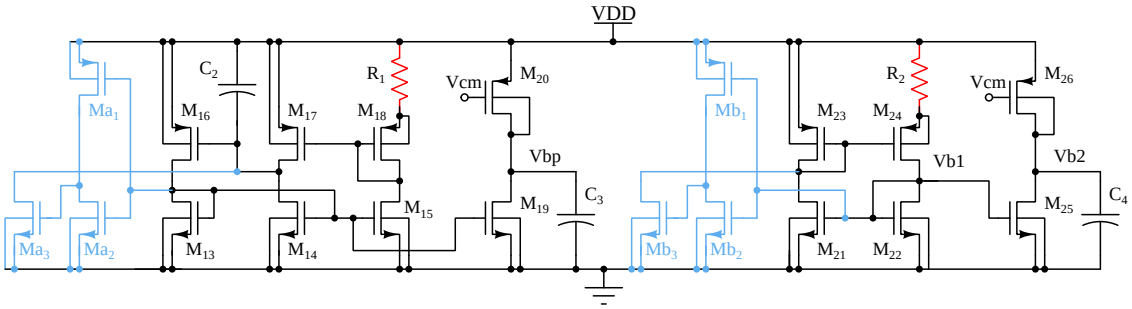
The proposed inverter-based OTA is shown in Figure 90. The main amplifier is composed of transistors M_{1-4}. These transistors are sized to operate in saturation and in weak or moderate inversion region according to the required trade-off of transconductance and speed. The cross-coupled pair composed of transistors M_7 and M_8 are connected to the main amplifier output to provide a negative conductance of $-gm_7$ for gain enhancement. The input common-mode voltage *vcm* is equal to VDD/2 and the output common-mode voltage is controlled by changing the bulk voltage of transistors M_1 and M_2. The CMFB circuit is composed of resistors Rcm to sense the output common-mode voltage, *vocm*, and a pseudo-differential error amplifier composed of transistors M_{9-12}. The error amplifier compares the *vocm* voltage with *vcm* and generates the *vbn* voltage to set the bulk voltage of transistors M_1 and M_2. At typical corner *vbn* is designed to be equal to VDD/2 and thus increases the control range. Also, a small capacitor C_1 may be used to filter high-frequency components or for frequency compensation of the CMFB loop.

To reduce the GBW variation across PVT corners the bulk voltage *vbp* is generated by an auxiliary biasing circuit as follows: transistor M_{19} works as a current source and transistor M_{20} has the same channel length (L) as M_{3-4} and a channel width (W) N times smaller. The gate terminal of M_{20} is connected to *vcm* and its bulk terminal is connected at its drain in a diode connection fashion generating the voltage *vbp* that is applied to bulk terminal of the main amplifier PMOS transistors. M_{19} is biased by the constant Gm proportional to absolute temperature (PTAT) current source, composed of transistors M_{13-18} and the off-chip resistor R_1. Thus, the bias current increases with temperature reducing transconductance variations since in weak-inversion $gm = I_D/nU_T$, where U_T is the thermal voltage. This PTAT current source presents low supply voltage sensibility and capability of low-voltage operation, providing better current stability at low supply

Figure 90 – Schematic diagram of the proposed pseudo-differential inverter-based OTA.



(a) Main Amplifier and CMFB circuitry



(b) Bias circuitry

Source: The author

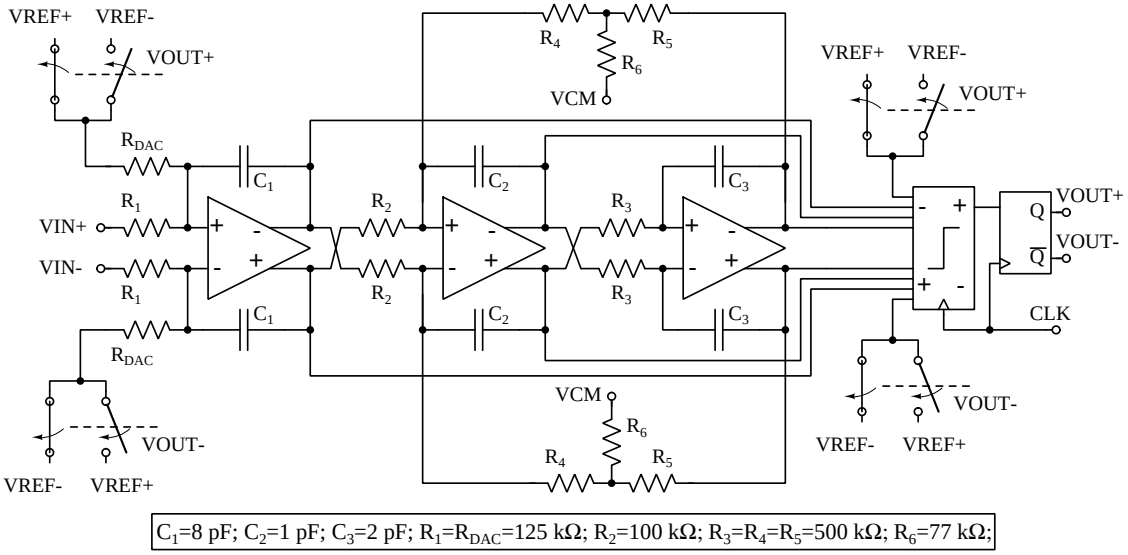
voltages than the traditional beta-multiplier current source. However, it requires the small capacitor C_2 for stability purposes (NAUTA; NORDHOLT, 1985).

The transconductance variation of transistors M_7 and M_8 is mitigated by biasing the current sources M_5 and M_6 with the beta multiplier current reference composed of transistors M_{21-24} and the off-chip resistor R_2. Also, the bulk voltage of transistors M_7 and M_8, vb2, are generated by the auxiliary circuit composed of M_{25} and M_{26}. Finally, transistors M_{a1-a3} and M_{b1-b3} compose the startup circuit of each current reference, and small capacitors C_3 and C_4 may be used to attenuate high-frequency switching components from the modulator.

6.2 Validation of the Proposed Amplifier

The proposed inverter-based OTA topology was used to the design a 0.6-V third-order, single-bit CT-SDM in a 180-nm tripple-well CMOS process with a signal bandwidth of 100 kHz. This CT-SDM topology is identical to the one already presented in section 5.2. It is implemented with an ELD compensated cascade of integrators feed-forward topology with the weighted quantizer introduced in (ZHANG *et al.*, 2011) and the resonator feedback resistor is designed with a T network resistor. The modulator simplified schematic diagram is shown in Figure 91. More details of the electric implementation of this modulator are given in section 6.4.

Figure 91 – Schematic of the CT-SDM used to validate the proposed OTA.



Source: The author

6.2.1 OTA Simulation Results

To verify the effectiveness of the proposed OTA, the results of PVT corners as well as Monte Carlo transistor-level simulations of the OTA of the first integrator are herein provided since it limits the modulator in-band noise. This OTA was designed to provide a GBW of only 1.5× the modulator sampling frequency (10 MHz), taking into account a load of 100 kΩ||8pF. The common-mode input voltage of the inverters is 0.3 V, the bias current of each inverter is set to 20 µA and the current reference is 2 µA at nominal conditions. The inverter transistors length is set to 1.0 µm in order to provide a good trade-off between intrinsic gain and reverse short channel effects. The negative conductance cell presents a transconductance of $gm_{7,8} = 12$ µS at typical corner, providing margin that $gm_{7,8}$ is lower than the total output conductance across PVT variations. Thus, the OTA DC gain is increased from 33.7 dB to 41.9 dB. All transistors of the OTA are medium-V_T devices ($V_T \approx$ 200mV) with exception of M_{1-4} and M_{20} that are standard V_T transistors ($V_T \approx$ 400 mV) operating in the border between weak and moderate inversion with a $gm/I_D = 24$. The aspect ratio of the transistors of the inverters in [µm/µm] are $(W/L)_{1,2} = 10 \times (27.42/1.00)$ and $(W/L)_{3,4} = 10 \times (68.58/1.00)$.

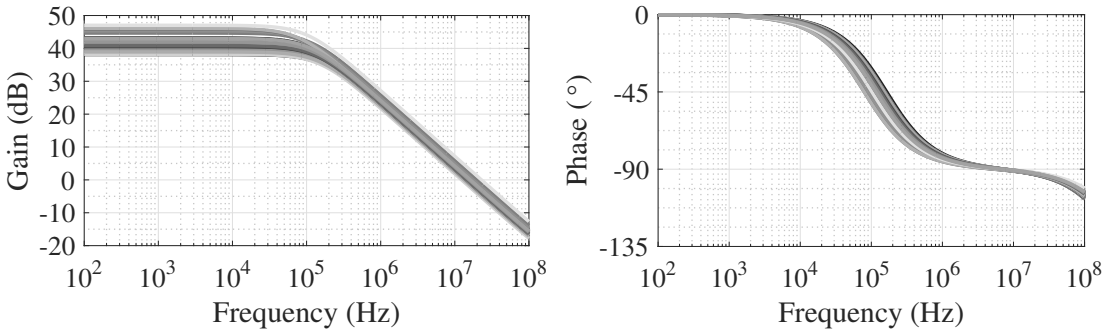
The simulated OTA performance is summarized in Table 22. The designed OTA achieves a DC gain of 41.93 dB and a GBW of 15.55 MHz and the total current consumption, including the biasing circuitry, is 52 µA. The frequency response across process (TT, FF, SS, FS, SF), voltage (0.54 V, 0.60 V and 0.66 V) and temperature (0 °C, 25 °C and 85 °C) corners is shown in Figure 92. The GBW variation is ±5.4% for power supply variations of ±10% at typical process corner and only ±3.9% across process and temperature at nominal power supply. The minimum GBW is 12.35 MHz, a reduction

of 20.6% across all PVT corners and the DC gain variation is due to the variation of the conductance $-gm_7$.

Table 22 – Simulated performance of the proposed OTA at typical corner.

VDD (V)	0.54	0.60			0.66
Temperature (°C)	25	0	25	85	25
DC Gain (dB)	40.85	42.14	41.93	41.23	43.00
GBW (MHz)	14.72	15.28	15.55	15.91	16.20
PM (degrees)	88.48	88.05	88.06	88.09	88.00
CMRR @ DC (dB)	55.39	62.36	61.67	57.61	62.34
PSRR+ @DC (dB)	60.90	65.87	65.27	59.80	65.11
PSRR- @DC (dB)	62.99	69.07	68.87	63.04	68.90
Static Current (µA)	49.32	47.86	52.04	61.95	54.98

Figure 92 – AC open-loop results of the proposed OTA across PVT corners.

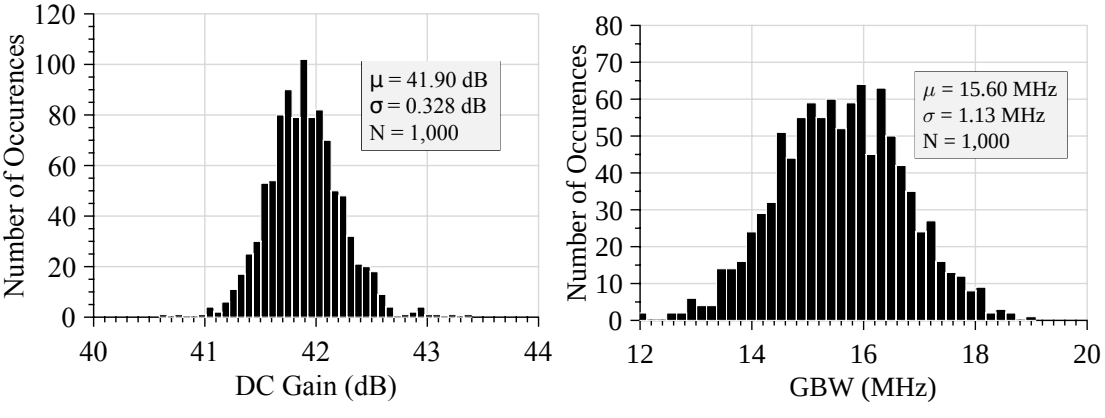


(a) Open-loop gain (b) Phase Margin

Source: The author

Monte Carlo simulation including process and mismatch variations for 1,000 samples was carried out and the histogram for DC gain and GBW are shown in Figure 93.

Figure 93 – Monte Carlo simulation results (process+mismatch) at VDD=0.6 V and T=25°C.



(a) DC gain (b) GBW

Source: The author

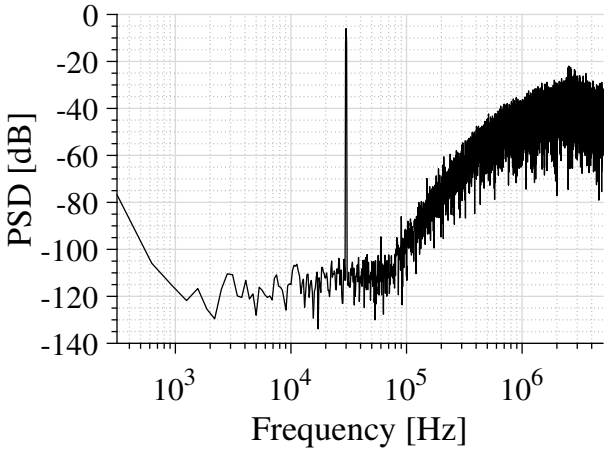
The DC gain is well defined and in all cases is higher than 40 dB while the minimum GBW, taking into account a 3σ range, is 12.21 MHz.

Since the non-idealities of the second and third OTAs are noise-shaped, their requirements are relaxed. The second OTA is implemented with a scaled-down bias current of 5x and a negative conductance at its output of 4 µS due to different loading. The second and third OTAs are equal due to the reduced specification of the third OTA GBW.

6.2.2 CT-SDMs Simulation Results

The total power consumption of the designed modulator is 48.65 µW and it achieves an SNDR of 73.66 dB under nominal conditions for a 30-kHz input signal with amplitude of -6.02 dBFS (300 mVpp), leading to an FoM_W of 61.75 fJ/conv. The output power spectrum density is shown in Figure 94. At supply voltages of 0.54 V and 0.66 V the SNDR is 71.57 dB and 73.85 dB, respectively.

Figure 94 – Output PSD at nominal conditions.



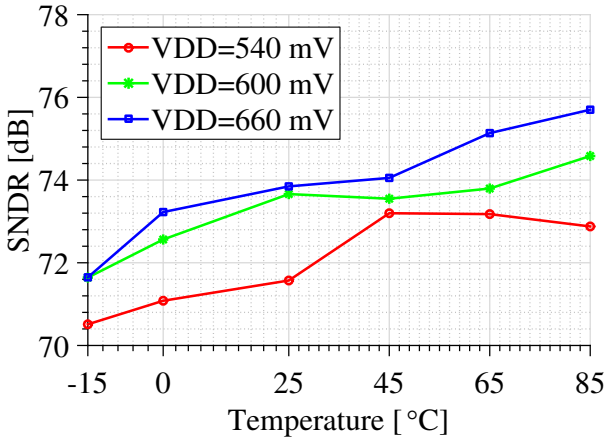
Source: The author

The impact of temperature at different supply voltages in the SNDR is also evaluated at typical corner, as shown in Figure 95. One can observe a small linear SNDR dependence on temperature and a small dependence on VDD due to the reduced variation of the GBW of the proposed inverter-based OTA. The minimum SNDR is 70.51 dB and an SNDR variation of 2.93 dB across temperature is verified at nominal supply voltage while other low-voltage CT-SDM presents an SNDR variation of up to 17.6 dB due to the amplifiers GBW variation (HE; PUN; KINGET, 2009). Also, the maximum SNDR variation is 5.19 dB considering voltage and temperature variations.

6.3 CT-SDM with Assisted Integrator

It was verified by simulation that the proposed amplifier can operate with supply voltages as low as 500 mV, and so thus the modulator loop-filter. However, if the amplifier supply voltage is reduced below 500 mV, there is a significant reduction of the GBW

Figure 95 – SNDR versus temperature at different VDD.



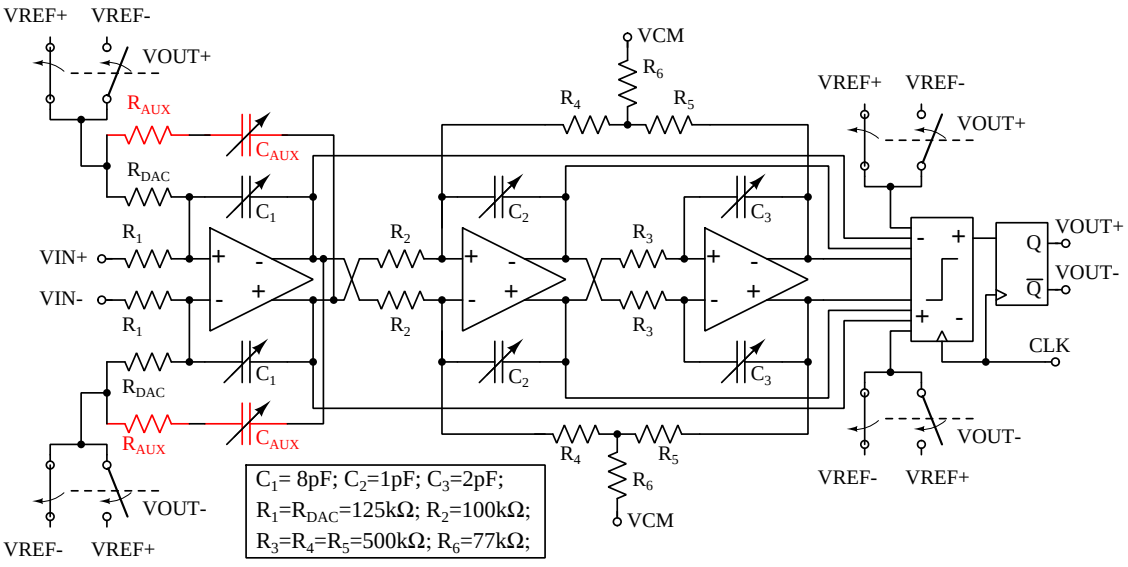
Source: The author

and the DC gain starts decreasing. Thus, this works adopts a passive integrator assistance technique to compensate the first amplifier GBW reduction and enable the modulator loop filter operation at supply voltages of 500 mV and below.

6.4 Circuit-Level Implementation

Figure 96 depicts the proposed schematic-level CT-SDM with the passive integrator assistant path highlighted in red. This modulator is based on the same one used to validate the proposed amplifier. Thus, along with the inclusion of the integrator assistance, the modulator BW was reduced to 50 kHz (oversampling increased to 100) since the loop-filter zero effect start decreasing at supply voltages below 500 mV.

Figure 96 – Schematic diagram of the fabricated low-voltage assisted CT-SDM.

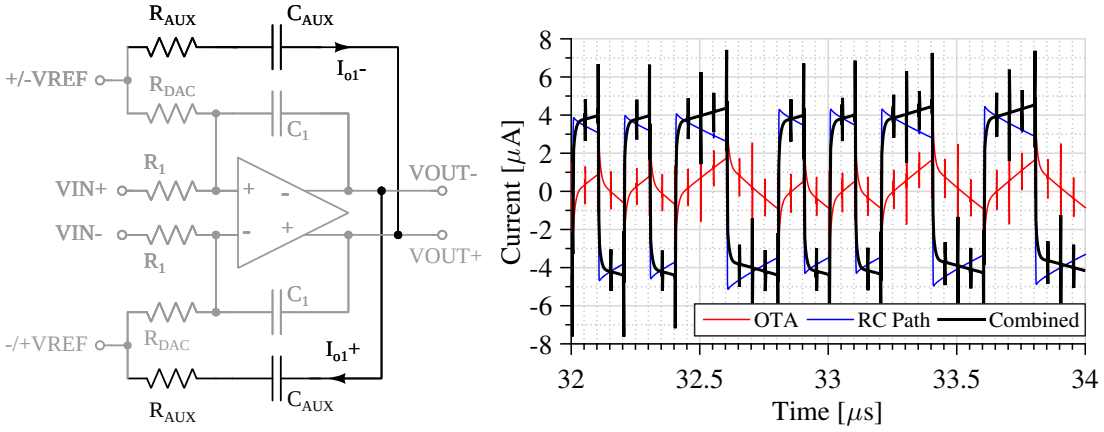


Source: The author

6.4.1 Amplifier Assistance and Thermal Noise

Single-bit NRZ DACs are a good choice to design low-voltage CT-SDMs. However, the sharp transitions of the DAC signal impacts in the first integrator linearity since the first integrator amplifier should source and sink pulsed currents due to the DAC feedback. If the amplifier is not able to source or sink such pulsed currents, virtual ground disturbances occurs leading to a nonlinear behavior that degrades the modulator SNDR. Different design strategies to smooth the DAC output signal or to source and sink part of the integrator total output current are presented in the literature as the assisted amplifier technique (PAVAN; SANKAR, 2010), the use of passive filters in the feedback path (LI *et al.*, 2018) or the use of finite-impulse response (FIR) DACs (LV *et al.*, 2018). In this work, the amplifier of the first integrator was assisted by a passive RC path introduced in (ZELLER *et al.*, 2014) and already approached in section 3.4.0.1. However, the assistant RC path is connected at the DAC feedback input, as depicted in Figure 97 (a). This extra path provides the high-frequency current components to the integrator output, diminishing the amplifier speed requirements. Figure 97 (b) shows the first OTA output current, the RC path current and the combined integrator current obtained by a schematic-level simulation of the proposed modulator. It improves the integrator linearity and lowers the unity-gain bandwidth and slew-rate requirements of the first amplifier at the cost of an area overhead since the capacitor C_{AUX} is equal to the first integrator capacitor.

Figure 97 – Differential active-RC integrator with assistant RC path.



(a) Assisted Integrator (b) Differential Current

Source: The author

The modulator total input-referred noise $\bar{v}_{ir}^2$ is basically unchanged after adding the assistant RC path. It is defined by the following expression (ZHANG *et al.*, 2011).

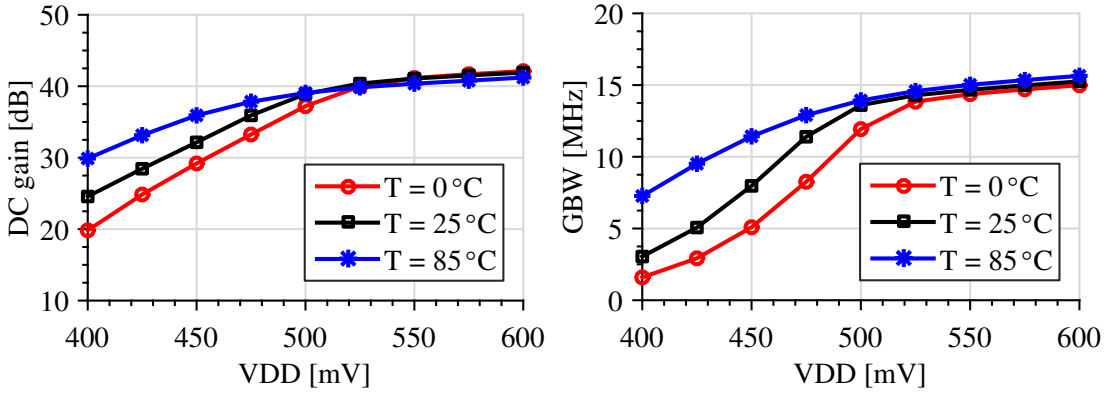
$$\bar{v}_{ir}^2 \approx 2 \times (\bar{v}_{R_{in}}^2 + \bar{v}_{DAC}^2) + 4 \times \bar{v}_{in-OTA}^2 \ [V^2/Hz] \tag{60}$$

Where $\bar{v}_{R_{in}}^2$ and $\bar{v}_{DAC}^2$ are the noise from input and DAC resistors, respectively, and $\bar{v}_{in-OTA}^2$ is the input-referred noise of the first OTA.

6.4.2 Loop-Filter Amplifiers

The amplifier of the first integrator was designed to provide a GBW higher than Fs and a DC gain near to 40 dB when the amplifier is operated at 0.5 V. Monte Carlo simulations (1,000 runs) of the amplifier extracted layout indicates an average DC gain of 38.53 dB and a standard deviation (σ) of 1.50 dB while the average GBW is 13.54 MHz with σ of 945 kHz. Figure 98 presents the post-layout simulation results of the amplifier DC gain and GBW across VDD variations for different temperatures. For supply voltages lower than 500 mV it is verified a significant reduction of the amplifier DC gain and GBW. The CMFB control range reduces with VDD affecting the control of *vocm* that starts increasing since the *vbn* voltage goes near VDD. Thus, the inverters start operating away from the maximum DC gain region since the input common-mode voltage is equal to VDD/2. However, the GBW reduction is compensated by the assistant RC path in the first integrator as aforementioned. According to transient-noise post-layout simulations, the first OTA with DC gain around 30 dB and a GBW equal to Fs ensures an SNDR of 74 dB at 0.5 V. The second and third amplifiers are identical but properly scaled to save power. It includes the main amplifier bias scaling as well as the negative conductance scaling to avoid loop instability.

Figure 98 – Post-layout simulated amplifier DC gain and GBW as a function of VDD and temperature.



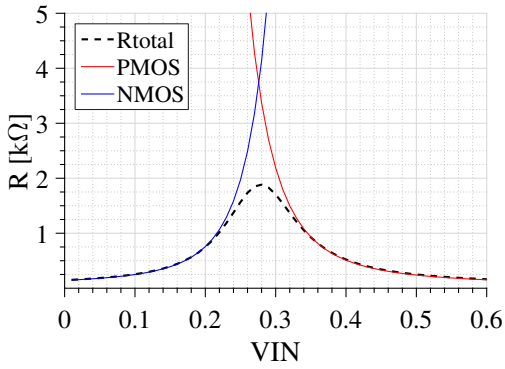
(a) DC gain versus VDD (b) GBW versus VDD

Source: The author

6.4.3 NRZ DAC Circuit Implementation

The NRZ DAC was designed with resistors and transmission gates implemented with medium-V_T devices. The size of the transmission gate transistors were defined in order to provide a good trade-off between resistance and turn on/off time. The transmission gate transistors size are: NMOS = 5×4.00 µm/0.30 µm and PMOS = 5×10.00 µm/0.25 µm. Figure 99 presents the NRZ DAC switch on resistance.

Figure 99 – NRZ DAC switches resistance.

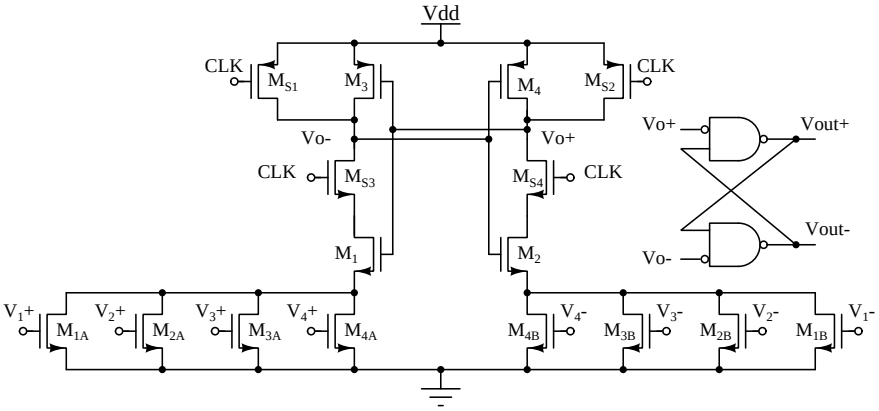


Source: The author

6.4.4 Feed-Forward Coefficients Summation and Quantization

This design used a four-input weighted quantizer according to the topology used in the first CT-SDM prototype. The quantizer schematic is shown in Figure 100.

Figure 100 – Four-Input Weighted Quantizer.



Source: The author

The feed-forward coefficients a_x are implemented by sizing the low-V_T input transistors width according to Equation 61. All other transistors are medium-V_T devices. Table 23 presents the quantizer transistors size.

$$a_1 : a_2 : a_3 : a4 \rightarrow 7.97 : 2.72 : 5.60 : 0.3657 \rightarrow W_1 : W_2 : W_3 : W_4 \tag{61}$$

6.4.5 Tunable Capacitor Array

The RC constant of active-RC integrators is susceptible to process variations and usually a RC tuning scheme is employed to cope with these variations. The RC time constant is implemented with high-resistance poly resistor with 1037 $\Omega/\square$ and MiM capacitors. Monte Carlo simulations (1,000 runs) indicate a resistor standard deviation of 3.7% while the capacitors standard deviation is 5%. Based on these results, non-correlated and cor-

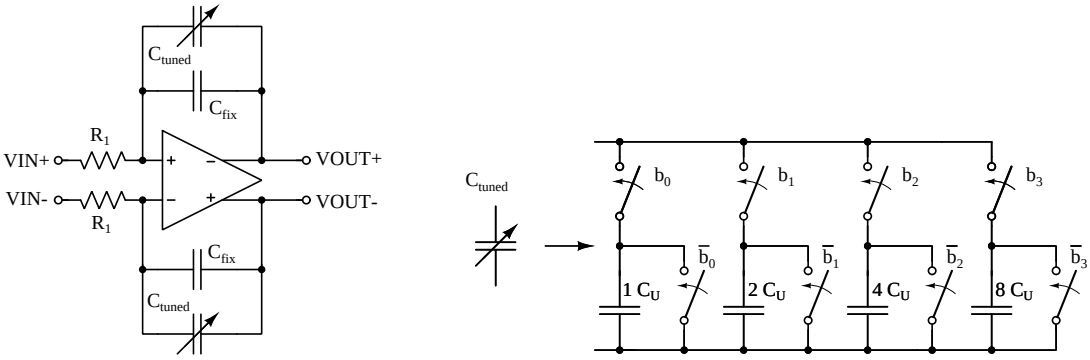
Table 23 – Transistors size of the four-weighted input quantizer.

Transistors	W/L (µm/µm)
M_{S1}, M_{S2}	$1\times$ 4.00/0.25
M_{S3}, M_{S4}	$1\times$ 6.00/0.30
M_1, M_2	$1\times$ 8.40/0.30
M_3, M_4	$1\times$ 6.00/0.30
M_{1A}, M_{1B}	$2\times$ 2.00/0.50
M_{2A}, M_{2B}	$31\times$ 2.00/0.50
M_{3A}, M_{3B}	$15\times$ 2.00/0.50
M_{4A}, M_{4B}	$44\times$ 2.00/0.50

related statistical analysis were carried out providing a RC time constant variation, in the 3σ range, of 18.93% and 25.08%, respectively. Thus, a RC tuning is required.

The RC tuning could be performed by using resistor (ZHANG *et al.*, 2011) (LV *et al.*, 2019) or capacitor arrays (BREEMS *et al.*, 2016). In this work, all capacitors (C_{AUX}, C_1, C_2 and C_3) are implemented with a fixed capacitor (C_{fix}) in parallel with a 4-bit binary-weighted capacitor array to provide RC time-constant tuning, as depicted in Figure 101.

Figure 101 – Digitally reconfigurable active-RC integrator.



(a) Active-RC integrator. (b) 4-bit reconfigurable capacitor bank.

Source: The author

The capacitance tuning step is defined by the unitary capacitor C_U. The capacitor C_{fix} is composed of 17 unitary capacitors C_U and its capacitance is around 70% of the nominal integrating capacitance. The values of C_U and C_{fix} were chosen such that $C_{fix} + 8 \times C_U$ equals the nominal capacitance.

The capacitor array tuning range is calculated by Equation 62 while the tuning accuracy is provided by Equation 63.

$$\text{Tuning range} = \frac{C_{MAX}}{C_{MIN}} = \frac{C_{fix} + 15 \times C_U}{C_{fix}} = 1.88 \tag{62}$$

$$\text{Tuning accuracy} = \frac{C_U}{C_{fix} + 8 \times C_U} = \frac{C_U}{17 \times C_U + 8 \times C_U} = 4\% \tag{63}$$

It should be noted that during layout design, the unused spaces were filled with dummy cells for better matching as shown in Figure 102.

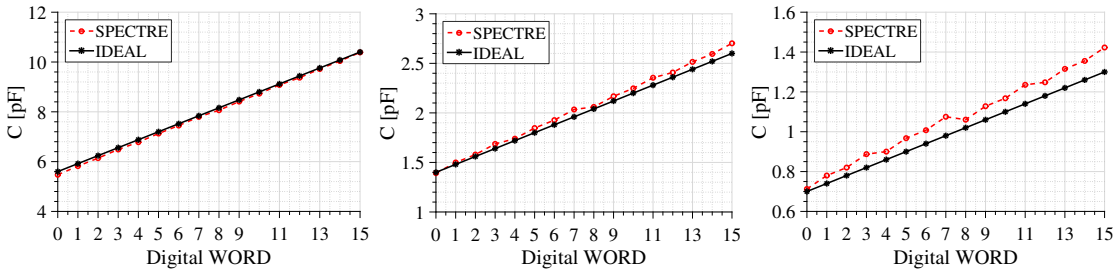
Figure 102 – Tunable capacitor layout.

Source: The author

The non-used array capacitors are shorted to avoid floating nodes and undesired effects. All switches in the capacitor bank are transmission gates composed of medium-V_T transistors. The same switches are used in all capacitor banks. The sizing of the transmission gate transistors was performed to provide a linear tuning range for the first integrator capacitor, taking into account the series resistance and series capacitance. The transistors size are: NMOS = 2.50 µm/0.25 µm and PMOS = 3.0 µm/0.3 µm.

Figure 103 presents the ideal and simulated capacitance value of the capacitor bank versus the 4-bit digital control word.

Figure 103 – Tunable capacitance versus the 4-bit digital word.



(a) 1st Int. capacitor (b) 2nd Int. capacitor (c) 3rd Int. capacitor

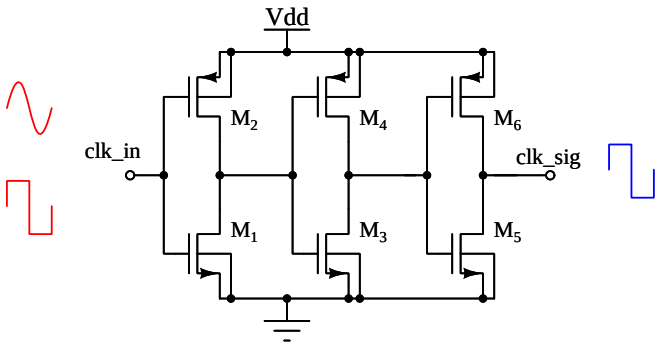
Source: The author

6.4.6 Clock Circuit and Output Buffers

The clock signal applied at the modulator input passes through buffer composed of a chain of three inverters to provide sharp rise and fall transitions. The clock buffer schematic is shown in Figure 104. The inverters are designed with medium-V_T devices and the sizing was performed taking into account a 2.5× factor. The transistors are designed with the minimum length of 0.3 µm while the width of M_1 and M_2 are equal to 2.4 µm and 4.0 µm, respectively. Electric simulations indicate that the buffered clock signal

presents sharp rise and fall transitions for both sinusoidal or square-wave external clock signals.

Figure 104 – Clock buffer.



Source: The author

The CT-SDM digital output passes through a 4-stage CMOS inverter chain designed to drive the parasitic capacitance (package, routing and EVB capacitances) and measurement probes. A capacitive load of 25 pF was considered during the output buffer design.

6.5 Layout

The complete layout of the proposed CT-SDM is depicted in Figure 105. Dedicated power pins to supply the digital circuitry and output buffers were included in the final chip enabling the measurement of the digital circuitry power consumption for accurate FoM comparison. The analog ground (0 V) is shared with the digital circuitry and output buffers due to the IC limited number of pins.

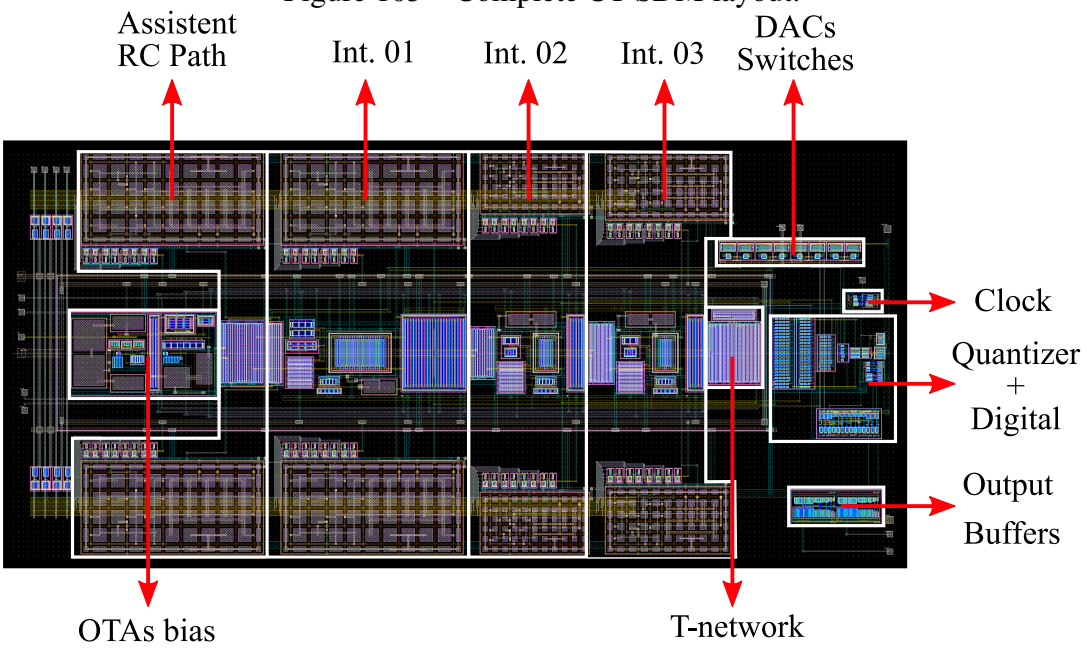
The loop-filter amplifiers and their bias circuit have been placed in the middle of the layout and are surrounded by a N-type guard ring. The integration capacitors are placed on top and bottom providing a complete symmetric path while the input resistor of the integrators are place in between each loop-filter amplifier. The clock generator, quantizer and DAC switches are placed in the right side, after the loop filter, and the output buffers are placed in the bottom right, apart the modulator loop filter.

6.6 Post-Layout Simulation Results

This section presents the post-layout simulation results of the modulator extracted layout (RCC extraction). These simulations are time consuming and were carried out with the *Spectre* simulator in conservative mode with the APS++ option selected. The output PSDs shown in this Section are calculated with a 32k-points FFT. In these simulations, the modulator digital power supply is set to 0.6 V..

Initially, the loop-filter supply voltage was set to 0.5 V. The circuit was simulated with a 15-kHz input signal with amplitude of -6.02 dBFS (250 mV) and transient simulations

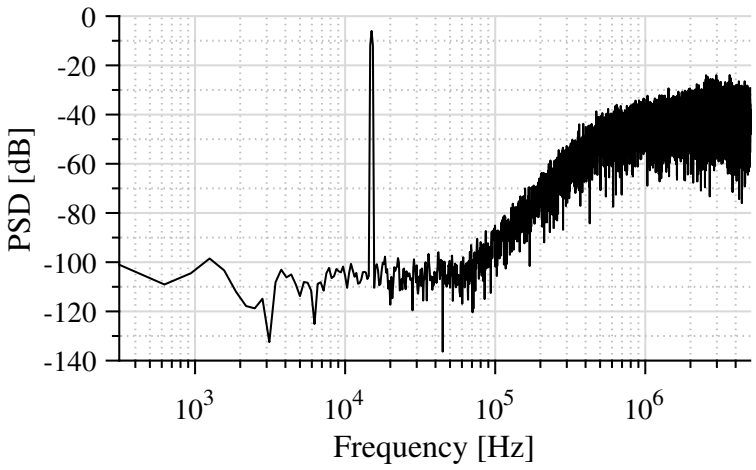
Figure 105 – Complete CT-SDM layout.



Source: The author

with and without noise were performed. When noise is not considered, the achieved SNR/SNDR is 84.45/80.70 dB, while the ideal SQNR for a -6.02 dBFS input signal is 87.15 dB. When noise is considered (transient-noise simulation available in Spectre), the SNR/SNDR drops for 78.11/77.98 dB. Figure 106 presents the modulator output PSD for a transient-noise simulation where a SFDR of -90 dB is achieved since the third-order harmonics of the input signal are below -90 dBFS.

Figure 106 – Output PSD for a 15-kHz input signal with amplitude of -6.02 dBFS: Post-layout simulation with noise.



Source: The author

For loop-filter supply voltages of 450/550 mV, the SNDR is 74.14/82.23 dB without considering noise. For transient-noise simulations, the achieved SNDR is 67.95 dB for a loop-filter supply voltage of 450 mV.

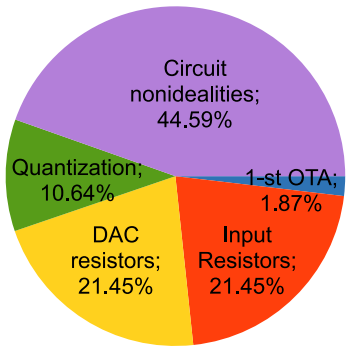
The modulator total power consumption is 31.91 µW. The loop filter draws 63.82 µA from a 0.5-V power supply while the average digital current is 8.72 µA for a 0.6-V power supply. The output buffers draw 105.7 µA for a 25-pF capacitive load, but their power consumption is not taken into account.

Table 24 – Post-layout transient-noise simulation results of the designed modulator for a -6.02 dBFS input signal.

Parameters	Results
Technology (nm)	180
Supply voltage (V)	0.50/0.60
Fs (MHz)	10
BW (kHz)	50
SNR/SNDR (dB)	78.11/77.98
SFDR (dB)	90
ENOB (bits)	12.66
DR (estimated)	83.77 dB
Power (µW)	31.91
FoM_W (fJ/conv.)	49.27

The in-band noise breakdown estimated by transient-noise simulations of the extracted layout is depicted in Figure 107. However, the modulator SNDR is noise limited, and a noise-floor increase of approximately 6 dB was verified in experimental measurements as shown in the next section.

Figure 107 – Estimated in-band noise breakdown of the proposed CT-SDM.



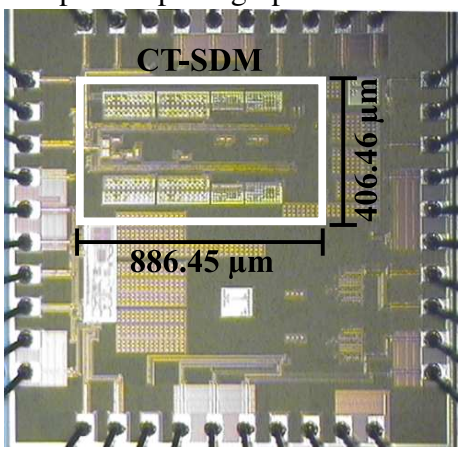
Source: The author

6.7 Measurement Setup

The presented CT-SDM was fabricated in a TSMC 180-nm CMOS process with deep n-well devices. The modulator active area is 0.36 mm^2 and the chip microphotograph is shown in Figure 108.

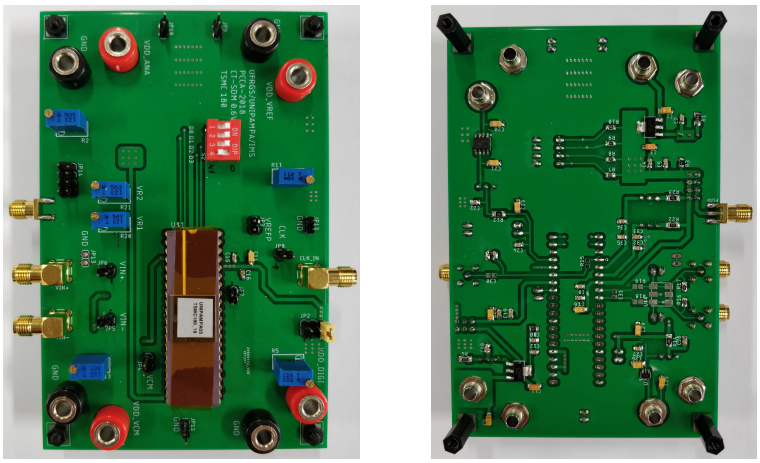
The fabricated IC was assembled in DIP40 package and a two-layer custom-designed EVB, depicted in Figure 109, was used for chip testing. Only one EVB was built and the measured chips were connected to the PCB by a DIP40 socket.

Figure 108 – Chip microphotograph of the second prototype.



Source: The author

Figure 109 – EVB used to characterize the second CT-SDM prototype.



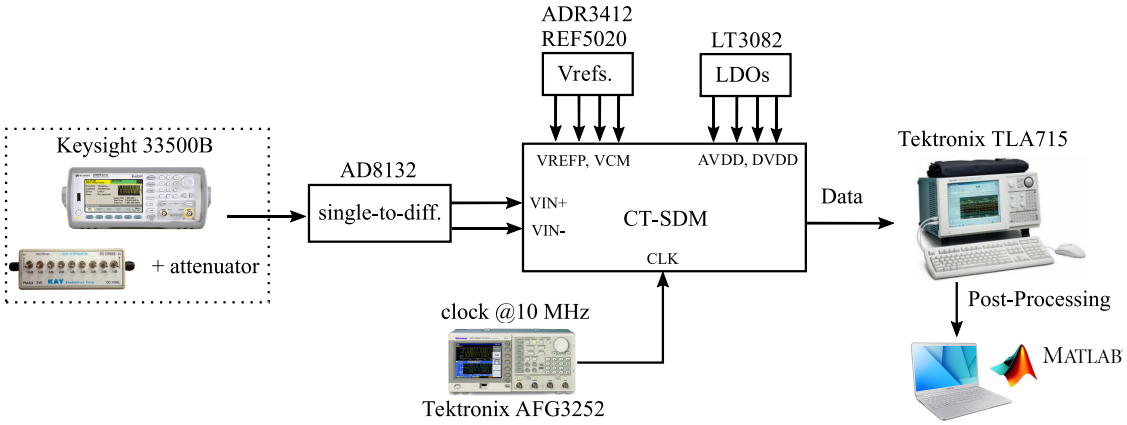
(a) Top. (b) Bottom.

Source: The author

The modulator analog and digital power supplies were generated by two on-board, and individually regulated, LDOs LT3082. Bypass capacitors of 10 µm, 100 nF and 10 nF were used at the regulator output and also as close as possible of the chip power-supply pins to provide clean DC supply voltages. The amplifiers' common-mode voltage of VDD/2 was generated by a high-precision ADR3412 CMOS voltage reference followed by an adjustable resistor divider and a first-order RC filter. The positive reference voltage was generated by a low-noise TI5020 voltage reference followed by an adjustable resistor divider and a first-order RC filter. Also, bypass capacitors of 10 µm, 100 nF and 10 nF are used as close as possible of the chip reference voltage pins.

The measurement of this modulator took place at the Integrated Microsystems Group at Università degli sduty di Pavia. Thus, a different setup was used to characterize this prototype. Figure 110 illustrates the measurement setup diagram while Figure 111 shows the experimental measurement setup.

Figure 110 – Measurement setup diagram of the second CT-SDM prototype.



Source: The author

The clock signal was provided by an AFG3252 signal generator with an RMS jitter of 100 ps. The input signal was generated by a Keysight 33500B waveform generator. A KAY passive attenuator with 20 dB of attenuation was used at the signal generator output to provide input signals with amplitude lower than 10 mV. The single-ended to differential conversion was performed by an auxiliary board with an AD8138 fully-differential amplifier. The modulator power consumption was measured by a Keythley 2000 multimeter (6 1/2 digits). The digital output was captured by a TLA 715 logic analyzer and post-processed on Matlab using a 64k-point FFT.

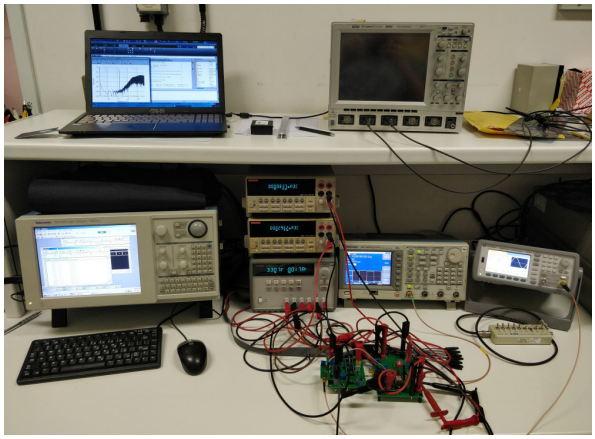
6.8 Measurement Results

This section presents the measurement results of the proposed CT-SDM with amplifier assistance technique. The measurement process was conducted at room temperature and no temperature characterization was performed due to the unavailability of a thermal chamber. Two samples were measured in this work and since both presented very similar results the provided graphics and plots are from sample I.

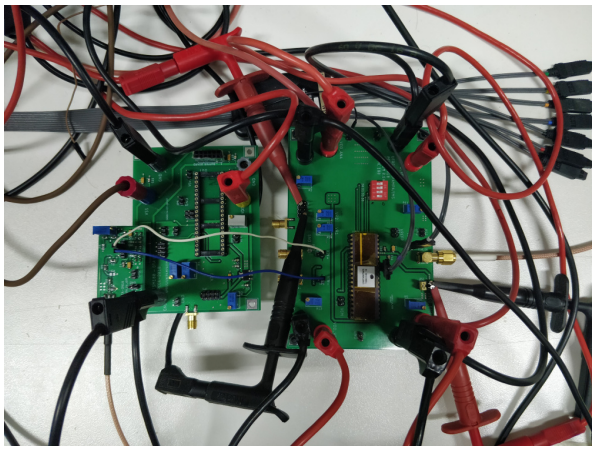
The main characterization was performed using an input signal frequency of 15 kHz in order to include the second-order (HD2) and third-order (HD3) harmonic distortions inside the 50-kHz signal bandwidth. The CT-SDM operates with a clock frequency of 10 MHz and the input clock signal is a square wave with an amplitude of 600 mVp-p and a DC level of 300 mV.

An SNDR reduction was verified for digital supply voltages lower than 600 mV. It probably occurred by a voltage drop in the digital power line inside de chip, or by the increase of the DAC switches resistances since no clock boost technique was used to drive the NRZ DAC switches. Thus, all measured results were carried out for a digital supply voltage of 600 mV.

Figure 111 – Measurement setup of the second CT-SDM prototype.



(a) Measurement setup.



(b) Zoom in the EVB.

Source: The author

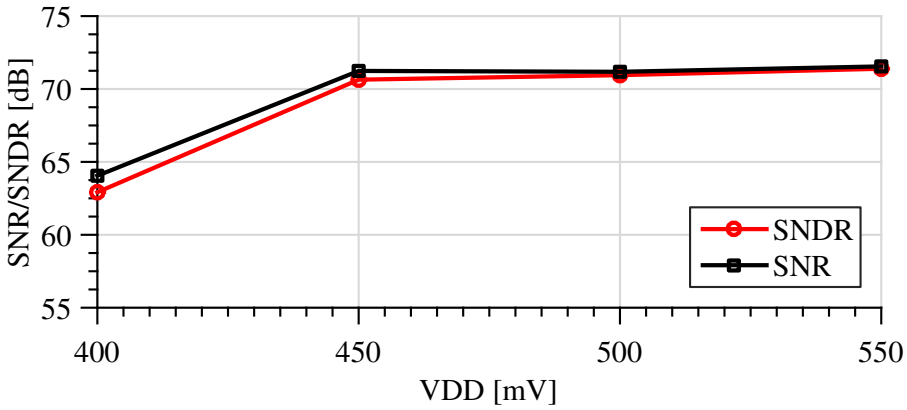
Figure 112 presents modulator peak SNR and SNDR behavior across the analog supply voltage variation. In this analysis the digital supply as well as the off-chip bias resistors are kept constant. If the supply voltage is reduced below 0.45 V the SNDR is reduced mainly due to the proposed amplifier (DC gain reduction) since the transistors threshold voltage is around 400 mV. No SNR/SNDR degradation occurs for supply voltages as high as 550 mV.

The following results considers the modulator loop filter operating with a supply voltage of 0.45 V while the digital supply voltage is 0.60 V. The modulator total power consumption is 28.72 µW, from which 23.98 µW is for the analog part and 4.74 µW is for the digital circuitry according to the estimated power breakdown shown in Figure 113.

Figure 114 shows the measured SNR and SNDR as a function of the 15-kHz input signal amplitude. The measured DR is 78.30 dB.

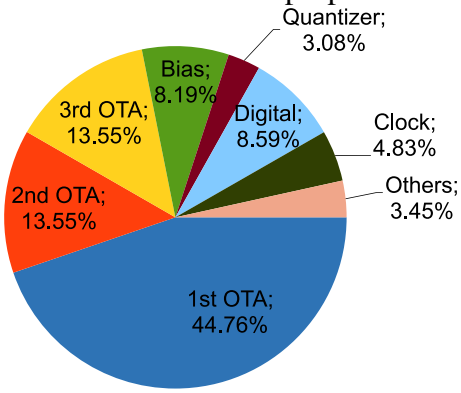
Figure 115 shows the modulator output PSD for a 15-kHz input signal with amplitude of 260 mVp. The measured SNR and SNDR are 71.24 dB and 70.64 dB, respectively. The modulator achieves an SFDR in excess of 80 dB due to its highly linear behavior.

Figure 112 – Measured peak SNR/SNDR versus the loop-filter supply-voltage: Sample I.



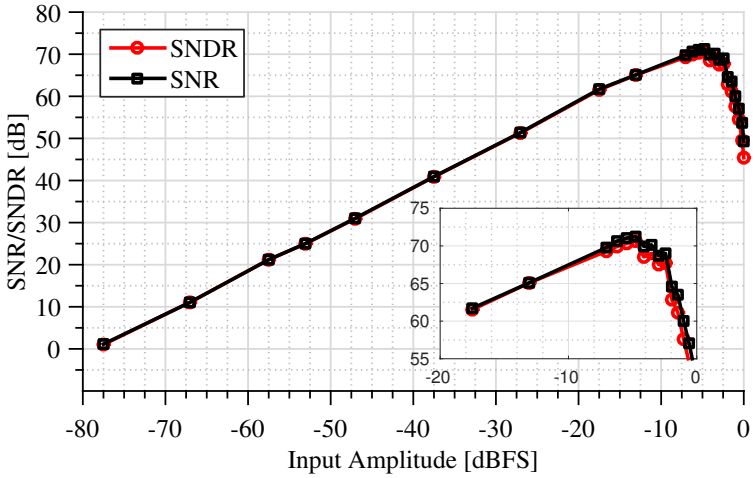
Source: The author

Figure 113 – Power breakdown of the proposed CT-SDM: Sample I.



Source: The author

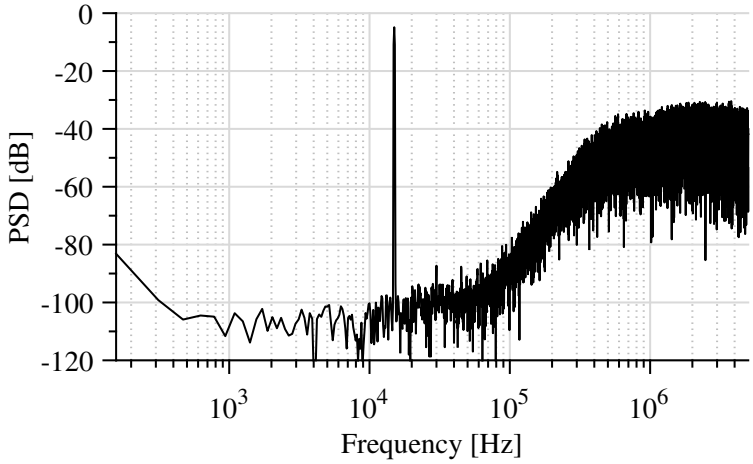
Figure 114 – Measured SNR/SNDR versus the 15-kHz input signal amplitude: Sample I.



Source: The author

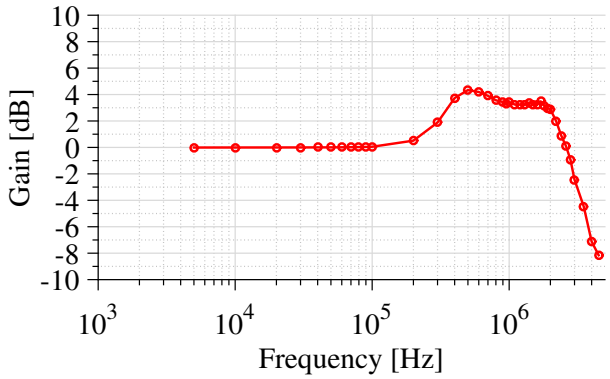
The STF was measured using a -12.04 dBFS input signal and an STF peak of 4.34 dB at 0.5 MHz is verified, as depicted in Figure 116.

Figure 115 – Measured output PSD for -4.76 dbFS 15-kHz input signal: Sample I.



Source: The author

Figure 116 – Measured normalized STF: Sample I.



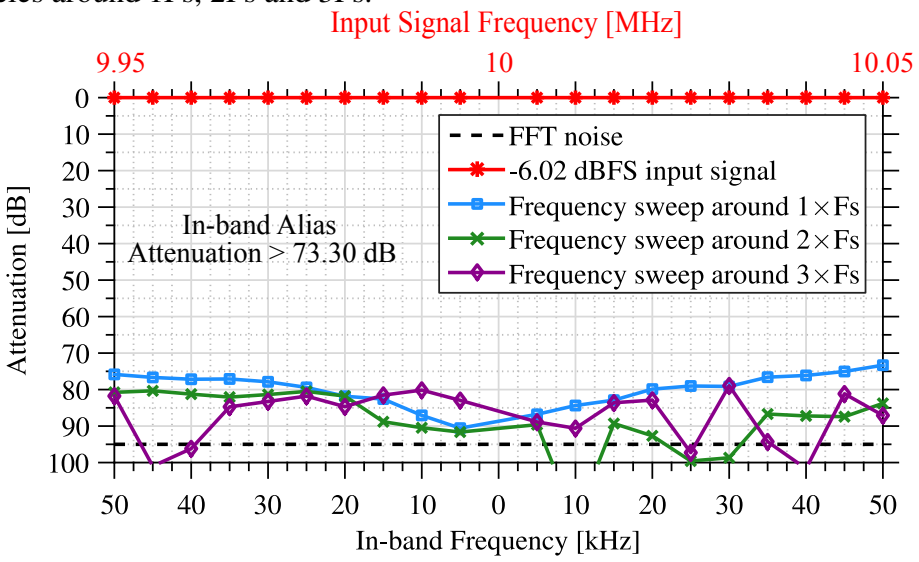
Source: The author

Figure 117 shows the measured inherent in-band anti-alias attenuation for a -6.02-dB_{FS} input signal with frequencies around Fs, 2Fs and 3Fs. An in-band anti-alias attenuation larger than 73.30 dB is achieved. In this analysis, a Tektronix AFG3102 signal generator provided the modulator fully-differential input signal.

The modulator input common-mode rejection ratio was also verified. For this analysis, an HP 3245-A universal source was used to apply equal signals at both modulator inputs. Figure 118 shows the modulator output PSD for a 30-kHz common-mode input signal with amplitude of 25 mV (-25.1 dBFS). The noise-floor increase at low frequencies is generated by the universal source that is connected directly to the modulator inputs. The modulator completely eliminated the common-mode input signal component. However, the modulator can became unstable for common-mode input signals with amplitude equal or higher than 50 mV. For loop-filter supply voltages of 500 and 550 mV, the modulator operates completely stable for input common-mode signals with amplitude of 50 mV and 100 mV, respectively.

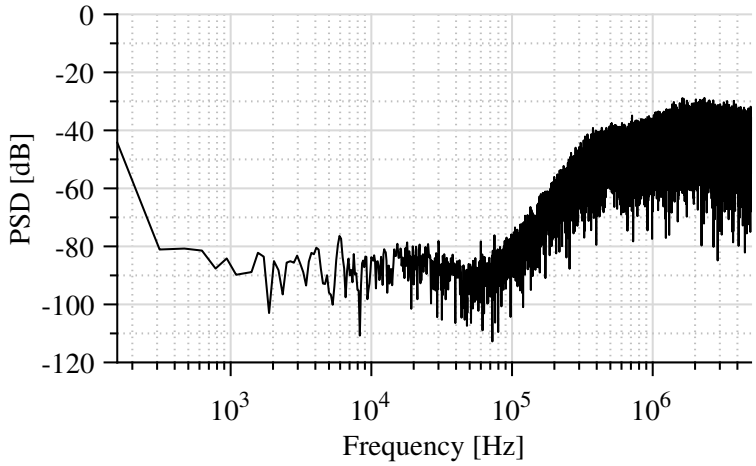
The two measured samples worked properly considering the same trimming and Tables 25 and 26 summarizes the measured results of both samples.

Figure 117 – Measured in-band anti-alias attenuation for a $-6.02\ dB_{FS}$ input signal with frequencies around 1Fs, 2Fs and 3Fs.



Source: The author

Figure 118 – Output PSD for a 25-mV 30-kHz common-mode input signal. Sample I.



Source: The author

Table 25 – Measured main parameters of the CT-SDM second prototype: Sample I

Supply (mV)	400	450	500	550
Fs (MHz)	10	10	10	10
BW (kHz)	50	50	50	50
Analog current (µA)	28.81	53.29	64.38	70.64
Digital current (µA)	7.98	7.90	8.33	8.98
Peak SNR (dB)	64.05	71.24	71.18	71.55
Peak SNDR (dB)	62.92	70.64	70.95	71.39
ENOB (bits)	10.15	11.44	11.49	11.56
DR (dB)	65.55	78.3	80	78.85
Power (µW)	16.31	28.72	37.18	44.74
FoM_W (fJ/step)	142.62	103.24	128.99	147.52
FoM_S (dB)	160.41	170.70	171.28	169.33

Table 26 – Measured main parameters of the CT-SDM second prototype: Sample II

Supply (mV)	400	450	500	550
Fs (MHz)	10	10	10	10
BW (kHz)	50	50	50	50
Analog current (μA)	25.13	49.14	59.03	65.36
Digital current (μA)	8.05	7.95	7.97	9.11
Peak SNR (dB)	63.47	69.82	69.74	71.11
Peak SNDR (dB)	60.5	68.76	67.19	70.11
ENOB (bits)	9.75	11.12	10.86	11.35
DR (dB)	68.9	78	78.19	78.75
Power (μW)	14.88	26.88	34.29	41.41
FoM_W (fJ/step)	171.93	119.98	183.41	158.23
FoM_S (dB)	164.16	170.69	169.82	169.56

6.9 Performance Summary and Comparison with Related Works

Table 27 summarizes the measured results and provides a comparison with related state-of-the-art inverter-based SDMs. The presented circuit achieves a Walden figure-of-merit (FoM) of 103.23 fJ/conv. and a Schreier FoM of 170.70 dB, which are comparable with recent inverter-based low-voltage modulators. Despite using a digital supply voltage of 0.6 V, the presented circuit proves to be a good approach to implement sub-0.5V inverter-based CT-SDMs in 180-nm CMOS technologies. However, some clock boost technique should be used to drive the resistive DAC switches for a true sub-0.5V operation. Also, a process node with dual-MiM capacitors option, and an improved layout, could reduce the modulator area.

Table 27 – Performance comparison with state-of-the-art low-voltage SDMs with inverter-based amplifiers.

Parameters	This work CT-SDM II	[1] JSSC'18	[2] JSSC'19	[3] TCAS-II'17	This Work CT-SDM I
Architecture	CT	CT	CT	DT	CT
Technology (nm)	180	90	130	65 LP	130
Supply (V)	0.45/0.60 (A/D)	0.4	0.3	0.5	0.6
Fs (MHz)	10	10.4	6.4	2	10
BW (kHz)	50	50	50	20	100
OSR	100	104	64	50	50
Peak SNR (dB)	71.24	N/A	68.7	65.3	69.04
Peak SNDR (dB)	70.64	74.4	68.5	60.8	59.43
SFDR (DB)	82.43	85.2	82.6	N/A	60.51
DR (dB)	78.3	78.5	72.2	70.1	74.2
AAF attenuation (dB)	>73.30	N/A	N/A	N/A	N/A
Power (μW)	28.72	26.4	26.3	43.4	89.5
Area (mm^2)	0.36	0.144	0.014	0.38	0.232
FoM_W (fJ/step)	103.23	61.55	120.95	1,210.97	584.79
FoM_S (dB)	170.70	171.27	164.99	156.73	164.68
FoM_{SNDR} (dB)	163.04	167.17	161.29	147.43	149.91

[1] - (LV *et al.*, 2018) - *IEEE Journal of Solid-State Circuits*.
[2] - (LV *et al.*, 2019) - *IEEE Journal of Solid-State Circuits.*
[3] - (PARK; HWANG; JEONG, 2017) - *IEEE Trans. on Circuits and Systems II: Express Briefs*.

6.10 Discussions

An improved PVT compensated inverter-based OTA for the design of low-voltage continuous-time sigma-delta modulators has been presented. The proposed biasing scheme has been verified through transistor-level circuit simulations in a 180-nm CMOS process. It guarantees a robust definition of the inverter GBW and DC gain across PVT corners and mismatch variations, preventing the design of an oversized circuit. Simulation results of a complete 0.6-V CT-SDM with the proposed OTA are given to show the circuit applicability. This same amplifier topology is operated deep in weak-inversion and is used to design a CT-SDM with the loop-filter operating at supply voltages as low as 0.45 V while the digital circuit operates at 0.6 V.

The loop-filter uses an amplifier assistance technique. This inverter-based modulator was fabricated in a 180-nm CMOS process and occupies an area of 0.36 mm^2. Measurement results show that the designed modulator achieves a DR of 78.30 dB over a 50-kHz bandwidth while consuming only 28.72 μW, providing a Schreier FoM of 170.7 dB.

7 CONCLUSIONS

In this thesis, several aspects to design energy-efficient low-voltage CT-SDMs with inverter-based amplifiers have been investigated. An extended literature review is presented and it is followed by the silicon implementation of two prototypes operating with supply voltages as low as 0.6 V.

The first prototype is a third-order low-pass single-bit CT-SDM with a 100-kHz signal bandwidth. The loop-filter is designed with single-stage inverter-based amplifiers that use an on-chip bulk-bias technique to control the output common-mode voltage and to mitigate PVT variations. Also, a negative conductance cell is used at the amplifier output for DC gain enhancement. To increase power efficiency, a single-amplifier biquad resonator is used in the loop filter. To enable the SAB implementation with low DC gain amplifiers, i.e $\leq$40 dB, a compensation technique to mitigate the effects of amplifier's finite DC gain in the resonator transfer function is introduced, providing a resonator transfer function similar to the one achieved by using amplifiers with 80 dB of DC gain. Thus, the proposed modulator has only two amplifiers in the loop filter and explores the use of SAB in the context of low-voltage CT-SDMs. Fabricated in a GF 130-nm CMOS process (CMOS8RF-DM) with an active area of 0.232 mm^2, the modulator achieves a 74.2-dB DR and a peak SNR/SNDR of 69.04/59.43 dB while consuming 89.50 µW (including output buffers) from a 0.6-V power supply.

The second CT-SDM is also a third-order low-pass single-bit modulator and is fabricated in a 180-nm CMOS process with an active area of 0.36 mm^2. The loop filter is composed of three single-stage low-voltage PVT compensated inverter-based OTAs with reduced GBW variation. The proposed amplifier operating point is provided by a bulk-based current mirror and uses an auxiliary circuit to generate the bulk voltage of the PMOS transistors of the inverters to mitigate PVT variations and the control of the output common-mode voltage is performed by controlling the bulk voltage of NMOS transistors. To improve the overall modulator power efficiency, a passive RC path is used to assist the amplifier of the first integrator. The modulator loop filter operates with a supply voltage as low as 0.45 V while the digital circuitry operates at 0.6 V. The modulator total power consumption is 28.72 µW. For a 50-kHz signal bandwidth, the measured peak SNR/SNDR is

71.24/70.64 dB and the achieved DR is 78.3 dB, leading to a Schreier figure-of-merit of 170.70 dB.

The investigation of inverter-based amplifiers for data converters and analog filters for IoT applications is a promising research field. Despite sensor applications, different narrow-band IoT protocols require data converters with signal bandwidths in the range from 100-kHz to 200-kHz as the Narrow-Band IoT (NB-IoT) and the Extended Coverage GSM IoT (EC-GSM-IoT) protocols (3GPP, 2016). Thus, CT-SDMs with intrinsic AAF could be an alternative approach to SAR ADCs and its preceding anti-alias filter. Both modulators introduced in this thesis present an intrinsic AAF and provide competitive FoMs when compared to related and recently reported low-voltage CT-SDMs.

7.1 Future Works

The experimental results provided in this work shows the effectivity of using inverter-based amplifiers to enhance the power efficiency of low-voltage CT-SDMs. Although experimental measurements provided satisfactory results, the proposed CT-SDMs performance could be enhanced by improving some issues in the proposed circuits or by exploring new loop-filter architectures and circuit techniques. Suggestions for further research directions are summarized below:

- Experimental measurements of the first prototype indicate a third-order harmonic that reduced the achieved SNDR. A possible solution to avoid this non-ideality is to assist the first integrator amplifier as approached in Chapter 6 or (PAVAN; SANKAR, 2010).

- A possible solution to provide a single 0.45 V supply for the second prototype is to use some clock-boost circuit technique for proper switching of the NRZ DACs, and to optimize the sizing of the amplifier transistors. This circuit could also be redesigned in a triple-well CMOS process with lower threshold voltages transistors to enable sub-0.4 V operation.

- To improve power efficiency and reduce the first integrator amplifier GBW in both prototypes, one should consider the use of a 1.5-bit quantizer (3 levels) instead of a 1-bit quantizer (2 levels) since it reduces by half the quantizer steps and improves the modulator linearity and SNDR. Also, it reduces unnecessary switching, providing a more stable loop. A straightforward 1.5-bit DAC implementation is introduced by (JANG; LEE; CHAE, 2019) and is suggested for future implementations.

- A general improvement for the designed amplifiers is to enhance the CMFB network. An alternative approach is to use the CMFB circuit proposed in (LV *et al.*, 2018) and (LV *et al.*, 2019). It avoids the use of resistors to sense the output common-mode voltage, avoiding increasing the amplifier output conductance.

- An interesting alternative to decrease the amplifier output conductance and minimize the amplifier DC gain variations under process variations and mismatch is the use of parallel association of transistors, as demonstrated by (BRAGA *et al.*, 2017). In (GIRARDI; BAMPI, 2004), the use of trapezoidal association of minimum-length transistors in inverter amplifiers is investigated, but no evaluation of process and mismatch in the designed circuit is addressed. Thus, the study of trapezoidal association of transistors to design inverter-based amplifiers in nanometer CMOS process tolerant to PVT variations is also a suggested research topic.

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