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Reliability Evaluation of FinFET-based SRAMs in the Presence of Resistive Defects

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of the requirements for the degree of
PhD in Microelectronics

Advisor: Prof. Dr. Tiago Roberto Balen
Coadvisor: Prof[a]. Dr[a]. Letícia Maria Bolzani Poehls

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DEDICATION

I dedicate this work to my wife, my parents, and my siblings.

"Nobody told me it was impossible, so I did"

— JEAN COCTEAU

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ABSTRACT

The development of Fin Field Effect Transistor (FinFET) has made possible the continuous scaling-down of Complementary Metal-Oxide-Semiconductor (CMOS) technology, overcoming issues caused by the Short-Channel Effects. In parallel, the increasing need to store more and more information has resulted in the fact that Static Random-Access Memories (SRAMs) occupy a great part of integrated systems. Manufacturing process deviations have introduced different types of defects, strong and weak, that directly affect the SRAM's reliability, causing different faults. One of the main factor that reduces the reliability and the lifetime of the FinFET-based SRAMs are the weak resistive defects. Weak resistive defects are considered the most important cause of test escapes, since opposing the strong resistive defects, that is easily detectable, weak defects require more than one consecutive operation for being propagated at logic level. In this context, this work investigates resistive defect implications on the reliability of FinFET-based SRAMs along with the combined effects of ionizing particle impacts in the SRAM transistors considering the presence of such resistive defects. Firstly, a study on functional implications regarding manufacturing resistive defects in FinFET-based SRAMs is presented. In more detail, a complete analysis of static and dynamic fault behavior is performed through electrical simulations of FinFET-based SRAMs considering different technological nodes. The results show that the sensitivity to this kind of defect is related to the size of technology, in which higher technological nodes are more sensitive to open defects and smaller technologies are sensitive to bridge defects. Secondly, a TCAD model of a FinFET-based SRAM cell was developed in order to allow the evaluation of cell sensitivity to ionizing particles causing Single Event Upsets (SEUs). In this part of the work was developed a new model representing ion strike in FinFET-based SRAM cells. Then, SPICE simulations were performed considering the current pulse parameters obtained with TCAD. Finally, weak resistive defects are injected into the FinFET-based SRAM cell. Results show that weak defects may have either a positive or negative influence on the cell reliability, depending on the position where it is, against SEUs caused by ionizing particles.

Keywords: FinFET. SRAM. Resistive Defects. SPICE. TCAD. Reliability. Single Event Transient Modeling.

Avaliação da confiabilidade de SRAM baseada em FinFET sob Defeitos Resistivos

RESUMO

O desenvolvimento do *Fin Field Effect Transistor* (FinFET) tornou possível a redução contínua da tecnologia *Complementary Metal-Oxide-Semiconductor* (CMOS), contornando os problemas causados pelos efeitos de canal curto. Paralelamente, a crescente necessidade de armazenar grande quantidade de informação resultou no fato de que *Static Random-Access Memories* (SRAM) ocupam grande parte dos sitemas integrados. A variabilidade dos processos de fabricação pode causar vários tipos de defeitos, fortes e fracos, que afetam diretamente a confiabilidade de SRAMs, propagando diferentes tipos de falhas. Um dos principais fatores que reduzem a confiabilidade e a vida útil das SRAMs baseadas em FinFET são os defeitos resistivos fracos. Os defeitos resistivos fracos são considerados a causa mais importante de "*test escape*", pois ao contrário dos defeitos resistivos fortes, que são facilmente detectáveis, os defeitos fracos requerem mais de uma operação consecutiva para serem propagados em nível lógico Neste contexto, além da investigação dos defeitos resistivos fracos, este trabalho propõe investigar os efeitos de impacto de partículas ionizantes na confiabilidade de SRAMs baseadas em FinFET na presença destes defeitos. Primeiramente, é apresentado um estudo das implicações funcionais de defeitos resistivos de manufatura em SRAMs baseadas em FinFET. Mais detalhadamente, uma análise completa do comportamento de falha estática e dinâmica é realizada por meio de simulações elétricas em um bloco de memória SRAM baseado em tecnologia FinFET, considerando diferentes nós tecnológicos. Os resultados mostram que o grau de sensibilidade ao tipo de defeito está relacionado ao tamanho da tecnologia, sendo que nodos tecnológicos maiores são mais sensíveis a defeitos de circuito aberto (open) e tecnologias menores são mais sensíveis a defeitos de curto circuito (bridges). Posteriormente, um modelo TCAD de uma célula SRAM baseada em FinFET foi desenvolvido para permitir a avaliação do impacto de partículas ionizantes que causam o *Single Event Upsets* (SEUs). Nesta parte do trabalho, foi desenvolvido um novo modelo de curva para a representar o ataque iônico em células SRAM baseadas em FinFET. Em seguida, foram realizadas simulações SPICE considerando os parâmetros do pulso de corrente obtidos com o simulador TCAD. Finalmente, defeitos resistivos fracos foram injetados na célula SRAM baseada em FinFET. Os resultados mostram que defeitos fracos podem ter

uma influência positiva ou negativa na confiabilidade das células contra SEUs causados por impacto de partículas ionizantes.

Palavras-chave: FinFET, SRAM, Defeitos Resistivos, SPICE, TCAD, Confiabilidade, Modelagem de *Single Event Transient*.

LIST OF ABBREVIATIONS AND ACRONYMS

A-CELL	Aggressor cell
ASET	Analog Single Event Transient
ASU	Arizona State University
BL	Bit Line
BOX	Buried Oxide
BPTM	Berkeley Predictive Technology Model
BSIM	Berkeley Short-channel Insulated Gate Field Effect Transistor Model
CMG	Common MultiGate
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
dDRDF	dynamic Deceptive Read Destructive Fault
DELTA	Depleted Lean-Channel Transformer
DGFET	Double-Gate Field Effect Transistor
DGMOS	Double-Gate Metal-Oxide-Semiconductor
DIBL	Drain-Induced Barrier Lowering
dIRF	dynamic Incorrect Read Fault
DRAM	Dynamic Random Access Memory
DRDF	Deceptive Read Destructive Fault
dRDF	dynamic Read Destructive Fault
EI	Electrostatic Integrity
FDSOI	Fully Depleted SOI
FET	Field Effect Transistor
FFM	Functional Fault Model
FinFET	Fin Field Effect Transistor.

FOX	Field Oxide
FP	Fault Primitive
GAA	gate-all-around
GOS	Gate Oxide Short
HD	High-Density
HFin	Height of Fin
HP	High-performance
IC	Integrated Circuit
IGFET	Insulated Gate Field Effect Transistor
ILD	Inter Layer Dielectric
IRF	Incorrect Read Fault
ITRS	International Technology Roadmap for Semiconductors
LET	Linear Energy Transfer
LP	Low Power
LSTP	Low-STandby Power
LV	Low Voltage
MBU	Multi-Bit Upset
MCU	Multi-Cell Upset
MIGFET	Multiple Independent Gate Field Effect Transistor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MuG	Multiple-Gate
NFin	Number of Fin
NMOS	Negative Metal-Oxide-Semiconductor
PD	Pull-Down
PDK	Process Design Kit

PDSOI	Partially Depleted Silicon-On-Insulator
PG	Pass Gate
PMOS	Positive Metal-Oxide-Semiconductor
PTM	Predictive Technology Model
PTM-MG	Predictive Technology Model for Multi-Gate
PU	Pull-Up
PUCRS	*Pontifícia Universidade Católica do Rio Grande do Sul*
RAM	Random Access Memory
RDF[1]	Random Dopant Fluctuations
RDF[2]	Read Destructive Fault
RF	Radio Frequency
SCE	Short-Channel Effect
SEB	Single Event Burnout
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SoC	Systems on Chip
SOF	Stuck-Open Fault
SOI	Silicon-On-Insulator
SRAM	Static Random Access Memory
SNM	Static Noise Margin
STI	Shallow Trench Isolation
TCAD	Technology Computer-Aided Design
TF	Transition Fault

TFin	Thickness of Fin
TSMC	Taiwan Semiconductor Manufacturing Company
UFRGS	*Universidade Federal do Rio Grande do Sul*
UTBB	Ultra-thin Body and Buried Oxide
V-CELL	Victim cell
VDSM	Very Deep Sub-micron
VDT	Voltage-Doping Transformation
VTC	Voltage Transfer Characteristic
WL	Word Line

LIST OF SYMBOLS

A	ampere
CF_{ds}	Disturb Coupling Fault
CF_{ir}	Incorrect Read Coupling Fault
CF_{rd}	Read Disturb Coupling Fault
CF_{tr}	Transition Coupling Fault
cm	Centimeter
cm^2	Centimeter squared
d	Material density
e	Electronic Charge
F	Faulty behavior observed
GaAs	Gallium Arsenide
GHz	Gigahertz
GND	Ground
HfO_2	Hafnium Oxide
kΩ	Kilo ohms
I_{DS}	Current of drain to source
I_{off}	Off Current
I_{off_norm}	Normalized Off Current
I_{peak}	Peak Current
$I_{plateau}$	Plateau Current
I_{sat}	Saturated Current
I_{sat_norm}	Normalized Saturated Current
I_{Thresh}	Threshold Current
L	Channel length

L_{eff}	Effective channel length
LET_f	Threshold Linear Energy Transfer as a function of the length
LET_{th}	Threshold Linear Energy Transfer
MeV	Mega Electron Volt
mg	Milligram
nm	Nanometer
ns	Nanosecond
pA	Picoampere
pC	Picocoulomb
ps	Picosecond
Q_{crit}	Critical Charge
Q_{coll}	Collected Charge
Q_{dep}	Deposited Charge
Q_{exc}	Excess Charge
Q_{exc_alt}	Altered Excess Charge
Q_{exc_nom}	Nominal Excess Charge
R	Output or read operation
R_{crit}	Critical Resistance
S	Sensitizing sequence
S_{aa}	Stress aggressor-aggressor
S_{av}	Stress aggressor-victim
Si	Silicon
S_{va}	Stress victim-aggressor
S_{vv}	Stress victim-victim
T	Device Thickness
t_{dep}	Thickness of deep electric field penetration

TiN	Titanium Nitride
^{TM}	Trademark
t_{ox}	Thickness of gate oxide
V_{bi}	Built-in voltage
V_{DD}	Voltage drain supply
V_{DS}	Voltage of drain to source
V_{GS}	Voltage of gate to source
V_{TH}	Threshold voltage
V_{THCC}	Short channel threshold voltage
$V_{TH\infty}$	Long channel threshold voltage
W	Channel width
W_{eff}	Effective channel width
W_{min}	Minimum channel width
wt_hi	radius of heavy-ion defined as the perpendicular from the track
x_j	Thickness of source and drain junction
ε_{si}	Permittivity constant of silicon
ε_{ox}	Permittivity constant of silicon oxide
μA	Microampere
μm	Micrometre
τ_1	Rise Timing Constant
τ_2	Fall Timing Constant

LIST OF FIGURES

LIST OF TABLES

CONTENTS

1 INTRODUCTION

Along the evolution of the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) technology in Very Deep Sub-Micron (VDSM) circuits, Moore's law (MOORE et al., 1965) has been followed doubling the number of transistors in the same area every eighteen months. This has occurred since the commercial implementation of the first Integrated Circuit (IC).

However, with the increase of leakage current and Short-Channel Effects (SCEs) observed in the Complementary Metal-Oxide-Semiconductor (CMOS) technology, it was not feasible to shrink transistor feature size below 22 nm using MOSFET (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015). To continue the scaling down of technology nodes, Fin Field-Effect Transistors (FinFETs) were introduced as an alternative transistor technology to replace planar CMOS devices. FinFET is built as a multi-gate transistor. In other words, the FinFET channel has the shape of a fin and is involved by the gate, all placed on top of oxide. This design approach improves the electrostatic control of the transistor's channel (HUANG et al., 1999) and hence solves some of the aforementioned problems evolving planar CMOS technology for nodes beyond 22 nm. In more detail, leakage current, SCEs, and Random Dopant Fluctuations (RDFs) are mostly eliminated as doping levels are reduced to a minimum in FinFETs (VILLACORTA; SEGURA; CHAMPAC, 2016). Consequently, the majority of microelectronic companies are gradually replacing planar CMOS transistors with FinFETs in their state-of-the-art processors.

As a result of these changes in technological paradigms caused by the introduction of FinFET technology, several circuit devices needed to be redesigned, tested, and evaluated. In parallel, due to the always-increasing need to store more and more information on chips, Static Random-Access Memories (SRAMs) have become the main contributor to the overall area of integrated systems (WILSON, 2013) and hence are cited as particularly important, motivating this work's focus. Further, SRAMs are designed at the dimensional limits of technology, being statistically more likely to be affected by manufacturing defects (BOSIO et al., 2012), generating the need for intensive test procedures during the manufacturing stage. Therefore, SRAMs require efficient testing, i.e., tests with high fault coverage and low cost. Resistive defects have traditionally been a concern in the CMOS technology test scenario. More recently, this concern shifted towards weak resistive-open and weak resistive-bridge defects as their probability of occurrence may

increase in nanometer technologies due to the ever-growing number of interconnections between layers (DILILLO et al., 2004).

While the influence of resistive defects in circuit parameters (e.g. voltage, current) is irrefutable, it is easier to evaluate their impact by analyzing which faulty behaviors they lead to. Functional faults are deviations from expected behavior of the memory under a set of operations (GOOR; AL-ARS, 2000). Faults can be static (whose propagation occurs with one operation only) and dynamic, where at least two consecutive operations are required to sensitize the fault. Weak defects generally cause dynamic timing dependent faults, meaning that at least a 2-pattern sequence is necessary to sensitize them (BORRI et al., 2005). Moreover, the number of dynamic faults is directly correlated to the presence of weak resistive defects (DUBEY; GARG; MAHAJAN, 2010).

With the scaling down of technological nodes, resistive defects are likely to be one of the main reliability challenges in IC design (SIMSIR; BHOJ; JHA, 2010). These defects have been modeled and studied in CMOS technology and are known to generate dynamic faults (BORRI et al., 2005). However, the detection of weak resistive defects and, therefore, dynamic faults may not be trivial. In fact, open/resistive vias are the most common origin of test escapes in deep-submicron technologies (NEEDHAM; PRUNTY; YEOH, 1998). Thus, a complete understanding of this specific type of defect and the faults it causes is essential to improve manufacturing test procedures. Commonly, dynamic faults have been related to two aspects: the physical position and size of the defect. Varying defect positions have been evaluated for planar CMOS SRAM cells and the classification into either resistive-open, a resistor between two circuit nodes that share a connection, or resistive-bridge, a resistor between two nodes that should not be connected was established (HAMDIOUI; GOOR, 2000). Regarding defect size, it can be used to estimate the fault's strength. As previously mentioned, weak defects are defects able to sensitize dynamic faults; simulating different defect sizes allows to identify the specific resistance necessary to start sensitizing a certain defect at logic level. This resistance, known as critical resistance, defines the threshold between a fault-free and faulty behavior.

Traditionally, the characterization of fault behavior observed in defective SRAM cells has been performed following a well-established methodology based on SPICE electrical simulations. Many works focused on evaluating the resistance in which a certain defect starts to sensitize faults. This resistance, known as critical resistance, is the threshold between a fault-free and faulty behavior (SEGURA et al., 1992). Critical resistances

of resistive-open defects were investigated in (DILILLO et al., 2004; BORRI et al., 2005; DILILLO et al., 2005; VATAJELU et al., 2013; MARTINS et al., 2016) adopting technological nodes of 130 nm down to 40 nm, while critical resistances of resistive-bridge defects were investigated in (FONSECA et al., 2010a; FONSECA et al., 2010b) adopting technological nodes of 90 nm down to 40 nm.

However, all these previous researches were conducted using planar CMOS technology. So far, little research has been conducted considering resistive defects in FinFET memories. In (HARUTYUNYAN et al., 2014a), the authors modeled resistive open and bridge defects taking into account the physical structure of 28 nm FinFET devices aiming to observe possible unique faults of this technology. No further works have been proposed focusing on smaller nodes. This is especially worrisome since 10 nm FinFET devices are currently in production (INTEL, 2018a; SAMSUNG, 2018; INSIGHTS, 2017).

Another important topic to be discussed is the Single Event Effects (SEEs) which occur in ICs, as the Single Event Upset (SEU) when dealing with SRAMs. This event leads to functional faults in circuit operation, known as soft errors. It is usually caused by the incidence of an ionizing particle in the device. The ionizing particle generates a current pulse inside the transistor. For older technologies, the current pulse was accurately modeled by a double exponential current waveform. However, for the actual technologies as the FinFET, the current pulse shape becomes much more complex, and its behavior still need to be correctly modeled (NICOLAIDIS, 2011). Furthermore, a characterization of a current pulse for FinFET SRAM is discussed in this work.

It is known from the literature that radiation can lead to soft errors in FinFETs (as bit-flips in SRAM cell) even at ground level (HUBERT; ARTOLA; REGIS, 2015; ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO, 2015). Some studies consider a comparative analysis of SEEs between FinFET and other technologies (planar CMOS and SOI) (HUBERT; ARTOLA; REGIS, 2015), where this work also perform an analysis with FinFET-based SRAM at different altitude levels. An analysis of weak resistive defects was already carried out for planar SRAM cells in many works as in (HAMDIOUI; GOOR, 2000). Further, an analysis of the radiation susceptibility of CMOS SRAM cells in the presence of weak resistive defects is presented in (MEDEIROS; POEHLS; VARGAS, 2016). Considering this, we propose to analyze the influence of weak resistive defects on the FinFET-based SRAM robustness under single event effects. Because the FinFET structure is physically more complex than planar CMOS, a more precise and realistic simulation tool is necessary. Thus, a FinFET-based SRAM cell is modeled using

Technology Computer-Aided Design (TCAD) and simulations of ionizing particle impacts are carried out at physical level. Further, the transient current generated by such event is modeled at electrical level.

1.1 Goal and Contributions of this Thesis

The introduction of new transistor technologies in the industry, such as FinFET, and the migration of circuit designs to this technology, justify the studies to ascertain the reliability of the system, and tests must be improved to ensure this. Thus, this work presents an investigation of the behavior of FinFET-based SRAM cells affected by weak defects with an initial focus on resistive defects. In particular, this work intends to map and determine how manufacturing defects, specifically resistive-open and resistive-bridge defects, impact in the behavior of FinFET SRAM cells. Resistive defects with different magnitudes were injected in-memory bit cells aiming to detect static and dynamic faults. The analysis was performed through electrical simulations using Hspice^{TM} software and adopting Predictive Technology Model (PTM) (ASU, 2011) of multi-gate transistors based on 20 nm, 16 nm, 14 nm, 10 nm, and 7 nm bulk FinFET.

In the end, reliability studies were conducted considering the injection of ionizing particles over an SRAM cell modeled in a TCAD software (Sentaurus^{TM}). The main goal is to obtain by physical simulation: the minimum value of Linear Energy Transfer (LET) of an incident particle that results in a bit-flip (LET$_{th}$, or threshold LET) for FinFET SRAM cells designed in a technology node of 14 nm; the proposal of a SPICE model for the obtained current curves; and the study of the impact of resistive defects on the reliability of FinFET SRAM cells under single events.

To clarify, the contributions of this thesis are:

- A full mapping of the faults caused by resistive defects in the FinFET-based SRAM block considering, single and couple faults, static and dynamic faults, different operation temperatures, also considering a low variation of temperature for weak defects analysis, and several technology nodes;

- Study the behavior from the impact of an ionizing particle in a FinFET-based SRAM cell, considering three kinds of layout configuration;

- Developing of new equations for the implementation of bit-flips caused by SEE in FinFET-based SRAM cell for electrical simulation, considering different cell's layout configuration;
- Finally, the evaluation of the effect combined of weak resistive defects and SEE in FinFET-based SRAM cells.

1.2 Thesis Organization

Chapter 2 presents the theoretical basis for the understanding of this work, as the challenges of miniaturization, thus, there is the introduction of FinFET technology and SRAM circuit. Then, in Chapter 3 is the background focused on resistive defects and the problem of radiation effects in electronic devices is presented in order to introduce the background necessary to follow chapter 5.

Chapter 4 presents the reliability evaluation of FinFET-based SRAM under resistive defects, its method of implementation, and the validation of the design already developed. Chapter 5 presents the TCAD simulations of SEE over the FinFET-based SRAM, and the proposal of a SPICE model to inject the currents whit the shapes observed in the physical simulations. Chapter 6 describes the final remarks and future works that could be done using the obtained data and simulation models developed in this work. Finally, in Chapter 7 the list of publications achieved during the doctorate period is shown.

In Appendix A, there is some complementary background as the Short Channel Effect, which is explained to justify the development of new device technologies. Next, other kinds of commercial state-of-the-art devices are presented, the SOI MOSFET. Next, the design of an SRAM block is briefly explained. Thus, definitions of Test Theory and Fault Models associated with resistive defects are explained.

2 CHALLENGES OF MINIATURIZATION, FINFET AND SRAM

This chapter will present a discussion about the challenges of miniaturization of Integrated Circuits (ICs). Then, it will present the two focus elements of this work: the FinFET technology with its characteristics, with a brief description of the Predictive Technology Model (PTM) adopted as a model in this work. Finally, the design of an SRAM block and its operation are explained, followed by the emphasis on a FinFET-based SRAM.

2.1 Challenges of Miniaturization

During the last decades, advances in Very Deep Sub-Micron (VDSM) technology allowed the technology miniaturization according to Moore's law, which predicted the number of transistors in the same area to double every eighteen months (MOORE et al., 1965). However, the nature of scaling has already changed. There is a growing concern that scaling of devices in any form is slowing down, and there is a good chance that it will eventually become infeasible to cost-effectively manufacture devices below a certain feature size (ROY et al., 2013).

In this context, the scaling roadmap for ICs has been extrapolated from the current Moore's law regime into three main domains, namely 1) More-Moore; 2) Beyond CMOS; and 3) More-than-Moore. The first domain is expected to deal with traditional silicon Complementary Metal-Oxide Semiconductors (CMOS) and its scalability, in other words, the continuation of Moore's Law is known as the "More Moore" domain (HEINIG et al., 2014). The "Beyond CMOS" domain consists of various nanotechnologies beyond ultimately scaled CMOS (e.g., carbon nanotubes, Si nanowire, spintronics, etc.), which can potentially replace silicon and CMOS in the future. The "More-than-Moore" domain encompasses various disruptive device paradigms such as flexible electronics, nanoelectromechanicals (NEMS), biochips, heterojunction devices, solar cells, fuel cells, etc. Note that the devices in the "More-than-Moore" domain are not necessarily nanoscale, and they often provide auxiliary functions that cannot easily be realized in CMOS technology. Considering the "More-Moore" domain, the continuous evolution of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) technology has been enabling miniaturization and aggressive technology integration.

Focusing on the More-Morre domain, initially some enhancement techniques to increase performance were implemented along with the reduction of the transistor tech-

nology. Among the proposed solutions is the Strain technique, which is a technique to generate traction or compression in the transistor channel, increasing the mobility in planar Complementary Metal-Oxide-Semiconductor (CMOS) technologies. Furthermore, an N-channel MOS (NMOS) transistor uses traction to keep away the atoms, improving the mobility of the electrons; on the other hand, on P-channel MOS (PMOS) the channel compression causes the atoms to approach, facilitating the mobility of the gaps through the crystal lattice (ROBERDS; DOYLE, 2003).

Continuing the miniaturization process, the leakage current in traditional CMOS transistor at the gate became significant, and may not be more ignored in the future. With this in mind, there was a need for the introduction of high-K oxide (Hafnium Oxide — HfO_2), to increase the value of dielectric strength in insulation, thereby decreasing the leakage current, and the return of metal (Titanium Nitride — TiN) to the transistor's gate between the insulation and the polysilicon to prevent depletion therein. This way, the traditional CMOS transistor was reached, the limit being the technological node of 20 nm (COLINGE et al., 2008).

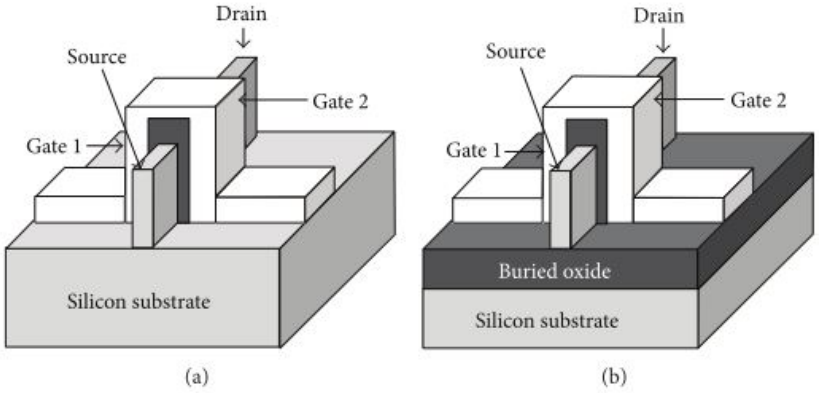
Starting from transistors with 22 nm technological nodes of MOSFET technology, the gate terminal begins to lose control over the potential distribution and current flow of the channel region of the transistor. This happens due to the phenomenon of the Short Channel Effect (SCE), which occurs due to the proximity between the source and the drain. The electric field created by these two terminals interferes in the field created by the gate. This compromises the entire operation of the device. Facing this adversity, new types of transistors have emerged to overcome the problem. There are two types currently used, the Silicon-On-Insulator (SOI) MOSFET and MultiGate devices, which will be mentioned in the text as FinFET, where through these technologies it is possible to continue the evolution of the technological nodes (COLINGE et al., 2008).

Nowadays, FinFET technology is already replacing CMOS transistors in state-of-the-art ICs by major electronics companies such as Intel which uses the term trigate (INTEL, 2018a), and Samsung (SAMSUNG, 2018). These references have already migrated to FinFET technology owing to its reduced short channel effects, electrostatic characteristics (TANG et al., 2001; YU et al., 2002; CHANG et al., 2011), and its compatibility with standard CMOS manufacturing process (COLINGE et al., 2008).

2.2 The Types of FinFET Technology

There are some alternatives to the method of manufacturing FinFET devices. The FinFETs can be SOI FinFET or bulk FinFET. Although FinFETs implemented on SOI slides are quite common, the FinFETs have been also implemented in conventional wafers. Figure 2.1 shows a comparison between FinFET implemented on conventional wafers (bulk) and SOI. In bulk FinFETs all fins share the same silicon substrate (this is called bulk). On the other hand, in SOI FinFETs, all fins are physically isolated. SOI technology is briefly explained in the Appendix A.

Figure 2.1: Comparative between (a) bulk and (b) SOI FinFET.

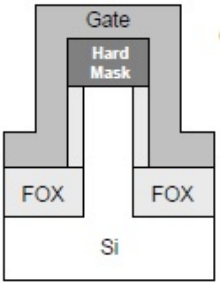


Source: BHATTACHARYA; JHA,2014.

The two types of FinFETs have characteristics that are close enough in terms of cost, performance, and production, so both probably will coexist in the market, for some years However many companies are preferring to use bulk technology because it is easy to migrate from traditional MOSFET technology (BHATTACHARYA; JHA, 2014), and it is the technology used by Intel Company because this work will focus in the Bulk FinFET technology.

Bulk FinFET was developed and used by Intel starting in the 22 nm node in 2012 (AUTH, 2012), using the triple gate model, they chose it due to the lower manufacturing cost because, and it uses the planar CMOS fabrication model as a basis. The electrical characteristics from bulk FinFET are lower than the SOI FinFET, but the lower manufacturing cost is enough to it be adopted by Intel (CHI, 2012). It is interesting to mention that the FinFET maybe be built with a dense insulator, a hard mask in the top of the gate as shown in Figure 2.2 (FOX means Field Oxide layer), turning this form as a Double-Gate type.

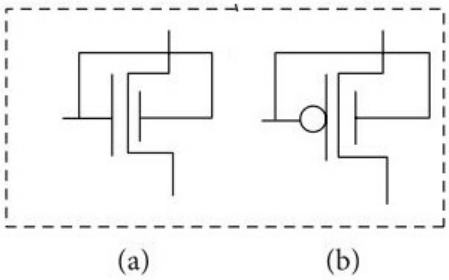
Figure 2.2: Bulk FinFET with Hard Mask



Source: COLINGE et al.,2008.

In Figure 2.3 it is presented the electrical schematic symbol of the FinFET transistors, there is no difference in the symbols for SOI or bulk FinFET.

Figure 2.3: FinFET Schematic (a) nFinFET, (b) pFinFET



Source: BHATTACHARYA; JHA,2014.

2.3 FinFET Characteristics

Once the bulk FinFET is the main device that will be treated in this work, its manufacturing characteristics will be discussed below. Firstly, it is presented how to size FinFETS (determine the number of fins), and thus some FinFET types ere presented.

2.3.1 FinFET Advantages

The main advantages of FinFET technology, according to (BHATTACHARYA; JHA, 2014; SIDDHARTHAN; MEENAKSHI, 2013) over planar CMOS technology are:

- An excellent control over the conduction channel by the gate. The sub-threshold behavior of FinFETS is near the ideal, which is very difficult to achieve in a planar MOSFET;
- Short channel effects are reduced due to excellent channel control;

- High-density integration, due to its three-dimensional structure;
- Low variability: the fin's body is slightly doped, it reduces the effects of Random Dopant Fluctuations (RDF);
- The FinFET can operate at lower voltages than planar technology reducing both dynamic and static consumption;
- In FinFET-based SRAM cells, the Static Noise Margin (SNM), which is the minimum voltage noise to change the value of a cell, is much higher than the planar transistor due to the low RDF in FinFET.

2.3.2 Defects in FinFET Technology

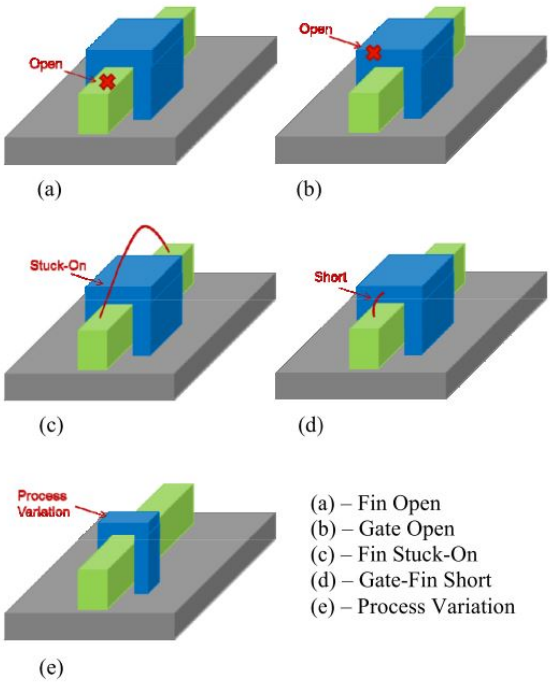
FinFET fault models must be established since the conventional models may not cover all possible aspects of defects in the technology as presented in (HARUTYUNYAN et al., 2014a). These models are still under study by the academic community. It is important to notice that the defect is a physical abnormality in the device, and the fault model is how that defect manifests itself in the circuit. Therefore, the possible defects that can occur in FinFET must be observed. Figure 2.4 presents the reevaluation of some types of defects. These defects are:

(a) Fin Open: Open defect in fin;
(b) Gate Open: Open defect in the gate;
(c) Fin Stuck-On: short defect between source and drain;
(d) Gate-Fin Short: Short defect between gate and fin;
(e) Process Variation: Process variations and parameters variations of fin.

The analysis focused on FinFET-based SRAMs should consider the following defects: shorts and opens between memory cells, shorts and opens internally in a cell, as well as peripheral defects occurring in circuits such as address decoders or sense amplifiers (HARUTYUNYAN et al., 2014a). It is important to mention that, for the above-presented defects, the types a), b), c) and d) may manifest as resistive defects.

Studies about the stuck-open faults (SOF) on FinFET devices were performed in (VAZQUEZ et al., 2009) and (CHAMPAC et al., 2012), and reports that the classical SOF behavior is altered by the increase of leakage current and the smaller node capacitances in

Figure 2.4: FinFET Defects.

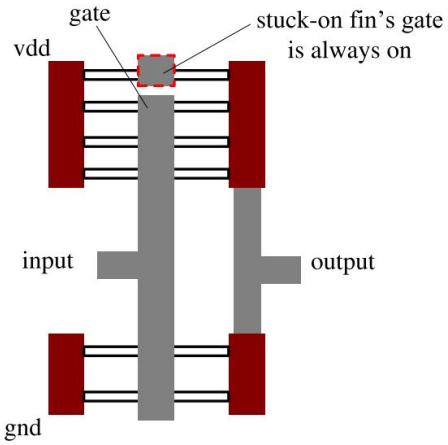


Source: HARUTYUNYAN et al.,2014a.

the device. The current from SOF in FinFET is a combination of classical and nonclassical responses in function of the fan-out, fan-in, clock period, leakage current, noise, V_{DD}, and temperature. The work proposes two vector strategies to improve the robustness of SOF detection in the presence of leakage current. Also, authors in (SIMSIR; BHOJ; JHA, 2010) and (BHOJ; SIMSIR; JHA, 2011) propose a fault modeling for FinFET applying open and short defects in logic gates (INV and NAND). It was verified that most opens and shorts in FinFET logic circuits have corresponding fault models in planar CMOS.

In (LIU; XU, 2012) various types of defects on logic circuits with FinFETs were studied. The defects were considered in the fins: stuck-on, stuck-open, and gate oxide short. It was verified that different number of fins result in different faulty behaviors. The proportion of defective fins determine if the device is faulty-free, or if it has a stuck-open fault or delay fault. Furthermore, because the characteristic configuration of FinFET, one defect can be propagated through the back gate of a fin, thus, new test generation strategies are required to detect delay faults. Also, it was verified that any incorrect doping or geometrical imperfection on the crystal structure in the fin will make the whole fin as a wire. Furthermore, any connection between the source and the drain will also make the fins act similarly to a wire, as illustrated in Fig 2.5. In both cases, the fin will be always in short between the drain and source.

Figure 2.5: The circuit for fins stuck-on in a logic gate.



Source: LIU; XU,2012.

2.3.3 Predictive Models for Electrical Simulations

The Predictive Technology Model (PTM) (ASU, 2011) developed by the Arizona State University (ASU) was initially developed for electrical simulation for planar CMOS technology nodes up to 20 nm based on the BSIM4 model (BERKELEY). The ASU PTM model improved the methodology of the Berkeley Predictive Technology Model (BPTM) (CAO et al., 2000) that uses empirically extraction model parameters from early-stage silicon data, the ASU PTM take into account significant physical correlations among parameters. In the work (SINHA et al., 2012), the PTM for multi-gate transistors (PTM-MG), for sub-20 nm technology nodes (FinFETS), was developed using BSIM-CMG (Berkeley Short-channel IGFET Common Multi-Gate) model (DUNGA et al., 2008), with the nodes of 20 nm, 16 nm, 14 nm, 10 nm, and 7 nm. This electric model has been used to describe the behavior of both bulk FET and SOI FET (COLINGE et al., 2008). The PTM-MG has two application-specific versions, high performance (HP) and low-standby power (LSTP). This second was used in the work presented in the thesis because of the low leakage current, between the drain and source when the transistor is cut off (ASU, 2011). The parameters of PTM-MG technology and the supply voltage for each node are presented in Table 2.1. It is important to mention, that because it is a predictive model, certain differences and limitations can be found in the model and may influence the results slightly compared to commercial technologies. As a curiosity, it is valid to mention that it was developed in (CLARK et al., 2016) in collaboration with ARM Ltd a 7 nm predictive process design kit (PDK) called the ASAP7 PDK for design layout in academic use.

Table 2.1: Supply voltage and physical parameters of PTM-MG technology by nodes

Parameter	Technological Node				
	20 nm	**16 nm**	**14 nm**	**10 nm**	**7 nm**
Supply Voltage (V)	0.90	0.85	0.80	0.75	0.70
Gate Lenght (nm)	24.0	20.0	18.0	14.0	11.0
Fin Height (nm)	28.0	26.0	23.0	21.0	18.0
Fin Thickness(nm)	15.0	12.0	10.0	8.00	6.50
Effective Width (nm)	71.0	64.0	56.0	50.0	42.5
Oxide thickness (nm)	1.40	1.35	1.30	1.20	1.15
Work-function - NFET(eV)	4.56	4.59	4.60	4.60	4.61
Work-function - PFET(eV)	4.62	4.59	4.57	4.57	4.56

Source: ASU 2011.

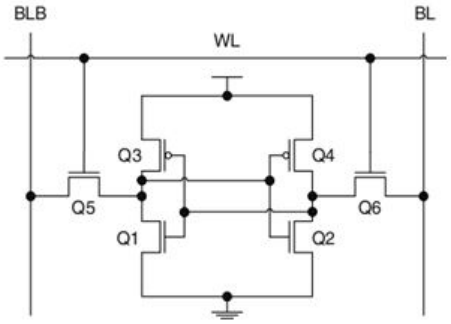
2.4 SRAM Circuit

In digital circuits, the manipulated information needs to be stored in systems suitable for this purpose: the memories. Memory circuits can be classified according to their volatility. Volatile memories lose information stored when the power supply is removed, opposing the non-volatile type. The memory circuit studied in this work will be one of the volatile types, specifically the Random Access Memory (RAM).

There are two types of MOSFET RAMs: dynamic and static. Dynamic RAMs (DRAMs) store the binary data in capacitors, and allow for a larger reduction of the cell area, however, require more elaborate read and write circuits. On the other hand, static RAM (SRAM), which is the focus of this work, uses cross-coupled inverters as storage cells for information.

The SRAM adopted in this work is the 6T type, because it is the model most widely used of SRAM (NEISSER; WURM, 2015). It is composed of a set of six transistors (Q_n) as shown in Figure 2.6. The cell consists of two inverters with cross-connections and two access nMOS transistors. The access transistors are activated when Word Line (*WL*) is selected with logic value '1', thus connecting one of the inverters to the Bit Lines (*BL*) and its opposite polarity counterpart ($\overline{BL}$ or *BLB*). The access transistors act as a transmission gate, allowing bi-directional current flow between the cell and the *BL* and *BLB* columns. It is important to mention that the SRAM cell structure is divided into three parts with its proper notation (PU: PG: PD), where PU, PG, and PD are respectively: the pull-up (the two PMOS transistors from inverters); the pass gate consisting of two NMOS transistors; and finally, the pull-down are the two NMOS transistors from inverters. The SRAM block structure, its modes of operations, and Static Noise Margin (SNM) are presented in the Appendix A.

Figure 2.6: 6T-Cell SRAM Schematic.



Source: SEDRA; SMITH,2004.

2.5 FinFET-Based SRAM Configuration

In SRAM blocks designed with planar CMOS technology, the cell size is optimized to provide stable operation as provide similar time for read and write operations, and increase the noise tolerance. In FinFET technology, the discrete nature of fins (limited to a quantized number) impacts the design of the cell. Therefore, it is not possible to design the cell with an ideal robustness ratio such as in CMOS. Therefore, this increases the need for auxiliary circuits to provide adequate robustness, especially for the smaller cells (BURNETT et al., 2014).

Throughout the published works, many configurations have been defined for SRAM cell design. Three main approaches have been used as presented in (BURNETT et al., 2014), (JAN et al., 2012) and (KARL et al., 2013): the high-density (HD); the low voltage (LV) - which can also be referred to as low power (LP); and the high performance (HP). These settings use different numbers of fins for each part of the cell configuration (PU: PG: PD). The HD, LV and HP configurations are: (1:1:1), (1:1:2), and (1:2:2). This relation of transistor sizes can be checked in Table 2.2.]A layout simplified of the 6T FinFET-based SRAM for the three structures: HD, LV, and HP cells are depicted in Figure 2.7. In the Figure, in green is represents the Fins, and in red the gates.

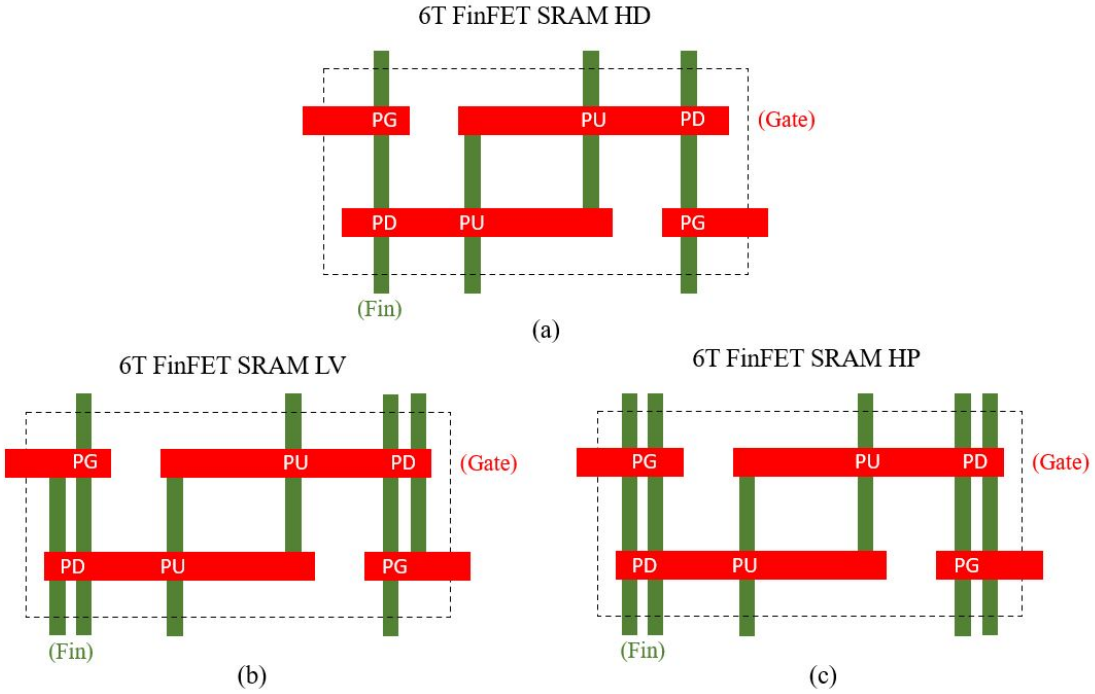
Table 2.2: Number of fins for FinFET SRAM cells

Configuration	**(PU:PG:PD)**
HD	(1:1:1)
LV	(1:1:2)
HP	(1:2:2)

Source: BURNETT et al., 2014.

With the objective of comparing electrical characteristics of FinFET-based SRAM of a 20 nm technology with a CMOS-based of 22 nm node, a study comparing physi-

Figure 2.7: Simplified Layout of the 6T FinFET-based SRAM a) HD b) LV c) HP.



Source: Copetti, 2021 based on the description given in BURNETT et al., 2014.

cal/electrical characteristics of 6T and 8T-SRAM was performed in (FARKHANI et al., 2014). The comparison confirms that FinFET presents lower process variations, lower leakage power consumption, more robustness, and reliability.

3 FAULTS IN FINFET-BASED SRAM

This Chapter is presented some faults sources for the FinFET-based SRAM circuit that will be the research focus of this work, it is the resistive defects and the faults from radiation effects. Initially, the defects for planar CMOS are presented as a comprehension of how the defects could happen in FinFET technology, followed by the fault models related to SRAM blocks. Then, the existing study about the defects in FinFET-based SRAM technology is presented. Finally, the impact of single effects generate for radiation sources on FinFET-based SRAM is discussed.

3.1 Resistive Defects Definition

This work intends to study the behavior of defective memory cells under resistive defects. Therefore, a description of this kind of defect will be presented, along with the forms of manifestation and the methods used to identify and analyze it.

Resistive Defects are divided into resistive-open and resistive-bridge. The resistive-open defect is defined as a resistor between two nodes of a circuit that should be connected. When the resistive value between the nodes is high, a special case of this defect takes place that generates a well-known fault called stuck-open, thus blocking the transmission of the signal in the circuit (LI; TSENG; MCCLUSKEY, 2001). The Fault theory is presented in the Appendix A.

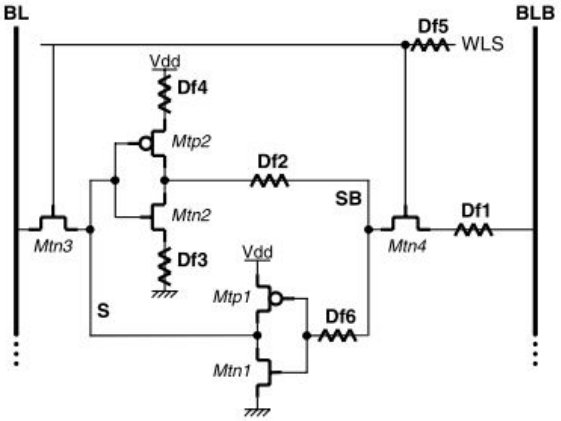
The resistive-bridge defect is defined as a resistor between two nodes of the circuit which should not be connected, forming a short. When the resistive value between the nodes is very high, it manifest as a special case of this defect that generates a well-known fault called stuck-at, thus locking the node with other nodes or supply signal (FONSECA et al., 2010a).

For ten years now, a variation of the resistive defect has received more attention, it is named weak resistive defect (or simply weak defect) which may result in dynamic faults. Different from the static faults which always cause a wrong value in the circuit, the dynamic faults are not noticeable in many manufacturing tests because they are designed to detect static faults (HAMDIOUI et al., 2003; HAMDIOUI et al., 2006). Weak defects may cause small voltage disturbance of the node of cell in SRAMs, that can generate time-dependent faults, that is, faults that occur at certain time intervals performing repetitive

operations in the cell (HAMDIOUI; GOOR, 2000). These faults will become recurrent as the circuit degrades.

The work developed in (DILILLO et al., 2004) models, in an SRAM cell, the dynamic behavior caused by resistive-open, through resistors inserted in the nodes of the circuit (by simulation), as it can be observed in Figure 3.1. Each resistor has been named with a Df (Defect) from 1 to 6.

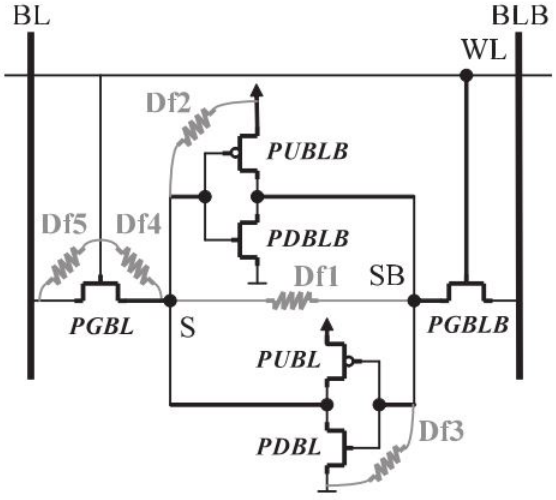
Figure 3.1: Resistive-open Defect characterized in an SRAM cell.



Source: DILILLO et al. 2004.

Another work was developed in (FONSECA et al., 2010a) that models, in an SRAM cell, the dynamic resistive-bridge defects through resistors inserted between the nodes of the circuit, as can be observed in Figure 3.2. Again, each resistor has been named with a Df (Defect) from 1 to 5.

Figure 3.2: Resistive-bridge defect characterized in an SRAM cell.



Source: FONSECA et al. 2010a.

3.2 Fault Models Associated to Resistive Defects

The existence of imperfections in the manufacturing process may lead the memory cells to be affected by manufacturing defects such as resistive-open and/or resistive-bridge defects that can compromise the correct behavior of the device. These defects can be characterized as strong or weak defects based on the nature of the fault they sensitize: strong defects are usually related to static faults, while weak defects are associated with dynamic faults. Faulty behaviors can be specified using Fault Primitives (FP), which characterizes the sensitizing sequence (S), the faulty behavior observed (F), and the output of read operations (R) (GOOR; AL-ARS, 2000), it follows the notation <S/F/R>. A non-empty set of fault primitives is known as a Functional Fault Model (FFM). The FPs can be classified as static or dynamic according to the number of required operations in order to sensitize the fault. Furthermore, the number of necessary operations to sensitize the fault may depend on many factors, such as defect resistance, operating temperature, process corner, among others (DILILLO et al., 2005).

Additionally, an FP can also be classified by the number of cells involved: single-cell and multi-cell FP. In a single-cell FP, faulty behaviors are only observed in the defective cell. In multi-cell FP (also known as coupling-faults), two cells (or two groups of cells) interact to produce a fault. The cell that suffers the faulty behavior is the victim (v-cell), while the cell that triggers the fault is the aggressor (a-cell). It is important to note that the resistive defect may be present either in the a-cell and/or in the v-cell (GOOR; AL-ARS, 2000; HAMDIOUI; AL-ARS; Van De Goor, 2002). Whereas an FFM is defined as a set of FPs, FFM will assume their characteristics, resulting in the following classifications: static and dynamic FFM; single-cell and multi-cell FFM. In more details, FFMs can represent the following fault space that was considered in this work, and described in (GOOR; AL-ARS, 2000):

- State Fault (SF_x) (GOOR; AL-ARS, 2000): a cell is said to have a SF if its logic value flips when no operation is performed on it;

- Transition Fault (TF_x) (GOOR; AL-ARS, 2000): a cell is said to have a TF if it fails to undergo a transition from ‘0’ to ‘1’ when it is written;

- Write Disturb Fault (WDF_x) (GOOR; AL-ARS, 2000): a cell is said to have a WDF if a non-transition write operation causes a transition in it;

- Read Destructive Fault (RDF_x) (ADAMS; COOLEY, 1996): a cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns the incorrect value to the output. This type of fault can also have a dynamic behavior classified as $dRDF_{xy}$ (GOOR; AL-ARS, 2000);

- Deceptive Read Destructive Fault ($DRDF_x$) (ADAMS; COOLEY, 1996): a cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, but changes the contents of the cell. This type of fault can also have a dynamic behavior classified as $dDRDF_{xy}$ (GOOR; AL-ARS, 2000);

- Incorrect Read Fault (IRF_x) (GOOR; AL-ARS, 2000): a cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, even though the correct value is still stored in the cell. This type of fault can also have a dynamic behavior classified as $dIFR_{xy}$ (GOOR; AL-ARS, 2000);

- Stuck-at Fault (SAF_x) (GOOR, 1991): a cell is said to have a SAF (also know State Fault) when the cell is stuck and stores only one logic value '0' or '1';

- No Store Fault (NSF) (FONSECA et al., 2010a): this fault is the opposite of SAF, where a cell with NSF cannot retain any logic value in their nodes;

- Weak Read Fault (WRF) (FONSECA et al., 2010a): a cell is said to have a WRF when, during the read operation, the sense amplifier cannot produce the correct logic output due to the small voltage difference between bit lines.

There is also a special analysis of dynamic fault, which can manifest in one cell through the influence of another cell. Therefore, operations are performed on aggressor cell (a-cell), but the activation through *WL* affects a victim cell (v-cell) on the same line. It is known as dynamic two-cell FFM (HAMDIOUI; AL-ARS; Van De Goor, 2002).

- Disturb Coupling Fault (CFds) (GOOR; AL-ARS, 2000): This fault occurs in groups of at least two cells where it is sensitized when a read or write operation in an a-cell affects v-cell or a group of v-cells, forcing them to change their stored values. This type of fault can also have a dynamic behavior classified as $dCFds_{x;yz}$ (GOOR; AL-ARS, 2000);

- Transition Coupling Fault (CFtr) (GOOR; AL-ARS, 2000): This fault occurs when a transition write operation performed on the v-cell fails due to a given logic value

stored in the a-cell. Thus, the fault is sensitized by a write operation on the v-cell and setting the a-cell into a given state;

- Read Disturb Coupling Fault (CFrd) (GOOR et al., 1996): This fault occurs when a read operation performed on v-cell changes the data in the cell and returns the incorrect value on the output if a given value is present in the a-cell. This type of fault can also have a dynamic behavior classified as $dCFrd_{x;yz}$ (GOOR; AL-ARS, 2000);

- Incorrect Read Coupling Fault (CFir) (GOOR; AL-ARS, 2000): This fault occurs when a read operation performed on v-cell returns an incorrect value on the output when a given value is present in the a-cell. This type of fault can also have a dynamic behavior classified as $dCFir_{x;yz}$ (GOOR; AL-ARS, 2000).

Table 3.1 shows the FFMs observed in this work and their respective FPs. As previously mentioned, an FFM is composed of a set of FPs represented by <S/F/R>. On single-cell faults, S may assume none or one operation of read or write for a static FFM, and two or more operations for dynamic FFM.

For simplification purposes, the FPs of dynamic FFMs are represented by only two operations. F represents the faulty behavior of the cell and is represented by a logic '1' or '0'. R is the output of a read operation, represented by a logic '0' or '1'. If no read operation is performed, '-' is adopted, the symbol $\forall$ means that any write operation can be performed. For coupling faults, S assumes the form of x;y, where x is the operation in the a-cel,l and y is for v-cell. Furthermore, xx is used to represent a dynamic behavior of more than one operation. It is important to note that, in this work, dynamic FPs are comprised of a write operation followed by consecutive n read operations. Thus, it is necessary to repeatedly read a cell and evaluate the retrieved value (GOOR; AL-ARS, 2000).

3.3 Defects in FinFET-based SRAM Technology

In the literature there are some studies related to defects in FinFET-based SRAMs. The paper (LIN; CHAO; HSU, 2013), was investigated the gate oxide short (GOS) effects in FinFETs. This work proposes one test method to FinFET-based SRAM. It was discovered the behavior in FinFET of saturation drain current decreasing are more difficult to detect over the planar CMOS. These tests can detect undetectable GOSs of traditional tests.

Table 3.1: Functional Fault Models and their respective Fault Primitives.

FFM	Fault Primitives
SF_x	<0/1/->; <1/0/->
TF_x	<0w1/0/->; <1w0/1/->
WDF_x	<0w0/1/->; <1w1/0/->
RDF_x	<0r0/1/1>; <1r1/0/0>
$dRDF_{xy}$	<0w0r0/1/1>; <1w1r1/0/0>; <1w0r0/1/1>; <1w1r1/0/0>
$DRDF_x$	<0r0/1/0>; <1r1/0/1>
$dDRDF_{xy}$	<0w0r0/1/0>; <0w1r1/0/1>; <1w0r0/1/0>; <1w1r1/0/1>
IRF_x	<0r0/0/1>; <1r1/1/0>
$dIRF_{xy}$	<0w0r0/0/1>; <0w1r1/1/0>; <1w0r0/0/1>; <1w1r1/1/0>
SAF_x	<∀/1/->; <∀/0/->
CFds	<x;0/1/->; <x;1/0/->
$dCFds_{x;yz}$	<xx;0/1/->; <xx;1/0/->
CFtr	<x;0w1/0/->; <x;1w0/1/->
CFrd	<x;0r0/1/1>; <x;1r1/0/0>
$dCF_{x;yz}$	<x;0w0r0/1/1>; <x;0w1r1/0/0>; <x;1w0r0/1/1>; <x;1w1r1/0/0>
CFir	<x;0r0/1/0>; <x;1r1/0/1>
$dCF_{x;yz}$	<x;0w0r0/1/0>; <x;0w1r1/0/1>; <x;1w0r0/1/0>; <x;1w1r1/0/1>

Source: GOOR; AL-ARS, 2000.

The effects of open defects, logic and dynamic behavior, located in the gate of FinFET in logic cells is studied in (MESALLES et al., 2016). The location of defects in the gate influence the fault behavior, in some positions the fault is similar to planar CMOS, and in other is different. It reported that open defects in FinFET cells are more difficult to detect than planar CMOS.

A study aiming to model FinFET-specific faults and synthesizing test algorithms for their detection are developed in (HARUTYUNYAN et al., 2014b) and (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015). It shows that FinFET-based SRAM is more prone to dynamic faults and is more stable to process variations faults. Furthermore, it is shown that static coupling faults are typical for both FinFET and planar-based SRAM.

An analysis for Automotive Application-aware is developed in (TSHAGHARYAN et al., 2018) modeled testing of aging fault in FinFET-based SRAM. This analysis combines the impact of aging on process variation and different test conditions. A test solution was developed providing full coverage for aging faults.

The work presented in (PEREZ et al., 2020) analyzed the behavior of hard-to-detect full opens unique to FinFET in SRAM memory cells. In more detail, the work

focus on the behavior analysis of open-gate defects for the SRAM cell in its three modes of operations using realistic defect models. It was verified that to increase the detection of these faults a higher power supply voltage can be used in the SRAM cells.

Besides this analysis of defects in FinFET-based SRAM developed, there is not during the time of the development of this thesis the full map of each resistive defect in an SRAM block made of FinFET. This is one of the points of the contribution of this thesis.

3.4 Study of Radiation Effects in FinFETs

Effects of radiation in integrated circuits is a significant research topic. As FinFETs are a relatively new technology, studies about radiation effects in FinFET-based SRAM are of great importance, due to be a newer technology and there is little information regarding it. In the following subsections, the influence of radiation on integrated circuits will be presented along with the definitions of common terms in the field.

3.4.1 Single Event Effect

The Single Event Effect (SEE) is a singular event that occurs in integrated circuits that is caused by the strike of strongly ionizing particles. It occurs when an ionizing particle (heavy-ion or alpha particle, for example) reaches the IC and loses energy by forming electron-hole pairs along to the bulk, which can cause faults if collected in a reverse-biased PN junction. Therefore, if this charge is greater than the charge storing elementary information in the affected node the event manifests itself. Such kind of event can also be manifested by the physical changes that the particle can cause inside the transistor (NICOLAIDIS, 2011).

The SEE can be classified according to how the error is presented: hard error and soft error. Hard errors are non-recoverable errors, in other words, a defect generated in the circuit. An example is the Single Event Burnout (SEB), where the ionizing particle is strong enough to generate a plasma-filament inside the transistor resulting in a dielectric breakdown in gates or capacitors (HOHL; GALLOWAY, 1987).

Soft errors are bit inversions that may be recovered by a reset, a power cycle or simply a rewrite of the information. They include a great variety of manifestations depending upon the device considered. In analog devices, Single Event Transient (SET)

also called Analog Single Event Transient (ASET) is mainly transient pulses in operational amplifiers, comparators or reference voltage circuits. In combinational logic, SETs are transient pulses generated in a gate that may propagate in a combinatorial circuit path and eventually be latched in a storage cell as a flip-flop (NICOLAIDIS, 2011).

In bulk CMOS technology, parasitic current in PNPN structures may be triggered giving a Single Event Latch-up (SEL). It is associated with a strong increase in power supply current. The SEL can be destructive by overheating of the structure and localized metal fusion. A SEL needs a power cycle to be deactivated (NICOLAIDIS, 2011).

In memory devices (as SRAM cells), latches, and registers, single events are mainly called Single Event Upset (SEU). This corresponds to a flip of the cell state. When for one particle interaction many storage cells are upset, a Multi-Cell Upset (MCU) is obtained. If more than one bit in a word is upset by a single event, a Multi-Bit Upset (MBU) is obtained. For complex integrated circuits, loss of functionality due to perturbation of control registers or clocks is called Single Event Functional Interrupt (SEFI). Functionality may be recovered by a power cycle, a reset or a reload of a configuration register (NICOLAIDIS, 2011).

With the proximity of connections and the reduced supply voltage, FinFET-based SRAMs are becoming more susceptible to SEUs, even at ground level (ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO, 2015). Traditionally, the major sources of radiation-induced soft errors, at ground level or flight altitudes are: (1) alpha particles, originated by the radioactive contamination existing in the packaging (BAUMANN, 2001; KIM et al., 2018); (2) the high-energy neutrons from cosmic radiation (generating secondary reactions); (3) heavy-ions(HOHL; GALLOWAY, 1987) and (4) the interaction of cosmic ray thermal neutrons with devices containing borophosphosilicate glass (BAUMANN, 2001). The work reported in (HUBERT; ARTOLA; REGIS, 2015) shows that for SRAMs, protons, and muons (unstable elementary particles with a mass between the proton and electron and 2.2 μs lifetime (NAGAMINE, 2003)) are also among the particles able to generate SEUs at ground level in bulk FinFET technologies.

3.4.2 Single Events in SRAM Blocks

The ionizing particle that hits the transistor, entering its crystalline structure, creates electron-hole pairs along the particle ionization track, which may go deep in the body. The generated carriers may be collected in a PN Junction (such as drain-substrate or

drain-well), with the separation of electron-hole pairs and by the diffusion of minority carriers toward the space charge layer boundaries where they are accelerated by the electric field, generating a current pulse. The magnitude of the generated current pulse is proportional to the energy transferred by the particle inside the transistor, called Linear Energy Transfer (LET) (NICOLAIDIS, 2011).

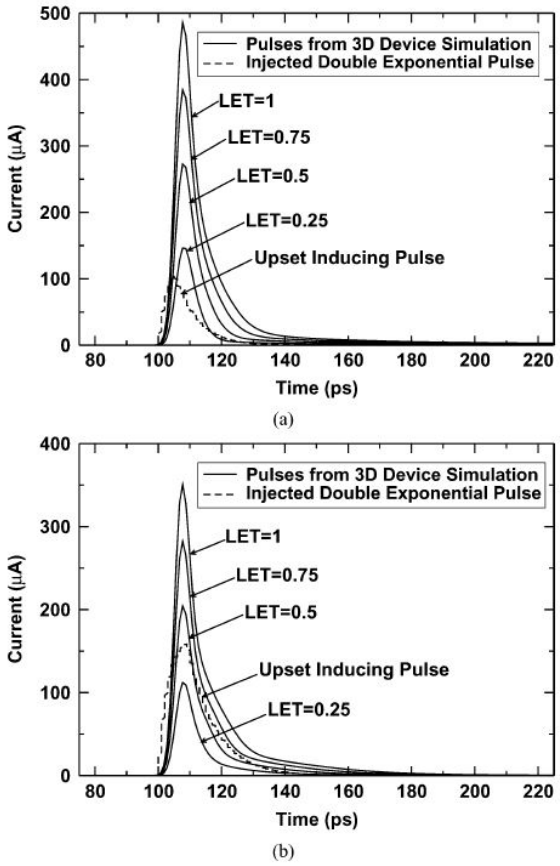
A mathematical equation, the well-established Messenger's double exponential model (MESSENGER, 1982) is often used to describe the waveform of the current pulse in circuit simulations. This waveform is arbitrary and mostly adapted to facilitate convergence in the calculation. In practice, several different waveforms can be obtained depending upon the location and length of the track (NICOLAIDIS, 2011).

To compare, (BAJURA et al., 2007) presents the relation of current pulses obtained from 3D device simulation (TCAD) and the classical double exponential pulse injected at critical nodes of SRAM in a 90 nm technology. The dashed curves in Figure 3.3 are the smallest double-exponential pulses that induce an upset in the SRAM following a strike in an "off" NMOS (a) and PMOS transistor (b), respectively. The cross-coupled inverters are highly asymmetric in this technology, the pull-down NMOS transistors have higher drive strength than the PMOS pull-ups. For this reason, there is a difference in the minimum injected total charge required for a bit upset to occur depending on the value stored at the cell.

This minimum injected total charge that causes a bit-flip is defined as a critical charge. It is important to mention that the definition of critical charge in SRAMs, according to (BAUMANN, 2005) is not as intuitive as for logic circuits, where it is associated exclusively with the charge stored in the node and the drive strength of the restoration transistors. In SRAMs the feedback plays an important role, collaborating with the behavior of the transient current pulse. Two ways of defining the critical charge can be found in the literature. The first one considers the value of deposited or collected charge that starts to generate bit-flips. The second definition considers the value of the charge flowing in excess during the transient current in the affected node, which considers also the charge flow due to the circuit dynamics (hence not merely the collected charge). Indeed, the critical charge values computed from 3D device simulation currents, according to (NASEER et al., 2007), are approximately 3 times smaller than those found using current models.

It is important to mention that in many experiments, a device's SEU threshold is expressed in terms of the threshold LET value (the minimum LET of incident particles

Figure 3.3: Charge collection photo-current profiles (plain lines) resulting from 3-D TCAD simulation of heavy-ion strikes on (a) an NMOS transistor, and (b) a PMOS transistor.



Source: BAJURA et al. 2007.

that start generating errors) instead of the critical charge. According to (CREME-MC), these two parameters are related by the formula:

$$Q_{crit} = \frac{LET_{th}.T.d.e}{X} \tag{3.1}$$

where: Q_{crit} is the critical charge, LET_{th} is the threshold LET expressed in MeV-cm²/mg, T is the device thickness in microns, d is the material density which value is 2.32 g/cm³ fo Si and 5.32 g/cm³ for GaAs, e is the electronic charge with value $1.602x10^{-7}$ pC, X is the energy needed to create one electron-hole pair which is 3.6 eV for Si and 4.8 eV for GaAs. Simplifying the formula for each material results, for Silicon:

$$Q_{crit} = 1.03x10^{-2}.LET_{th}.T[pC] \tag{3.2}$$

and for Gallium arsenide:

$$Q_{crit} = 1.78x10^{-2}.LET_{th}.T[pC]. \tag{3.3}$$

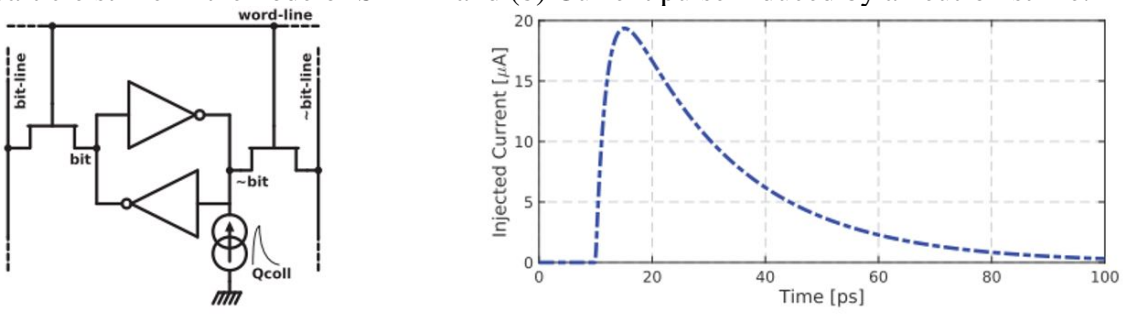
3.4.3 Drain Current under SEE in SRAM in new Technologies

For planar CMOS technology, the charge collection was accurately modeled by a double exponential current waveform as shown in Figure 3.3. However, for advanced technologies, the current pulse shape becomes much more complex. But, even for recent technologies as FinFET, the Messenger's double exponential model it still being applied due to its simplicity (ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO, 2015). In the mentioned work a study of radiation-induced soft errors in FinFET-based SRAMs under process variations is performed, using electrical simulations with Arizona State University predictive models (PTM) (ASU, 2011). The study uses a current source in an internal node of an SRAM to simulate a SEE as shown in Figure 3.4 (a). The characteristics of the current follow the parameters described in (PETERSEN et al., 1982; MAVIS; EATON, 2007), in which the current source is a double exponential following the equation:

$$I(t) = \frac{Qcoll}{\tau_2 - \tau_1}.(e^{\frac{-t}{\tau 2}} - e^{\frac{-t}{\tau 1}}) \tag{3.4}$$

where I(t) is the injected current, τ_1 and τ_2 are the rise and fall timing constants, dependent on the particle and the technology, and Q_{coll} is the amount of charge collected by the circuit. The work uses the data described in (LIU et al., 2014) of an induced current pulse caused by neutron particle which takes around 80 ps and with the parameters τ_1 = 2 ps and τ_2 = 20 ps, in the FinFET technology. In Figure 3.4 (b) the double exponential wave used to model the strike at electrical level is depicted.

Figure 3.4: Electrical configuration of the experiment in (ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO, 2015) : (a) Schematic of current pulse induced by the particle strike in the node of SRAM and (b) Current pulse induced by a neutron strike.



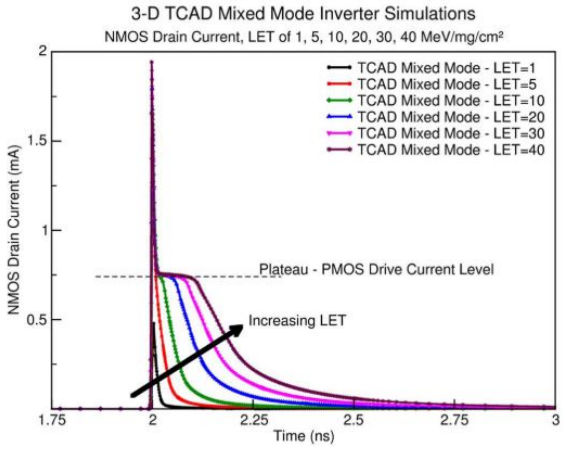
(a) (b)

Source: ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO 2015.

Some works try to model the correct drain current behavior for smaller technologies as the work in (KAUPPILA et al., 2009) and in (BLACK et al., 2015). The work

(KAUPPILA et al., 2009) describes a study of radiation-induced in TCAD with an inverter in 90 nm CMOS technology using the model of (PETERSEN et al., 1982; MAVIS; EATON, 2007). The experiments describe that the drain current observed has a peak current and a plateau region with a duration higher than the standard double exponential, Figure 3.5 present this behavior. Note that the plateau duration increase together with the LET.

Figure 3.5: 3D TCAD simulations results showing single-event induced nMOS drain current for various LET values from the work in (KAUPPILA et al., 2009).

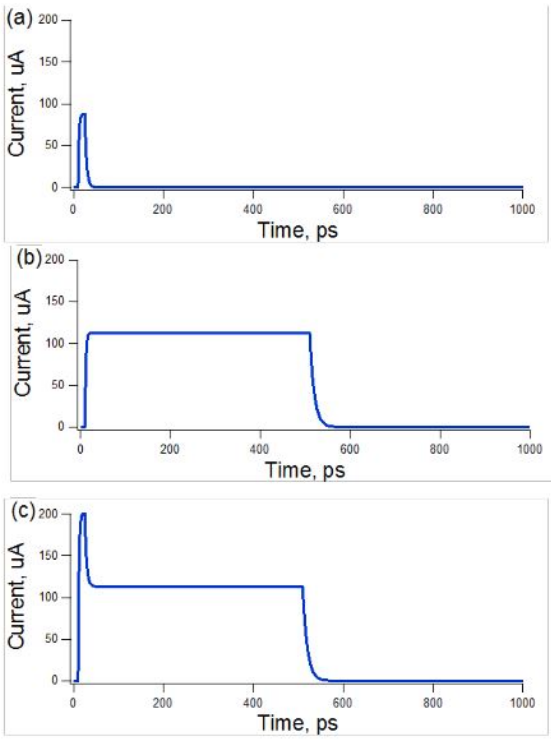


Source: KAUPPILA et al. 2009.

In (BLACK et al., 2015) this drain current behavior was modeled as described earlier for a 90 nm technology. The work uses a combination of two curves to determine a new current curve to perform SET simulations, a dual double-exponential current source. This dual double-exponential current source model is composed of two parallel double-exponential current sources, one for prompt charge collection ($I_{Prompt}(t)$) and other for sustained charge collection ($I_{Hold}(t)$). As identified in Figure 3.5, there is a short high current peak (I_{Peak}), followed by a sustained shelf double exponential current source with I_{Peak} equal to the short high current. Figure 3.6 shows the example of the two individual current sources and the result of their parallel combination, the dual double-exponential current source model.

Both individual current sources presented in Figure 3.6 - (a) and (b) have four parameters that need to be determined: I_{Peak}, (t_{d2} - t_{d1}), τ_1 and τ_2. Based on results obtained from the experiments of an SEE simulation on a single transistor, the three parameters of time are setted for each current source, the short duration current source $I_{Prompt}(t)$ has (t_{d2} - t_{d1}) = 15 ps, τ_1 = 2 ps, and τ_2 = 4 ps. For the sustained current source $I_{Hold}(t)$: τ_1 = 2 ps, and τ_2 = 10 ps, (t_{d2} - t_{d1}) are variable depending of the amount of deposited charge (BLACK et al., 2015).

Figure 3.6: Drain Current with plateau modeled: (a) short peak, I_{Prompt}(t), (b) sustained, I_{Hold}(t), and (c) dual double-exponential current sources.



Source: BLACK et al. 2015.

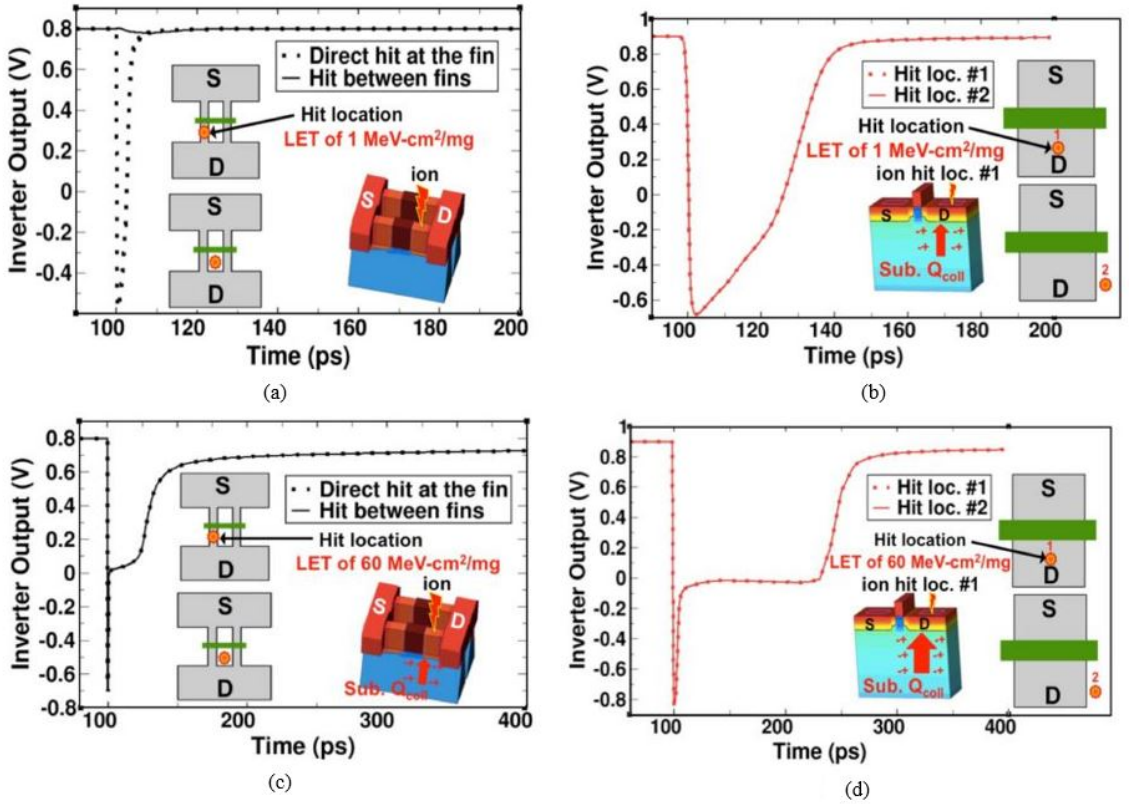
The peak values for I_{Peak} and I_{Hold} are determined through a set of simulations using a basic inverter and a capacitor in the output as determined by (BLACK et al., 2015). Firstly, the auxiliary parameter, threshold current, is determined (I_{Thresh}) with the necessary current to flip the inverter output from V_{DD} to V_{SS} using the parameters of I_{Prompt}(t): (t_{d2} - t_{d1}) = 15 ps, τ_1 = 2 ps except τ_2 from I_{Hold}(t), τ_2 = 10 ps. Then, to the current peak from I_{Hold}(t), the same procedure is used, with the parameters of I_{Hold}(t): (t_{d2} - t_{d1}) = 500 ps, τ_1 = 2 ps, and τ_2 = 10 ps. The value of 500 ps is a parameter obtained in (NARASIMHAM et al., 2007), where it is verified that a SET pulse produced by heavy ions in 90 nm CMOS is observed between 500 ps to 900 ps. So, 500 ps is was chosen as the minimum for the current occurrence. Finally, the peak current from the I_{Prompt}(t) is determined by the equation:

$$I_{Prompt} = I_{Thresh} - I_{Hold}. \tag{3.5}$$

However, some works study the behavior of transient curves in FinFET, as for example in (NSENGIYUMVA et al., 2017), in which a comparison between the radiation incidence in a 16 nm bulk FinFET inverter and a 28 nm bulk planar inverter is performed using 3D TCAD. The radiation incidence in the TCAD simulation follows the method-

ology presented in (NSENGIYUMVA et al., 2016), as a heavy-ion model with Gaussian charge distribution with a track radius of 10 nm. It was used two levels of LET intensity called low (1 Mev-cm^2/mg) and high (60 Mev-cm^2/mg) with could cause a charge collected by the transistor beyond the critical charge necessary to cause a bit-flip. These LETs are shown in Figure 3.7 where the orange spots in the transistor layout represent the ion hit location. Analyzing the low-LET results, the behavior of curves is similar to the traditional double exponential curve, however, with high-LET, the curve has a different aspect. It is important to mention that in the low-LET experiment, there is current manifestation only when the particle hits directly the fins, differently from the other cases.

Figure 3.7: Impact of transistor structure on low-LET 3D TCAD single-event transient response: (a) 16 nm bulk FinFET inverter low-LET, (b) 28 nm bulk planar inverter low-LET, (c) 16 nm bulk FinFET inverter high-LET and (d) 28 nm bulk planar inverter high-LET.



Source: NSENGIYUMVA et al. 2017.

Considering the background presented of SEE in FinFET-based SRAM, in this thesis, a study of SEE was carried out in the FinFET SRAM cell considering the structure alternatives and considering the aggregate impact of resistive defects. The motivation for this work comes from the lack of information about how these combined effects affect FinFET SRAM cells. This type of analysis is unprecedented in the literature and the main contribution of this thesis.

4 RELIABILITY ANALYSIS OF FINFET-BASED SRAM UNDER RESISTIVE DEFECTS

This chapter presents the reliability analysis performed on FinFET-based SRAM considering the presence of resistive defects. The specification and implementation of the SRAM design used in this study are also detailed in this chapter.

4.1 Specification

The analysis of defects is carried out in an SRAM block with 1024 lines per 1024 columns, as the design presented in (MARTINS et al., 2016). However, only eight columns (8 x 8) of SRAM cells are implemented along with the auxiliary operating circuits. Capacitances are used to emulate the remainder of the block. These capacitances were calculated using the capacitance input from the cells. Posteriorly, with the study of different nodes, each capacitance needed to be calculated again.

The electrical simulations were performed using the Hspice^{TM} tool from Synopsys. A Predictive Technology Model (PTM) available in (ASU, 2011) is used to model the FinFETs. This library was developed in cooperation with ARM, modeling a FinFET technology, based on BSIM-CMG as described in section 2.13. This library presents models for technological nodes of 20, 16, 14, 10 and 7 nm for HP (High Performance) and LSTP (Low-Standby Power) applications.

The SRAM cells architecture employed in the developed array are the 6T (6 transitors) type, as shown in Figure 2.6. The auxiliary blocks are described in Chapter 2.6. The cell design consists of High Density (HD) model, which is explained in Chapter 2.7. The simulation setup, the modeled defects and the evaluation of defect size on fault behavior are described in the following.

4.2 Simulation Setup

The electrical simulations considers a FinFET-based SRAM block connected to functional blocks, using a 20 nm low-standy power PTM compact model and considering temperatures of -40 ºC, 27 ºC, and 125 ºC. Furthermore, this work analyzes the impact of resistive defects on SRAM blocks designed in smaller technological nodes, such as 16 nm, 14 nm,

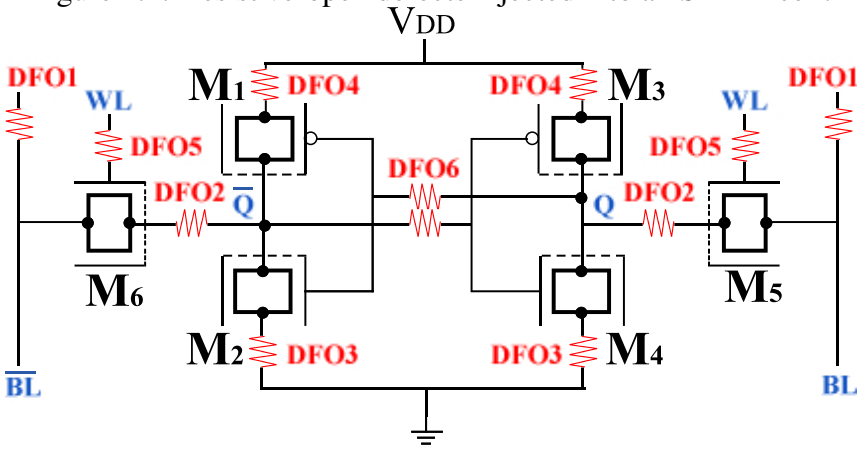
10 nm, and 7 nm. Table 2.1 in Chapter 2.13 presents the supply voltage adopted for each node. The operational clock signal frequency chosen is set to 1 GHz.

To recreate an SRAM block as genuine as possible, auxiliary circuitry was used. A differential sense amplifier was adopted for read operations, while write operations were assisted by write buffers. Pre-charge circuits, row-decoders, and registers complete the setup. All circuits, including memory cells, were designed using the low power technological library. The auxiliary circuits are described in the Appendix A. As stated before, the SRAM cell was designed using only one fin in each transistor to achieve higher densities.

4.2.1 Modeled Defects

In this work, a set of 12 defects was modeled and injected into a memory cell, one at a time. Six of them are classic resistive-open defects, previously studied for bulk CMOS technology (BORRI et al., 2005). In summary, resistive-open defects are non-designed resistances between two nodes that have a connection. Figure 4.1 depicts the scheme adopted to model the resistive-open defects.

Figure 4.1: Resistive-open defects injected into an SRAM cell.

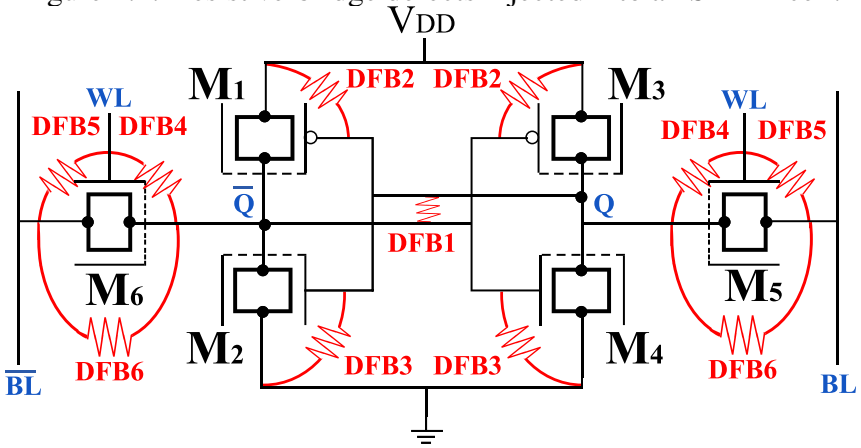


Source: COPETTI et al. 2017.

The other six analyzed defects are resistive-bridges, which are resistive connections between nodes that, upon design, were not connected (DILILLO et al., 2004). Figure 4.2 shows the set of resistive-bridge defects analyzed in this work. DFB1-DFB5 are classic resistive-bridge defects that have been previously analyzed in CMOS technology (FONSECA et al., 2010a). DFB6 is a new defect that, considering FinFET architecture, may create a bridge between drain and source of transistors (LIU; XU, 2012). Due to the

cell's symmetry, only one instance of each defect is necessary to analyze their impact on the cell's behavior.

Figure 4.2: Resistive-bridge defects injected into an SRAM cell.



Source: COPETTI et al. 2017.

4.2.2 Evaluation of Defect Size on Fault Behavior

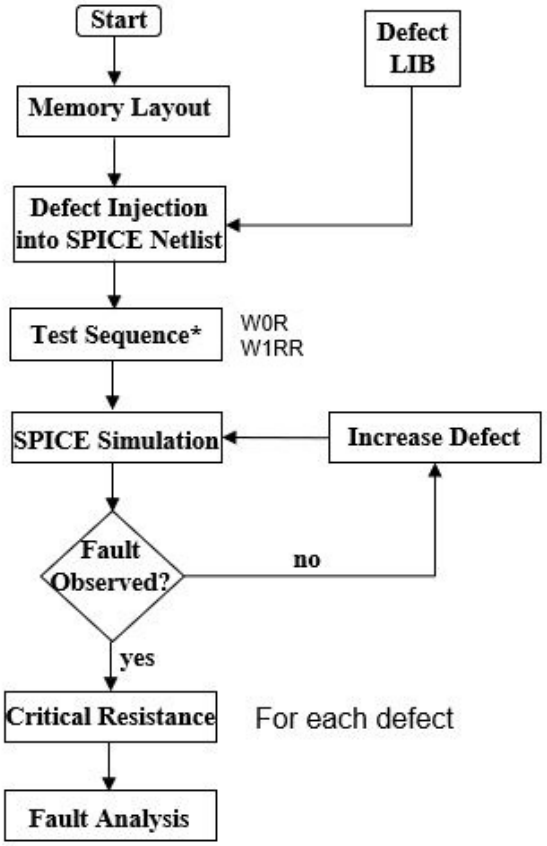
To analyze the impact of each defect on the behavior of memory cells, an automated tool was developed. For each defect, simulations were performed while varying the resistance value of modeled defects up to a maximum of 20 MΩ, or until the occurrence of a static fault. The resistance on this iteration is defined as "upper limit" and, based on this resistance value, the tool simulates the circuit over again, this time using increasingly weaker resistances to observe either dynamic faults or fault-free behavior.

Applying this procedure, it is possible to observe three distinct cases: the defect is too weak to sensitize any type of fault at the logic level, the defect is weak but great enough to sensitize dynamic faults, and the defect is great enough to sensitize static faults. The output of read operations and internal nodes of the cell are analyzed to identify faults.

To evaluate defects that result in single static faults, simple verification of the value is performed after the defect is injected. The experimental procedure follows the test flow presented in Figure 4.3. The developed automatic tool was developed in C language, it injects defects into the SPICE Netlist of the memory array, based on a defect library file (LIB), it is a set of defective cells developed in the netlist. A set of test sequences is executed by the tool for each defect composed of a pair of operations of write and read to analyze static faults (0W1R1, 1W0R0). To evaluate dynamic faults, a write followed by n read operations is performed ($0W1(R1)^n$ and $1W0(R0)^n$), where n is number of op-

erations). Note that n was defined to be at a maximum of 7 read operations because was verified that with a greater number of read operations the fault was not detected, in this testing block. The analysis for coupling faults is similar, with the exception that for this type of fault, operations may be performed in certain cells, while evaluation is performed in a different cell or group of cells in the array. The analysis of the electrical parameters was made by the tool through the measure files given by the Hspice.

Figure 4.3: Defect Injection Flow.



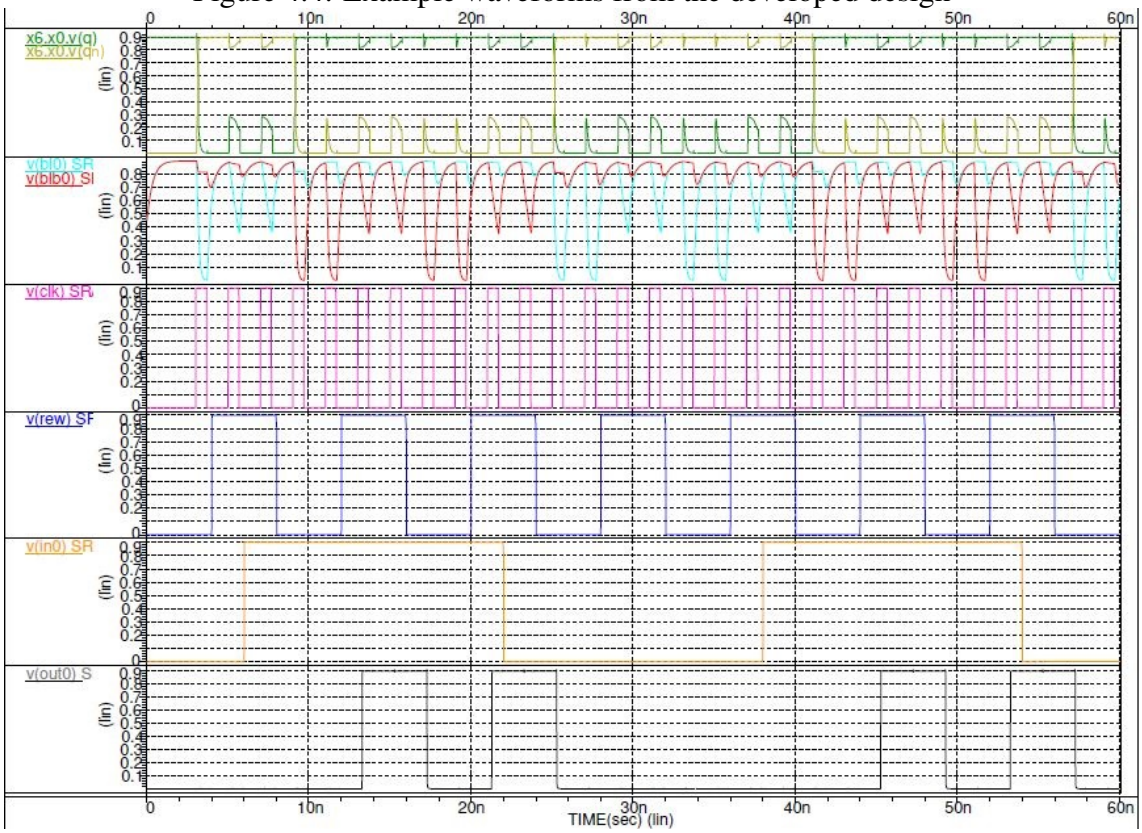
Source: The Author (2020).

4.3 Validation

An example of the behavior of the simulated SRAM block without defects is shown in Figure 4.4. In this example, a series of readings are being carried out and written in the cells of the same line.

The observed signals of Figure 4.4 are ‘v(bl0)’ and ‘v(blb0)’ which are the bit lines of the first column. The signals ‘v(q)’ and ‘v(qn)’, which are the internal signals of a cell in the first column. The ‘v(rew)’ signal is the write and read control defined during the low level of ’v(clk)’ and it is read at the rise of ‘v(clk)’. The block is in write mode when

Figure 4.4: Example waveforms from the developed design



Source: The author (2018).

'v(rew)' is at low level, and at the high level the block will be in reading mode. In writing mode, the data in 'v(in0)' is used for write, and 'v(out0)' signal is given generated in the reading. Changes within the cell and in the bit columns can be observed during reading and write operations.

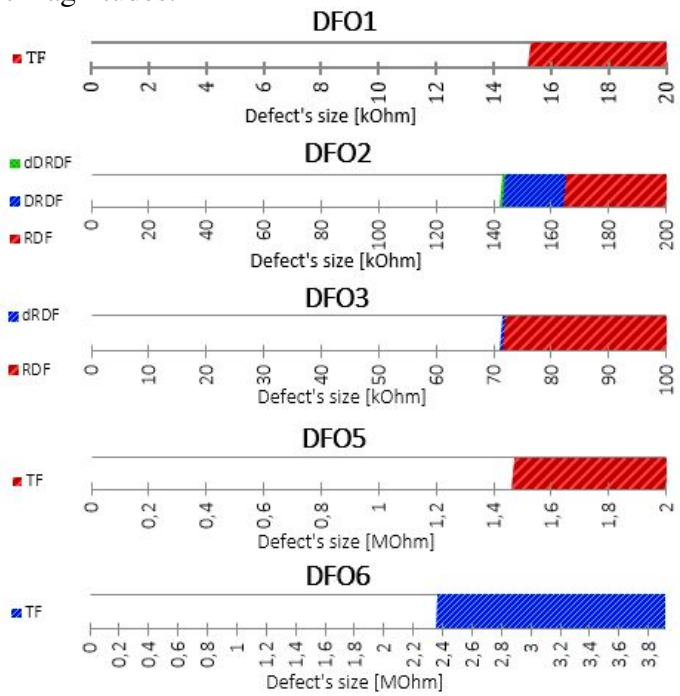
4.3.1 Results of Resistive Defect Analysis

This subsection summarizes the results and discusses the relationship between defect size and cell behavior. First, results obtained for resistive-open defects and resistive-bridge defects considering the 20 nm node in a nominal temperature of 27 °C are presented. Next, an evaluation comparing the behavior of this same node in temperatures of -40 °C and 125 °C are presented. These analyses were first presented in (COPETTI et al., 2017), and are further extended by repeating the same experiment using smaller technological nodes. In all analyses, the obtained results are the fault observed and the critical resistance.

4.3.1.1 Resistive-Open Defects

Results for resistive-open defects are shown in Figure 4.5, which illustrates the relationship between defect size and faults observed on affected cells at room temperature (27 ºC). For DFO4, within the specified range of 0-20 MΩ, no faults were observed at 27 °C. Observing the remaining defects, it is possible to conclude that DFO1 is the most critical one; it demonstrates a fault-free interval of only 15.3 kΩ. Dynamic behaviors were only reported for DFO2 and DFO3. It is possible to summarize the results: TFs can be observed for defects DFO1, DFO5, and DFO6. RDF and dRDF can be observed injecting DFO3. Finally, DRDF and dDRDF are observed when injecting DFO2 and DFO3. An example of a dDRDF-7 occurring with a DFO3 of 71.5 kΩ is shown in Figure 4.6.

Figure 4.5: Faults observed during simulations of SRAM cells affected by resistive-open defects of different magnitudes.

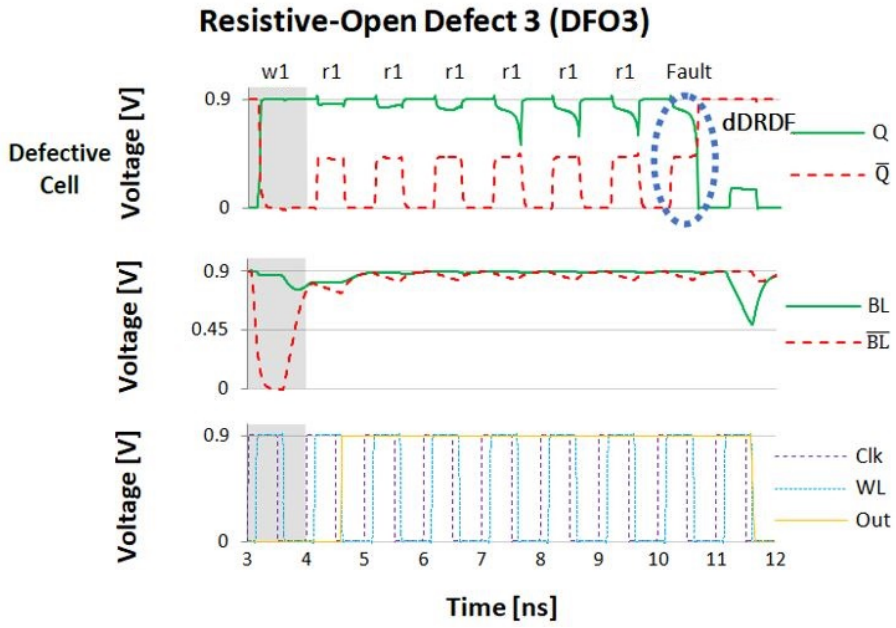


Source: COPETTI et al. 2017.

4.3.1.2 Resistive-Bridge Defects

As previously mentioned, resistive-bridge defects create connections between nodes that were not planned upon the design. Therefore, depending on the defect size, such defects may actively unbalance the cell and cause faults such as NSF and SAF. The full relation between defect size and observed faults is depicted in Figure 4.7. From the obtained results, it is possible to conclude that the most critical resistive-bridge defect is DFB3 as it creates the greatest faulty behavior interval (from 0 to 46 kΩ).

Figure 4.6: Example of a dDRDF-7 occuring with a DFO3 of 71.5 kΩ.

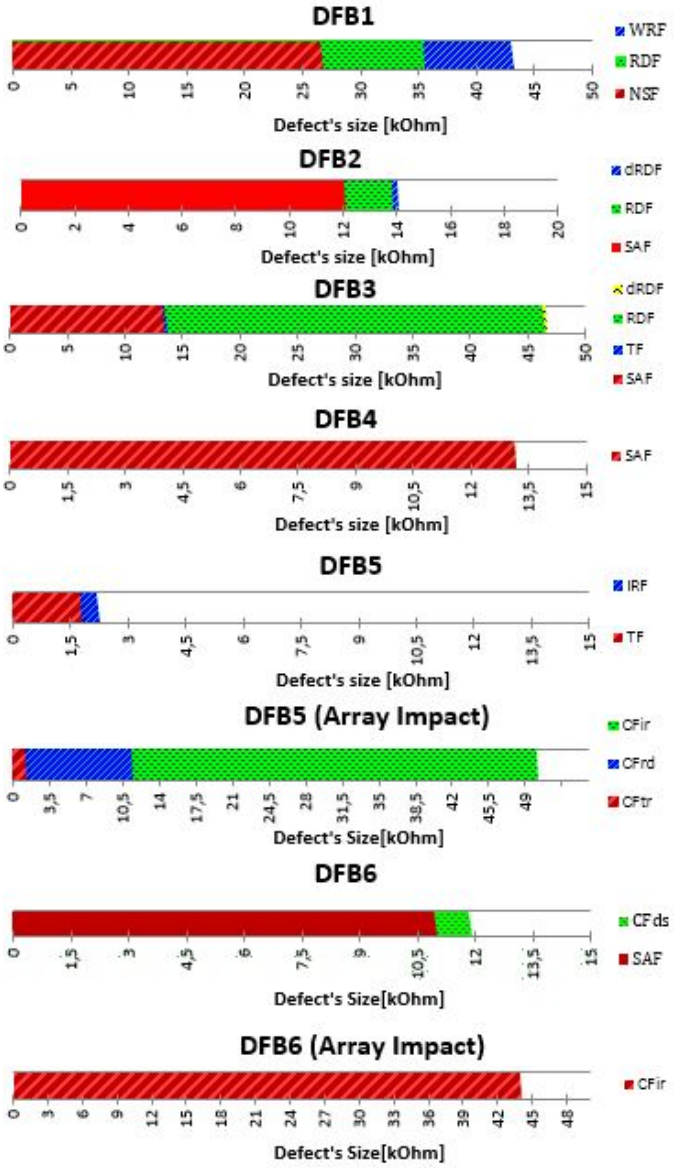


Source: COPETTI et al. 2017.

However, there is a different aspect of resistive-bridge defects the results draw special attention to: as such defects create connections, a resistive-bridge defect affecting one cell may have an impact in other fault-free neighbour cells, causing Coupling Faults (CF). In Figure 4.7, this was defined as “Array Impact”, and observed for defects DFB5 and DFB6. It is important to mention that these “Array Impact” faults affected fault-free cells. Figure 4.8 depicts this behavior. It shows the simulation of a cell that is located at row 0 and is affected by a resistive-bridge defect (DFB5) that creates a connection between the word line 0 (WL0) and $\overline{BL}$ of magnitude 11.5 kΩ. This defect size does not sensitize any fault in a-cell (aggressor), as shown in Figure 4.7. A write ‘0’ operation is successfully performed on the cell, followed by three consecutive read operations in the same cell on row 0. The faulty behavior is observed in a v-cell (victim) in row 1, as a dynamic CF_{rd}, and in a v-cell in row 2 as a CF_{rd}.

By performing a read operation on row 1 (Figure 4.8), $\overline{BL}$ is not able to charge as it is being drained by the *WL0*. This results in an IRF, as can be seen in the *Out* signal. As all of the three analyzed cells are located on the same column, they all share the same output signal. A subsequent read operation has a bigger impact, causing a dynamic CF_{rd} on the cell. The same destructive behavior is observed when performing subsequently read operations in another fault-free cell from a different row, this time a static CF_{rd} can be observed.

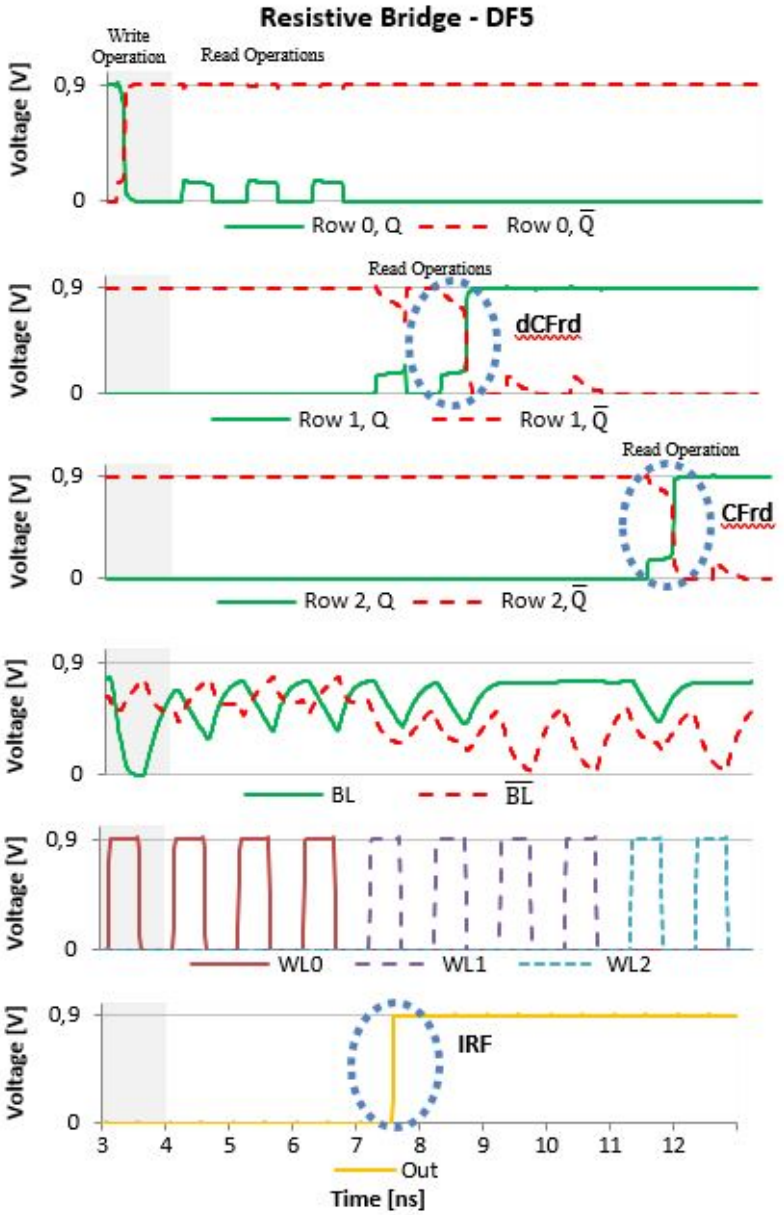
Figure 4.7: Faults observed during simulations of SRAM cells affected by resistive-bridge defects of different magnitudes.



Source: COPETTI et al. 2017.

Additionally, operations performed on fault-free cells can affect defective cells as long as they are in the same column. This way, the fault-free cell is the aggressor and the faulty cell is the victim. Figure 4.9 illustrates this fault behavior on a cell affected by DFB6, which creates a resistive-bridge between source and drain of transistor M5, connecting $\overline{BL}$ and $\overline{Q}$. As the fault-free cell on row 2 is written, the value on the defective cell on row 1 is flipped. This happens due to the shared connection between $\overline{BL}$ and $\overline{Q}$. As $\overline{BL}$ is discharged due to a write '0' operation, $\overline{Q}$ discharges as well, causing a misbalancing, and eventually a flip on the stored value. This can also be considered as a "following-signal" behavior, as $\overline{Q}$ follows the value on $\overline{BL}$. The same behavior is observed on cells affected by DFB4, as the affected node is now connected to *WL*.

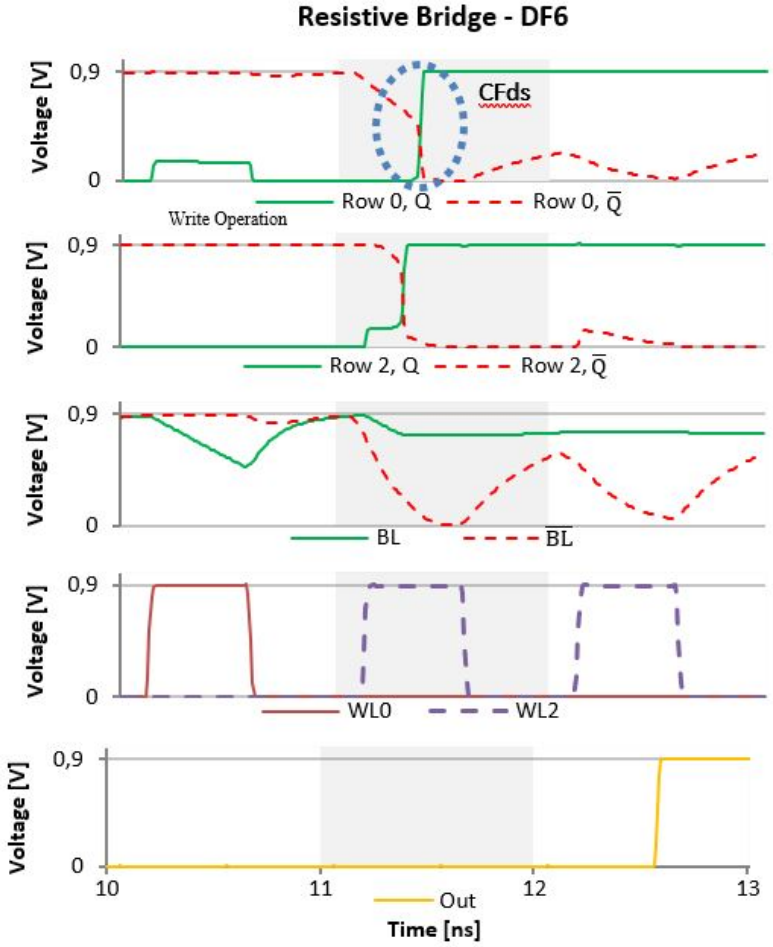
Figure 4.8: Simulation output of a cell affected by a resistive-bridge causing faults on other cells of the array.



Source: COPETTI et al. 2017.

Figure 4.10 depicts this particular behavior. It shows the simulation of a cell affected by a DFB4 of magnitude 13 kΩ. In Figure 4.7, this behavior is classified as SAF. This defect creates a connection between $\overline{Q}$ and WL. This way, $\overline{Q}$ follows the voltage on WL, causing an inconsistent behavior that may not be trivial to detect. The behavior observed resembles a SAF as the cell can only store '1' while the word line is off.

Figure 4.9: Simulation output of a cell affected by a resistive-bridge defect suffering a destruction fault caused by an operation in a neighbour cell.



Source: COPETTI et al. 2017.

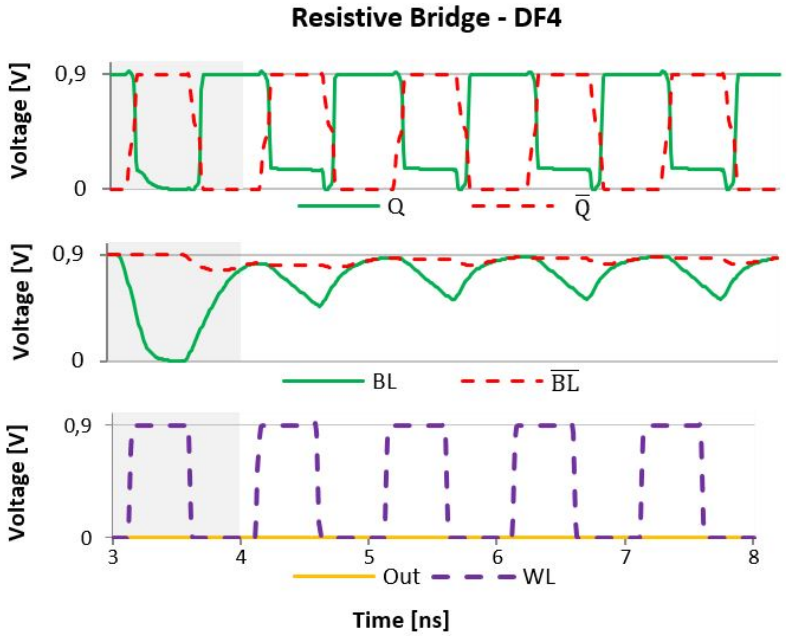
4.3.1.3 Impact of power supply variation

In order to understand the impact of power supply voltage on the functional behavior of FinFET-based SRAM cells in the presence of resistive defects, electrical simulations have been performed varying power supply voltage from 0.7 V to 1.1 V, adopting steps of 0.05 V.

In the next graphs in Figure 4.11, the faulty behavior associated with resistive-open defects will be analyzed while varying the power supply voltage. Figure 4.11 - (a) depicts the behavior of the FinFET-based SRAM cell in the presence of DFO1. It is possible to observe that increasing the power supply voltage makes the FinFET-based SRAM cell less robust to TF with the increase of voltage.

Figure 4.11 - (b) depicts the results related to DFO2. The observed faulty behavior, when varying the power supply voltage and increasing the defect size, is similar to the one observed when injecting a DFO1. The difference is that instead of observing a TF

Figure 4.10: Simulation output of a cell affected by a resistive-bridge defect connecting $\overline{Q}$ to the word line.



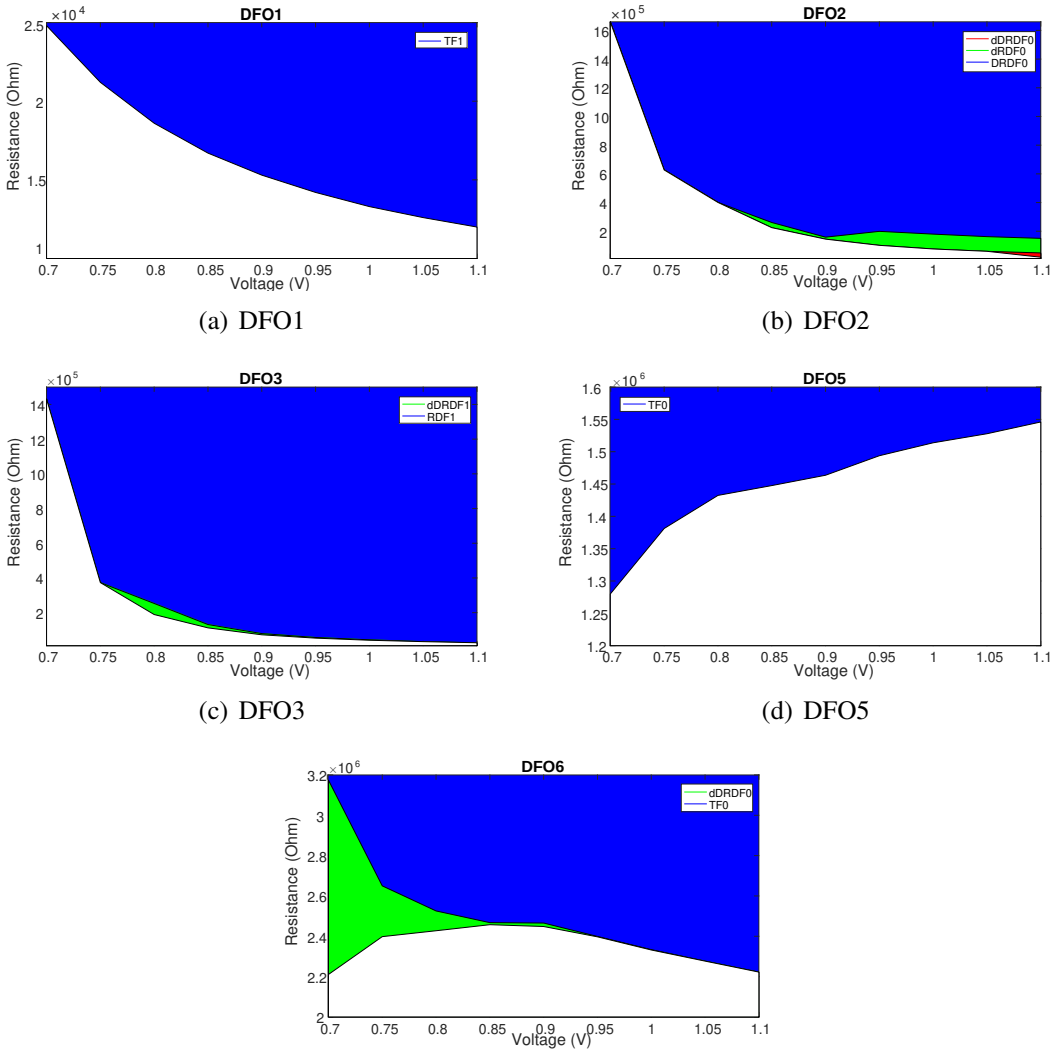
Source: COPETTI et al. 2017.

only, it is also possible to observe dDRDF, dRDF, and DRDF fault types. Note that the faulty behavior observed when injecting a DFO3, in Figure 4.11 - (c) is similar to the one observed when considering a DFO2. The injection of a DFO4 does not cause faults in this situation. In other words, no faults are propagated at a logic level.

Figure 4.11 - (d) depicts the faulty behavior observed when injecting DFO5. The graph shows a similar behavior when varying the power supply voltage. Basically, the increase of the power supply voltage makes the cells more robust, since it is necessary to inject a slightly bigger resistance to propagate a fault at the logic level. In Figure 4.11 - (e) shows that DFO6 causes dynamic faults (dDRDF) at the FinFET-based SRAM cell with lower voltages. On the other hand, the impact of increasing the power supply voltage on the defective FinFET-based SRAM cell is negative, since a weaker defect is able to cause TFs.

Before presenting the results related to resistive-bridge defects it is important to mention that a smaller resistance value means a stronger defect. In other words, a weak defect is modeled using a big resistance, which means that resistive-bridge defects have the inverse behavior of resistive-opens. Figure 4.12 - (a) summarizes the faulty behavior observed when injecting a resistive-bridge defect at position 1 (DFB1). Basically, when increasing the power supply voltage, the defect size necessary to propagate a faulty behavior is smaller.

Figure 4.11: Faulty behavior associated to Open Defects with supply voltage variation.



(a) DFO1

(b) DFO2

(c) DFO3

(d) DFO5

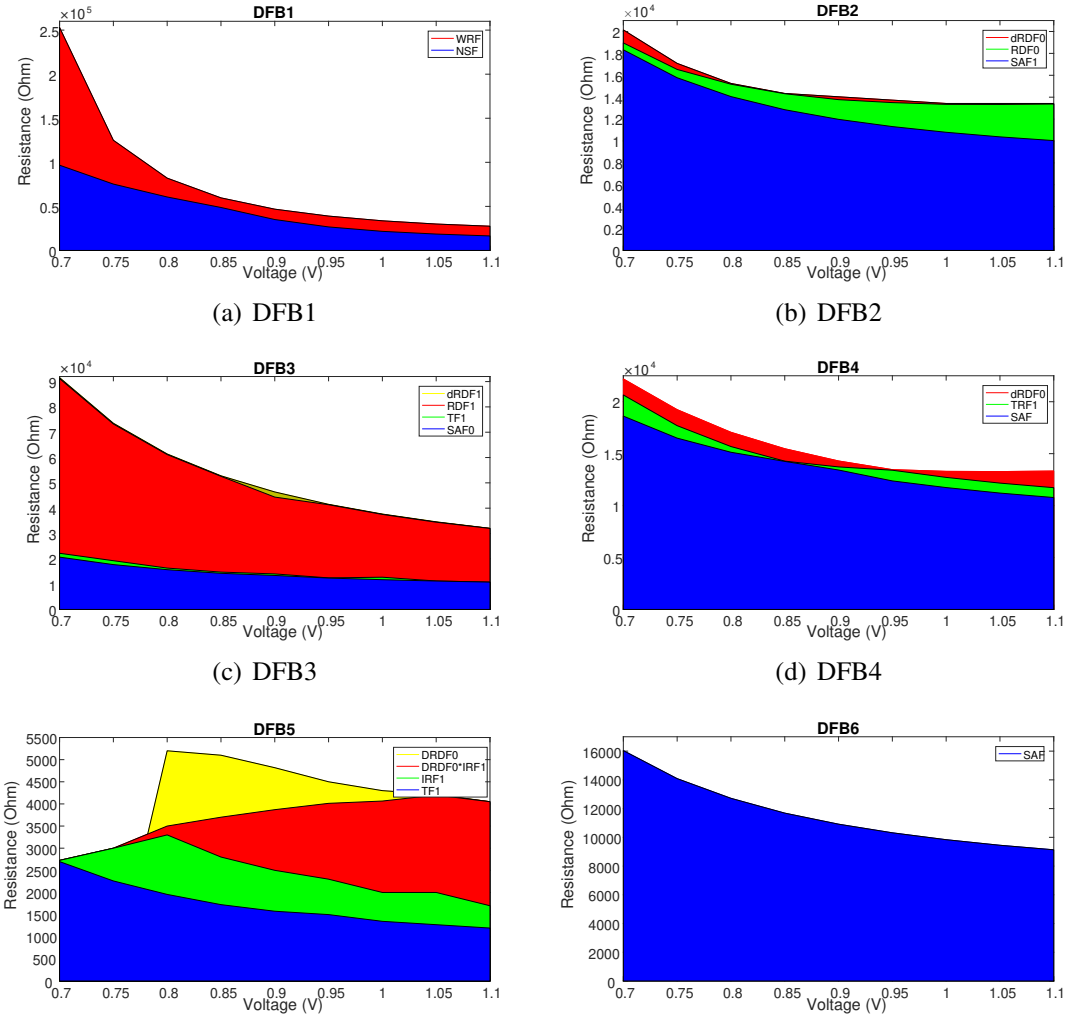
(e) DFO6

Source: The author (2019).

The injection of DFB2 (Figure 4.12 - (b)) causes three different faulty behaviors. For the FinFET-based SRAM cell, we observe RDFs instead of TFs. Another important aspect to be considered is that the type of faults did not change when varying the power supply voltage. It seems that the defect size plays a more important role in the observed faulty behavior.

The injection of DFB3 (Figure 4.12 - (c)) causes dynamic faults at the FinFET-based SRAM. Observing the graphs, it is possible to see that the defect magnitude necessary to propagate a faulty behavior at logic level changes when increasing the power supply voltage. Basically, a stronger defect is needed in order to propagate the fault at the logic level. Similar behavior is observed when considering a DFB4. However, the impact of increasing power supply voltage when considering the CMOS-based SRAM

Figure 4.12: Faulty behavior associated to Bridge Defects with source voltage variation.



(a) DFB1 (b) DFB2

(c) DFB3 (d) DFB4

(e) DFB5 (f) DFB6

Source: The author (2019).

cell is very expressive, since it is necessary to inject a stronger defect to cause a SAF or a TF, as it is possible to see in Figure 4.12 - (d).

Completely different behavior is observed when injecting a DFB5. Figure 4.12 - (e) shows there is an overlap with the increasing of power supply voltage, in DRDF0*IRF1 there are an overlap of faults, which is, in the red region, if the data is '1' occurs an IRF and if is '0' a DRDF, and the DRDF behavior not appears in low voltage. The increasing of the power supply voltage accelerates the cell output signal and causes a synchrony loss of the flip-flop. However, the region related to the occurrence of TFs decreases with increasing power supply voltages, which means that a TF is propagated with stronger defects or in other words with small resistance values.

Finally, Figure 4.12 - (f) depicts the results observed when varying the power supply voltage for a FinFET-based SRAM cell in the presence of a DFB6. Note that this

defect exclusively occurs for this kind of memory cell. It is possible to observe the same tendency observed for the other resistive-bridge defects, except for the DFB5.

4.3.1.4 Analysis considering different operating temperatures

Table 4.1 shows the comparison between the critical resistances for resistive-open and resistive-bridge defects considering three different temperatures, -40 °C, 27 °C, and 127 °C. Analyzing the results obtained throughout simulations, it is possible to observe that for each defect, a similar relation between critical resistances and temperature exists. In DFO1, DFO2, DFO3, DFO4, DFO6, DFB2, and DFB5 an increased temperature worsens the critical resistance. On the contrary, DFO5, DFB1, DFB3, DFB4, DFB5 (cell and array) and DFB6 are more prominent in lower temperatures.

Table 4.1: Critical Resistance Values for Different Temperatures

DF	Critical Resistance for Temperature [kΩ]		
	-40 °C	**27 °C**	**125 °C**
DFO1	16.9 (TF)	15.3 (TF)	13.6 (TF)
DFO2	297 (dDRDF)	144 (dDRDF)	73.0 (dRDF)
DFO3	137 (dDRDF)	71.5 (dRDF)	37.2 (dRDF)
DFO4	-	-	6600 (dRDF)
DFO5	1400 (TF)	1470 (TF)	1600 (TF)
DFO6	2580 (TF)	2460 (TF)	2.230 (TF)
DFB1	54.4 (WRF)	41.6 (WRF)	30.8 (WRF)
DFB2	13.9 (dRDF)	13.8 (dRDF)	14.8 (dRDF)
DFB3	54.6 (dRDF)	46.4 (dRDF)	37.8 (dRDF)
DFB4	14.1 (dRDF)	13.2 (dRDF)	12.8 (dRDF)
DFB5	1.74 (TF) 57.5 (dCF$_{ir}$)	2.13 (IRF) 59.5 (dCF$_{ir}$)	3.53 (IRF) 38.2 (dCF$_{ir}$)
DFB6	11.61 (SAF) 52.6 (dCF$_{ir}$)	10.92 (SAF) 44.0 (dCF$_{ir}$)	10.52 (SAF) 32.0 (dCF$_{ir}$)

Source: The Author (2017).

The operating temperature affects critical resistances since the current capabilities of the transistors are also affected. In this manner, the process of charging and discharging the nodes and the resistive-open and bridge defect's value is affected by temperature.

On one hand, for resistive-open defects, the high temperature facilitates the occurrence of faults, because it lowers the critical resistance. However, for DFO5, low resistance slightly moved the cell's operational window to a more convenient period within higher temperatures, resulting in an improvement of operation in this design. Further, it is interesting to note, that DF4 only causes faults at the highest temperature setting.

On the other hand, resistive-bridge defects are more likely to sensitize faults considering lower temperatures. Note that the critical resistance value necessary to cause RDFs decreases with temperature for DFB2 and DFB3 because the resistance alters the discharge characteristics of nodes. Note that for resistive-bridge defects a smaller resistance value represents a stronger defect. Considering DFB5, it is possible to observe that the TF occurs with a smaller resistance value when simulating the memory cell operating at -40 ºC. Finally, coupling faults are more prominent in low temperature, since a weaker defect is necessary to cause the fault.

The presented analysis considering different operating temperatures demonstrates a pattern for FinFET-based SRAMs and will further assist in future researches on evaluating weak resistive defects' impact on memory cells.

4.3.1.5 Impact of Temperature on Occurrence of Dynamic Faults

Weak defects may be responsible for dynamic faults in SRAM cells. The degree of the dynamic behavior that, in this case, can be assumed as the number of operations necessary to sensitize the fault, has generally been linked to the defect's physical location and size. However, the operating temperature of the memory circuit has demonstrated to be a key factor in the dynamic behavior of the fault as well. A defect that causes dynamic behavior at nominal operating temperatures may sensitize static faults at higher temperatures or do not sensitize any faults at all when the memory array is operating below nominal temperature.

Table 4.2 presents an analysis of the characteristics of dynamic behaviors presented for FinFET, these tables outline the fault observed in each simulation, followed, in the case of dynamic faults, by the number of consecutive operations. In this analysis the considered defect sizes were chosen in such a way that they sensitize dynamic faults with two or three consecutive read operations at nominal operating temperature (27 °C). The behavior of each defect was analyzed with temperatures close to nominal, ranging from 24 °C to 32 °C.

Analyzing Table 4.2, it is possible to note some particular behaviors. Defects DFO2 and DFO3 become stronger as the temperature increases. The defects DFB2 and DFB5 become stronger with rising temperatures, while DFB4 reduces its critical resistance when incrementing temperatures.

Table 4.2: Fault behavior when considering temperatures next to the nominal temperature of 27 °C

Temp.	Defect					
	DFO2 145 kΩ	**DFO3 72 kΩ**	**DFB2 13.7 kΩ**	**DFB3 45.75 kΩ**	**DFB4 45.75 kΩ**	**DFB5 11.79 kΩ**
24 °C	-	-	dRDF-2	dRDF-2	-	dRDF-2
25 °C	-	-	dRDF-2	dRDF-2	dRDF-5	dRDF-2
26 °C	-	-	dRDF-2	dRDF-2	dRDF-5	dRDF-2
27 °C	dDRDF-3	dDRDF-3	dRDF-2	dRDF-2	dRDF-5	dRDF-3
28 °C	dDRDF-2	dRDF-2	dRDF-2	dRDF-2	dRDF-4	-
29 °C	dDRDF-2	dRDF-2	dRDF-2	dRDF-2	dRDF-4	-
30 °C	dDRDF-2	dRDF-2	dRDF-2	dRDF-3	dRDF-4	-
31 °C	dDRDF-2	dRDF-2	dRDF-2	-	dRDF-2	-
32 °C	dDRDF-2	dRDF-2	RDF	-	dRDF-2	-

Source: The Author (2018).

4.3.1.6 Analysis considering different technology nodes

In order to evaluate the impact of resistive defects on smaller technology nodes, an extensive fault mapping process was carried out, adopting different technological nodes: 16 nm, 14 nm, 10 nm, and 7 nm. Tables 4.3 to 4.8 present the faults observed in each simulation setup, including the 20 nm node as reference. The resistance values shown represent the critical resistance responsible to sensitize a fault at the logic level.

The tables follow the same structure. The first column presents the type of defect, while the second column shows the resulting faults. The remaining columns report the critical resistance in kΩ to each analyzed technological node. Faults sensitized by resistive-open defects (DFOs) were first observed by injecting defects with the resistance presented, while faults sensitized by resistive-bridge defects (DFBs) were observed by injecting resistances ranging from zero up to the value presented. If a defect did not sensitize any fault during the simulation setup, then its analysis is shown as '-'. It is also important to mention that, to DFOs, the higher the value of the resistance, the higher is the robustness of memory built on that node, and to DFBs the logic is the reverse.

The tables are grouped into two sets according to the kind of defect. In the first set, Tables 4.3 to 4.5, the critical resistance associated with resistive-open defects is analyzed considering three different operating temperatures. The second set, Table 4.6 to 4.8 presents the results for bridge defects.

Analyzing the results obtained in Table 4.3, it is possible to observe a significant change in critical resistance for the same defect in different technological nodes. The only exceptions are DFO1 and DFO4. To DFO1 critical resistance remained around 14

kΩ, because the core of the cell is more robust due the inverter pair. To DFO4 there are no faults detected for the setup adopted in these simulations. For all other resistive-open defects, the scale-down of technological nodes made them less relevant, as only stronger defects are now able to sensitize faults. The critical resistance for DFO2 in a 7 nm technological node makes the cell designed in this technology 3000% more robust to such defect, if compared to its critical resistance on 20 nm equivalent design.

Table 4.3: Critical resistances for SRAMS designed in different technological nodes considering resistive-open defects, at 27 °C

Defect	**Fault**	**Critical Resistance for Technological Nodes [kΩ]**				
		20 nm	**16 nm**	**14 nm**	**10 nm**	**7 nm**
DFO1	TF	15.3	13.8	12.2	13.7	16.6
DFO2	DRDF	144.3	225.2	463.9	937.4	4500.0
	RDF	165.4	232.2	505.4	-	-
	dDRDF	144.2	224.5	461.0	923.8	4041.2
DFO3	RDF	71.6	103.4	190.1	357.9	1345.9
	dRDF	71.5	103.3	189.5	356.3	1324.8
DFO5	TF	1471.1	1858.0	2385.6	2778.4	3137.5
DFO6	TF	2457.5	3665.9	5105.0	6055.0	7685.0

Source: The Author (2018).

Similar behavior can be observed in the results shown in Tables 4.4 and 4.5, which present the results obtained for the simulations injecting resistive-open defects with the operating temperature set to 125 ºC and -40 ºC, respectively. Once again, all defects presented a significant increase in critical resistance, except for DFO1. Note also that DFO4 only caused faults when considering a temperature of 125 ºC and the range of resistance used in the executed simulations.

Table 4.4: Critical resistances for SRAMS designed in different technological nodes considering resistive-open defects, at 125 °C

Defect	**Fault**	**Critical Resistance for Technological Nodes [kΩ]**				
		20 nm	**16 nm**	**14 nm**	**10 nm**	**7 nm**
DFO1	TF	13.6	11.5	9.5	10.1	11.2
DFO2	RDF	73.1	93.0	137.7	206.3	420.3
	dRDF	73.0	92.8	137.4	205.9	420.0
DFO3	RDF	37.3	46.2	64.9	92.8	182.3
	dRDF	37.2	46.1	64.8	92.7	182.1
DFO4	dDRDF	6598.7	17662.9	-	-	-
DFO5	TF	1566.9	1947.0	2440.5	2851.4	3145.8
DFO6	TF	2231.5	3384.4	4671.6	5485.2	6225.0

Source: The Author (2018).

In Tables 4.6, 4.7, and 4.8, the results obtained from the analysis of faults caused by resistive-bridge defects in the temperatures of 27 °C, 125 °C and -40 °C are shown,

Table 4.5: Critical resistances for SRAMS designed in different technological nodes considering resistive-open defects, at -40 °C

Defect	Fault	Critical Resistance for Technological Nodes [kΩ]				
		20 nm	16 nm	14 nm	10 nm	7 nm
DFO1	TF1	17.8	16.2	14.9	17.4	21.7
DFO2	DRDF0	404.0	694.6	-	-	-
	dDRDF0	304.4	688.4	7414.0	-	-
DFO3	RDF	170.0	261.3	1301.3	-	-
	dRDF1	147.6	260.4	1285.0	9187.6	-
DFO5	TF	1482.4	1764.7	2278.1	2713.3	3060.8
DFO6	TF0	2557.6	3830.4	5345.0	6360.0	7985.0

Source: The Author (2018).

respectively. Analyzing the results obtained in Table 4.6, it is possible to observe a significant change in critical resistance (increasing 84%) for the defect DFB1, when moving from 20 nm to 7 nm technology. Reducing the technology node also causes some variation to the value of critical resistance for the remaining defects. The lowest values tend to appear for the 14 nm technology, while for 7 nm the value increases when compared to any other technology node simulated.

It is important to mention that some faults are masked by others. This happens to TF in DFB1, which is masked by NSF and SAF. This also occurs with WRF in DFB2 and DFB3. In older technologies, a well-defined range for such behavior is encountered, while FinFET's technology range of transitions is comparably diffuse since the critical resistance values often differ by less than 1 kΩ. There are presented some faults with the same value, because these faults are noted for some nodes, but are masked for another. For example, in DFB1 for the 7 nm technology, WRF and RDF are masked by NSF.

Observing some faults, the SAF can be noticed that the stuck digital value could be different, according to how the resistance is presented in the cell. For example, in defect DFB2, SAF is stuck-at '1', however, this would be '0' if the resistance is connected to $\overline{Q}$. For the CF_{ir} array faults of DFB5 and DFB6, the value of critical resistance keeps the highest in all cases; this event occurs due to the variations in the register's sensibility in the set of V_{DD} and frequency of operation.

The analysis of DFB5 and DFB6 are divided into two parts: the analysis of faulty-cell and the analysis of impact in array caused in the fault-free cells. For the CFir array faults, the value of critical resistance keeps the higher in all cases; this event occurs due to the variations in the register's sensibility for the set V_{DD} and frequency of operation.

In Table 4.7 and 4.8, it is observed that the effect of temperature variation is more prominent in the 7 nm node, whose the critical resistance in Table 4.7 is lower than the

Table 4.6: Critical resistances for SRAMS designed in different technological nodes considering resistive-bridge defects, at 27 °C.

Defect	**Fault**		**Critical Resistance for Technological Nodes [kΩ]**				
			20 nm	**16 nm**	**14 nm**	**10 nm**	**7 nm**
DFB1	NSF		26.67	32.93	49.14	58.70	75.78
	WRF		43.11	45.38	49.14	58.70	75.78
	RDF		35.21	37.85	49.14	58.70	75.78
	dRDF		35.39	43.73	50.04	59.80	76.88
DFB2	SAF1		11.98	11.09	10.58	11.38	13.40
	TF		11.98	11.09	10.60	11.42	13.92
	RDF		13.80	12.18	11.36	12.34	14.40
	dRDF		14.04	12.20	11.44	14.62	15.56
DFB3	SAF0		13.22	12.82	12.56	12.55	15.04
	TF		13.46	13.42	13.10	13.14	17.60
	RDF		46.41	45.48	45.42	53.03	66.92
	dRDF		46.42	45.49	45.44	53.04	67.00
DFB4	SAF0		13.20	12.32	11.54	12.56	15.02
	RDF		13.20	12.82	12.64	13.80	16.26
DFB5	Cell	TF	1.65	1.66	1.36	1.37	2.29
		IRF	2.12	2.02	1.24	1.26	2.34
	Array	CF_{tr}	1.67	1.67	1.36	1.37	2.32
		CF_{rd}	11.36	10.68	9.40	10.34	12.24
		CF_{ir}	50.19	26.31	24.29	27.50	38.98
		dCF_{rd}	11.92	10.68	9.61	10.66	12.36
		dCF_{ir}	50.20	10.87	24.40	27.66	39.01
DFB6	Cell	SAF0	10.92	10.02	9.67	10.26	11.16
	Array	CF_{ds}	11.86	10.02	9.67	10.26	11.16
		CF_{rd}	11.36	10.68	9.40	10.34	12.24
		CF_{ir}	44.00	22.83	20.81	24.02	35.50
		dCF_{ir}	44.01	22.88	20.88	24.12	35.65

Source: The Author (2018).

20 nm node. However, in Table 4.8 the situation is inverted and the critical resistance of the 7 nm node is higher. It may be noted that the dynamic fault occurrence rate is higher when compared to open defects for all nodes.

Analyzing the presented data, in general, the robustness for resistive-open defects increases with the reduction of the node. For resistive-bridge, considering mainly the DFB1 defect, the relationship is inverse. This behavior is mainly due to the lower charge stored at the memory cell circuit nodes as the technology node decreases, given the lower capacitances and supply voltage. As open defects act by hindering the charge and discharge of nodes, with less charge at the nodes a higher resistance of the open defect is necessary to have the same impact in charge and discharge dynamics when compared to bigger technology nodes. On the other hand, for the short defects, with less stored charge, it is easier to transfer charge from a given node that is shorted to another of distinct volt-

Table 4.7: Critical resistances for SRAMS designed in different technological nodes considering resistive-bridge defects, at 125 °C

Defect	**Fault**		**Critical Resistance for Technological Nodes [kΩ]**				
			20 nm	**16 nm**	**14 nm**	**10 nm**	**7 nm**
DFB1	NSF		18.70	18.52	20.16	27.27	43.88
	WRF		32.09	29.55	30.31	35.69	44.06
	RDF		21.88	20.04	21.26	27.63	43.80
	dRDF		21.97	20.14	21.36	28.07	44.06
DFB2	SAF1		11.60	10.12	9.21	9.61	10.78
	TF		11.60	10.12	9.21	9.61	10.80
	RDF		14.78	12.14	10.44	10.56	11.50
	dRDF		14.95	12.20	10.68	10.68	11.60
DFB3	SAF0		12.86	11.20	9.88	10.38	11.80
	TF		12.86	12.22	9.96	10.42	12.84
	RDF		37.81	34.63	32.66	36.25	42.77
	dRDF		37.82	34.64	32.68	36.26	42.79
DFB4	SAF0		12.84	11.18	9.86	10.36	11.80
	RDF		12.84	11.18	10.22	10.36	12.16
	dRDF		12.85	11.19	10.41	10.53	12.17
DFB5	Cell	TF	1.57	1.57	1.24	1.20	2.00
		IRF	3.48	3.54	2.77	2.83	3.06
	Array	CF_{tr}	1.57	1.57	1.24	1.21	2.02
		CF_{rd}	10.74	9.19	7.60	8.11	9.20
		CF_{ir}	38.74	16.12	14.96	17.76	23.36
		dCF_{rd}	10.78	9.21	7.67	8.19	9.25
DFB6	Cell	SAF0	10.52	9.09	8.44	8.84	9.55
	Array	CF_{ir}	10.52	9.09	8.44	8.84	9.56
		dCF_{ir}	31.99	12.25	11.09	13.89	19.49

Source: The Author (2018).

age, thus increasing the minimum value of resistance needed to sensitize a fault in smaller technologies.

Table 4.8: Critical resistances for SRAMS designed in different technological nodes considering resistive-bridge defects, at -40 °C

Defect	**Fault**		**Critical Resistance for Technological Nodes [kΩ]**				
			20 nm	**16 nm**	**14 nm**	**10 nm**	**7 nm**
DFB1	NSF		47.35	60.60	66.90	83.08	113.81
	WRF		55.74	60.60	66.91	83.08	113.81
	RDF		55.05	60.60	66.90	83.08	113.81
	dRDF		56.14	61.02	67.12	85.45	114.74
DFB2	SAF1		12.76	12.34	12.20	13.38	16.22
	TF		12.76	12.40	12.46	13.92	18.48
	RDF		13.86	12.92	12.44	13.38	16.28
	dRDF		14.04	13.73	14.03	16.17	20.14
DFB3	SAF0		14.08	13.78	13.56	15.20	18.92
	TF		14.99	15.34	14.02	15.70	22.96
	RDF		54.62	55.99	58.51	71.21	96.33
	dRDF		54.63	56.00	58.52	71.29	97.02
DFB4	SAF0		14.06	13.76	13.54	15.20	18.92
	RDF		14.08	13.76	13.54	15.20	18.92
DFB5	Cell	TF	1.74	1.84	1.51	1.55	2.89
		IRF	2.12	2.02	1.24	1.26	2.34
		dRDF	0.65	1.81	1.52	1.58	2.66
	Array	CF_{tr}	1.74	1.84	1.52	1.51	2.85
		CF_{rd}	11.88	12.04	11.12	12.64	15.44
		CF_{ir}	57.61	33.07	31.38	38.05	49.53
		dCF_{rd}	13.12	12.05	11.44	12.65	15.82
		dCF_{ir}	57.62	33.08	31.39	38.06	49.54
DFB6	Cell	SAF0	11.62	11.00	10.60	10.96	12.96
	Array	CF_{ds}	12.86	12.92	12.86	14.30	12.96
		CF_{ir}	52.58	28.04	24.25	30.92	42.40
		dCF_{ir}	52.59	28.06	24.27	30.94	42.42

Source: The Author (2018).

5 EVALUATING THE IMPACT OF IONIZING PARTICLES ON FINFET-BASED SRAMS WITH WEAK RESISTIVE DEFECTS

In this chapter the evaluation of impacts of ionizing particles on FinFET-based SRAMs with weak resistive defects. To evaluate the transient effects caused by ion strikes, a layout of 14 nm FinFET-based SRAM cell was designed and modeled in Sentaurus^{TM} TCAD tool.

5.1 Specification and Implementation

The technological node of 14 nm was chosen because it was being employed by SRAM manufacturing companies in 2018, the year that this part of the work began (INTEL, 2018b). This section describes the methodology of modeling of an SRAM cell used, and also how to simulate ionizing particle strikes at the physical level, as well as the SPICE modeling of resistive defects.

5.1.1 SRAM Cell Modeling in TCAD

Initially, the 3D model of a FinFET SRAM was developed using Sentaurus^{TM} TCAD to study SET/SEU effects. In comparison with SPICE simulations, this tool allows larger flexibility to control the device's physics aspects, including the impact location of ionizing particles and its associated LET. This study considers three models of FinFET-based SRAM cells: HD (High-Density), HP (High Performance) and LV (Low Voltage). Because of the discrete nature of fins, it is not possible to tune the transistor parameters to obtain an ideal robustness/area ratio, as it would be feasible in planar CMOS. Therefore, each model has its configuration with a different distribution of fins in the cell's transistors. The SRAM cell structure is divided into three parts with their proper notation (PU: PG: PD), meaning respectively: pull-up, pass-gate, and pull-down (BURNETT et al., 2014). As an example, the HD configuration adopts a (1:1:1) configuration, meaning that all the cell transistors are composed of a single fin.

The transistors model developed with the Sentaurus^{TM} tool was calibrated using the physical characteristics described by 2015 ITRS (NEISSER; WURM, 2015) for a 14 nm cell, which are described in Table 5.1, also the worfunction used for the metals are

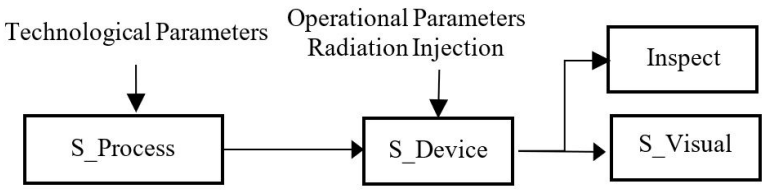
4.623 eV. This methodology was chosen during the development of the work because I didn't have the authorization to use commercial technology parameters. Figure 5.1 shows the model/simulation flow adopted in the Synopsys Sentaurus^{TM} environment (GUIDE, 2016). Firstly, the physical process of cells was developed, using the Sentaurus Process (S_Process) tool. The mesh grid configured in these simulations was generated given special attention to the active zones as the channel, source, and drain. Using the Sentaurus Device (S_Device) tool, the operational parameters of the circuit are implemented to validate it. The curve of Static Noise Margin (SNM) was obtained at this stage aiming to evaluate the reliability of the circuit to noise fluctuations. Then, the injection of the ionizing particle is modeled, using the same tool. The Sentaurus Visual (S_Visual) tool was used to analyze the electrical behavior, by wave verification. The Inspect tool was used to verify the transient operations while injecting radiation.

Table 5.1: Adopted Physical Parameters for FinFETs

Physical Parameters	**Values [nm]**
Physical Gate Length	26
Fin width	8
Fin Height	42
Fin Pitch	42
Poly Pitch	90
Effective Width	92
Metal Pitch	56

Source: The Author (2020).

Figure 5.1: Simulation flow used in TCAD.



Source: The author (2020).

5.1.2 Modeling Ion Strike

The heavy-ion injection in TCAD simulation follows the methodology presented in (NSENGIYUMVA et al., 2016), considering a Gaussian charge distribution with a track radius of 10 nm. To model the worst case of such particle strike, the charge track length should be longer than the fin height, with normal incidence over the drain of the sensitive transistor

(off-state transistor). The sensitive transistor is the pull-down transistor when the node (inverter output) is charged with a logic '1', or the pull-up transistor when the node is '0'.

In the simulation setup, the input parameters for the heavy ions are given in charge per track length (pC/μm). To convert this value into the LET parameter the relation of 1 pC/μm is equivalent to a 97 MeV-cm²/mg LET in silicon (KIM et al., 2018). For example, the alpha particles due to radioactive contamination in the packaging material can result in 0.015 pC/μm, which approximated 1.5 MeV-cm²/mg (KIM et al., 2018). This analysis aims to find the threshold LET that causes a bit-flip in the cell. Considering this LET, the drain current in the affected transistor is evaluated, modeled and compared with the traditional double exponential. The obtained current shape is modeled in SPICE to allow transient injections and resistive defects at the same time. This analysis is made with SPICE, since TCAD simulations demand a huge computational effort.

In the following, an example of the instruction of ionizing particle injection is done in SDevice using the HeavyIon command in the Physics function,

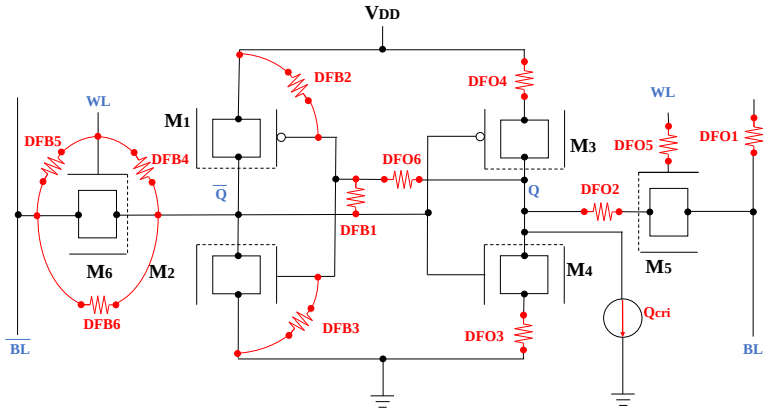
```
Physics
        HeavyIon (
        Direction = (1,0,0)
        Location = (0,0.029,0.090)
        Time = 1.0e-12
        Length = 0.09
        wt_hi = 0.01
        LET_f = 1.8
        Gaussian
        PicoCoulomb
        )
```

where: Direction($\vec{x}$, $\vec{y}$, $\vec{z}$) the direction vector of the particle after the start of impact; Location (x, y, z) is the initial striking spot of the particle using x, y, and z coordinates (μm), and x is the coordinate parallel to the plane; Time is the duration of the particle (s); Length of the particle (μm); wt_hi is the radius of the particle defined as the perpendicular from the track; LET_f is the LET of the particle; Gaussian, is how the particle distribution; and PicoCoulomb is a flag that determines that wt_hi is in μm, and LET_f is given in pC/μm.

5.1.3 Injecting Resistive Defects

The electrical simulations to evaluate the robustness of a FinFET-based SRAM cell are performed using Hspice^{TM} from Synopsys, adopting the Arizona State University's 14 nm FinFET Predictive Technology Model (PTM) (ASU, 2011), combining single event transient with weak resistive defects. For this purpose, the injected charge to simulate single events in SPICE is set with a value lower than the excess charge observed when simulating a particle strike with LET = LET$_{th}$, while simultaneously injecting resistive defects. In this case, the values of resistances that simulate the defects are varied through an automated tool, which interacts with the SPICE simulator. In this work, the critical resistances (R$_{crit}$) are the limit defect resistances that result in a bit-flip when simulating a transient with a correspondent charge disturbance lower than the critical one. The methodology for resistive defects injection is the same described in Chapter 4. Figure 5.2 shown the classical defects presented in (HAMDIOUI; GOOR, 2000) and an extra DFB6, was implemented because the results presented in (LIU; XU, 2012) and (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015). This is done to observe if resistive defects may turn the cell more prone to SEUs. The opposite was also verified, simulating an event depositing the critical charge (Q$_{crit}$) at the same time that resistive defects are injected, to determine if the single event effect (SEE) is attenuated due to a given defect.

Figure 5.2: FinFET-based SRAM cell with injected defects and transient current.



Source: The author (2020).

5.2 Validation

This section presents the results divided into three parts: (a) the modeling and validation of the FinFET-based SRAM cell in TCAD; (b) TCAD-based SEE injection results and comparison with SPICE injections; (c) the influence of resistive defects on cell reliability under single events.

5.2.1 SRAM Cell Validation

As described before, a FinFET SRAM cell was implemented based on physical parameters obtained from 2015 ITRS (NEISSER; WURM, 2015), and as presented in (BURNETT et al., 2014). Three different models were adopted, whose configurations (number of fins of the transistors), along with the corresponding area, are shown in Table 5.2 In Figure 2.7 was presented the simplified layout of these cells. As an example, Figure 5.3 shows an LV SRAM cell modeled in 3D-TCAD. Different from this cell, the HD configuration, the most compact, would not possess a fin column on each side of the cell, and the HP configuration would show two fins in the pass-gate. To reproduce industrial devices, only HD and LV cells use source and drain regions with a polyhedron over the fin. Note that these structures do not cause a considerable current variation in the transistor when compared with the HP cell. Electrically, the LV model has a more robust SNM for a read operation, and the HP model is faster during reading and writing operations (BURNETT et al., 2014). Comparing my cell with a commercial can be appointed that the shape of fins inside the oxide is not so linear, normally the fins have a shape more triangular.

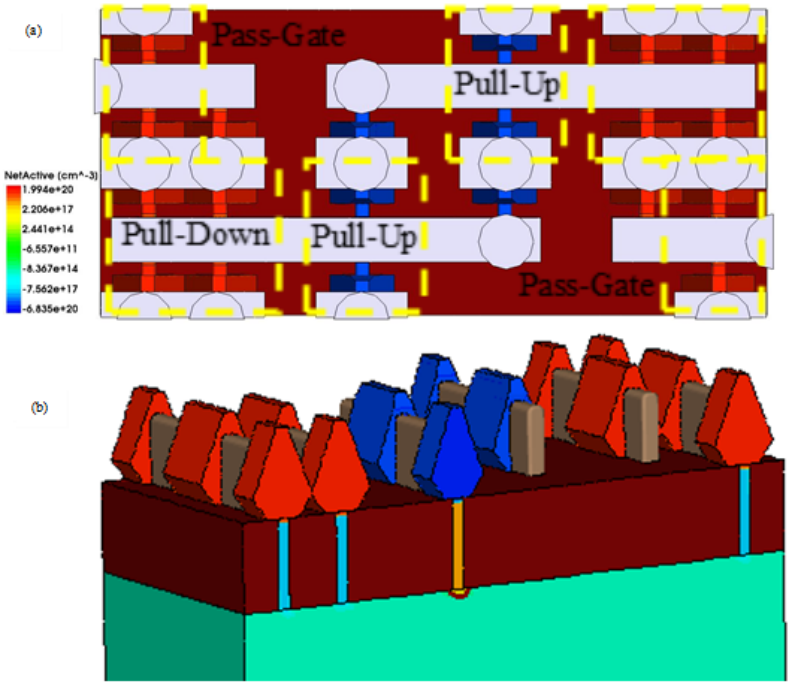
Table 5.2: Number of fins of different SRAM cells design

Configuration	**(PU:PG:PD)**	**Area (µm²)**
HD	(1:1:1)	0.0558
LV	(1:1:2)	0.07092
HP	(1:2:2)	0.07092

Source: The Author (2020).

To validate if the electrical operation of the device is compatible with the 14 nm node used as target technology, the electrical behavior was compared to the drain current/gate voltage data from the Arizona State University's Predictive Technology Model (PTM) (ASU, 2011) at the nominal temperature of 27 ºC. The I_D x V_G (drain current x gate voltage) normalized behavior presents in Figure 5.4 the drain current, for both p and

Figure 5.3: FinFET LV SRAM cell implemented in this work: (a) top view; (b) 3D view without gate and metals.



Source: The author (2020).

n FinFETs, considering two drain voltages to compare: 0.05 V and 0.8 V. Table 5.3 shows the off and saturation currents. The off current is obtained with 0 V at drain voltage and the saturation current with 0.8 V, both with drain voltage at 0.8V. The normalized currents are the currents divided by the fin pitch in µm, thereby 0.042 µm for the developed transistor and the y-axis is in the logarithmic scale. Note that there is a discontinuity in the current of pFET at 0 V, unfortunately, this is the best model that I could develop for the work, maybe a more accurate refine in the circuit generation could solve this.

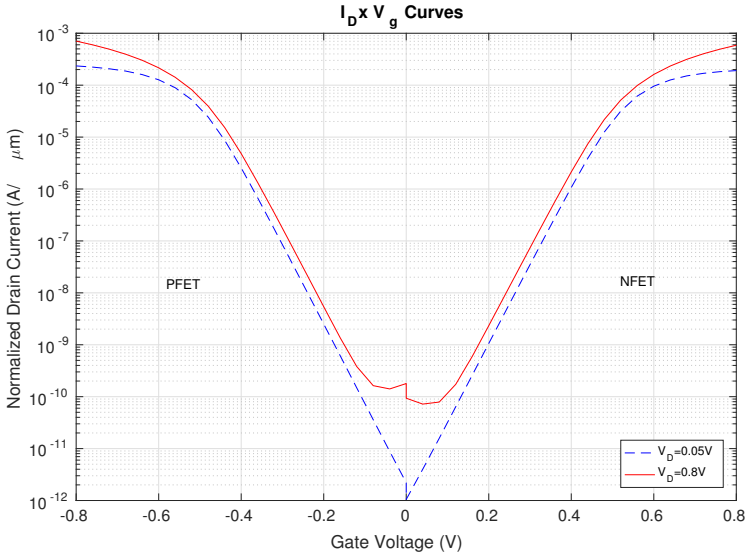
Table 5.3: Electrical Characteristics of the FinFET Modeled in TCAD

Transistor	**Current**	**Modeled**
NFET	I_{off}	3.920 pA
	I_{off_norm}	93.33 pA/µm
	I_{sat}	24.69 µA
	I_{sat_norm}	587.9 µA/µm
PFET	I_{off}	7.505 pA
	I_{off_norm}	178.7 pA/µm
	I_{sat}	29.63 µA
	I_{sat_norm}	705.6 µA/µm

Source: The Author (2020).

Figure 5.5 shows the hold SNM butterfly curve of one of the cells developed following the methodology in (ARANDILLA; ALVAREZ; ROQUE, 2011), it is shown the voltage transfer characteristic of the two inverters of transistors, VTC(L) is the voltage

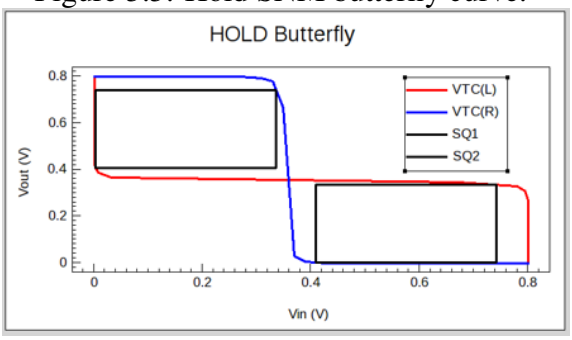
Figure 5.4: Normalized Drain Current x Gate Voltage Curves from the modeled FinFETs.



Source: The author (2020).

transition for the left inverter and VTC(R) for the right inverter, and SQ1 and SQ2 are the squares that are created inside the curves, the SNM value is the value of the smallest side of the square, the maximum voltage is 8.0 V. Table 5.4 presents the hold, read and write SNM for the three designs of SRAM cells. There are low discrepancies for all design variants of the SRAM Cell. Therefore, the cells developed in TCAD, in this work, are suitable to model the cells designed in 14 nm node.

Figure 5.5: Hold SNM butterfly curve.



Source: The author (2020).

Table 5.4: Static Noise Margin for FinFET-based SRAM Developed in TCAD

Cell	Hold_SNM	Read_SNM	Write_SNM
HD	0.33	0.15	0.39
LV	0.34	0.18	0.38
HP	0.33	0.15	0.39

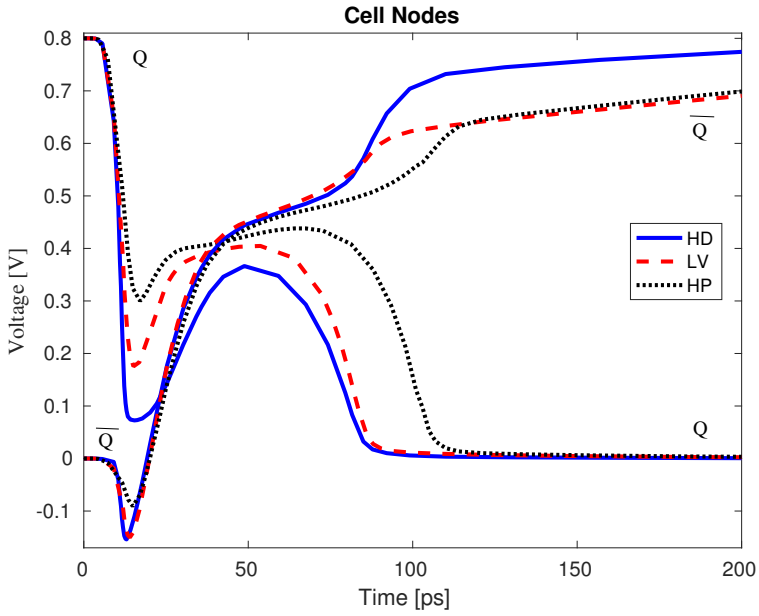
Source: The Author (2020).

5.2.2 Results of TCAD single event transient simulations

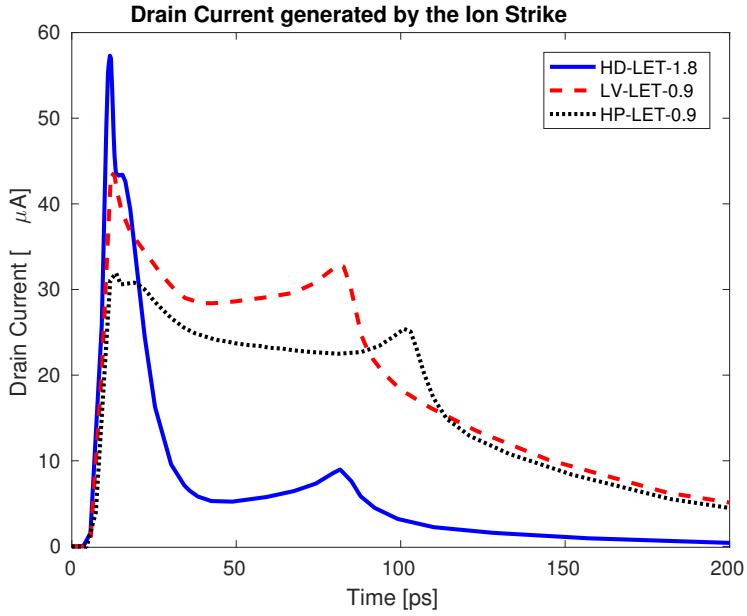
The heavy-ion simulation considers the particle strike in the corresponding time of 10 ps. The parameters used to model the ion track were already described in Subsection 5.1.2. Considering the cell's design with a depth of 1 µm, the deep length for the ion track was set as 0.9 µm. Figure 5.6 presents the behavior of cells in a simulation where an SEU is observed. The hit point of the ion strike is the center of the drain of the left pFET when it was storing '0' perpendicular to the plane. Figure 5.6 (a) presents the bit-flip caused by ionizing particles with the lower LETs (threshold LET, or LET_{th}) in the different designed cells, or, in other words, when Q_{crit} is achieved. However, as presented in the background with the discussion made in (BAUMANN, 2005), it will be considered the value of charge flowing in excess during the transient current in the affected node, which considers also the charge flow due to the circuit dynamics (hence, not merely the collected charge). Figure 5.6 (b) shows the drain current observed for particles (with LET = LET_{th}) injected at one of the inverter's nFET transistors. One can notice a plateau region on the current pulses, corresponding to the occurrence of the feedback action. The feedback action tends to activate the nFET transistor, which is nominally off before the transient. As can be observed from Figure 5.6 (a), the plateau happens while both transistors are simultaneously in a conduction state (near the inverter trip point). Since the n devices of LV and HP cells are built with two fins, the current on this plateau is higher, which facilitates the inversion of the bit stored in the cell. Thus, it is expected that the LET_{th} for these two models are similar. It is important to mention, that this is the first work that was published that shows the plateaus behavior in a FinFET-based SRAM cell.

The data presented in Table 5.5 demonstrates that the HD cell is the most robust when considering transients injected in pull-down transistors; the LET_{th} obtained with TCAD simulations is higher. The table's remaining columns show the charge which is injected to simulate the heavy-ion, the deposited charge (Q_{dep}) and the excess charge (Q_{exc}). The Q_{dep} is calculate with the Equation 3.5 using the deep length of the ion track instead of the device thickness, because in TCAD the deepness of charge generation is an important parameter for the calculator in the tool. The Q_{exc} is the charge disturbance on the affected node (integral of the transient current). Despite the lower LET_{th}, one may notice that Q_{exc} is higher for LV and HP cells, due to circuit dynamics. Another point that deserves attention is that not all the deposited charge is collected, as also discussed by (BAUMANN, 2005). Indeed, related works, often consider the quantity denominated

Figure 5.6: Bit-flip analysis: (a) Bit-flip in the cell; (b) Current generated by the ion strike.



(a)



(b)

Source: The author (2020).

Q_{exc} as the critical charge in SPICE-based injection campaigns. However, it is clear that this may lead to an erroneous evaluation regarding the circuit's reliability, especially for SRAMs, as can be observed in Table III. Indeed, according to (NASEER et al., 2007), Q_{crit} values computed from 3D device simulation currents are approximately 3 times smaller than those found using current models. Therefore, this work uses the value of LET_{th}, based on the values obtained with TCAD, for reliability comparison purposes. Additionally, for SPICE simulations, we use the quantity Q_{exc}, which is the charge distur-

bance on the circuit due to the impact of a particle with LET = LET_{th} on the drain of the sensitive transistor. From here on, we avoid using the term critical charge in our analysis, since smaller LET values and deposited charges may result in a higher amount of excess charge as observed in TCAD simulations and Table 5.5.

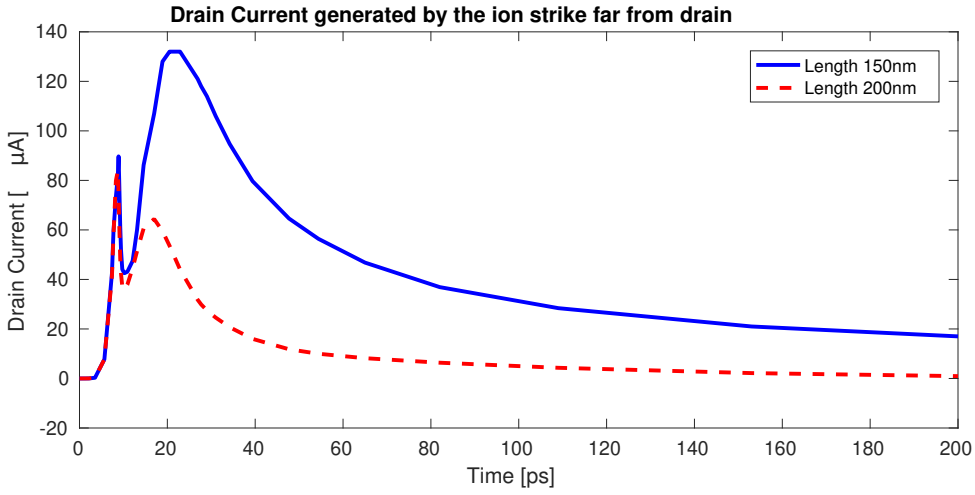
Table 5.5: Threshold LET and Deposited Charges (TCAD)

Cell	**LET_{th}(MeV-cm²/mg)**	**Q_{dep}(fC)**	**Q_{exc}(fC)**
HD	1.8	16.7	1.24
LV	0.9	8.34	3.79
HP	0.9	8.34	3.55

Source: The Author (2020).

The distance of the ion impact from the transistor drain and the track length also play an important role. Figure 5.7 shows the drain current that results from the impact of a particle with LET = 80 MeV-cm²/mg occurring 112 nm from the drain region's center of the pFET in the HD cell. The current difference observed in this figure is only caused by the variation of the charge track length from 150 nm to 200 nm. Integrating the results, one obtains a charge of 9.0 fC and 11 fC, respectively. It is possible to see that a much higher LET is needed to produce similar amount of charge collection, able to generate a bit-flip, if the impact occurs far from the drain.

Figure 5.7: Drain current with different charge track length implemented with ion far from the drain.



Source: The author (2020).

The observed current curves in TCAD simulations were then modeled as current sources in SPICE. The well-established Messenger's double exponential model (MESSENGER, 1982) is still being applied in related works to simulate SEEs due to its simplicity, even for recent FinFET technologies (ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO, 2015). However, in some cases, this model may not represent the actual

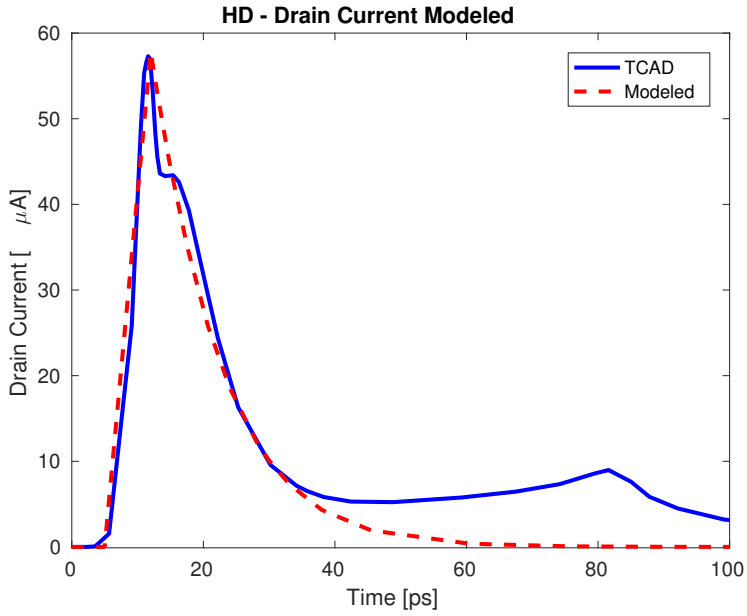
current behavior. For instance, in this work the double exponential is suitable to model a particle with LET = LET_{th} striking the pull-down transistor of the HD cell, because the current from the plateau has low effect in the bit-flip, while the same is not true to the LV and HP cell, Figure 5.6 (b).

A previous work investigating single events in FinFETs (ROYER; GARCIA-REDONDO; LOPEZ-VALLEJO, 2015) considered the following values using the double exponential time constants for execution of SPICE simulations: τ_1 = 2 ps and τ_2 = 20 ps (time constants of rising and falling exponentials, respectively). However, TCAD simulations in the present work, showed that, for strikes on nFET of the HD configuration, the rising and fall times are similar, resulting in τ_1 = 6 ps, τ_2 = 9 ps, and ($t_{d2} - t_{d1}$) = 7 ps (t_{d1} and t_{d2} are the initial times of both exponentials). Therefore, the double exponential curve is shown in Figure 5.8 (a) was used to perform transient injections on HD cell in SPICE, though varying the current peak, according to the desired injected charge. Both curves (TCAD and SPICE modeled double exponential) are shown in Figure 5.8 (a).

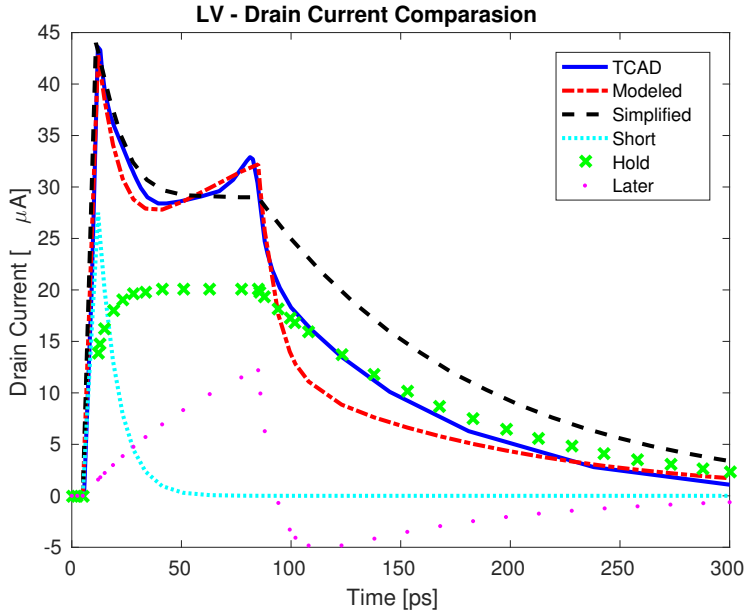
Further, the pulse shapes observed for the LV and HP configurations are significantly different from the double exponential. Hence, following the methodology proposed by (BLACK et al., 2015), a combination of three exponential sources in SPICE is proposed to represent the behavior. The first is the double exponential with τ_1 = 6 ps, τ_2 = 8 ps, and ($t_{d2} - t_{d1}$) = 7 ps with a short peak, the second source is a long double exponential with τ_1 = 6 ps, τ_2 = 100 ps, and ($t_{d2} - t_{d1}$) = 80 ps. Finally, an exponential curve with a slow rising time constant complete the modeling, whit τ_1 = 85 ps, τ_2 = 8 ps, and ($t_{d2} - t_{d1}$) = 80 ps. These curves are shown in Figure 5.8 (b).

Although these three source models fit the observed transients very well, a further simplification may be executed. Figure 5.9 shows a comparison of curves with different particle LETs for LV cell, including a simulation in where no bit-flip has occurred. Based on these and other performed simulations, it was verified that besides the current peak value, the plateau amplitude and time duration are the main parameters of the curve related to bit-flips. Therefore, the component of the later peak from the proposed curve can be removed to simplify the model, though keeping the plateau as also shown in Figure 5.8 (b).

Figure 5.8: Transient current modeled in spice for (a) HD cell and (b) LV cell.



(a)



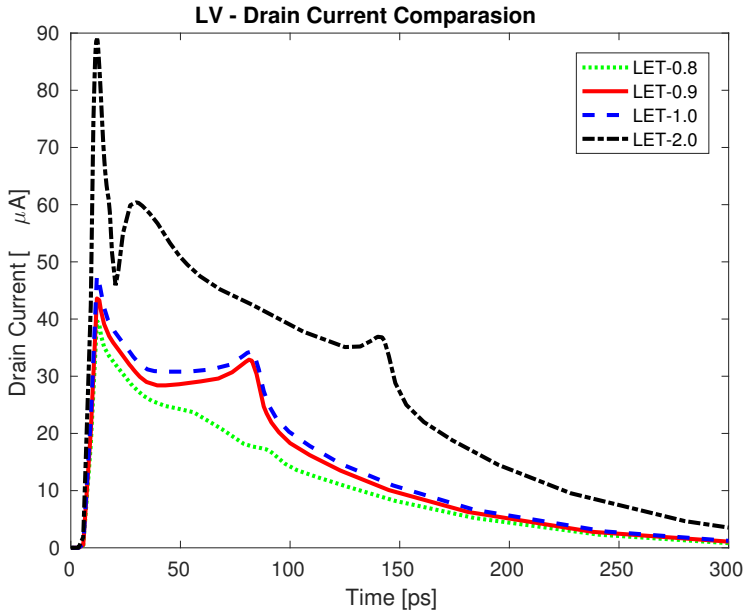
(b)

Source: The author (2020).

5.3 Evaluation: Influence of resistive deffects on SEU reliability

Electric simulations were performed with Hspice^{TM} using the 14 nm PTM technology, simulating the ionizing particle as a current source inside the node of the transistor when it stores '0', according to the models presented in Subsection 3.4.3 The nominal values of excess charge corresponding to the transient effects (Q_{exc_nom}), the peak current (I_{peak}) and the plateau current ($I_{plateau}$) are summarized in Table 5.6. Note that the values of

Figure 5.9: Comparison of curves with different particle LETs for LV cell (TCAD).



Source: The author (2020).

Q_{exc_nom} were obtained by integrating the current pulse, considering the lower values of I_{peak} that resulted in bit-flips in the SPICE model, and modeling the same value of plateaus observed in TCAD. This way, some variations in Q_{exc_nom} were observed when compared to TCAD. This is due to the application of different technological parameters for the TCAD model and the SPICE PTM model.

Table 5.6: Excess Charge Configuration

Cell	**Q_{exc_nom}(fC)**	**I_{peak}(µA)**	**$I_{plateau}$(µA)**
HD	1.01	63.5	-
LV	5.28	47.0	31.0
HP	5.46	47.9	32.1

Source: The Author (2020).

Table 5.7 shows the observed values of critical resistances, along with the values of simulated excess charge and the corresponding current peak and plateau. This value simulated Q_{exc_alt} was reduced from Q_{exc_nom} in 10% to verify if the weak defects can anticipate the bit-flip occurs. For resistive open defects, the critical resistance is the lowest value that, considering the reduced value of Q_{exc_alt}, results in a bit-flip. For resistive bridges, the critical resistances are the highest values that render the cell susceptible to SEUs. The defects marked with '*' indicate that this defect was injected into a different inverter of the cell than the transient was injected into.

Looking at Table 5.7 it is possible to observe that weak resistive defects may indeed modify the cell robustness. Examples are DFO2 and DFO4, which are low resistance

Table 5.7: Weak resistive defects that increase the SEU sensitivity of the studied SRAM cells

Cell	Q_{exc_nom}(fC)	I_{peak}(µA)	$I_{plateau}$(µA)	R_{crit}(Ω)
HD	0.909	56.0	-	DFO2 = 399
				DFO4* = 91
				DFB1 = 1.524 M
				DFB2* = 1.680 M
				DFB3&4 = 710.6 k
				DFB6 = 1.680 M
LV	4.77	41.6	28.0	DFO2 = 4351
				DFO4* = 920
				DFB1 = 209.5 k
				DFB2* = 1.145 M
				DFB3&4 = 106.8 k
				DFB6 = 145.0 k
HP	4.94	43.6	29.1	DFO2 = 3480
				DFO4* = 708
				DFB1 = 638.7 k
				DFB2* = 348.3 k
				DFB3&4 = 163.1 k
				DFB6 = 348.4 k

Source: The Author (2020).

open defects, as well as DFB2 and DFB6, which represent high resistances for bridge defects (weak defects). These values of defects may not be detectable in production tests, even those considering dynamic faults, according to the results presented in the previous chapter, specifically in Table 4.3 until 4.8.

The opposite situation was also investigated: simulating the nominal value of excess charge that generates a bit-flip in a healthy cell. It was possible to observe that some defects may turn the cell more robust to the SEUs, as shown in Table 5.8. It is interesting to notice that some defects may have distinct impacts when occurring in the inverter that suffers the SEU or during their occurrence in the opposite inverter. For example, if DFO2 occurs in the inverter hit by the ion, the bit-flip occurrence is facilitated, while, if it occurs in the opposite inverter, a higher collected charge is needed to turn the event into an SEU.

To conclude the analysis of this chapter, it is important to mention that the values of resistance of defects that make the cell more sensitive to the SEEs are very low for open defects and very high for bridge defects. These defects are below the limit of occurrence of dynamic faults, making these defects prominent to the test escapes during the manufacturing stage. In face this, a FinFET-based SRAM cell should be developed considering the effects of SEEs.

Table 5.8: Weak resistive defects that prevent bit-flips, considering the critical excess charge (spice)

Cell	$\mathbf{Q}_{exc\_nom}$**(fC)**	$\mathbf{R}_{crit}(\Omega)$
HD	1.01	DFO2* = 2429
		DFO3 = 5623
		DFO4 = 1603
		DFO6 = 2715
		DFB2 = 645.1 k
		DFB3&4* = 11.30 k
		DFB6* = 645.1 k
LV	5.28	DFO2* = 7052
		DFO3 = 2044
		DFO4 = 4128
		DFO6* = 664
		DFB3&4* = 168.3 k
		DFB6* = 1.322 M
HP	5.46	DFO2* = 310
		DFO3 = 132
		DFO5 = 4803
		DFO5 = 157
		DFO6 = 351
		DFO6 = 5.122 M
		DFB3*&4* = 5.036 M
		DFB6* = 5.122 M

Source: The Author (2020).

6 CONCLUSIONS

This work presents a comprehensive analysis on the behavior of FinFET-based SRAMs affected by resistive defects. The range of analyzed defects is vast and includes weak resistive-open and weak resistive-bridge defects that may escape manufacturing tests. Faulty behaviors detected by an automated tool were mapped and categorized in different kinds of faults. Further, the impact of defects on other cells of the array was evaluated, showing that defects that do not sensitize faults in the defective cell may still compromise the behavior of other cells. The fault models categorized comprise single and couple, static and dynamic faults. Finally, each defect was further characterized considering three different operating temperatures (-40 °C, 27 °C, and 125 °C) and five technological nodes (20 nm, 16 nm, 14 nm, 10 nm, and 7 nm).

Defects were injected by modifying the spice netlist of the SRAM cell, including resistors to emulate opens and bridges. Simulation results show that increasing the temperature amplifies the impact of resistive-open defects on memory cells. Moreover, a significant increase in critical resistance was observed when mapping faults in smaller technologies, especially for a specific defect regarding cell location (DFO4 - Figure 5.2). Thus, it is possible to conclude that stronger open defects are more likely to sensitize faults in further scaled memories when comparing with weak defects. Except for DFO5, where increasing the temperature amplifies the impact of resistive-open defects on memory cells.

As for resistive-bridge defects, each defect showed a particular behavior when considering different operating temperatures, mainly for the 7 nm node, that suffers great influence of temperature variation. Besides some exceptions, lower temperatures increase the critical resistance. Coupling faults were observed in cells affected by defect types DFB5 and DFB6.

Dynamic faults will increase their range of appearance with the reduction of technology, to the open defects. Consequently the 7 nm technology presents a high dynamic fault rate. Considering bridge defects the occurrence of dynamic faults is variable.

It is important to mention that weak defects, which do not cause any faulty behavior, may become a reliability concern over the lifetime. Under these circumstances, the necessity to adopt defect-oriented test methodologies for performing the manufacturing test procedures increases.

Finally, with this mapping and characterization of different resistive defects, it is possible to analyze the impact of these defects when considering memory blocks in combination with other reliability issues, such as aging and/or noise tolerance.

This work also performed an analysis of the impact of SEEs on defective FinFET-based SRAM cells. To accomplish this, three variants of an SRAM cell were modeled with a TCAD simulator, according to technical parameters of a 14 nm FinFET form ITRS 2015. In a subsequent step, ion strikes were simulated in the modeled cells. As a secondary contribution, the obtained current shapes and the corresponding excess charges for the different design variants (HD, LV, and HP) were modeled. Furthermore, unusual behavior of current was observed and modeled in the FinFET-based SRAM cell when hit by an ionizing particle, which can alter the radiation analysis in this kind of circuit.

This work also remarks that physical (TCAD) simulations may be mandatory if the goal is to evaluate the design sensitivity to a given energy spectrum of incident particles. This is due to a specific SRAM circuit dynamic: a particle with lower LET may result in a higher value of excess charge, as demonstrated in this work. Therefore, SPICE simulations that consider this value as a comparison parameter (or considering it as critical charge), maybe not accurately representing the actual reliability of the memory against single events in real radiation environments.

In this work, considering the TCAD simulation data, the HD cell demonstrated to be more robust than HP and LV cells, since a higher LET was necessary to trigger a bit-flip. This may be assumed valid for ion strikes in the pull-down network. After a discussion on the suitability of applying the double exponential model to simulate SEEs in this technology, the obtained current shapes observed in TCAD, while simulating ion strikes, were modeled in SPICE. For certain cell configurations and particle energy conditions, the double exponential is still a satisfyingly accurate model, while for other cases different current modeling had to be proposed.

Finally, this work shows that weak resistive defects may indeed affect the behavior of the cell under single events. In fact, some weak defects may turn the cell more prone to SEUs. However, some defects may prevent bit-flips to occur, considering the LET_{th} observed for a defect-free cell, making a higher particle LET necessary in order to generate an SEU. This ambiguous behavior is explained by the fact that the amount of excess charge due to a single event in SRAMs is highly dependent on the circuit's dynamic response, which indeed may be significantly modified by the occurrence of resistive defects.

6.1 Future Works

As future works, I recommend using the advantages of simulation of the Sentaurus TCAD 3D tool to generate a set of cells implementing physically the defects that cause weak defects in the cell. With these cells, it could be possible to model with the behavior of such defects more accurately.

A further possibility of continuation of this work's findings consists of using the injection charge modeled according to the described current source and to implement it in a defective cell. This would allow us to observe the region of dynamic faults and to verify how ionizing particles would affect of defective FinFET-based SRAM cells.

7 PUBLICATIONS DURING THE PHD PERIOD

The publications achieved during the doctorate period, related with the theme studied are described below:

- **Copetti, T. S.**, Balen, T. R., Brum, E., Aquistapace, C., & Poehls, L. B. (2020, April). Comparing the Impact of Power Supply Voltage on CMOS- and FinFET-Based SRAMs in the Presence of Resistive Defects. Journal of Electronic Testing 36(1), 1-14.

- **Copetti, T. S.**, Medeiros, G. C., Taouil, M., Hamdioui, S., Poehls, L. B. & Balen, T. R.(2020, March). Evaluating the Impact of Ionizing Particles on FinFET-based SRAMs with Weak Resistive Defects. In 2020 IEEE Latin American Test Symposium (LATS) (pp. 1-6). IEEE.

- Medeiros, G. C., Brum, E., Poehls, L. B., **Copetti, T.**, & Balen, T. (2019). Evaluating the Impact of Temperature on Dynamic Fault Behaviour of FinFET-Based SRAMs with Resistive Defects. Journal of Electronic Testing, 35(2), 191-200.

- **Copetti, T. S.**, Medeiros, G. C., Poehls, L. M., & Balen, T. R. (2019, May). Evaluating the Impact of Resistive Defects on FinFET-Based SRAMs. In IFIP/IEEE International Conference on Very Large Scale Integration-System on a Chip (pp. 22-45). Springer, Cham. First Online: 17 May 2019.

- **Copetti, T. S.**, Balen, T. R., Brum, E., Aquistapace, C., & Poehls, L. B. (2019, March). A Comparative Study Between FinFET and CMOS-Based SRAMs under Resistive Defects. In 2019 IEEE Latin American Test Symposium (LATS) (pp. 1-6). IEEE.

- **Copetti, T. S.**, Balen, T. R., Medeiros, G. C., & Poehls, L. M. (2018, April). The Effects of Resistive Defects in FinFET SRAMs. In 33º *Simpósio Sul de Microeletrônica* 2018 (SIM 2018), IEEE.

- Medeiros, G., Brum, E., Poehls, L. B., **Copetti, T.**, & Balen, T. (2018, March). Influence of temperature on dynamic fault behavior due to resistive defects in FinFET-based SRAMs. In 2018 IEEE 19th Latin-American Test Symposium (LATS)(pp. 1-6). IEEE.

- **Copetti, T. S.**, Balen, T. R., Medeiros, G. C., & Poehls, L. M. (2017, October). Analyzing the behavior of FinFET SRAMs with resistive defects. In 2017 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) (pp. 1-6). IEEE.

There are other works publishes during the doctored that comes from my master period that is not related to the work presented in this thesis.

- Martins, M. T., Medeiros, G. C., **Copetti, T.**, Vargas, F. L., & Poehls, L. B. (2017). Analysing NBTI Impact on SRAMs with Resistive Defects. Journal of Electronic Testing, 33(5), 637-655;

- **Copetti, T.**, Medeiros, G. C., Poehls, L. B., & Vargas, F. (2016). NBTI-Aware Design of Integrated Circuits: A Hardware-Based Approach for Increasing Circuits' Life Time. Journal of Electronic Testing, 32(3), 315-328;

- **Copetti, T.**, Medeiros, G., Poehls, L. B., Vargas, F., Kostin, S., Jenihhin, M., Raik, J & Ubar, R. (2016, April). Gate-level modelling of NBTI-induced delays under process variations. In Test Symposium (LATS), 2016 17th Latin-American (pp. 75-80). IEEE;

- Martins, M. T., Medeiros, G., **Copetti, T.**, Vargas, F., & Poehls, L. B. (2016, April). Analyzing NBTI impact on SRAMs with resistive-open defects. In Test Symposium (LATS), 2016 17th Latin-American (pp. 87-92). IEEE;

- **Copetti**, Poehls, L. B., & Vargas, F. (2016, April). Hardware-Based Approach for NBTI-Aware Design. In Test Symposium (LATS), 2016 17th Latin-American - Poster. IEEE.

REFERENCES

ADAMS, R.; COOLEY, E. Analysis of a deceptive destructive read memory fault model and recommended testing. In: **Proc. IEEE North Atlantic Test Workshop**. [S.l.: s.n.], 1996.

AGBO, I. et al. BTI analysis of SRAM write driver. **Proceeding of 2015 10th International Design and Test Symposium, IDT 2015**, p. 100–105, 2016.

ARANDILLA, C. D.; ALVAREZ, A. B.; ROQUE, C. R. K. Static noise margin of 6t sram cell in 90-nm cmos. In: IEEE. **2011 UkSim 13th International Conference on Computer Modelling and Simulation**. [S.l.], 2011. p. 534–539.

ASU, N. G. **Predictive Technology Model**. 2011. Disponível em: <http://ptm.asu.edu/>.

AUTH, C. 22-nm fully-depleted tri-gate CMOS transistors. **Proceedings of the Custom Integrated Circuits Conference**, 2012. ISSN 08865930.

BAJURA, M. A. et al. Models and algorithmic limits for an ecc-based approach to hardening sub-100-nm srams. **IEEE Transactions on Nuclear Science**, IEEE, v. 54, n. 4, p. 935–945, 2007.

BAUMANN, R. Soft errors in advanced computer systems. **IEEE Design and Test of Computers**, v. 22, n. 3, p. 258–266, 2005. ISSN 07407475.

BAUMANN, R. C. Soft errors in advanced semiconductor devices-part i: the three radiation sources. **IEEE Transactions on Device and Materials Reliability**, v. 1, n. 1, p. 17–22, 2001. ISSN 15304388.

BERKELEY, U. B. G. **BSIM Group**. Disponível em: <http://bsim.berkeley.edu/?page=BSIM4>.

BHATTACHARYA, D.; JHA, N. K. FinFETs : From Devices to Architectures. v. 2014, 2014.

BHOJ, A. N.; SIMSIR, M. O.; JHA, N. K. Fault models for logic circuits in the multigate era. **IEEE Transactions on nanotechnology**, IEEE, v. 11, n. 1, p. 182–193, 2011.

BLACK, D. A. et al. Modeling of Single Event Transients with Dual Double-Exponential Current Sources: Implications for Logic Cell Characterization. **IEEE Transactions on Nuclear Science**, v. 62, n. 4, p. 1540–1549, 2015. ISSN 00189499.

BORRI, S. et al. Analysis of dynamic faults in embedded-srams: Implications for memory test. **Journal of Electronic Testing**, Springer, v. 21, n. 2, p. 169–179, 2005.

BOSIO, A. et al. Advanced test methods for SRAMs. **Proceedings of the IEEE VLSI Test Symposium**, p. 300–301, 2012.

BURNETT, D. et al. FinFET SRAM design challenges. **ICICDT 2014 - IEEE International Conference on Integrated Circuit Design and Technology**, n. 512, p. 6–9, 2014.

BUSHNELL, M.; AGRAWAL, V. D. **Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits**. [S.l.]: Springer Science & Business Media, 2000. v. 17.

CAO, Y. et al. New paradigm of predictive MOSFET and interconnect modeling for early circuit simulation. **Proceedings of the Custom Integrated Circuits Conference**, p. 201–204, 2000. ISSN 08865930.

CHAMPAC, V. et al. Testing of stuck-open faults in nanometer technologies. **IEEE Design & Test of Computers**, IEEE, v. 29, n. 4, p. 80–91, 2012.

CHANG, J. et al. Scaling of soi finfets down to fin width of 4 nm for the 10nm technology node. In: IEEE. **VLSI Technology (VLSIT), 2011 Symposium on**. [S.l.], 2011. p. 12–13.

CHI, M.-h. Challenges in manufacturing finfet at 20nm node and beyond. **Technology Development, Global foundries, Malta, NY, USA.[Online]. Available: http://www. rit. edu/kgcoe/eme/sites/default/files/Min-hwa% 20Chi**, 2012.

CLARK, L. T. et al. Asap7: A 7-nm finfet predictive process design kit. **Microelectronics Journal**, Elsevier, v. 53, p. 105–115, 2016.

COLINGE, J.-P. Multigate transistors: Pushing moore's law to the limit. In: IEEE. **2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)**. [S.l.], 2014. p. 313–316.

COLINGE, J.-P. et al. **FinFETs and other multi-gate transistors**. [S.l.]: Springer, 2008. v. 73.

COPETTI, T. S. et al. Analyzing the behavior of finfet srams with resistive defects. In: IEEE. **Very Large Scale Integration (VLSI-SoC), 2017 IFIP/IEEE International Conference on**. [S.l.], 2017. p. 1–6.

CREME-MC, V. U. **Critical Charge and Threshold LET**. Disponível em: <https://creme.isde.vanderbilt.edu/CREME-MC/help/critical-charge-and-threshold-let>.

DILILLO, L. et al. Resistive-Open Defects in Embedded-SRAM Core Cells: Analysis and March Test Solution. In: **Proc. 13th Asian Test Symposium**. IEEE, 2004. p. 266–271. ISBN 0-7695-2235-1. ISSN 1081-7735. Disponível em: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1376569>.

DILILLO, L. et al. Resistive-open defect injection in sram core-cell: analysis and comparison between 0.13 μm and 90 nm technologies. In: ACM. **Proceedings of the 42nd annual Design Automation Conference**. [S.l.], 2005. p. 857–862.

DUBEY, P.; GARG, A.; MAHAJAN, S. Study of read recovery dynamic faults in 6t srams and method to improve test time. **Journal of Electronic Testing**, Springer, v. 26, n. 6, p. 659–666, 2010.

DUNGA, M. V. et al. Bsim-cmg: A compact model for multi-gate transistors. In: **FinFETs and Other Multi-Gate Transistors**. [S.l.]: Springer, 2008. p. 113–153.

FARKHANI, H. et al. Comparative study of finfets versus 22nm bulk cmos technologies: Sram design perspective. In: IEEE. **2014 27th IEEE International System-on-Chip Conference (SOCC)**. [S.l.], 2014. p. 449–454.

FONSECA, R. A. et al. Analysis of resistive-bridging defects in SRAM core-cells: A comparative study from 90nm down to 40nm technology nodes. **2010 15th IEEE European Test Symposium, ETS'10**, v. 1, p. 132–137, 2010. ISSN 15301877.

FONSECA, R. A. et al. Impact of resistive-bridging defects in sram core-cell. In: IEEE. **Electronic Design, Test and Application, 2010. DELTA'10. Fifth IEEE International Symposium on**. [S.l.], 2010. p. 265–269.

GOOR, A. J. V. D.; AL-ARS, Z. Functional memory faults: A formal notation and a taxonomy. In: IEEE. **VLSI Test Symposium, 2000. Proceedings. 18th IEEE**. [S.l.], 2000. p. 281–289.

GOOR, A. J. Van de. **Testing semiconductor memories: theory and practice**. [S.l.]: John Wiley & Sons, Inc., 1991.

GOOR, A. J. van de et al. March lr: A test for realistic linked faults. In: IEEE. **Proceedings of 14th VLSI Test Symposium**. [S.l.], 1996. p. 272–280.

GUIDE, S. D. U. Version M-2016.12, Synopsys. **Inc., Mountain View, CA**, v. 49, 2016.

HAMDIOUI, S. et al. Investigation of single-cell dynamic faults in deep-submicron memory technologies. In: **IEEE Proc. European Test Symposium Digest of Papers**. [S.l.: s.n.], 2006.

HAMDIOUI, S.; AL-ARS, Z.; Van De Goor, A. J. Testing static and dynamic faults in random access memories. **Proceedings of the IEEE VLSI Test Symposium**, v. 2002-Janua, p. 395–400, 2002.

HAMDIOUI, S.; GOOR, A. J. V. D. An experimental analysis of spot defects in srams: realistic fault models and tests. In: IEEE. **Proceedings of the Ninth Asian Test Symposium**. [S.l.], 2000. p. 131–138.

HAMDIOUI, S. et al. Importance of dynamic faults for new sram technologies. In: IEEE. **Test Workshop, 2003. Proceedings. The Eighth IEEE European**. [S.l.], 2003. p. 29–34.

HARUTYUNYAN, G. et al. Fault modeling and test algorithm creation strategy for FinFET-based memories. **Proceedings of the IEEE VLSI Test Symposium**, 2014.

HARUTYUNYAN, G. et al. Fault modeling and test algorithm creation strategy for finfet-based memories. In: IEEE. **2014 IEEE 32nd VLSI Test Symposium (VTS)**. [S.l.], 2014. p. 1–6.

HARUTYUNYAN, G.; TSHAGHARYAN, G.; ZORIAN, Y. Test and repair methodology for finfet-based memories. **IEEE Transactions on Device and Materials Reliability**, IEEE, v. 15, n. 1, p. 3–9, 2015.

HEINIG, A. et al. System integration -The bridge between More than Moore and More Moore. In: **Proc. 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE)**. IEEE, 2014. p. 1–9. ISBN 9783981537024. ISSN 15301591. Disponível em: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6800346>.

HOHL, J. H.; GALLOWAY, K. F. Analytical model for single event burnout of power mosfets. **IEEE Transactions on Nuclear Science**, IEEE, v. 34, n. 6, p. 1275–1280, 1987.

HUANG, X. et al. Sub 50-nm FinFET: PMOS. In: **Proc. International Electron Devices Meeting 1999. Technical Digest (Cat. No. 99CH36318)**. [S.l.]: IEEE, 1999. p. 67–70. ISBN 0780354109.

HUBERT, G.; ARTOLA, L.; REGIS, D. Impact of scaling on the soft error sensitivity of bulk, FDSOI and FinFET technologies due to atmospheric radiation. **Integration, the VLSI Journal**, Elsevier, v. 50, p. 39–47, 2015. ISSN 01679260. Disponível em: <http://dx.doi.org/10.1016/j.vlsi.2015.01.003>.

INSIGHTS, T. **TSMC 10 nm Process**. 2017. Disponível em: <https://www.techinsights.com/blog/tsmc-10-nm-process>.

INTEL. **Intel's 10 nm Technology: Delivering the Highest Logic Transistor Density in the Industry Through the Use of Hyper Scaling**. 2018. Disponível em: <https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/09/10-nm-icf-fact-sheet.pdf>.

INTEL. **Supply Update: An Open Letter from Bob Swan, Intel CFO and Interim CEO**. 2018. Disponível em: <https://newsroom.intel.com/news-releases/supply-update/#gs.rwc81o>.

JAN, C. H. et al. A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications. **Technical Digest - International Electron Devices Meeting, IEDM**, p. 44–47, 2012. ISSN 01631918.

KAREL, A. et al. Comparative study of Bulk , FDSOI and FinFET technologies in presence of a resistive short defect. p. 129–134, 2016.

KARL, E. et al. A 4.6 GHz 162 Mb SRAM design in 22 nm tri-gate CMOS technology with integrated read and write assist circuitry. **IEEE Journal of Solid-State Circuits**, v. 48, n. 1, p. 150–158, 2013. ISSN 00189200.

KAUPPILA, J. S. et al. A Bias-Dependent Single-Event Compact Model Implemented Into BSIM4 and a 90 nm CMOS Process Design Kit. v. 56, n. 6, p. 3152–3157, 2009.

KILCHYTSKA, V.; FLANDRE, D.; ANDRIEU, F. On the utbb soi mosfet performance improvement in quasi-double-gate regime. In: IEEE. **2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC)**. [S.l.], 2012. p. 246–249.

KIM, J. et al. Single-Event Transient in FinFETs and Nanosheet FETs. **IEEE Electron Device Letters**, IEEE, v. 39, n. 12, p. 1840–1843, 2018.

LI, J. C.-M.; TSENG, C.-W.; MCCLUSKEY, E. Testing for resistive opens and stuck opens. In: IEEE. **Test Conference, 2001. Proceedings. International**. [S.l.], 2001. p. 1049–1058.

LIN, C.-W.; CHAO, M. C.-T.; HSU, C.-C. Investigation of gate oxide short in finfets and the test methods for finfet srams. In: IEEE. **2013 IEEE 31st VLSI Test Symposium (VTS)**. [S.l.], 2013. p. 1–6.

LIU, H. et al. Soft-error performance evaluation on emerging low power devices. **IEEE Transactions on Device and Materials Reliability**, IEEE, v. 14, n. 2, p. 732–741, 2014. ISSN 15582574.

LIU, Y.; XU, Q. On modeling faults in finfet logic circuits. In: IEEE. **Test Conference (ITC), 2012 IEEE International**. [S.l.], 2012. p. 1–9.

MA, C. et al. Compact reliability model for degradation of advanced p-mosfets due to nbti and hot-carrier effects in the circuit simulation. In: IEEE. **2013 IEEE International Reliability Physics Symposium (IRPS)**. [S.l.], 2013. p. 2A–3.

MAGARSHACK, P.; FLATRESSE, P.; CESANA, G. Utbb fd-soi: A process/design symbiosis for breakthrough energy-efficiency. In: EDA CONSORTIUM. **Proceedings of the Conference on Design, Automation and Test in Europe**. [S.l.], 2013. p. 952–957.

MARSHALL, A.; NATARAJAN, S. Pd-soi and fd-soi: a comparison of circuit performance. In: IEEE. **Electronics, Circuits and Systems, 2002. 9th International Conference on**. [S.l.], 2002. v. 1, p. 25–28.

MARTINS, M. T. et al. Analyzing NBTI impact on SRAMs with resistive-open defects. **LATS 2016 - 17th IEEE Latin-American Test Symposium**, p. 87–92, 2016.

MAVIS, D. G.; EATON, P. H. SEU and set modeling and mitigation in deep submicron technologies. **Annual Proceedings - Reliability Physics (Symposium)**, p. 293–305, 2007. ISSN 00999512.

MEDEIROS, G. C.; POEHLS, L. B.; VARGAS, F. F. Analyzing the Impact of SEUs on SRAMs with Resistive-Bridge Defects. In: **2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)**. [S.l.]: IEEE, 2016. p. 487–492. ISBN 978-1-4673-8700-2.

MESALLES, F. et al. Behavior and test of open-gate defects in finfet based cells. In: IEEE. **2016 21th IEEE European Test Symposium (ETS)**. [S.l.], 2016. p. 1–6.

MESSENGER, G. C. Collection of Charge on Junction Nodes from Ion Tracks. **IEEE Transactions on Nuclear Science**, v. 29, n. 6, p. 2024—-2031, 1982.

MOORE, G. E. et al. **Cramming more components onto integrated circuits**. [S.l.]: McGraw-Hill New York, NY, USA:, 1965.

NAGAMINE, K. **Introductory muon science**. [S.l.]: Cambridge University Press, 2003.

NARASIMHAM, B. et al. Characterization of digital single event transient pulse-widths in 130-nm and 90-nm CMOS technologies. **IEEE Transactions on Nuclear Science**, v. 54, n. 6, p. 2506–2511, 2007. ISSN 00189499.

NASEER, R. et al. Critical Charge Characterization for Soft Error Rate Modeling in 90nm SRAM. p. 1879–1882, 2007.

NEEDHAM, W.; PRUNTY, C.; YEOH, E. H. High volume microprocessor test escapes, an analysis of defects our tests are missing. In: IEEE. **Test Conference, 1998. Proceedings., International**. [S.l.], 1998. p. 25–34.

NEISSER, M.; WURM, S. ITRS lithography roadmap: 2015 challenges. **Advanced Optical Technologies**, De Gruyter, v. 4, n. 4, p. 235–240, 2015.

NICOLAIDIS, M. **Soft Errors in Modern Electronic Systems**. Boston, MA: Springer US, 2011. v. 41. 1–4 p. (Frontiers in Electronic Testing, c). ISBN 978-1-4419-6992-7. Disponível em: <http://link.springer.com/10.1007/978-1-4419-6993-4>.

NOWAK, E. J. et al. Turning silicon on its edge. **IEEE Circuits and Devices Magazine**, v. 20, n. 1, p. 20–31, 2004. ISSN 87553996.

NSENGIYUMVA, P. et al. A Comparison of the SEU Response of Planar and FinFET D Flip-Flops at Advanced Technology Nodes. **IEEE Transactions on Nuclear Science**, IEEE, v. 63, n. 1, p. 266–272, 2016. ISSN 00189499.

NSENGIYUMVA, P. et al. Analysis of Bulk FinFET Structural Effects on Single-Event Cross Sections. v. 64, n. 1, p. 441–448, 2017.

PAVLOV, A.; SACHDEV, M. **CMOS SRAM circuit design and parametric test in nano-scaled technologies: process-aware SRAM design and test**. [S.l.]: Springer Science & Business Media, 2008. v. 40.

PEREZ, Z. et al. Analysis and detection of hard-to-detect full open defects in finfet based sram cells. In: IEEE. **2020 IEEE Latin-American Test Symposium (LATS)**. [S.l.], 2020. p. 1–6.

PETERSEN, E. L. et al. io-9 DOi. n. 6, p. 2055–2063, 1982.

RABAEY, J. M.; CHANDRAKASAN, A.; NIKOLIC, B. **Digital Integrated Circuits–A Design Perspective**. [S.l.]: Pearson Education, 2003.

ROBERDS, B.; DOYLE, B. S. **Technique to obtain high mobility channels in MOS transistors by forming a strain layer on an underside of a channel**. [S.l.]: Google Patents, 2003. US Patent 6,563,152.

ROY, K. et al. Integrated Systems in the More-Than-Moore Era: Designing Low-Cost Energy-Efficient Systems Using Heterogeneous Components. **IEEE Design and Test**, IEEE, v. 33, n. 3, p. 56–65, 2013. ISSN 21682356.

ROYER, P.; GARCIA-REDONDO, F.; LOPEZ-VALLEJO, M. Evolution of radiation-induced soft errors in FinFET SRAMs under process variations beyond 22nm. **Proceedings of the 2015 IEEE/ACM International Symposium on Nanoscale Architectures, NANOARCH 2015**, p. 112–117, 2015.

SAMSUNG. **Samsung Launches Premium Exynos 9 Series Processor Built on the World's First 10nm FinFET Process Technology**. 2018. Disponível em: <https://news.samsung.com/global/

samsung-launches-premium-exynos-9-series-processor-built-on-the-worlds-first-10nm-finfet/process-technology>.

SEDRA, A. S.; SMITH, K. C. **Microelectronic circuits, Fifth**. [S.l.]: ISBN: 0-19-514252-7, 2004.

SEEVINCK, E.; LIST, F. J.; LOHSTROH, J. Static-noise margin analysis of mos sram cells. **IEEE Journal of solid-state circuits**, IEEE, v. 22, n. 5, p. 748–754, 1987.

SEGURA, J. A. et al. Quiescent current analysis and experimentation of defective cmos circuits. **Journal of Electronic Testing**, Springer, v. 3, n. 4, p. 337–348, 1992.

SIDDHARTHAN, R.; MEENAKSHI, K. Fault Modeling and Analysis for FinFET SRAM Arrays. 2013.

SIMSIR, M. O.; BHOJ, A.; JHA, N. K. Fault modeling for finfet circuits. In: IEEE. **2010 IEEE/ACM International Symposium on Nanoscale Architectures**. [S.l.], 2010. p. 41–46.

SINHA, S. et al. Exploring Sub-20nm FinFET Design with Predictive Technology Models. **DAC Design Automation Conference 2012**, IEEE, p. 283–288, 2012.

TANG, S. H. et al. Finfet-a quasi-planar double-gate mosfet. In: IEEE. **Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International**. [S.l.], 2001. p. 118–119.

TSHAGHARYAN, G. et al. Modeling and testing of aging faults in finfet memories for automotive applications. In: IEEE. **2018 IEEE International Test Conference (ITC)**. [S.l.], 2018. p. 1–10.

VATAJELU, E. I. et al. Analyzing resistive-open defects in sram core-cell under the effect of process variability. In: IEEE. **Test Symposium (ETS), 2013 18th IEEE European**. [S.l.], 2013. p. 1–6.

VAZQUEZ, J. et al. Stuck-open fault leakage and testing in nanometer technologies. In: IEEE. **2009 27th IEEE VLSI Test Symposium**. [S.l.], 2009. p. 315–320.

VILLACORTA, H.; SEGURA, J.; CHAMPAC, V. Impact of Fin-Height on SRAM Soft Error Sensitivity and Cell Stability. **Journal of Electronic Testing**, Springer, v. 32, n. 3, p. 307–314, jun 2016. ISSN 15730727.

WALDRON, N. et al. Ingaas gate-all-around nanowire devices on 300mm si substrates. **IEEE Electron Device Letters**, IEEE, v. 35, n. 11, p. 1097–1099, 2014.

WILSON, L. International technology roadmap for semiconductors (itrs). **Semiconductor Industry Association**, 2013.

YU, B. et al. Finfet scaling to 10nm gate length. In: IEEE; 1998. **International Electron Devices Meeting**. [S.l.], 2002. p. 251–254.

APPENDIX A — ADDITIONAL BACKGROUND

In this appendix, complementary information about the topics presented in this work is presented. Firstly a study of the Short Channel Effect, the main responsible for limiting the shrinking of the traditional MOSFET transistor is presented. Secondly, a brief presentation about the two main technologies that have emerged to deal with Short Channel Effects is presented: SOI MOSFET technology and Multiple-Gate MOSFET (MuG MOSFET) devices, among them, the FinFET. Further, the characteristics of FinFET quantization are presented. Then, the design of an SRAM block and its operation are explained, followed by the Static Noise Margin explanation. Finally, a brief explanation of the Fault Theory is also presented.

A.1 Short Channel Effect

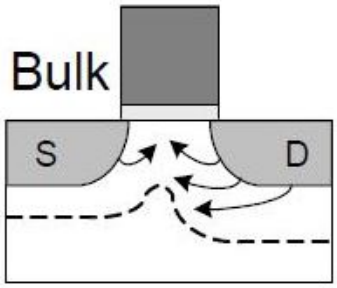
The Short Channel Effect occurs when the control of the gate over the channel region of the MOS transistor is hampered by the interference of the electric field lines from the source and the drain. As a result, the gate can not fully turn off the transistor, resulting in high leakage current. This phenomenon is known as the threshold voltage roll-off (COLINGE et al., 2008).

As explained in (COLINGE et al., 2008), the electric field lines between drain and source are propagated through the depletion region associated with the junctions. The electric field lines are illustrated in Figure A.1, where the higher number of lines from the drain to the gate represents that the electric field is higher in the drain when the transistor is conducting, the channel field increases from the source to the drain and reaches the maximum value close to the drain (MA et al., 2013). Its influence on the channel may be reduced by increasing the dopant concentration in the channel region, but for the devices of a small order of magnitude the required doping concentration becomes very high (10^{19} cm^{-3}) for the proper device operation.

The Short Channel Effect can be expressed through a mathematical model of Voltage-Doping Transformation (VDT), where it expresses the change in the threshold voltage of the device, as follows:

$$V_{THCC} = V_{TH\infty} - SCE - DIBL \tag{A.1}$$

Figure A.1: Electric field lines between source and drain in the channel region in bulk MOSFET.



Source: COLINGE et al.,2008.

where: V_{THCC} is the threshold voltage of the short channel; $V_{TH\infty}$ is the threshold voltage of a long channel device; SCE expresses the Short-Channel Effect; DIBL is the Drain-Induced Barrier Lowering.

The mathematician expression of SCE is expressed in

$$SCE = 0,64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}[1+\frac{x_j^2}{L_{eff}}^2]\frac{t_{ox}}{L_{eff}}\frac{t_{dep}}{L_{eff}}V_{bi} = 0,64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EIV_{bi} \quad \text{(A.2)}$$

and DIBL is expressed in

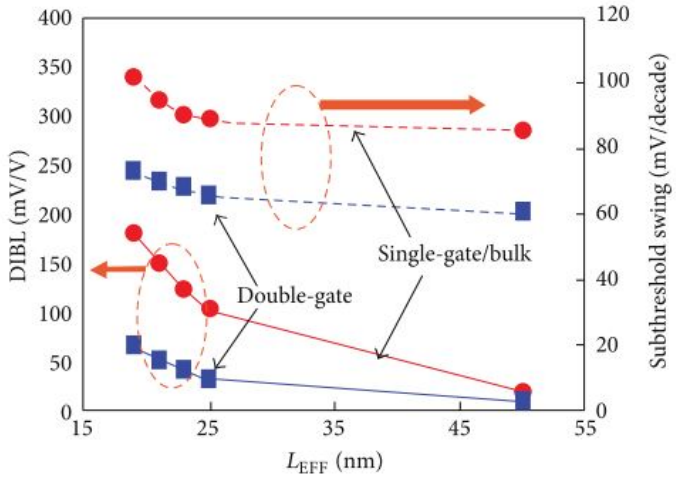
$$DIBL = 0,80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}[1+\frac{x_j^2}{L_{eff}}^2]\frac{t_{ox}}{L_{eff}}\frac{t_{dep}}{L_{eff}}V_{DS} = 0,80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EIV_{DS} \quad \text{(A.3)}$$

where: ε_{Si} and ε_{ox} are the silicon's permittivity constant and silicon oxide, respectively; L_{eff} is effective channel length; V_{DS} is the voltage between drain and the source; V_{bi} is the built-in voltage; t_{ox} is the thickness of the gate oxide; x_j is the junction thickness of the source and the drain; t_{dep} is penetration thickness of the electric field generated by the gate in the channel region, which it is equal to the thickness of the depletion region below the gate (COLINGE et al., 2008).

The parameter EI, presented in Equations A.2 and A.3 is the Electrostatic Integrity factor, it depends on the geometry of the device and is a measure of the electric field lines of influence of the channel region drain.

In Figure A.2 a comparison between single and double gates is presented, verifying the relationship of the effective length with DIBL and the sub-threshold voltage. The lower values obtained by the double gate, especially in DIBL, as seen in Equation A.1, where there is a difference of about 4 times for small dimensions, result in a smaller short-channel effect (NOWAK et al., 2004).

Figure A.2: Drain-Induced Barrier Lowering x Effective Channel Length for Single-gate/bulk and Double-gate.



Source: NOWAK et al.,2004.

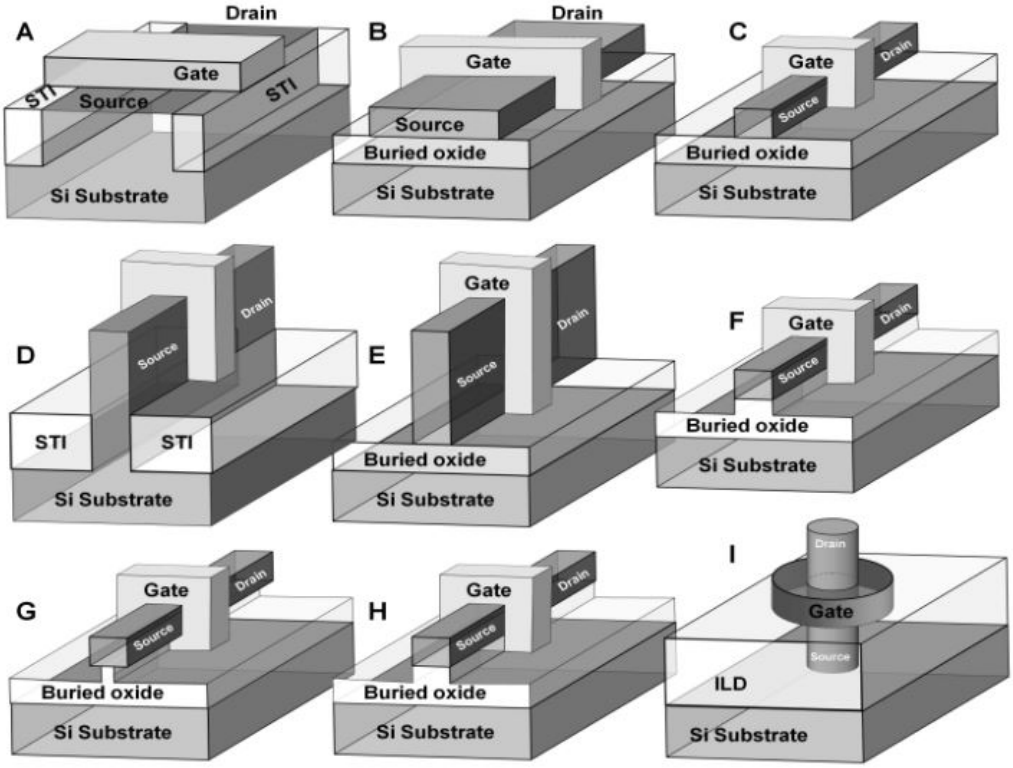
A.2 State-of-the-Art of MOSFET

Some transistor technologies of state-of-the-art are presented in the following. Figure A.3 shows: (A) the traditional planar MOSFET (bulk CMOS); (B) SOI MOSFET; (C) Triple-gate (trigate) SOI MOSFET (square); (D) Bulk trigate MOSFET (bulk FinFET); (E) SOI trigate MOSFET (SOI FinFET); (F) Pi-gate (Π-gate) SOI MOSFET; (G) Omega-gate (Ω-gate) SOI MOSFET; (H) Horizontal gate-all-around (GAA); (I) Vertical gate-all-around. Beyond the bulk FinFET presented in this work, the SOI MOSFET is presented here as complemented, because it is the main competitor of bulk FinFET in the transistor industry today. About the elements in Figure A.3, the shallow trench isolation (STI) is the oxide isolation for the bulk technology, and the interlayer dielectric (ILD) is the oxide isolation for the vertical GAA (WALDRON et al., 2014).

A.2.1 SOI MOSFET

The main Silicon-On-Insulator (SOI) MOSFET devices on the market are described in the following. SOI MOSFETs are classified according to the number of gates the transistor has. The transistor composed by a single gate is simply named SOI MOSFET. Regarding the other transistors, their structures are presented in the following sub-sections.

Figure A.3: Different types of MOSFET gate configuration.



Source: COLINGE,2014.

A.2.1.1 Single Gate SOI MOSFET

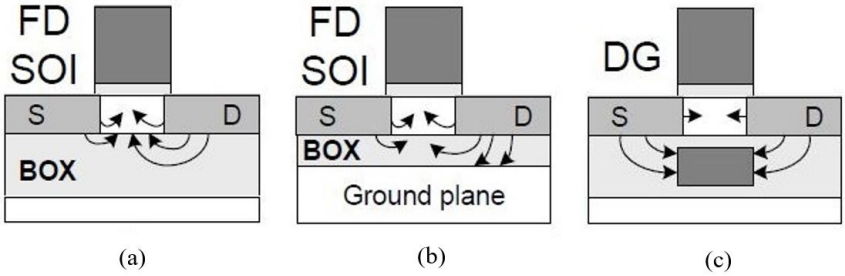
In the following, the technologies that composes the Single Gate SOI MOSFET are discussed. The Partially and Fully Depleted SOI MOSFET, and he Ultra-Thin Body and Buried Oxide SOI MOSFET and their physical characteristics are presented.

- **PD and FD SOI MOSFET:** The Partially Depleted (PD) SOI MOSFETs device is constructed on a silicon substrate, with an oxide layer in the middle. In the top layer of silicon, are the connections between the source and the drain regions. Below the drain region is a region which is known as a floating body. The active area of the silicon on the oxide is about 0.15 μm (MARSHALL; NATARAJAN, 2002).

  Throughout the evolution of technology, the Fully Depleted (FD) SOI MOSFET, with a better electrostatic relationship between the gate and the channel, was developed. The result is better linearity in the voltage-current curve in the drain, with higher gain, on the slope of the sub-threshold current. The FDSOI does not have the floating body, it has only the channel region and the source and drain areas, with small depth, less than 0.1 μm, and below that region is the oxide, on the substrate (COLINGE et al., 2008).

Regarding the Short Channel Effect in SOI MOSFET, both PDSOI and FDSOI MOSFETs, the electric field lines generated by the source and drain propagate through the Buried Oxide (BOX) before reaching the channel region, see Figure A.4-(a). The Short Channel Effect in the PDSOI and FDSOI devices may be better or worse than the effect on the planar MOSFET, depending on the thickness of the oxide film, silicon, and also on the dopant concentration (COLINGE et al., 2008).

Figure A.4: Electric field lines between source and drain on the channel region: (a) in the traditional FDSOI MOSFET (b) in the channel region on UTBB SOI MOSFET (c) in the channel region on Double-Gate MOSFET.



(a) (b) (c)

Source: COLINGE et al.,2008.

- **UTBB SOI MOSFET:** Ultra-Thin Body and Buried Oxide (UTBB) (FD) SOI MOSFET technology is the evolution of FDSOI, it is presented in Figure A.3-B. It has excellent electrostatic control of the gate in the channel and the reduced Short Channel Effect. This reduction occurs because of the ground plane below the thin layer of oxide (BOX), which has the function of absorbing the electric field generated by the source and drain, thus reducing its intensity in the channel region, see Figure A.4-(b). UTBB SOI MOSFET has the inconvenience of increasing the junction capacitance (COLINGE et al., 2008; MAGARSHACK; FLATRESSE; CESANA, 2013; KILCHYTSKA; FLANDRE; ANDRIEU, 2012).

A.2.1.2 Double Gate SOI MOSFET

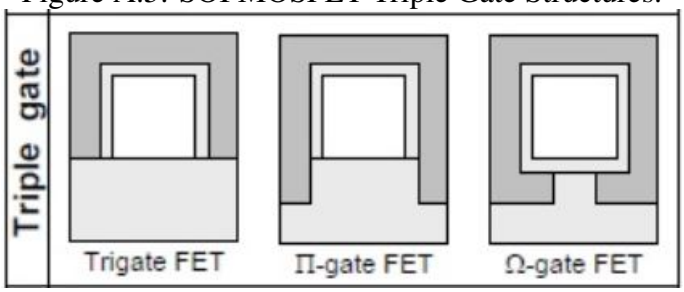
Following the two-dimensional gates transistors, namely Double-Gate MOS (DGMOS) are presented. Chronologically, the first DGMOS device is the XMOS which consists of an FDSOI with two gates connected. One gate is located inside the device and the channel is between these gates. This method solves the problem of the Short Channel Effect, which can be observed in Figure A.4-(c). The electric field generated between source and drain is blocked inside the oxide by the buried gate (COLINGE et al., 2008).

On the other hand, this method of manufacture proved to be very difficult to be implemented. Therefore, an alternative found is to raise the channel vertically on top of oxide, aiming to increase the area of influence of the gate, creating a triple gate device (MAGARSHACK; FLATRESSE; CESANA, 2013).

A.2.1.3 Triple Gate SOI MOSFET

These transistors consist of a silicon island on the body device. Initially, the triple gates are square with the three edges of the gate with similar dimensions. Therefore, the gate has a significant influence in three dimensions over the channel, turning in a trigate FET. Figure A.3-(C, F and G) show these trigate structures and Figure A.5 shows they gate section (COLINGE et al., 2008). The basis of this technology is on a UTBB SOI MOSFET transistor because it has a ground plane under a thin oxide (MAGARSHACK; FLATRESSE; CESANA, 2013).

Figure A.5: SOI MOSFET Triple Gate Structures.



Source: COLINGE et al.,2008.

The electrostatic integrity of the triple gate MOSFET can be improved by extending the edges of the gates to a depth below the channel region and the oxide. Therefore, two variations of the triple gate devices have emerged with better electrical characteristics: the MOSFET with the gate in Π format, and the MOSFET with the gate in Ω format (COLINGE et al., 2008). The Π-MOSFET has a small part of the gate buried beneath the channel, on the other side, Ω-MOSFET also has part of the gate buried, however, it makes a curve around the channel region almost forming a gate in four dimensions. However, the implementation of this trigate technology was still complicated for the foundry, so an alternative was to increase the height of the silicon island structures, This way forming a kind of "fin" over the body of transistor, thus the term FinFET was born (MAGARSHACK; FLATRESSE; CESANA, 2013). The electrical characteristics are not so well as the Π-gate and Ω-gate but it is easier to produce. Important to mention that, if the

insulation on the top of the fin is dense (hard mask), the FinFET is classified as a double gate (COLINGE et al., 2008).

A.2.1.4 Quadruple Gate SOI MOSFET

The Quadruple Gate SOI MOSFET also know as Gate-All-Around is the MOS device with a gate wrapped around the four dimensions of the conduction channel, in the horizontal or the vertical axis. Theoretically, it offers the best control over the channel, mainly the cylindrical GAA. This happens because of the influence of the great electric field of the gate in the channel stands out over the Short Channel Effect (COLINGE et al., 2008; WALDRON et al., 2014). However, this kind of technology is still expensive to be developed by companies, so it is not being implemented.

A.3 Fin Quantization

Firstly, an equation is used to determines the minimum width (W) of a Fin. Secondly, it is determined the number of fins necessary to get the total width of the transistor, this is known as "Width Quantization". It is important to mention that the equations treated in this section apply to the bulk FinFET and SOI FinFET (BHATTACHARYA; JHA, 2014).

The minimum width (W_{min}) is the smallest possible width of the technology is determined by the Equation:

$$W_{min} = 2 \times HFIN + TFIN \tag{A.4}$$

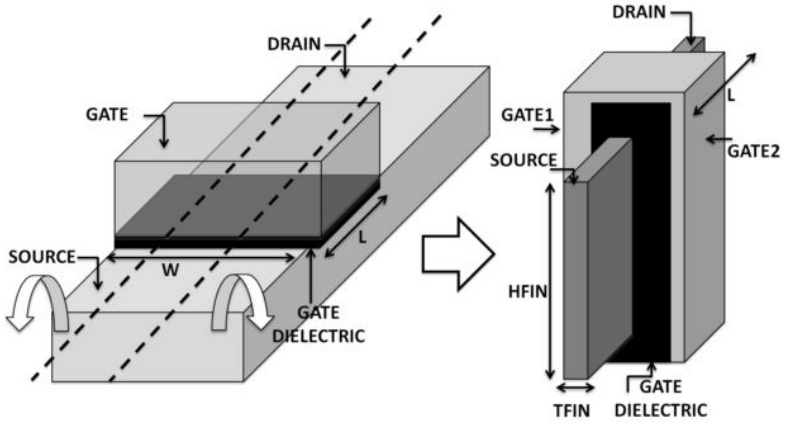
where HFIN is the Fin's height and TFIN is the Fin's thickness of (KAREL et al., 2016). There is also a simplified version of this equation that does not consider TFIN, because it is very small

$$W_{min} = 2 \times HFIN. \tag{A.5}$$

The Figure A.6 shows a comparison between a planar transistor and a FinFET, highlighting the Fin dimension parameters. One can check in the figure the parameters HFIN, TFIN and the length (L) of FinFET as well as the front grates and rear gates.

Because of the characteristics of the manufacturing process, it is not possible to individually modify the parameters of HFIN and TFIN for each transistor. Therefore, the

Figure A.6: Planar Transistor (left) and FinFET (right).



Source: KAREL et al.,2016.

adjusting of the value of the FinFET width W_{min} is made by multiplying the number of fins (NFIN). This is known as the quantization of width, the W is determined throughout the equation:

$$W = W_{min} \times NFIN. \tag{A.6}$$

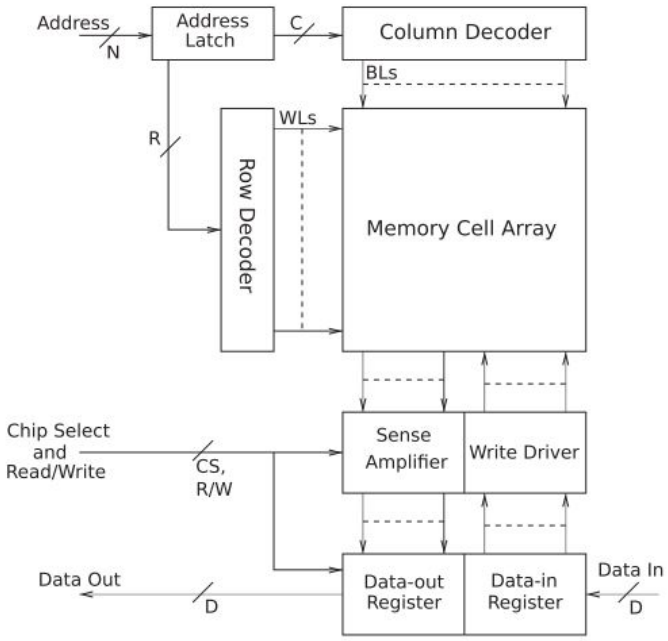
A.4 SRAM Block Structure

The SRAM blocks consist mostly of cells that store bits. The SRAM cells are organized in the form of an array as shown in Figure A.7. The cell array has 2^M lines and 2^N columns for a total storage capacity of 2^{M+N} (SEDRA; SMITH, 2004).

The SRAM block has three modes of operation: storage, read and write. The following is described each elucidating, and the function of the peripheral circuits (SEDRA; SMITH, 2004).

- Storage Mode: While there is no request to read or write in a cell, it is disconnected from the bit column not triggering the *WL*. It is also called Hold mode;
- Read Mode: First the pre-charge circuit polarizes the bit columns to a value of V_{DD}. Thus, a cell line is triggered through the *WL*, and after the sense amplifier is triggered reading the column sending the signal to the output register;
- Write Mode: The input data is sent through the input register to the write driver which writes the signal into the bit column, thus the cell is then connected through the *WL*.

Figure A.7: SRAM Block.

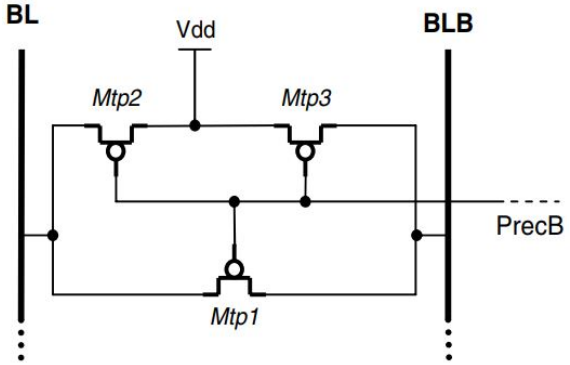


Source: AGBO et al.,2016.

In the memory block, there are circuits with specific functions which consist of: pre-charger, sense amplifier, writing driver, line decoder, a row decoder, and registers (AGBO et al., 2016). The designs of these blocks can be found in textbooks as (SEDRA; SMITH, 2004; RABAEY; CHANDRAKASAN; NIKOLIC, 2003).

Figure A.8 shows the pre-charge circuit. The pre-charge circuit is activated during the storage phase of the cell. Its function is to equalize *BL* and *BLB*, in order to keep the two bit lines with the same voltage. In this phase the signal *PrecB* is in low level and the V_{DD} voltage passes through the transistors *Mtp1*, *Mtp2*, and *Mtp3* to the bit lines (DILILLO et al., 2005).

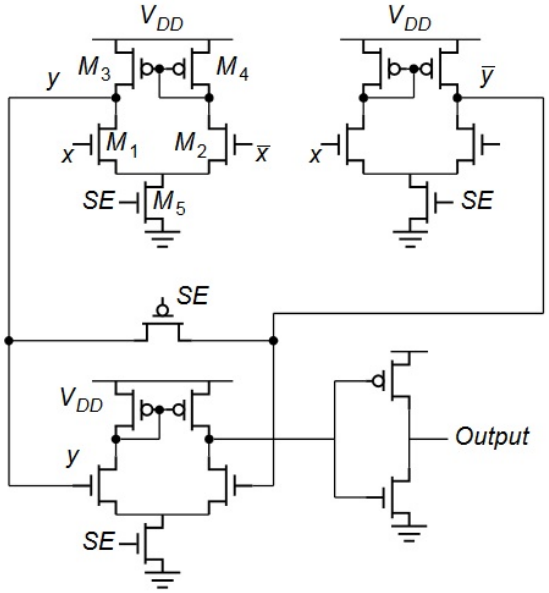
Figure A.8: Pre-charge circuit schematic.



Source: DILILLO et al. 2005.

Figure A.9 shows the differential amplifier used for reading. To be more precise a two-stage differential amplifier. The circuit can amplify a small potential difference between the inputs. Its effectiveness consists of rejecting the common noise, and amplifying the true difference between the signals, generating the logical data of '0' and '1'. The two-stage circuit allows a quick generation of output data. The signals x and $\overline{x}$ are connected to the bit lines, *SE* is the control signal, y and $\overline{y}$ are the signal of bits in the first stage of amplification, and the 'Output' signal is the logical value of the bit (RABAEY; CHANDRAKASAN; NIKOLIC, 2003).

Figure A.9: Differential sense amplifier schematic

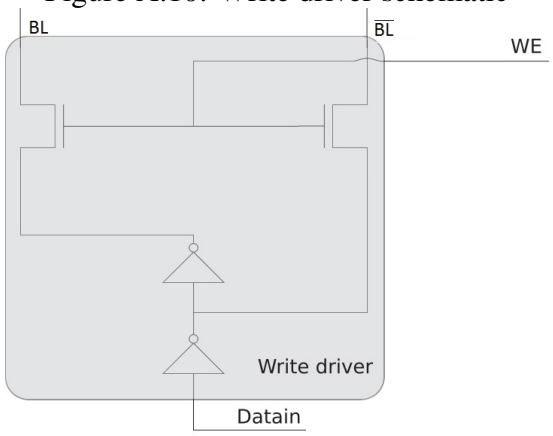


Source: RABAEY; CHANDRAKASAN; NIKOLIC 2003.

The write driver circuit is shown in Figure A.10, it consists of two inverter drivers, to generate the bit data, and two transistors to pass through the bit column (*BL* and $\overline{BL}$). The control signal is *WE* and the data input is *Datain*. It is interesting to mention that the focus of the inverters is to generate a strong zero in one of the bit columns so that the pMOS and nMOS from the inverters can be designed with the same dimension (AGBO et al., 2016).

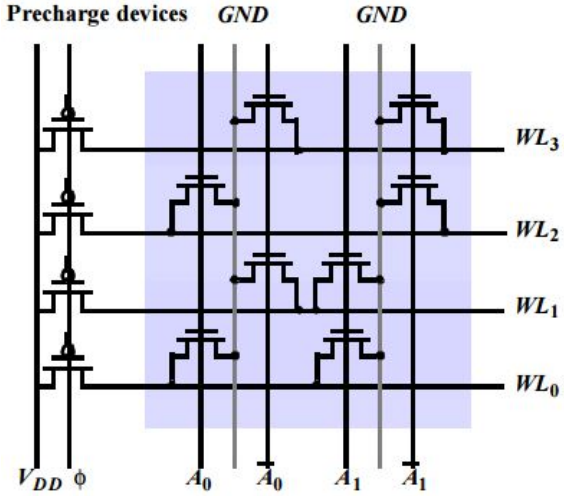
Figure A.11 presents the line decoder. The decoder consists of an optimized circuit based on NOR gates to drive a given line WL_n, controlled by the combinational input A_n, n is integer starting from 0. Note that the line activation only occurs when the precharge circuit signal is at a high level (ϕ = '0'), this means the block is out of idle mode (RABAEY; CHANDRAKASAN; NIKOLIC, 2003).

Figure A.10: Write driver schematic



Source: AGBO et al. 2016.

Figure A.11: Schematic of NOR Dynamic Line Decoder



Source: RABAEY; CHANDRAKASAN; NIKOLIC 2003.

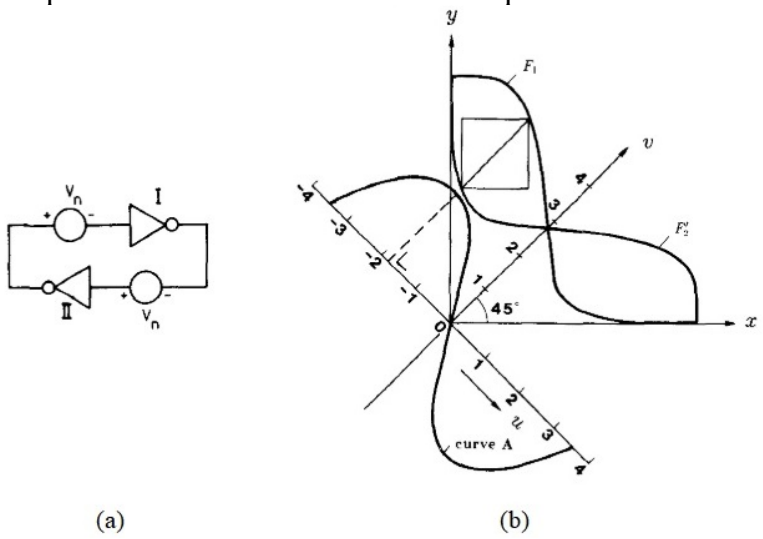
A.5 Static Noise Margin

It is important to evaluate the SRAM cell for stability in the presence of noise signals. Cell stability determines the sensitivity of operating conditions and process tolerances. The static noise margin (SNM) is a metric of stability of the SRAM cell that determines the noise's margin tolerable by the cell. In other words, SNM is the amount of voltage noise required at the input nodes to flip the value of the cell, it is obtained with the voltage transfer characteristic (VTC), the voltage transition curves, of the two cross-coupled inverters of the SRAM cell (SEEVINCK; LIST; LOHSTROH, 1987).

The obtaining of the SNM from an SRAM cell is made by plotting the VTCs of the two cross-coupled inverters by the injection of two voltage sources (Wn) in the input of inverters. The VTC of one of the inverters is rotated 45º flipped in relation with the

other concerning the axis y = x to form a “butterfly curve”. The SNM is the side of the smaller square that can be fitted inside the “eye” of the graph as shown in Figure A.12 (SEEVINCK; LIST; LOHSTROH, 1987).

Figure A.12: (a) Logic gate of SRAM bit cell with the source voltage Vn to SNM simulation and (b) sample SNM – the side of the smaller square fitted inside the "eye".

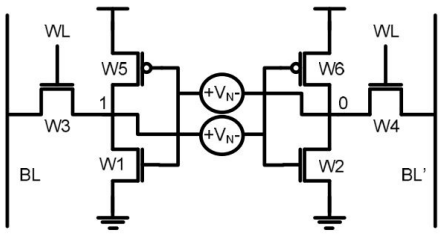


(a) (b)

Source: SEEVINCK; LIST; LOHSTROH 1987.

For simulating the SNM, it is required to insert two DC noise voltage sources one at the internal node of the bit cell. So, the VTCs are measured at the output of the inverters. Figure A.13 illustrates the schematic of a 6T SRAM cell to simulate the static noise margin. The sources V_N are the DC (Direct Current) noise sources (SEEVINCK; LIST; LOHSTROH, 1987).

Figure A.13: Schematic of a 6T SRAM bit cell with noise voltage sources for measuring SNM

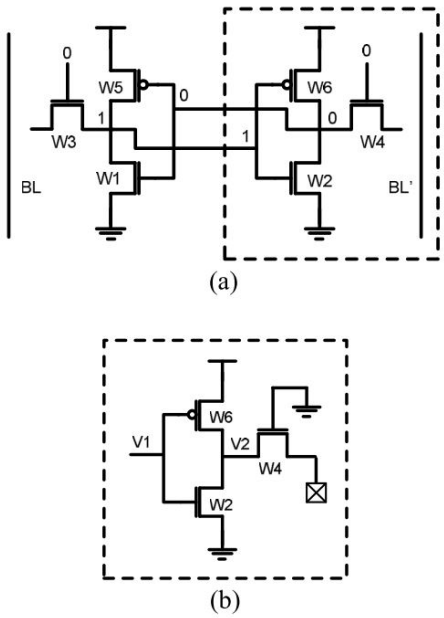


Source: SEEVINCK; LIST; LOHSTROH 1987.

There are three different SNMs that can be obtained from the 3 operations of SRAM; data retention or hold, read, and write:

- **Hold:** When the cell is in storage mode, the word lines are not active, the isolated cell must keep the data in the coupled inverters. Figure A.14-(a) shows the SRAM in storage mode and the corresponding circuit Figure A.14-(b) for measuring the SNM (SEEVINCK; LIST; LOHSTROH, 1987).

Figure A.14: Equivalent SRAM circuit during storage mode (a) and circuit to measure hold SNM (b)



Source: ARANDILLA; ALVAREZ; ROQUE 2011.

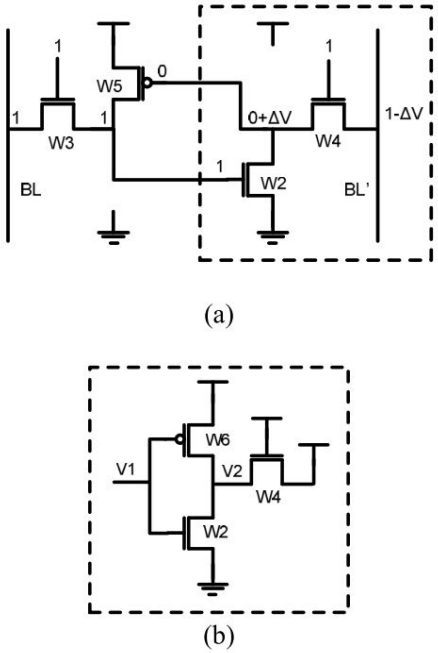
- **Read:** Obtained during the read operation, this is the most vulnerable situation for the cell because it must retain its state in the presence of the bit line precharged with '1'. Figure A.15-(a) shows the equivalent circuit during the read operation. At the start of the read operation, the bit lines are precharged to V_{DD} and then the word lines are activated to access the cell. The node storing '0' data pulls one of the bit lines to GND causing a voltage swing. The circuit for measuring the read margin is shown in Figure A.15-(b) (SEEVINCK; LIST; LOHSTROH, 1987).

- **Write:** The write SNM is defined as the minimum noise needed to flip the cell state during a write operation. The equivalent circuit for writing '0' to a cell storing '1' is shown in Figure A.16-(a). The bit line that is charged to '0' pulls the node of the cell storing '1' to '0' causing the cell to flip the state. Since the cross-coupled inverters have complementary data, their VTCs are measured using different circuits as shown in Figure A.16-(b) (PAVLOV; SACHDEV, 2008).

A.6 Fault Theory

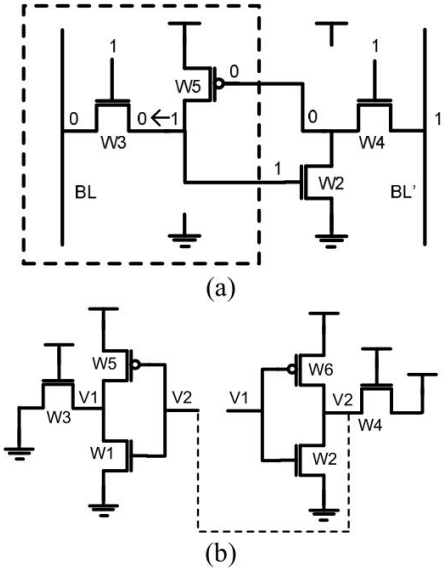
Imperfections in electronic systems are classified into various forms in the Fault and Test Theory literature. Therefore, the terminology used in this work, according to the definitions of (GOOR, 1991; BUSHNELL; AGRAWAL, 2000), are given below:

Figure A.15: Equivalent SRAM circuit during read access (a) and circuit to measure read SNM (b)



Source: ARANDILLA; ALVAREZ; ROQUE 2011.

Figure A.16: Equivalent SRAM circuit during write mode (a) and circuit to measure write SNM (b)



Source: ARANDILLA; ALVAREZ; ROQUE 2011.

- **Defect:** it is a non-intentional difference between the designed hardware and the built hardware. Some typical defects are manufacturing process defects; defects of materials; defects by degradation; and packaging defects;

- **Fault:** it is a representation of a Defect at an abstract functional level. The difference between Defect and Fault is more subtle. The fault is a functional imperfection

rather the defect is a physical imperfection. In logical circuits and memories, faults can be modeled to a set of functional fault models associated with the observed behavior in the device;

- **Error:** it is a wrong signal value, that means, for an input vector the output generated came with an unexpected result. For example, the output of a logic gate shows incorrect results;

- **Failure:** it is related to systems, the inaccuracy or interruption of system behavior. An electronic system that not operates as planned is presenting a failure. It is caused by error, a manifestation of faults in the system.

A.6.1 Fault Classification

The Fault is classified according to the way it manifests, and it is divided into hard and soft, where hard faults are permanent faults, and soft faults are non-permanent. This non-permanent faults may be a transient or intermittent fault (GOOR, 1991; BUSHNELL; AGRAWAL, 2000).

- **Hard Fault:** permanent faults caused either by bad electrical connections, broken or burned components, burnt-out chip wire, chip and package connection corroded or even errors in the circuit design. These faults can be modeled with a fault model;

- **Soft Transient Fault:** non-permanent faults that occur randomly caused by environmental conditions as ionizing particles, cosmic rays, air pollution, humidity, temperature, pressure, vibrations, power supply fluctuations, electromagnetic interference, static electrical discharges, and ground loops. These faults are critical mainly by memory integrated circuit, and do not have a well-defined fault model;

- **Soft Intermittent Fault:** non-permanent faults that occur randomly and consistently, it is caused by environmental conditions as loose connections, deterioration of components, critical timing, resistance and capacitance variations, physical irregularities, and noise. These faults can be modeled by permanent fault models, but the fault needs to be continuously tested until the fault be detected. In memory circuits, it is usually called dynamic faults. Eventually, intermittent faults can become permanent faults due to the degradation of the circuit.