Evento	Salão UFRGS 2022: SIC - XXXIV SALÃO DE INICIAÇÃO CIENTÍFICA DA UFRGS
Ano	2022
Local	Campus Centro - UFRGS
Título	Computação aproximada - circuitos aritméticos aproximados
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In approximate computing, approximate circuits are highly relevant to enable the efficiency of specific operations. This work aims to investigate the behavior of adder circuits known as Ripple Carry Adders (RCA) in cases where certain breaks in their carry chains occur. These breaks aim to optimize the operation of binary sums through an approximate adder circuit, thus revealing new efficient ways to approximate adder circuits, contributing to the development of approximate computation. Furthermore, the relationship between performance and error metrics represents an interesting design choice according to the number of breaks in the carry chain. In order to evaluate the impact of these breaks in operations involving Ripple Carry Adders, some experiments were carried out, taking into account the insertion of 0 or 1 logic in the modified carry chain, allowing the analysis of performance gain and functional errors generated. As a result, the impacts of interference on the RCA carry in chains could be graphically and metrically visualized through the use of error metrics related to the approximate computation. The different ways of making interference in the carry-in chains assure several different analysis options, guaranteeing the need for various forms of analysis on the subject. These results can be used as a basis for studying other adder architectures.