Design of Self-Checking Fully Differential Circuits and Boards

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***Abstract*—A design methodology for on-line testing analog linear fully differential (FD) circuits is presented in this work. The test strategy is based on concurrently monitoring via an analog checker the common mode (CM) at the inputs of all amplifiers. The totally self-checking (TSC) goal is achieved for linear FD implementations provided that the checker CM threshold is small enough with respect to the specified margins of erroneous behavior in the circuit outputs. The design methodology is illustrated for a switched-capacitor biquadratic filter and the self-checking properties evaluated for a hard/soft-fault model. A large checker threshold of 100 mV of CM is chosen since the filter implementation does not minimize nonidealities (e.g., amplifier offsets or clock feedthrough) which result in significant CM components. The circuit outputs are accepted to deviate within a 10% band. With the implemented checker, the TSC goal is not achieved for some faults in narrow regions of the frequency band. For the worst case, a hard fault which results in a 31% deviation is undetected in only a narrow band of approximately 310 Hz. The circuit can be made TSC with a checker threshold of 40 mV and an accepted output deviation of 15%. This is, however, more demanding on the checker (which currently takes less than 3% of the total area and about 7.6% of the total power) and requires an improved filter implementation to reduce CM components. Our solution consists of relaxing a bit the TSC property of the functional block and applying a periodical off-line test to make the checker strongly code disjoint (SCD). This is easy to implement since an off-line test is also required for the checker. The checker outputs a double-rail error indication which ensures compatibility with digital checkers and makes the design of self-checking mixed signal circuits straightforward. The circuit-level mixed-signal approach is extended to the board level by means of the IEEE Std. 1149.1 digital test bus.**

***Index Terms*—Boundary scan, fully differential circuits, mixed-signal test, safety applications, self-checking systems.**

I. Introduction

FROM the very first design, any integrated circuit (IC) undergoes prototype debugging, production, and periodic maintenance tests to simply identify and isolate or even replace faulty parts. In high-safety systems, such as automotive, avionics, high-speed train, and nuclear plants, poor functioning cannot be tolerated and detecting faults concurrently to the application also becomes essential. The on-line detection capability, used for checking the validity of undertaken operations, can then be ensured by self-checking circuits in these systems.

For many years, self-checking circuits have been designed for purely digital applications using error-detecting and error-correcting codes. However, there is now a need for extending this concept to the analog domain, since the integration of systems on chip is forcing an evolution toward designing (and hence testing) mixed-signal IC's.

In the last few years, several techniques on concurrent error detection for mixed-signal circuits have appeared. Some extend testing concepts coined for digital circuits to analog counterparts, and others exploit behavioral or structural properties inherent to some classes of analog circuits. The method we propose is aimed at mixed-signal circuits whose analog parts are fully differential (FD). The use of FD circuits has contributed to achieve the high linearity and/or the high signal-to-noise ratio required in high-performance linear and nonlinear applications [1]. Herein, we concentrate on the on-line testing of the analog parts of mixed-signal circuits.

In this paper, we propose an on-line testing approach for linear FD circuits based on monitoring the common mode (CM) at the inputs of the differential amplifiers (DOA's) via an analog checker. Compliance with self-checking digital parts is ensured since the checker outputs a double-rail error indication. The design of fully self-checking systems is also addressed by extending the testing capabilities of mixed-signal circuits to the board level. This extension is based on the merging proposed in [2] of the IEEE Boundary Scan Std. 1149.1 [3] with the Unified Built-In Self-Test Technique [4].

The paper is organized as follows. Section II briefly describes existing techniques on concurrent error detection (CED) for analog circuits. Section III reviews the basis of the digital self-checking theory. The extension of this theory to cope with analog circuits is described in Section IV. The design methodology for CED in linear FD circuits is detailed in Section V. This methodology is applied in Section VI for the design of a self-checking FD switched-capacitor (SC) biquadratic filter. Experimental results obtained with the fabrication of this circuit are described in Section VII. The extension of this CED methodology to mixed-signal circuits at the board level is described in Section VIII. Finally, Section IX concludes this work.

II. Previous Work

Recently, some techniques on concurrent error detection for analog and mixed-signal single-ended circuits have been published [5]–[7].

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The technique developed by Chatterjee in 1991 [5] is applicable to state variable systems, an important class of linear circuits. The concurrent error detection is based on the generation of additional state variables for the circuit such that checksum properties are satisfied. An error indication can then be obtained by combining the state variables and their derivatives by means of appropriate checkers. For this approach, the fault coverage is dependent on the kind of checking circuitry being used and the hardware overhead is virtually constant.

An on-line testing technique based on the assumption of some modularity in the system was proposed by Huertas *et al.* [6]. In this technique, the system is partitioned in similar functional blocks and a programmable counterpart is used to mimic every partition during testing. Then, considering identical inputs, a comparison mechanism can indicate whether the block under test behaves like the programmable block or not. On-line testing can thus be achieved serially for every system block, and full system replication is avoided.

A concurrent error detection technique based on time redundancy is applied to the design of a current-mode analog–digital (A/D) converter in [7]. In the proposed scheme, an input current and its complement with respect to the reference current are converted one after another. Then the digital data resulting from both conversions are compared by a double-rail checker to identify errors. A high coverage of transient and permanent faults on the switches is achieved thanks to the encoding of the input current in the second conversion. This technique can be easily extended to any algorithmic data converter.

Concurrent error detection in FD circuits has been addressed before in [8] and [9]. In [8], a differential code is defined. According to this code, the problems of designing self-checking mixed-signal circuits for a single hard-fault model are identified and a tentative way of facing them in the specific case of a sample-and-hold circuit is given. In [9], the redesign of DOA's is proposed as the means of ensuring the detection of single transient faults by corruption of the differential code at the amplifier outputs. Both approaches based on testing the circuit differential code result in a much simpler test technique for FD circuits than the approaches mentioned previously.

In comparison to previous works on testing FD circuits, ours has the following advantages for the case of linear circuits: 1) only the inputs of the DOA's are monitored. Since these must be at a virtual analog ground, checker precision is maximized due to the small amplitude of the signals observed; 2) a single analog checker may be used for simultaneously monitoring all stages of a linear FD circuit. This generally involves two or three DOA's whose inputs are placed closely to the checker in the actual layout. Individual checkers for each node may be used if this is not possible; 3) hard faults in DOA's and hard and soft faults in external components are considered in the fault model; and last, but not least, 4) the redesign of existing operational amplifiers can be avoided.

III. Review of Digital Self-Checking

In digital self-checking circuits, the concurrent error detection capability is achieved by means of functional circuits which deliver encoded outputs and checkers which verify whether these outputs belong to the error-detecting code [10]. The general structure is shown in Fig. 1.

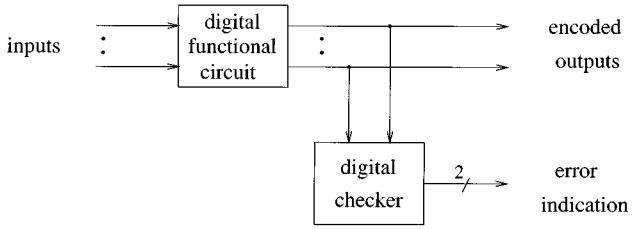


Fig. 1. Self-checking digital circuit.

Most often, self-checking circuits are aimed at reaching the **totally self-checking (TSC) goal**: *the first erroneous output of the functional circuit results in an error indication in the checker outputs.* The basic properties required for achieving this goal are independent of the circuit implementation, and they can be described at an abstract level in terms of the fault-free and faulty functions of the circuit [11]. As shown by the definitions in Table I, a functional circuit is TSC if it is self-testing and fault secure.

A TSC functional circuit is very desirable since transient faults as well as permanent faults can be detected. The faults can be immediately detected upon occurrence, thus preventing corruption of data. For fault detection, a TSC checker is required. The code-disjoint property is also required for a TSC checker since, as opposed to the functional circuit, noncode words can be applied to it.

The TSC property for a functional circuit (checker) gives sufficient, but not necessary conditions to ensure the TSC goal. This is because the self-testing property may not be necessary in a functional circuit (checker) for which the fault secure (code disjoint) property is ensured. The largest class of functional circuits which achieve the TSC goal is the strongly fault secure (SFS) circuits [12]. The largest class of checkers which achieves the TSC is the strongly code disjoint (SCD) checkers [13]. In SCD checkers, as in SFS circuits, some faults may be undetectable. A first undetectable fault may be recursively combined with other faults to give undetectable fault sequences. From a safety point of view, the SCD checker is able to transpose each noncode word input to a noncode word output, producing an error indication.

As exposed in [12], the effectiveness of TSC circuits is based on a hypothesis (see Table I) concerning the occurrence of multiple faults. This hypothesis is necessary to avoid the following situations when a fault sequence has occurred in the system without being detected [14].

1) Under the sequence, the functional block gives erroneous outputs that are code words.
2) Some faults of the sequence affect the functional block, and others affect the checker. Under the sequence, the functional block gives some erroneous output which is a noncode word and the checker transposes this noncode word output of the functional block as a code word on its outputs.

Under this hypothesis, it can be shown that a digital circuit made of TSC blocks, or from an SFS functional block on one hand and from a TSC, or a self-testing, or an SCD checker on the

TABLE I
DIGITAL SELF-CHECKING THEORY

TSC functional circuit. *A functional circuit G is TSC for a fault set F if it is fault secure and self-testing for the fault set F.*

Fault-secure. *G is fault secure for a fault set F if for all faults in F and all input values belonging to the input code space, the output value is either correct or it does not belong to the output code space.*

Self-testing. *G is self-testing for a fault set F if for each fault in F there is at least one input value belonging to the input code space that produces a value on the nodes being monitored which does not belong to the checking code space.*

Strongly fault secure. *A circuit G is strongly fault secure (SFS) for the fault set F if, for every fault in F, either a) G is TSC or b) G is fault secure and if a new fault in F occurs, for the obtained multiple fault, either the case a) or the case b) is true.*

TSC checker. *A checker G is TSC for a fault set F if it is fault-secure, code disjoint and self-testing for the fault set F.*

Code-disjoint. *A checker G is code disjoint if it always maps input values belonging to the input code space into output values belonging to the output code space, and input values which do not belong to the input code space into output values which do not belong to the output code space.*

Strongly code-disjoint. *A checker G is strongly code-disjoint (SCD) for a fault set F if before the occurrence of any fault G is code disjoint, and for every fault in F, either a) G is self-testing or (b) G always maps input values which do not belong to the input code space to output values which do not belong to the output code space and if a new fault in F occurs, for the obtained multiple fault, either case a) or case b) is true.*

Hypothesis. *In a system made of a functional circuit and a checker a) faults occur one at a time, and (b) between any two faults, enough time elapses so that the functional circuit inputs and the checker inputs receive all the elements of the respective input code spaces.*

other hand, achieves the TSC goal. However, the ability to detect faults (ensured by the TSC or SCD property) must be in practice accompanied by an ability to systematically exercise the circuits to ensure the previous hypothesis. A way of ensuring this hypothesis is by applying periodic test patterns. For example, a technique known as self-exercising checkers is proposed in [4] for the case that only noncode words can fully test the checker capability of signaling functional error occurrences.

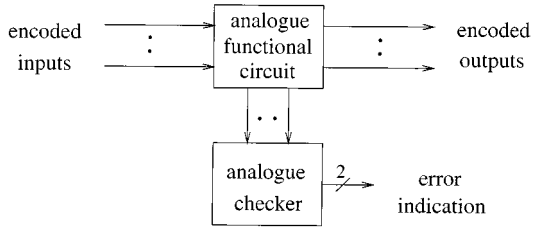


Fig. 2. Self-checking analog circuit.

IV. ANALOG SELF-CHECKING THEORY

Similar to digital self-checking circuits, the aim of designing analog self-checking circuits is to meet the TSC goal. The intention of this section is to show that the TSC goal can be attained for analog circuits in a similar way as for digital circuits, that is, designing self-checking functional blocks with associated analog checkers as shown in Fig. 2. This is possible since analog codes can also be defined, for example the differential and duplication codes [15]. A tolerance is required for checking the validity of an analog functional circuit, and this is taken into account within the analog code. For the sake of compatibility with the test of the digital parts, we expect the analog checkers to produce double-rail digital error indications.

The nodes to be monitored by an analog checker are not necessarily those associated with the functional circuit outputs, due to commonly used feedback circuitry. In addition, the most important difference is that the input and output code spaces of an analog circuit have an infinite number of elements. Signals can take analog values (e.g., input voltages and frequencies from a continuous space). Thus, the implementation, the input and output code spaces, and the function of analog circuits are of different nature than those of digital circuits. But at the abstract level considered in the previous section, the properties required for the fault-free and the faulty functions in order to reach the TSC goal in analog circuits remain the same as defined in the previous section.

However, since the input and output code spaces have in general an infinite number of elements, the hypothesis of the previous section becomes unrealistic. For these code spaces, an infinite number of input signals must be applied within a finite lapse of time. In order to cope with this problem, it is necessary to consider finitely self-checking circuits [16]. Some of the properties in Table I are then limited to the ones in Table II.

The definitions of finitely totally self-checking circuits and checkers come from the standard ones by substituting the self-testing concept by the finitely self-testing one [16]. In this case, for a given input fault set F, a finite subspace of the input code space must exist which has enough elements to put in evidence each fault in F. The largest class of functional circuits (checkers) which achieves the finitely TSC goal is finitely SFS (finitely SCD) checkers.

This theory is taken into account in the next section to develop a design methodology for self-checking FD linear analog circuits. With the design example of Section VI, we will show that the TSC goal is practically achieved for the functional block (despite considering a finite input space), but the TSC goal for the checker requires the use of a self-exercising circuit.

V. DESIGN METHODOLOGY FOR CED IN LINEAR FD CIRCUITS

The CED strategy is based on the observation of a balance property in the linear circuit under test. As shown by means of the definitions of Table III, the signals of the differential nodes must be within a differential code space, and the inputs of all differential amplifiers must also be at a virtual analog ground. The code space is defined by the maximum value of CM ϵ (**detection threshold**) accepted for a signal.

TABLE II
DEFINITIONS FOR ANALOG SELF-CHECKING THEORY

Finitely totally self-checking. *G is finitely TSC for a fault set F if it is fault-secure and finitely self-testing for the fault set F.*

Finitely self-testing. *G is finitely self-testing for a fault set F if there is a subspace Af of the input code space A such that: Af has a finite number of elements, and for each fault in F there is at least one input value belonging to Af that produces a value on the nodes being monitored which does not belong to the checker input code space.*

Finitely strongly fault secure. *A circuit G is finitely SFS for a fault set F if there is a finite subspace Af of the input code space A such that: for every fault in F, either a) G is fault secure with respect to A and self-testing with respect to Af, or b) G is fault secure with respect to A and if a new fault in F occurs, for the obtained multiple fault, either the case a) or the case b) is true.*

Finitely strongly code-disjoint. *A circuit G is finitely SCD for a fault set F if there is a finite subspace Af of the input code space A such that: before the occurrence of any fault G is code disjoint, and for every fault in F, either a) G is finitely self-testing with respect to Af or (b) G always maps input values which do not belong to the input code space into output values which do not belong to the output code space and if a new fault in F occurs, for the obtained multiple fault, either case a) or case b) is true.*

In linear balanced circuits, a single fault corrupts in general the circuit balance. The unbalance of the differential paths is compensated with an increase of CM at the inputs of a DOA. Also, some hard faults in a DOA can result in large differential signals at its inputs. In both cases, the corruption of circuit balance is observable at the inputs of the DOA's. Since the likelihood of a multiple fault which results itself in the compensation of the differential paths is very low, a single fault hypothesis can be made for the analysis of the self-checking properties. This analysis takes into account the detection threshold ϵ and the maximum voltage deviation σ (**erroneous behavior threshold**) admitted in the outputs of a fault-free circuit. To evaluate the self-checking properties, the fault set includes hard (catastrophic) faults in the DOA's and hard and soft (parametric) faults in the external components. In fact, hard faults in external components do not change the circuit dc operating point, and, thus, just detection for the limit parametric deviations needs to be ensured. However, hard faults in external components are also included since in the case that the circuit does not achieve the TSC goal, the maximum output deviations incurred are evaluated.

Bridges between differential lines were not included in this study since layout rules were introduced in the circuit implementation to prevent them. It is, however, possible to prove that for realistic values of bridge resistance nearly all of these faults in the analog parts of the circuit are detected by means of balance testing [17]. Just two faults in the differential lines of the output stage of a DOA may not be detectable and thus require an adequate layout rule. Shorts between double-rail digital signals are detectable with suitable double-rail digital checkers.

The balance testing circuitry is based on the CM amplifier of Fig. 3 [18]. If the differential signal S is balanced, ac signals V_c and V_c' approximately remain at their dc voltages. A CM signal at the inputs of the amplifier different from $V_{\rm ref}$ (which corresponds to the nominal analog ground) changes the current (and voltage) in node V_c, and the opposite effect results in node V_c' by virtue of the current sources. The ac gain of signals V_c and V_c' is proportional to the CM signal. The ac analysis of the circuit gives $V_c \approx -(gm/g_l)\,V_{\rm com}$ and $V_c' \approx g_m/g_l \approx V_{\rm com}$, where $V_{\rm com} = (S^+ + S^-)/2$ represents the CM signal. The threshold of the output inverters is then designed such that they signal a double-rail error indication when the CM signal exceeds a given threshold. The outputs 01 or 10 indicate correct performance, while 00 and 11 indicate circuit malfunction.

TABLE III
BALANCE PROPERTY FOR LINEAR FD CIRCUITS

Differential code. *Let any two differential nodes + and - carry the components S^+ and S^- (with respect to the analog ground) of a signal S. Then the relation $S^+ \approx -S^-$ will be satisfied for S. Also let ϵ be the maximum commom mode signal admitted for S. Then the differential code space will be made up of all S for which $\frac{|S^+ + S^-|}{2} < \epsilon$ is met, and the noncode space by those signals for which $\frac{|S^+ + S^-|}{2} > \epsilon$ applies.*

Balance property. *Let G be a linear differential circuit with input signals (U^+, U^-) and output signals (Y^+, Y^-) made up of switches and passive components and of a fully differential operational amplifier whose inputs (X^+, X^-) are virtually shorted. Then the circuit G is balanced if (a) (U^+, U^-) and (Y^+, Y^-) are in the differential code space and (b) (X^+, X^-) are virtually grounded within the differential code space.*

In order to ensure the TSC goal for the checker, an off-line testing phase is required for the test of the checker. This is because the finitely strongly code disjoint property of the checker cannot be ensured if faults accumulate during the circuit lifetime. For example, consider a circuit under test which is fault-free and a first fault that behaves like a stuck-at at any of the two outputs of the checker. This fault will not be detected. Then, a second stuck-at can occur on the other output and the checker will lose the capability of signaling functional error occurrences. It can be shown that code partitioning (as done in the case of digital checkers) cannot be used in the analog case for avoiding this problem [19]. Consequently, a self-exercising analog checker is required to guarantee the TSC goal.

In summary, the self-checking design methodology consists of five steps.

1) Obtain a FD implementation of the transfer function and define fault set.
2) Define the detection threshold ϵ of the checker according to the level of CM accepted and the fault coverage required.
3) Given the detection threshold ϵ and the erroneous behavior threshold σ, evaluate the self-checking properties of the functional circuit.

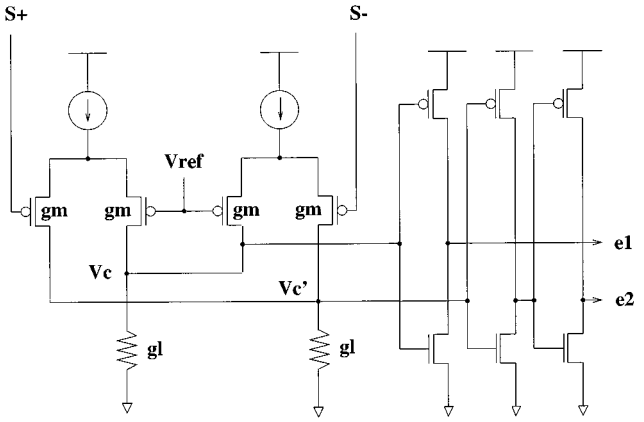


Fig. 3. Basic balance testing circuit.

4) Consider circuit safety and go back to step 2) if required.
5) Design a self-exercising checker for the differential code space obtained and evaluate its self-checking properties.
6) Evaluate the performance degradation of the circuit under test resulting from the checker connection.

VI. Design Example

The self-checking design methodology is exemplified in this section by means of a simple biquadratic filter which implements the transfer function $H(s) = -\omega_o^2/(s^2 + w_o s + w_o^2)$ where $w_o = 1/RC$ and R and C are the resistor and capacitor associated with each integrator. A single-ended continuous-time version of a circuit which implements this function is shown in Fig. 4.

A. FD Implementation and Fault Set

An FD implementation of the filter of Fig. 4 is shown in Fig. 5. An SC implementation has been used due to the high value of the time constant RC. Since the SC technique allows the implementation of noninverting integrators, the FD circuit does not require an inverting stage. The same time constant is achieved by means of small capacitors (8 pF) and large switched resistors (25 MΩ using a switching frequency of 40 kHz). The total power supply is 5 V and analog ground is 2.5 V.

The fault model includes catastrophic faults (opens and shorts) in all components and parametric faults in components external to the amplifiers. For transistors within the amplifiers, opens in all terminals and pairwise terminal shorts are considered. During fault simulation, a short was modeled as a 1-Ω resistor in parallel with the component. For an open, we used a 10-MΩ resistor in series. In the case of an open in a transistor gate, the transistor was removed when simulation allowed it. Otherwise, its gate and source were shorted and the gate disconnected from other nodes. For external components, the circuit dc operating point does not change as a result of a fault. These faults are then analyzed by means of a simple transfer function analysis. Catastrophic and parametric faults in these components are simply injected in the circuit transfer function which considers amplifiers with an open-loop gain of 10 000.

The analysis is further simplified by substituting the switched resistors by equivalent continuous-time resistors and considering hard and soft faults in these equivalent resistors. This model leads to a good coverage of faults occurring in the actual switched resistor as shown in Fig. 6. Fault simulation for an SC lossy integrator, which corresponds to the general building block used in the biquadratic filter, has been used to validate this result using an amplifier with an open-loop gain of approximately 10 000. The effect of switch stuck-on/stuck-open faults, capacitor open/short faults, and capacitance deviations can be modeled as a deviation of the nominal value of the equivalent continuous-time resistor. This deviation is indicated as the ratio R_{eq}/R_{eq_n}, where R_{eq} corresponds to the faulty value and R_{eq_n} to the nominal value of the equivalent resistor. Note that hard faults in the switches do sometimes result in a soft fault in the equivalent resistor.

B. Define Detection Threshold ϵ

The detection threshold ϵ is obtained according to the level of CM accepted and the fault coverage required for the selected fault set. The value of ϵ must guarantee the self-testing property.

By fault simulation, we observed that more than 95% of faults in a DOA affect the behavior of the amplifier and corrupt the balance of the circuit, regardless of the circuit input. Only about 4% of the remaining faults produce a CM signal at the DOA inputs that is proportional to the input signal amplitude and to the circuit gain. Detection of these faults depends on the checker threshold. For an input of 1-V differential and 1 kHz, these faults are detected with a threshold of approximately 45 mV. This must be added to CM induced by nonidealities such as DOA offset and clock feedthrough which can account for another 60 mV in the worst case. Thus, a threshold of 100 mV appeared convenient to guarantee the self-testing property of the amplifier. The remaining 1% of faults do not change at all the behavior of a DOA.

For external faults, note first that the same faults in components which are situated symmetrically in a differential implementation result in effects on the CM signal which differ in phase, but not in magnitude [20]. Therefore, only faults in the components on the top part of the filter need to be considered. In Fig. 5, faults in the components of the first (second) stage only affect the balance of node J (X). Fig. 7 shows the effects on the sensing node J of shorts and opens in the components of the first stage, considering the simplified AC analysis. These effects are made relative to the value of the input signal I (for an input of 1-V differential, the figure describes the actual value of CM).

Parametric faults have similar CM effects, but of a lesser magnitude than for the case of hard faults. Given the checker threshold, the minimum detected deviations (both positive and negative with respect to the nominal value) of each component can be determined for a given input amplitude at each circuit frequency, considering the simplified AC analysis. For each component, these values define the **fault detection boundary** [20] of the component. For example, Fig. 8 illustrates the fault detection boundaries for component C_6 and an input of 1-V differential. The boundary extends along both sides of the nominal value ($C_6/C_{6n} = 1$), which correspond to positive and negative component deviations. The region between boundaries corresponds to a region of nondetection. The region beyond a fault detection

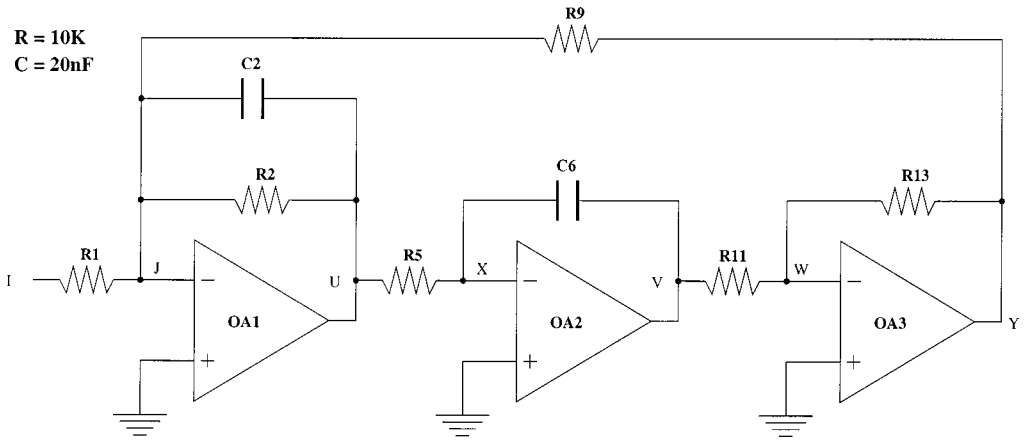


Fig. 4. Biquadratic filter.

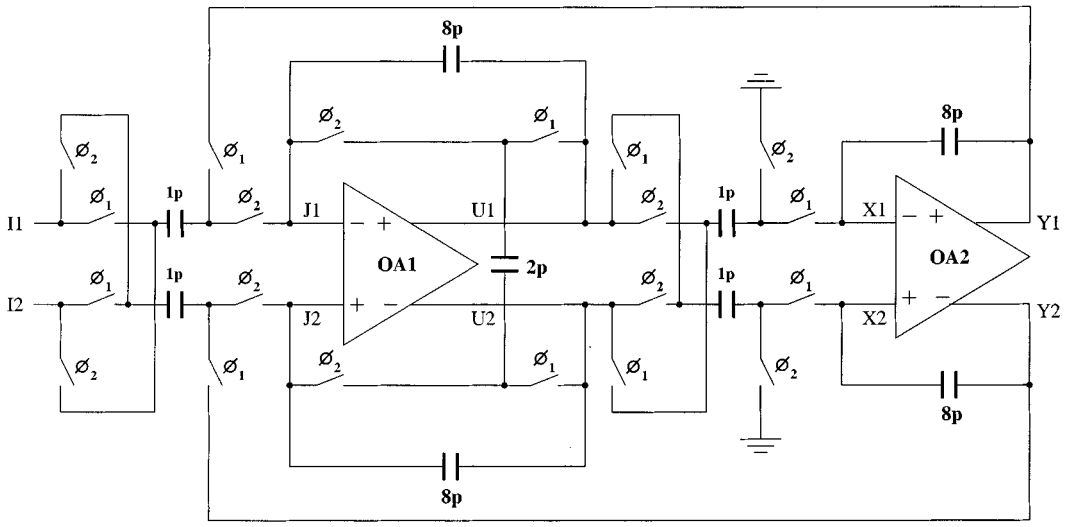
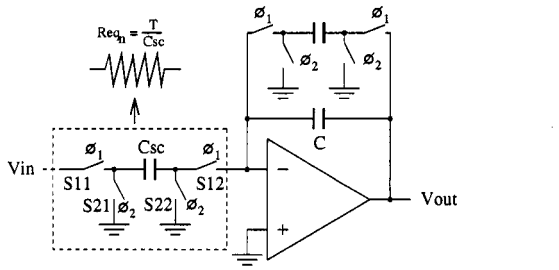


Fig. 5. FD switched-capacitor biquadratic filter.



Fault location	Switch								Capacitor			
	Stuck-open				Stuck-on				open	C↓	C↑	short
	S_{11}	S_{12}	S_{21}	S_{22}	S_{11}	S_{12}	S_{21}	S_{22}				
Req/Req_n	∞	∞	6.4	6.4	4	6.6	∞	2.7	∞	↑	↓	0

Fig. 6. Fault effects in a lossy integrator switched resistor.

boundary corresponds to deviations which will be detected. For the second stage, $\epsilon = 100$ mV and a 1-V differential input, a fault for a passive component with nominal value P_n is detected for $P/P_n > 1.34$ and $P/P_n < 0.76$. The soft-fault coverage is somewhat smaller for the first stage.

The soft-fault coverage figures are indeed conservative since the 60 mV of CM which can be present because of circuit nonidealities have not been considered here (this would just leave an effective CM of 40 mV for parametric deviations). Thus, the threshold of 100 mV chosen can ensure the self-testing property of the circuit with an input of 1-V differential. This input signal amplitude was chosen mainly to ensure a good fault coverage (which would be smaller for lower signal amplitudes) and to avoid the saturation of the fault-free circuit. It must be next evaluated if the circuit remains fault secure for the whole input code space and this detection threshold.

C. Evaluation of Self-Checking Properties

The evaluation of the fault secure property requires an erroneous behavior threshold σ. We consider $\sigma = 100$ mV for a differential input of 1 V (an accepted deviation of 10%). The operation regions of the frequency spectrum where the functional circuit can be considered TSC for the identified fault set are next analyzed.

With respect to hard faults internal to the amplifiers, it has been mentioned in the previous section that if we consider only

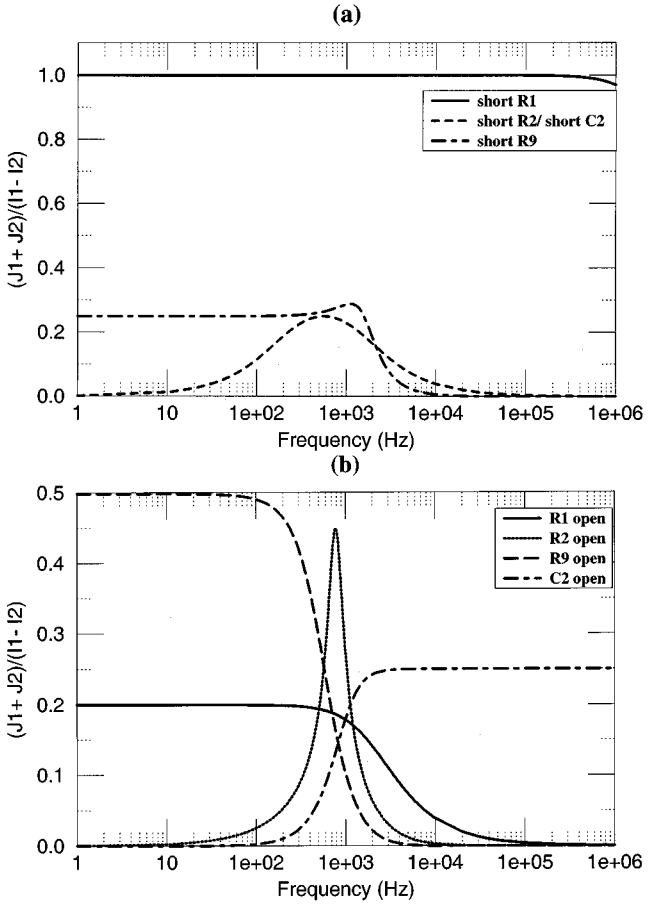


Fig. 7. Effect of hard faults on sensing node: (a) effect of shorts and (b) effect of opens.

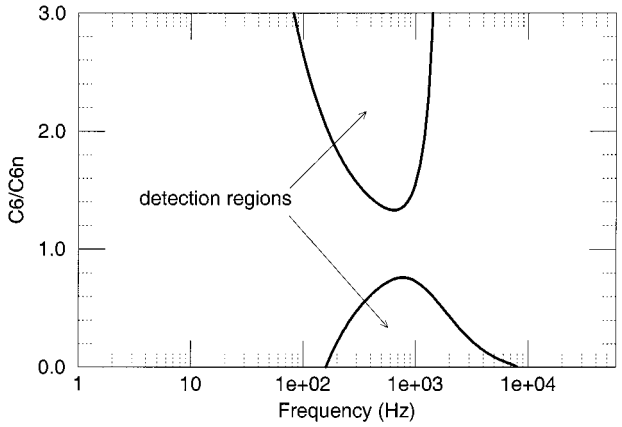


Fig. 8. Fault detection boundary for component C_6.

large enough input signals (e.g., 1-V differential), in total 99% of faults will be detected by balance testing. Furthermore, for these faults the functional circuit in which the DOA is inserted achieves the TSC goal for the whole frequency spectrum. For the 1% of faults which do not affect the amplifier behavior, the faulty circuit remains in a fault secure region, but nothing else can be concluded with respect to the TSC goal without performing a multiple fault analysis (which is not considered here).

For hard faults in external components, the results of the simplified AC analysis are illustrated in Fig. 9 for the second circuit stage. For example, a short in R_5 alters the gain and phase of the circuit as shown in Fig. 9(a) and (b), respectively. The fault is detected in the checker in the frequency band 160 Hz to 7.9 kHz [see Fig. 9(c)] for an input of 1 V. For frequencies outside this band the fault is undetected, but although the functionality may be slightly altered, the differences or the gains are so small that the circuit output is practically the same for the fault-free and the faulty circuit. The fault secure property is ensured and the circuit is TSC for a short in R_5.

For some faults, however, there exist regions where the circuit is nonself-checking. This is the case, for example, of an open in R_5. For $\sigma = 100$ mV, Fig. 9(d) shows that for the frequency at which the CM falls below 100 mV, the output deviation is still above 100 mV for an input of 1 V ($Y_1 - Y_{1f}$ is the difference between the fault-free and faulty output of the circuit). The circuit is nonself-checking for this fault in the band 1850–1962 Hz. The nonself-checking regions for the external hard faults are given in Table IV. The maximum deviations in the nonself-checking regions and their proportion with respect to the nominal output value are also shown in this table. The worst case occurs for an open in component C_2, with an undetected output deviation of 355 mV in a narrow band of approximately 310 Hz. This corresponds to a deviation of 31% with respect to the nominal value. An open in R_5 can give up to a 57% of deviation, but this occurs when the output signals have a low value close to the accepted deviation of 100 mV.

For parametric faults in external components, the circuit fault secure operation region is determined by considering the **erroneous behavior boundary** of each component. The minimum deviations (both positive and negative with respect to the nominal value) of each component at each circuit frequency which produce an output beyond the accepted erroneous threshold σ form the erroneous behavior boundaries of the component. Fig. 10(a) indicates these boundaries for component R_1, $\sigma = |Y_1 - Y_{1f}| = 100$ mV, and a differential input of 1 V. The boundaries extend along both sides of the nominal value ($R_1/R_{1n} = 1$). The region beyond the erroneous behavior boundary of a component corresponds to the circuit output deviations that are not acceptable. The region in between the two erroneous behavior boundaries is called the fault-secure operation region of the component.

For parametric faults, the self-testing and the fault secure properties are mapped onto the fault detection and the erroneous behavior boundaries. Thus, the regions for which the faulty circuit is not fault secure and the fault is not detected can be determined from the combination of both boundaries, as shown in Fig. 10 for components R_1 and C_2. In these regions, called nonself-checking regions, the TSC property is lost. For example, in Fig. 10(a) and for low frequencies, a fault in R_1 gives an erroneous output if $R_1/R_{1n} > 1.24$ or $R_1/R_{1n} < 0.83$, but an erroneous output can only be detected for $R_1/R_{1n} > 2.2$ and $R_1/R_{1n} < 0.6$. For the circuit example, all components have nonself-checking regions similar to those shown in Fig. 10

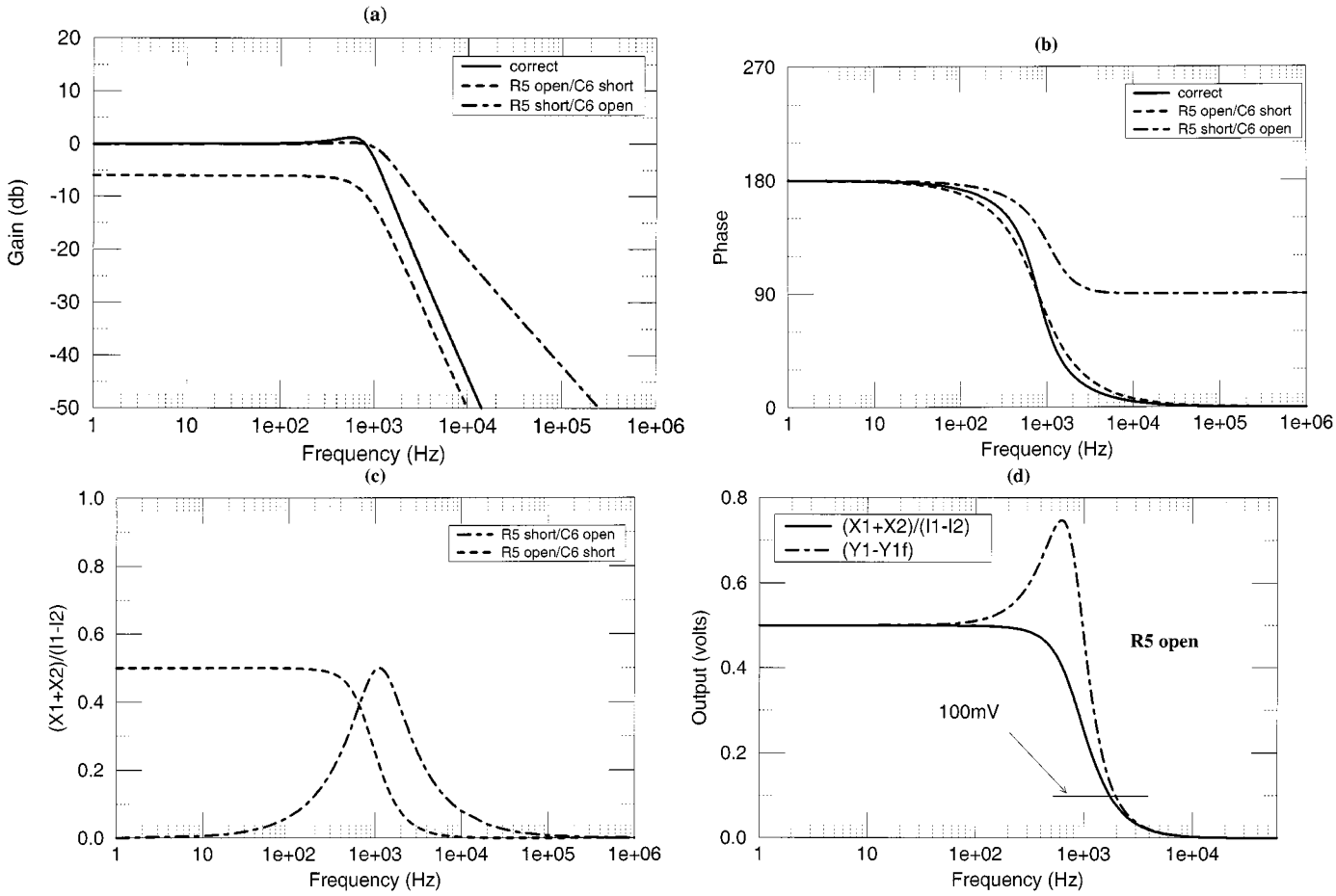


Fig. 9. Effect of hard faults in the second stage: (a) on circuit gain, (b) on circuit phase, (c) on balance node X, and (d) on circuit output.

TABLE IV
NONSELF-CHECKING REGIONS FOR CIRCUIT HARD FAULTS

Fault	Non-self-checking regions	max $\lvert Y1 - Y1f\rvert$	%
R1s, R1o, R5s, R9s, C6o	$\emptyset$	-	-
R2s, C2s	27 Hz – 85 Hz	300 mV	30
R2o	129 Hz – 340 Hz	335 mV	31
C2o	342 Hz – 650 Hz	355 mV	31
R5o, C6s	1850 Hz – 1962 Hz	115 mV	57
R9o	1000 Hz – 1260 Hz	241 mV	33

which differ in terms of component deviation and frequency ranges.

D. Improving Circuit Safety

From the previous analysis, it is concluded that the TSC goal is not ensured for the whole frequency spectrum with the checker threshold ϵ and erroneous threshold σ chosen. There are filter operation regions where the fault secure property is not ensured and the erroneous circuit behavior is not accompanied by an error indication provided by the checker.

1) The TSC goal cannot be ensured for the whole input code space with respect to the hard faults considered. According to Table IV, the maximum nondetected deviation $|Y_1 - Y_{1f}|$ is 355 mV (31% of deviation).
2) Considering the set of soft faults, in general, the TSC goal cannot be ensured for small component deviations.

However, due to the small differences between the outputs of the fault-free and faulty filters in the nonself-checking regions, the filter operation may be considered safe for a number of applications. In this case, a periodical off-line testing phase can be used for detecting those nondangerous faults and to prevent the accumulation of faults and loss of circuit safety. On the other hand, if higher degrees of safety are required, then the following approaches can be considered.

1) Use a lower checker threshold as the means to enlarge the regions of fault detectability. The minimum checker threshold is limited by the CM induced by circuit nonidealities.
2) Avoid the use of signals with low amplitudes. Although larger signals (maintaining the same value for σ) make the fault secure regions narrower, the regions of fault detectability are in general greatly improved leading to

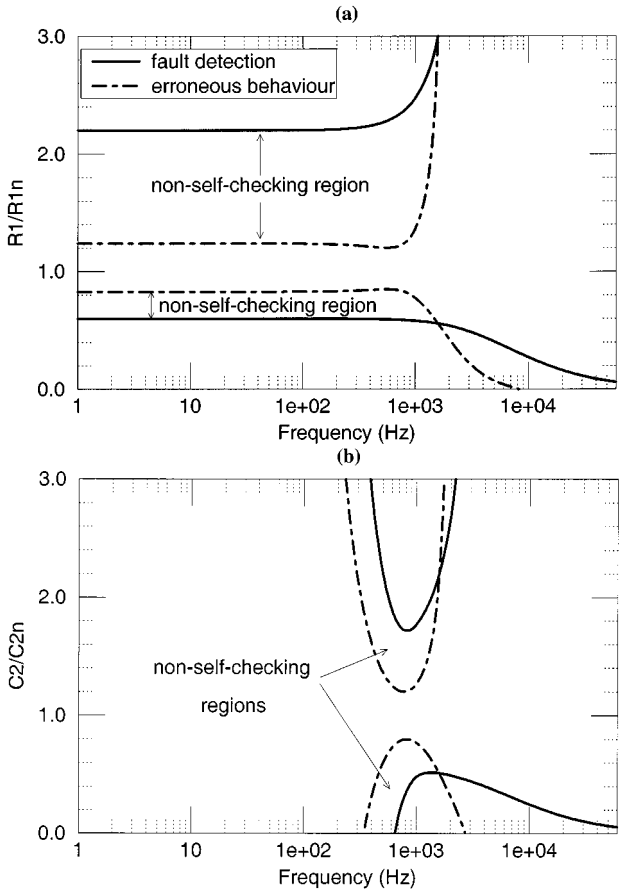


Fig. 10. Nonself-checking regions: (a) for component R_1 and (b) for component C_2, with $\epsilon = 100$ mV and $\sigma = 100$.

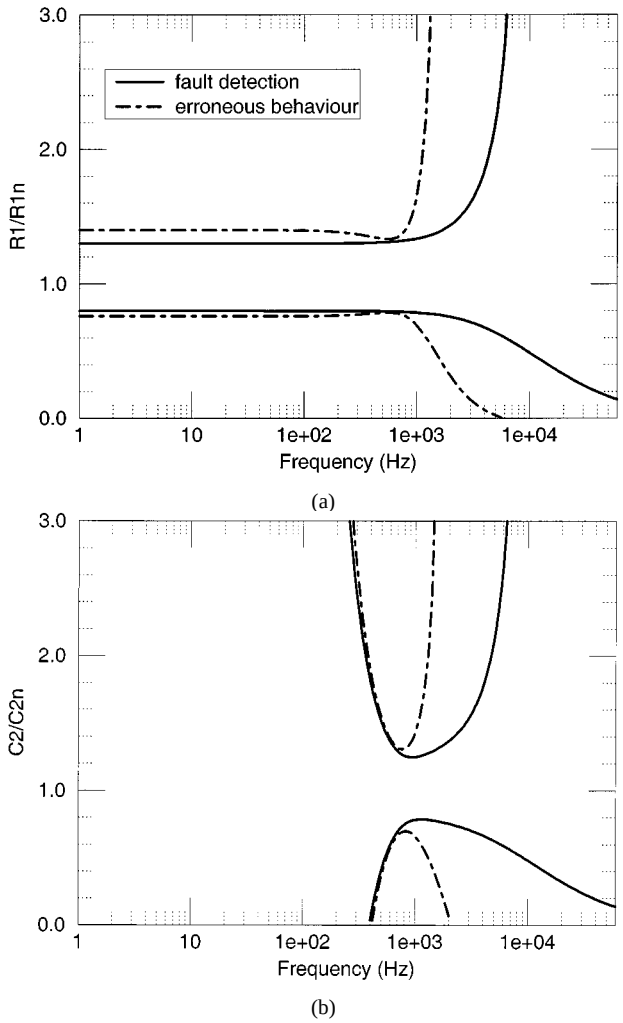


Fig. 11. TSC case: (a) component R_1 and (b) component C_2, with $\epsilon = 40$ mV and $\sigma = 150$ mV.

smaller nonself-checking regions. However, an increase in signal amplitudes may need to be accompanied by an increase in power supply.

3) Accept a higher erroneous behavior threshold σ as the means to enlarge the regions of fault secureness and, as a consequence, to enlarge the self-checking regions.

As an example, the circuit can be made TSC by considering a checker threshold $\epsilon = 40$ mV and an accepted deviation $\sigma = 150$ mV. This is shown in Fig. 11 for components R_1 and C_2. The regions of erroneous behavior fall completely within the regions of fault detection.

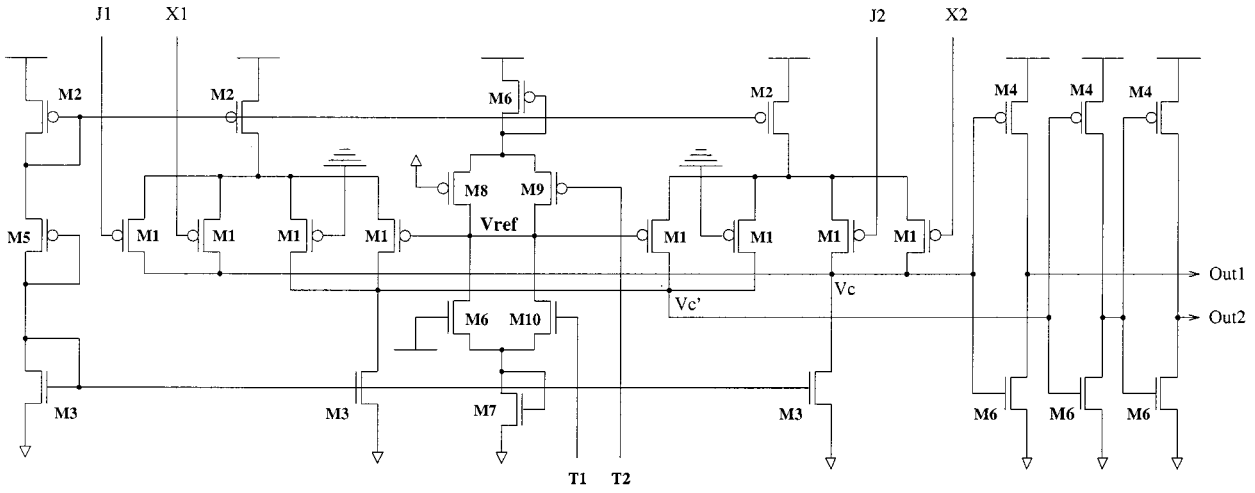
In general, given the deviation σ accepted, it is possible to conclude that the circuit can be made TSC by taking a value of checker threshold ϵ sufficiently low. However, in very demanding applications, this may require an accurate circuit layout to reduce the CM given by circuit nonidealities.

E. Analog Checker Design

Since both nodes J and X in Fig. 5 must be sensed, the basic scheme of Fig. 3 is extended in Fig. 12(a) by simply adding a second differential branch to the CM amplifier (the total power supply and analog ground of the checker are the same as for the SC circuit). Transistors M_6–M_{10}, which form a voltage divider controlled by digital signals T_1–T_2, generate the reference voltage $V_{\rm ref}$ of the amplifier. This voltage is analog ground for $T_1T_2 = 01$. Transistors M_1–M_3, which form the CM amplifier, are dimensioned such that an ac gain of ten is achieved. For correct performance, signals J and X are virtually grounded and V_c and V_c' remain at their dc values of approximately 1.5 V. A CM signal of 100 mV triggers one of the two minimal-size output inverters (which switch around analog ground at 2.5 V). With this, a tolerance window (–100, 100) mV is embedded in the circuit.

Since the differential signals observed have a minimum amplitude (just the tolerated CM), the distortion in the CM amplifier is minimal. This distortion increases with the number of branches observed, but it is negligible due to the very low amplitudes under correct performance. On the other hand, some hard faults in a DOA of the circuit application result in large differential signals at its inputs. These faults are also signaled by the checker due to the distortion introduced by the large differential inputs [an error is signaled for differential signals of a minimum of 500 mV in the checker of Fig. 12(a)].

As discussed in Section V, a periodic test of the checker is required to ensure the TSC goal. Similarly as in [21], this is done by means of a testing phase which periodically applies unbalanced (noncode) signals to the checker. In this test, the inputs of the functional circuit are kept at analog ground, thus keeping the checker inputs also at analog ground if the circuit is fault-free.

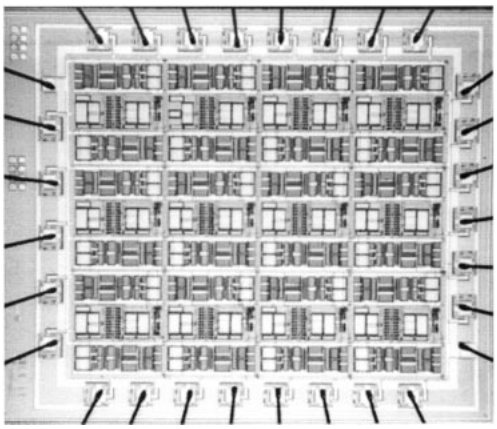


(a)

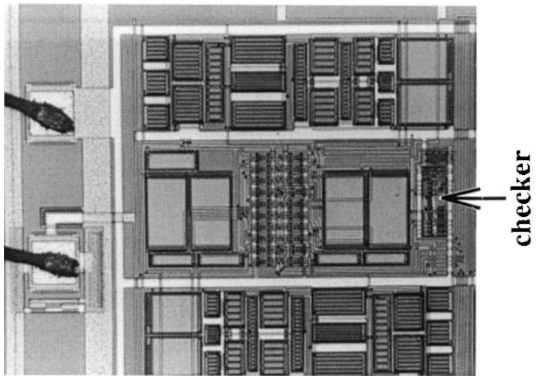
	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
W μm	2	26	2	5.9	2	2	2	5.4	11	4
L μm	3	2	2	2	6	2	5	2	2	2

(b)

Fig. 12. Analog checker: (a) schematics and (b) checker transistor sizing.



(a)



(b)

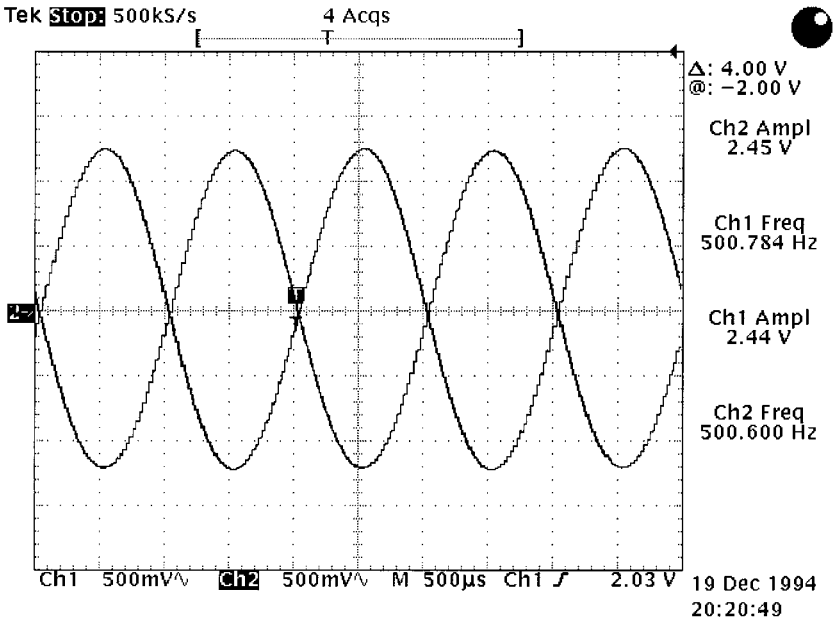
Fig. 13. Fabricated chip: (a) photo of the chip and (b) zoom on one of the filters.

Both edges of the tolerance window (100 and -100 mV) are generated one after the other in node $V_{\rm ref}$ by controlling T_1T_2 to 00 and 11, respectively. By fault simulation, we have observed that only two faults are not detected by this periodic off-line test. However, since these faults just make the tolerance window narrower, the checker is still finitely strongly code disjoint. Note that, although the checker may not be finitely self-testing, it will achieve the TSC goal.

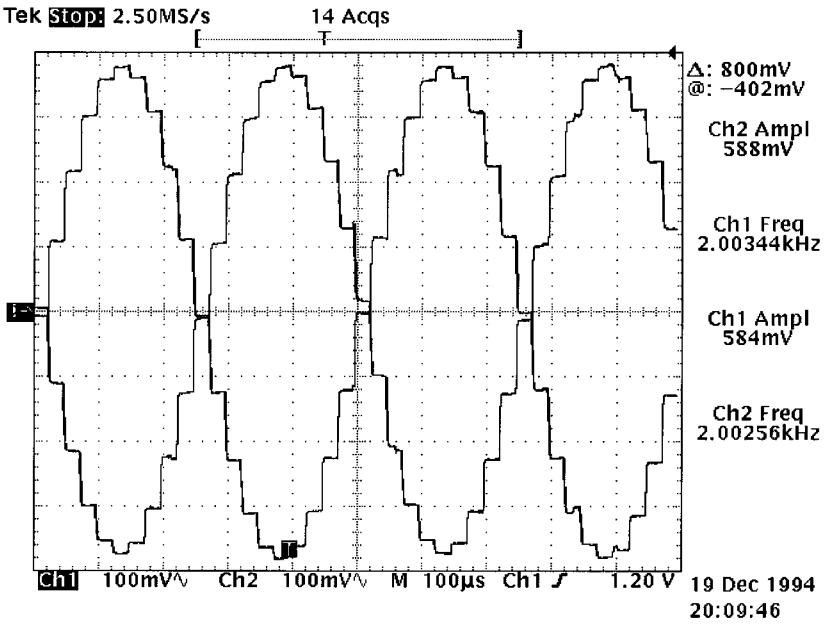
The silicon space required by the checker, as shown in Fig. 12(b), is very small. It takes less than 3% of the overall area and about 7.6% of the total power. The accuracy of the fabricated checker is discussed in the next section.

VII. Experimental Results

The AMS 1.2-μm double-metal double-poly process was chosen for the implementation of the analog circuit studied in this paper. A photo of the fabricated chip is shown in Fig. 13(a). A zoom on one of the filters in the chip is shown in Fig. 13(b). Fifteen chips were delivered, of which five were packaged. Four chips worked correctly and one was faulty. Each chip contains 12 copies of the filter: four copies are fault-free, and the other eight copies include one circuit fault. The injected faults are hard and soft faults in external components and hard faults in the DOA's. Two of the four fault-free filters have no checker, and the other two have a checker connected to them. This allows us to compare filter behavior and measure the performance degradation due to the checker. The programmable voltage divider has only been implemented in an unconnected checker of a fault-free filter. The analog inputs of this checker are directly connected to analog ground. For the other checkers, the reference voltage $V_{\rm ref}$ is directly connected to analog ground, and the analog inputs of the checker are connected to the inputs of the DOA's. Each filter takes about 0.59 mm^2 with about 3% for the analog checker. The checker outputs are EXNORed in order to produce a single error signal.



(a)

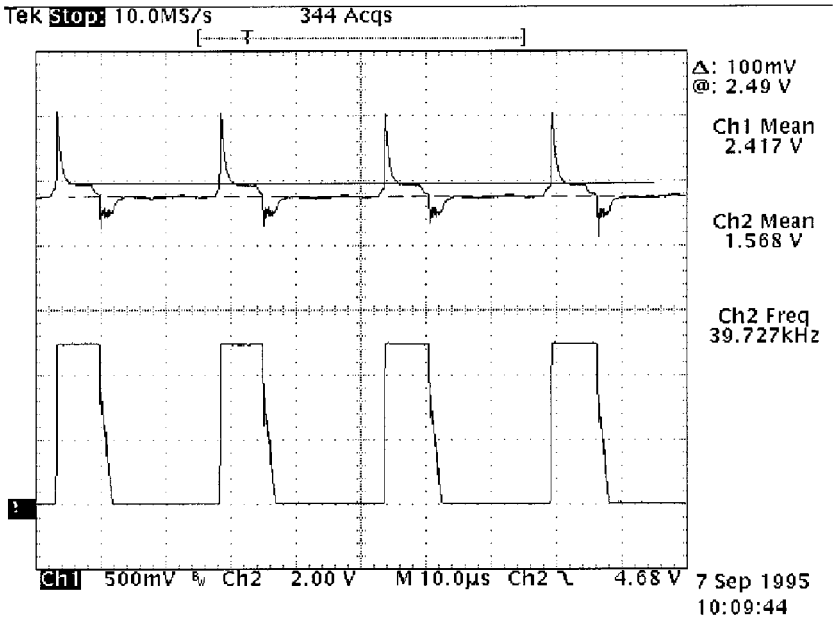


(b)

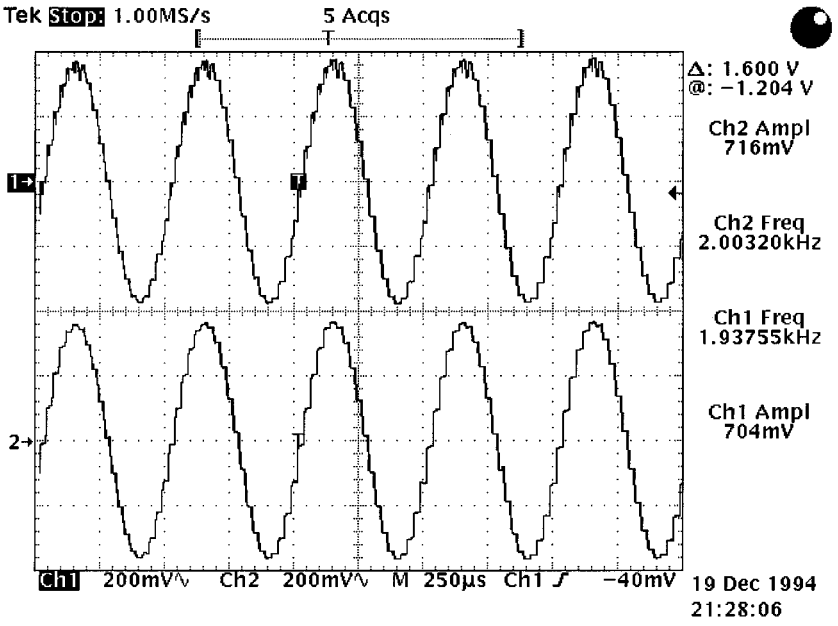
Fig. 14. Filter output for 1-V differential input: (a) 500 Hz and (b) 2 kHz.

The chips were tested on a digital GenRad 115 equipment, with the input analog signals being externally supplied. Fig. 14 shows the differential output signal of a fault-free filter for a 1-V differential input at two circuit frequencies. The ac performance of the filter is correct, but an additional dc gain of less than 6 dB is obtained in the fabricated filters. This dc gain is due to simplifications performed in the derivation of the SC circuit in Fig. 5.

The test of the unconnected checker is performed by connecting its signal T_2 to one of the SC clocks while T_1 is set to dc ground. This results in a periodic voltage at node V_{ref} of an amplitude of approximately 100 mV with respect to analog ground (2.5 V) as shown in the top test diagram of Fig. 15(a). The bottom time diagram shows the error output of the checker. The duration of the error pulse is correct according to the moment at which V_{ref} exceeds 100 mV. However, the output from the programmable voltage divider (V_{ref}) is in fact different from chip to chip, the smallest value being 84 mV and the largest 164 mV. Thus, a more precise voltage reference generator is required for actual applications (using resistive dividers at the expense of an increase in power consumption and checker space). The degradation in filter performance due to the presence of the checker is shown in Fig. 15(b). The output of a filter without the checker is shown in the top time diagram, and the bottom time diagram shows the output of a filter connected to a



(a)



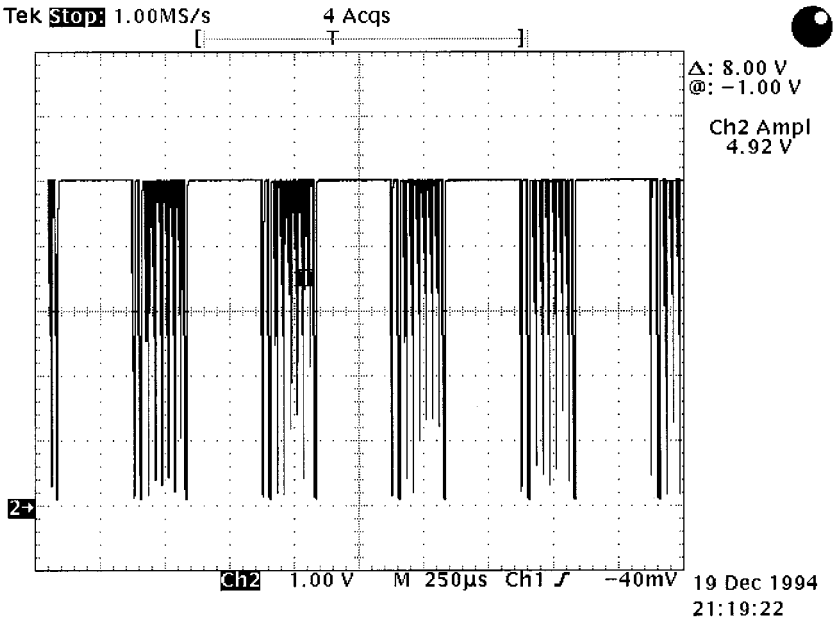
(b)

Fig. 15. Checker results: (a) self-test of the checker and (b) performance degradation.

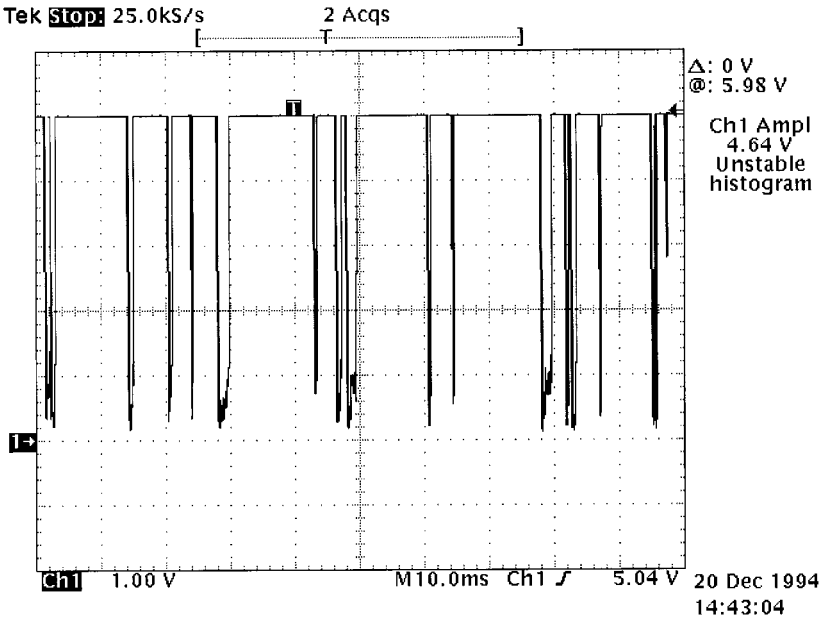
checker. Since the transistors at the DOA inputs are 333 times larger than those at the checker inputs, a negligible performance degradation is achieved.

It must be observed that the dc part of the signal is removed in all cases in Fig. 14. In fact, the dc output of the DOA's shifted down 500 mV with respect to the expected 2.5 V. This dc shift occurred in all filters in a chip, and it varies very little for the different chips (maximum of 10 mV). The analog ground of the checkers needs also to be shifted down to compensate for this dc shift. For each chip, the analog ground is adjusted so that a low checker output is obtained for the fault-free filters. After this compensation, the erroneous behavior is detected only in all faulty filters. Considering a 1-V differential input, Fig. 16(a) shows the checker output of a filter which includes a short in capacitor C_1. Fig. 16(b) shows the checker output for a soft fault in capacitor C_2 (the nominal value is 8 pF and the faulty implemented value is 2 pF) at 2 kHz. The error signal is at times low because of the pass by zero of the input signals and, therefore, of the CM signal.

In summary, fault detection is correct for all chips when the analog ground compensation was carried out. The fabricated chip made clearer that the test technique relies on careful DOA design in order to prevent large variations of input and output CM.



(a)



(b)

Fig. 16. Error signals: (a) short in capacitor C_1 and (b) deviation in capacitor C_2.

VIII. Concurrent Error Detection in Mixed-Signal Boards

The extension of concurrent error detection to the board level becomes a must when the goal is to design systems for high-safety applications. In [2], this kind of extension is proposed for digital boards by merging the self-checking circuit level technique with the boundary scan board level approach (see [3]). This proposal is based on the fact that the boundary scan path is not used during the normal operation of the board, thus being available for carrying the on-line error indicators of the circuit. The basic idea of the extension of this approach to mixed-signal circuits and boards is illustrated in Fig. 17.

In this approach, the error signals are captured and scanned out by means of a test data register called error indication register. The error indication register is part of an error memorization circuit which uses a network of double-rail digital checkers. These checkers are interconnected in such a way that error memorization is ensured even in the presence of a single fault in the checking circuitry. The double-rail checker in charge of compressing all circuit error indications is placed in between the multiplexor of boundary scan registers and the boundary scan serial data output (TDO). Although this approach does not fully comply with the design rules stated in [3], it provides a means of observing errors on line through the board boundary scan path.

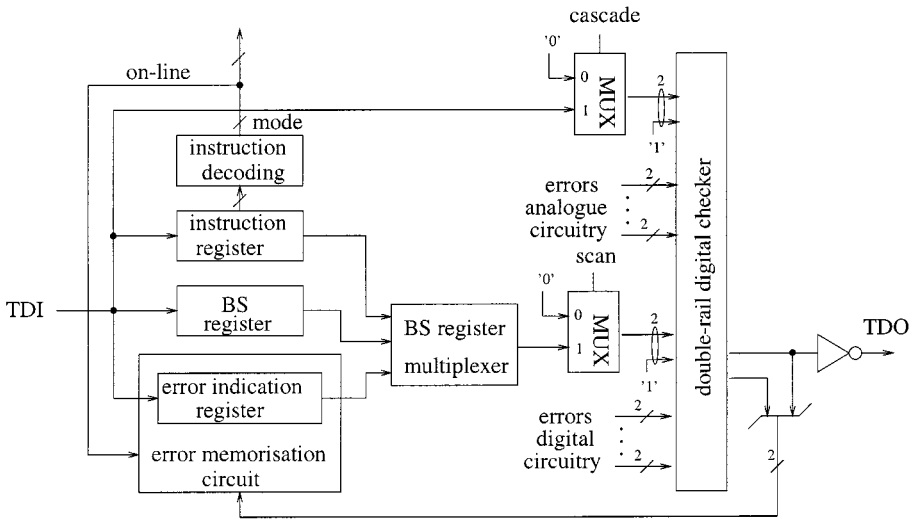


Fig. 17. Multiplexing the boundary scan and the error indication paths.

When the application is in progress, the "on-line" control signal is active ("1") and the signal "scan," generated by the IEEE 1149.1 test access port controller, is inactive ("0"). Then correctly double-rail encoded inputs ("01") are provided to the digital checker by the multiplexer. As a consequence, the digital checker outputs a global error indication as a function of the intermediate error indications coming from the circuit analog blocks and the digital circuitry and eventually coming from outside through the TDI pin (when "cascade" is active). Correct operation is thus signaled by a logic "1" at the input of the inverter and a "0" at the other checker output. A no-error indication, chosen to be "0," is then propagated to the board through TDO, as the means to improve the on-line coverage of open faults on the board boundary scan path [2], [3]. The error memorization capability is active during the circuit application in order to ease the task of diagnosing the board after an error has been detected.

When a test instruction or test data is off-line scanned, the "on-line" control signal is inactive ("0") and the signal "scan" is active ("1"). Then, by setting the intermediate error indications to a double-rail codeword, the bit being shifted through the BS multiplexer will reappear at TDO. Although the error memorization circuit is inactive during a scan operation, the contents of its error indication register is preserved and can be scanned for checking. Obviously, a complete self-checking boundary scannable architecture cannot be obtained without a special boundary scan register. This special register must accommodate codes and built-in checkers that will be used for testing on-line the board interconnects [2].

Finally, based on the circuitry of Fig. 17, three different approaches fitting different application speed requirements can then be used for compressing and propagating the circuit error indicators across the board. Two of them are presented in Fig. 18: the cascading of error indicators through the circuit global checkers and their parallel verification by means of a board global checker. The third approach, named mixed, simply merges the previous ones by verifying in parallel error indicators of cascading branches.

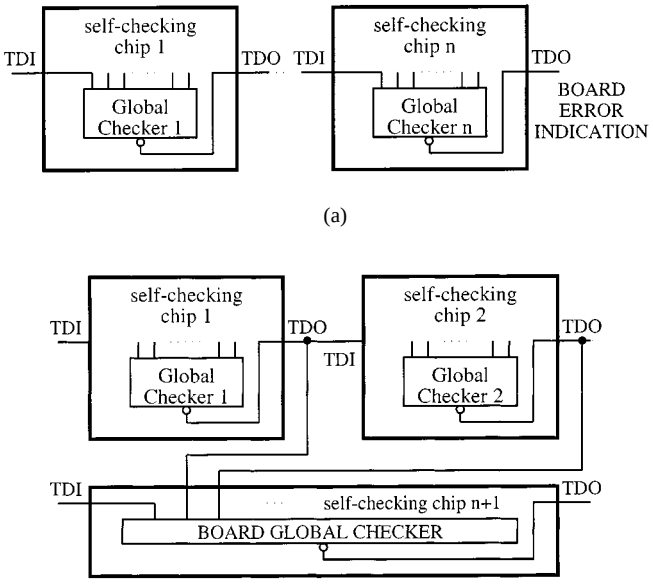


Fig. 18. Self-checking board: (a) cascading error indications and (b) parallel verification of error indications.

IX. Conclusions

A methodology aimed at the design of self-checking FD linear analog circuits is presented in this paper. A formal analysis of the faulty behavior of this type of circuits and the properties required to achieve the TSC goal is carried out. The test method is based on the observation of the CM at the inputs of the amplifiers in the circuit. Given the maximum acceptable deviation σ in the outputs of the self-checking circuit, the circuit can be made self-checking by taking a value of checker CM threshold ϵ sufficiently low. In high-performance applications where σ is very small (e.g., $\ll$10%), the acceptable CM at the amplifier inputs must also be very small (e.g., $\ll$100 mV), and this may require careful circuit layout to minimize circuit nonidealities (e.g.,

amplifier offsets, clock feedthrough, and charge injection) which introduce additional CM effects to those given by component deviations.

The test approach has been illustrated for the case of a switched-capacitor biquadratic filter where the checker takes less than 3% of the total area. This circuit can be made TSC with $\sigma = 15\%$ and $\epsilon = 40$ mV. However, since the circuit was not designed to limit additional CM due to circuit nonidealities, the checker threshold was set at $\epsilon = 100$ mV. For this case, it is shown that most faults are detected with $\sigma = 10\%$. For all the faults, the circuit is self-testing, but some of them are not detectable in narrow bands of the frequency band. The circuit can then be made totally self-checking by means of a periodic off-line test which is in any case required for the analog checker.

Besides the methodology itself, other novelties brought in by this work are:

- the use of a simple on-line analog checker capable of monitoring several circuit stages at the same time and of providing a digital error indication;
- the simultaneous study of both the hard and soft faults of components external to operational amplifiers and the hard faults of operational amplifier transistors;
- the definition of the operation regions (in terms of signal amplitudes, frequencies, the acceptable deviation of the transfer function, the checker tolerance window, and types of faults) in which the totally self-checking goal can be achieved by balance checking;
- the extension of the differential circuit testing approach to the on-line checking of mixed-signal boards.

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