Improved Ge Surface Passivation With Ultrathin SiO_X Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack

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***Abstract*—To realize high-mobility surface channel pMOSFETs on Ge, a 1.6-nm-thick SiO_X passivation layer between the bulk Ge substrate and HfSiO gate dielectric was introduced. This approach provides a simple alternative to epitaxial Si deposition followed by selective oxidation and leads to one of the highest peak hole mobilities reported for unstrained surface channel pMOSFETs on Ge: 332 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 0.05 MV/cm—a 2× enhancement over the universal Si/SiO_2 mobility. The devices show well-behaved output and transfer characteristics, an equivalent oxide thickness of 1.85 nm and an I_{ON}/I_{OFF} ratio of 3×10^3 without detectable fast transient charging. The high hole mobility of these devices is attributed to adequate passivation of the Ge surface.**

***Index Terms*—Germanium, high mobility, high-κ, metal gate, pMOSFET, surface passivation.**

I. Introduction

GERMANIUM channel MOS devices have been aggressively pursued for a 4.2× (hole) and 2.8× (electron) bulk mobility enhancement over Si [1], [2] for potential introduction beyond the 32-nm technology node. A long-channel low field mobility enhancement has also been correlated with improved device performance [3]. The availability of high-κ dielectrics for Si technology, notably HfSiO [4], provides an opportunity to revisit the poor surface passivation of Ge by its native oxides to achieve high-performance surface channel MOSFETs. Germanium devices fabricated using various high-κ [5] and interface-passivation techniques [6]–[8] perform better than their corresponding Si control devices but seldom provide significant enhancement over the universal Si/SiO_2 hole mobility. High-mobility Ge MOSFETs often use a buried channel architecture [9], [10], which exacerbates short-channel effects and, thus to a certain extent, negates the aim of introducing Ge channels for nanoscale devices. This report focuses on long-channel Ge pMOSFETs using an alternative deposited SiO_X interfacial layer that yields a mobility of 332 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 0.05 MV/cm, a 2× enhancement over the universal Si/SiO_2 hole mobility in a surface channel device.

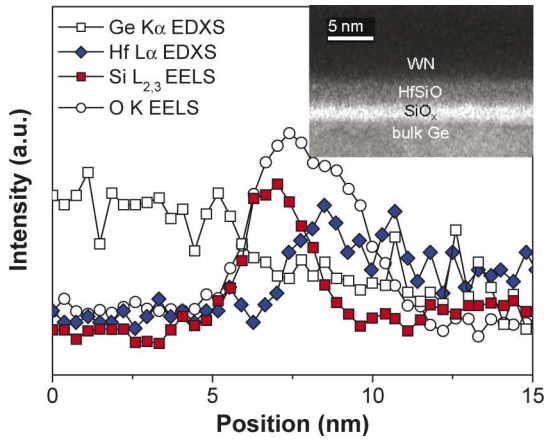

Fig. 1. EELS and EDXS elemental profiles across the Ge/SiOX/HfSiO/WN gate stack. Inset: Corresponding HRXTEM image. The SiO_X and HfSiO thicknesses are 1.6 and 2.7 nm, respectively.

II. Experimental

pMOSFETs were fabricated using a conventional four-mask process flow on Sb-doped ($\sim 5 \times 10^{14}$ cm^{-3}) bulk Ge wafers from Umicore. Plasma-enhanced chemical vapor deposition (PECVD) was used to deposit 400 nm of field-isolation oxide. Active areas were patterned and etched using optical lithography and a CF_4-based dry etch to remove 350 nm of the PECVD oxide. The remaining PECVD oxide was removed during a 1% HF rinse immediately prior to the gate dielectric deposition to minimize the exposure of bulk Ge to the atmosphere. An ultrathin passivation layer of SiO_X was then deposited directly on the Ge surface. SiO_X deposition was immediately followed by HfSiO deposition using an atomic-layer-deposition process described before [11], [12]. WN was used as one of the gate electrode materials in a series of experiments. A 220-nm-thick TaN electrode was then deposited on each of these metal gates

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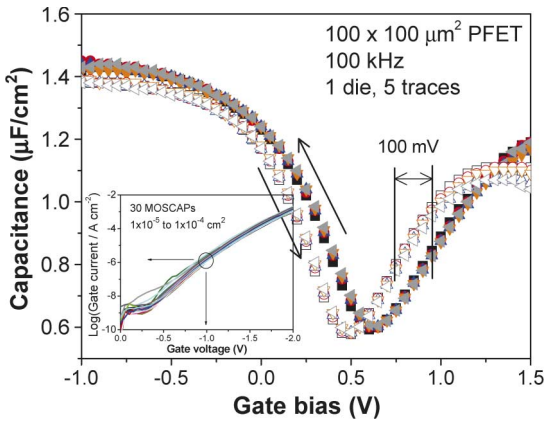

Fig. 2. Repeated high-frequency C–V traces on a MOSFET with grounded source and drain show hysteresis of ∼100 mV close to the flatband voltage. Inset shows gate leakage of $\sim 1 \times 10^{-6}$ A/cm^2 at 1-V gate bias in accumulation.

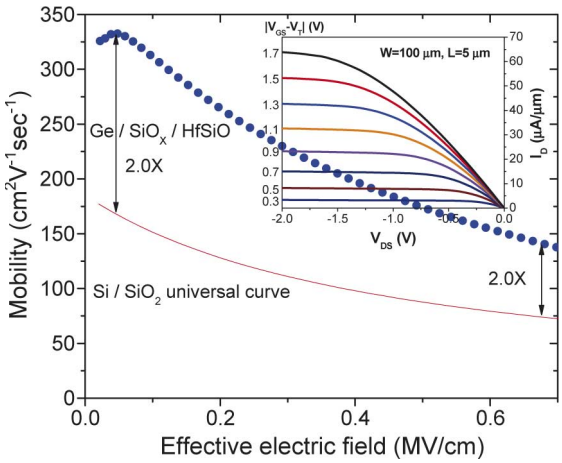

Fig. 3. Hole mobility for Ge pMOSFETs is compared with universal Si hole mobility as a function of the effective electric field for the Ge/SiO_X/HfSiO/WN stack. Output characteristics are well behaved with negligible offstate gate or junction leakage as shown in the inset.

to form the gate stack. Long-channel devices (1–100 μm) were fabricated in this experiment. A 10-keV 1×10^{15} cm^{-2} B^+ implant was used to form P^+ source and drain regions. PECVD contact-isolation oxide was then deposited. Activation was performed after Al metallization at 400 °C for 20 min in an N_2 ambient. This activation anneal is sufficient to provide an $I_{\mathrm{D-ON}}/I_{\mathrm{D-OFF}}$ ratio of 3×10^3.

III. Results and Discussion

Fig. 1 shows scanning transmission electron microscopy electron energy loss spectroscopy (EELS) and energy-dispersive X-ray spectroscopy (EDXS) line scans taken from a MOSFET. The Si and O profiles overlap at the interface with Ge suggesting that a SiO_X passivation layer directly on Ge was achieved. Based on the EDXS data, the presence of Ge in SiO_X and HfSiO cannot be ruled out. The amorphous SiO_X interlayer and the amorphous HfSiO are believed to slow Ge diffusion into the high-κ [13]. Segregation of Ge from SiO_2 is also well documented [14]. The high resolution cross sectional transmission electron micrograph (HRXTEM) image shown in the inset of Fig. 1 further indicates an abrupt Ge/SiO_X interface and 1.6 nm of SiO_X in the gate stack. X-ray photoelectron-spectroscopy data on companion monitor wafers (not shown) also confirmed the absence of elemental Si in the sample. Ge in both elemental and oxidized forms was observed. Indeed, Ge–O bonds are expected at the interface between Ge and SiO_X, if the Si is completely oxidized. The combined physical characterization data indicate a surface channel Ge device. While a buried channel architecture may improve mobility versus a surface channel FET, it is not scalable due to exacerbated short-channel effects and may have limited relevance beyond the 32-nm node. The narrowband gap of Ge may allow supply voltage to be scaled further and reduce short-channel effects. Fig. 2 shows the capacitance voltage (C–V) characteristics measured on a MOSFET. A hysteresis of ∼100 mV was observed, which is significantly less than that reported for HfO_2 on GeON interfaces [15], [16]. Frequency dispersion (not shown) is negligible between 1 and 100 kHz. Such promising results are attributed to the adequate passivation of Ge surface states by a wideband gap SiO_2-like overlayer, which may act as a barrier between the substrate and eventual trapping centers. Excellent hysteresis results for samples with HfSiO on Si(100) [11] lead us to speculate that the origin of the hysteresis may not be due to bulk trapping in the HfSiO but rather due to "border traps" [17] at the SiO_X/HfSiO interface. Gate leakage shown in the inset of Fig. 2 is comparable to benchmark data for Ge [16]. The Berkeley quantum mechanical capacitance voltage (QMCV) simulation code [18] modified for Ge was used to estimate a gate stack equivalent oxide thickness (EOT) of ∼1.85 nm from the fit to the MOSCAP C–V characteristics [19]. From the TEM image, the total insulator thickness is estimated to be 4.3 nm, and a corresponding k value of ∼9 is suggested. This is much lower than the k value for HfSiO, and the degradation is attributed to the significantly thick SiO_X layer. An interface state density (D_{IT}) of $\sim 1 \times 10^{13}$ cm$^{-2} \cdot$ eV^{-1} close to the mid-gap was extracted using the statistical model of the conductance method [19], which is considered to be one of the most sensitive methods to determine D_{IT} [20]. The interface state density is significantly high, and we speculate that the enhanced trap response arises from traps at both the Ge/SiO_X as well as the SiO_X/HfSiO interfaces. Further improvements to this passivation scheme may include better passivation of traps at the SiO_X/HfSiO interface as well. Effective mobility was extracted using the split C–V technique. A peak mobility of 332 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1} at 0.05 MV/cm was observed as shown in Fig. 3. This is an enhancement of 2.0× over the universal Si/SiO_2 mobility. To our knowledge, this is one of the highest mobilities reported on unstrained surface channel Ge devices (Table I). Significant enhancement (∼2.0X) is retained at fields as high as 0.7 MV/cm. This significant mobility enhancement can be achieved with adequate interface quality coupled with a high-κ material that is capable of 90% universal SiO_2 mobility on Si(100) [4]. It is also important to consider the subtle differences between the two idealized alternative device configurations: 1) SiO_X directly on a Ge surface and 2) One or two monolayers of epitaxial Si on Ge and a SiO_2 layer on top [8]. Both of these approaches are, in principle, very similar to each other and have been

TABLE I
BENCHMARK MAXIMUM ("PEAK") HOLE MOBILITIES INCLUDING ENHANCEMENT FACTOR OVER THE UNIVERSAL Si/SiO_2, EOT, EXTRACTION METHOD, D_{IT}, AND SUBTHRESHOLD SLOPE REPORTED ON Ge

Gate stack on Ge	Max. μ_h ($cm^2\ V^{-1}s^{-1}$)	EOT (nm)	Device	μ_h extraction	D_{IT} ($cm^{-2}eV^{-1}$)	S.S. (mV/dec)	Ref.
SiO_X/HfSiO/WN	**332**	**1.85**	**MOSFET**	**I_D, split CV**	$1x10^{13}$	96 (I_S)/168	**Present**
ZrO_2/Pt	313	0.6-1	ringFET	$I_{D,LIN}$ eqn.	N.A.	N.A. (I_D)	21
$Si/SiO_x/HfO_2$/TaN	250	1.4	MOSFET	split CV	$2x10^{11}N_{IT}$	N.A. (I_S)	7
GeON/LTO/Al	310	8.0	ringFET	split CV	$5x10^{11}$	82 (I_S)	22
ZrSiO/Mo	230	< 2.0	—	—	N.A.	99 (I_S)	13
$GeON/HfO_2$/TaN	200	1.8	MOSFET	split CV	N.A.	80 (I_S)	23
SiO_x/HfO_2/TaN	194	1.55	ringFET	split CV	N.A.	N.A. (I_S)	24
$Si/SiO_2/HfO_2$/TaN	170	2.6	MOSFET	—	$5x10^{11}N_{IT}$	N.A. (I_S)	8
$Ge/Si/SiO_2/HfO_2$/TaN	**358**	1.2	MOSFET	ID, split CV	$2x10^{11}$ N_{IT}	100 (I_{DS})	**25**

successfully implemented for enhanced hole-mobility demonstrations. Our results indicate that our current approach may in fact be more beneficial for high-performance Ge MOSFETS. However, further investigation is required before the presence of a few monolayers of unoxidized Si at the top of the channel can be suggested as a possible reason for some mobility degradation. The current results definitely corroborate the well-known Si/high-κ result: The presence of a high band gap SiO_2-like interfacial layer improves mobility. The inset of Fig. 3 shows well-behaved output characteristics, with flat drain–current in the saturation region. Fig. 4 shows transfer characteristics indicating an I_{ON}/I_{OFF} ratio of about 3×10^3, a threshold voltage of $+0.5$ V, and a subthreshold slope of 168 mV/dec. Junction leakage is shown in the inset of Fig. 4. Even though high-quality junctions allow for a discussion of the actual drain–current as opposed to the often shown source current, subthreshold conduction is still dominated by junction leakage. Subthreshold slope extracted using the source current instead of the drain–current at high drain bias is significantly lower: 96 mV/dec. Further optimization of the S/D activation, as well as the area/perimeter leakage mechanisms are currently under investigation. Work-function optimization is being pursued to attain a negative V_T for the PMOS device.

A steep subthreshold slope and low C_{IT} are consistent with the significantly high mobility observed from dc I_D–V_G and split C–V measurements. However, ac conductance measurements still indicate a significant D_{IT}. These may be attributed to "border traps" [17] within the SiO_X and/or at the SiO_X/HfSiO interface. These defects, although observed in a gate conductance measurement, would not interfere strongly with a dc-device performance, thus allowing the high hole mobility observed in these devices. Single-pulse I_D–V_G measurements showed no drain–current degradation (data not shown), indicating minimal fast transient charge trapping; this could mean that the C–V hysteresis is primarily due to trapping at or close to the SiO_X/HfSiO interfaces rather than in the bulk of HfSiO. This is currently under further investigation.

IV. CONCLUSION

High-mobility surface channel pMOSFETs on bulk Ge using a 1.6-nm-thick SiO_2-like layer to passivate the Ge/dielectric interface were demonstrated. Combined with HfSiO high-κ and WN metal gate, this approach enabled a peak hole mobility of 332 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 0.05 MV/cm, corresponding to a 2.0× enhancement over universal Si/SiO_2 mobility. The devices show an I_{ON}/I_{OFF} ratio of 3×10^3 without detectable fast transient charging at an EOT of 1.85 nm. C–V frequency dispersion is negligible between 1 and 100 kHz. Interface state density close to mid-gap was $\sim 1 \times 10^{13}$ $cm^{-2} \cdot eV^{-1}$ based on conductance measurements. The high mobility and steep subthreshold slope based on source-current measurements are consistent with an improved surface passivation scheme. The high D_{IT} observed from conductance measurements and a C–V hysteresis may be attributed to border traps at the SiO_X/HfSiO interface. This processing scheme points to optimized SiO_X/HfSiO stacks as viable candidates to enable high-mobility surface channel Ge FETs for the 22-nm technology node and beyond.

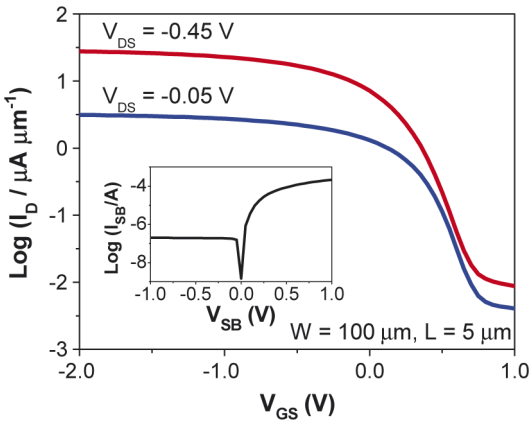

Fig. 4. Transfer characteristics show $V_T = 0.5$ V at $V_{DS} = -50$ mV, I_{ON}/I_{OFF} ratio of 3×10^3 and subthreshold slope of 166 mV/dec. Subthreshold conduction is still dominated by junction leakage and subthreshold slope extracted from the corresponding source-current measurement is 96 mV/dec.

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