Threshold Shifting of NMOS Transistors by Arsenic Ion Implantation Prior to Gate Oxidation

JOEL PEREIRA DE SOUZA AND E. CHARRY, MEMBER, IEEE

Abstract—**This paper reports on the threshold adjustment of NMOS transistors by arsenic ion implantation in the channel region directly into bare silicon just before the gate oxidation. Experimental results showed very good uniformity and reproducibility of the threshold voltages, low body effect, and high mobility values.**

NOMENCLATURE

- C_0 Gate oxide capacitance.
- C_1 Exponential factor of the Frohman-Bentchkowsky mobility field dependence [8].
- L' Effective channel length.
- Q_I Implanted charge density.
- Q_{IS} Electrical activated portion of the implanted charge that lies in silicon after all thermal process.
- V_{BS} Substrate-source reverse bias.
- V_{DS} Drain-source voltage.
- V_T Threshold voltage.
- α Q_{IS}/Q_I final electrical active fraction of the implanted charge in the channel.
- β Proportionality constant between the threshold shift and the implanted charge.
- ΔV_T Threshold voltage shift.
- ϕ_{FP} Acceptor substrate Fermi level.

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J. P. de Souza was with the Laboratório de Microeletrônica da Universidade de São Paulo, 05508, São Paulo, SP Brasil. He is now with the Instituto de Física da UFRGS, 90 000 Porto Alegre, RS, Brasil.

E. Charry was with the Laboratório de Microelectrônica da Universidade de São Paulo, 05508, São Paulo, SP, Brasil. He is now with the Departamento de Ingenieria Electrica, Universidad del Valle, Apartado de Correo 2188, Cali, Colombia.

I. INTRODUCTION

THE USE OF depletion-type transistors as a load in digital integrated circuits offers several advantages over enhancement or resistive load devices [1]. There are also depletion-type discrete devices such as single and dual gate MOSFET's which are widely employed in the electronics industry. Nowadays, this type of device is also becoming very important for applications in analog integrated circuits [2].

The usual process for adjusting the threshold of depletion-type NMOS devices consists of phosphorus or arsenic ion implantation through the gate oxide. However, if a shallow implantation profile has to be achieved in order to get devices with low body effect, the amount of impurities introduced into the silicon substrate can be affected by small variation in the oxide thickness, consequently bringing about dispersion in the threshold voltage value. In order to improve the control over the channel doping we performed that implantation step just before the gate oxidation. Moreover, we used arsenic because of its low diffusivity into silicon. In this way, the

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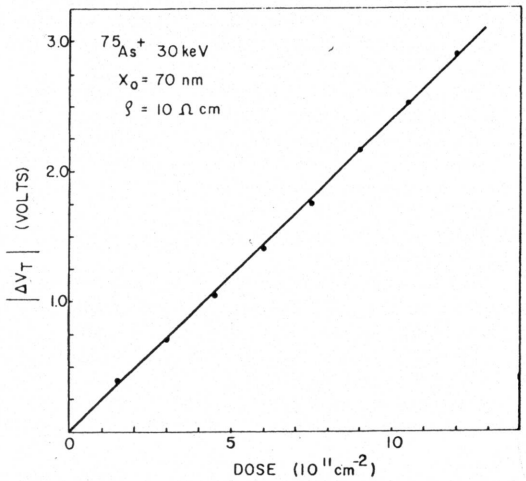

Fig. 1. Magnitude of threshold voltage shift as a function of the implanted dose.

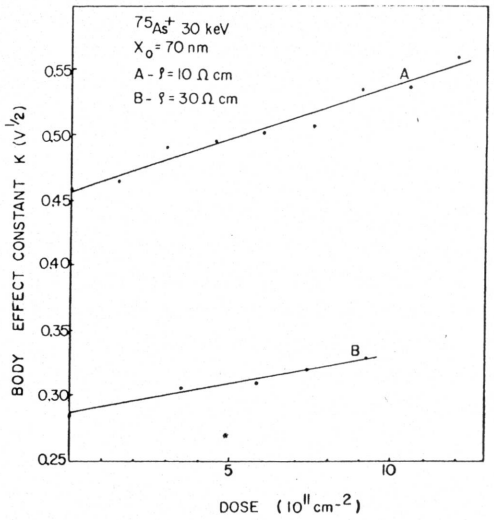

Fig. 2. Body effect constant as a function of dose for two values of resistivity.

final doping profile can be as shallow as the one obtained by the conventional process with low temperature anneal step. Therefore, these devices can have low body effect with their threshold voltage very accurately adjusted to the desired value.

The annealing of the defects generated by the ion implantation and the electrical activation of the arsenic are realized during the gate oxidation.

II. Experimental Procedure

For the present work, depletion-type NMOS Al-gate transistors and Van der Pauw structures were prepared with a process similar to that presented in ref. [3]. We used p-type silicon wafers, 10- and 30-Ω · cm resistivity, ⟨100⟩ orientation, and $1\frac{1}{2}''$ diameter. After the opening of the gate windows, arsenic was implanted with doses ranging from 1.40×10^{11} to 1.20×10^{12} cm^{-2} with 30-keV energy. The gate oxidation was performed in O_2 plus 5 percent HCl atmosphere at 1000°C in order to grow 70-nm oxide thickness.

III. Results and Analysis

Fig. 1 shows the experimental results of the threshold voltage shift versus the implanted doses, for long channel devices ($L' = 20\ \mu m$). The threshold voltages were measured in the linear region with small V_{DS} (100 mV). Because of the strictly linear relationship we can write

$$\Delta V_T = \beta Q_I. \tag{1}$$

For our particular case β is equal to $1.52 \times 10^7\ F^{-1}$. By measurement of surface carrier density in the Van der Pauw devices [4], [5], we determined that the electrically active fraction α of the implanted charge that lies in the channel after all thermal process has an average value of 0.76. However, the ratio α/C_0 agrees very well with β, so we can rewrite (1) as

$$\Delta V_T = \alpha Q_I / C_0 \tag{2}$$

or

$$\Delta V_T = Q_{IS} / C_0 \tag{3}$$

TABLE I
Frohman-Betchkowsky Exponent C_1 [8]

L' (μm)	C_1
200	0.10
20	0.10
10	0.11
5	0.23
3	0.36

as expected for shallow implanted channel devices [6].

The maximum dispersion in the threshold voltage values was ±50 mV for devices across each wafer for every dose, or for different wafers implanted with the same dose, and it is mainly due to variations in the effective surface charge density Q_{ss}, as detected by unimplanted control devices. These results were confirmed by several fabrication runs performed at different times.

Fig. 2 shows the body effect constant as a function of the implanted dose. The body effect constant was assumed as the slope of the experimental V_T versus $(V_{BS} + 2\phi_{FP})^{1/2}$ plot. The low values obtained warrant the good performance of these devices for both digital and analog applications.

The mobility values range from 800 to 650 $cm^2/V \cdot s$ being inversely dose dependent. These mobility values indicate that the silicon substrate underneath the gate oxide is well annealed.

The drain characteristics agree very well with the classic one [7] using field mobility dependence of Frohman-Bentchkowsky [8] with the C_1 exponent dependent on the channel length. In Table I we quote the C_1 values which gave the best fit between the theoretical and experimental curves, for devices with several channel lengths.

Depletion-type NMOS Si-gate transistors also were fabricated in few runs using the described process of threshold voltage shifting. The results obtained are in close agreement with the above reported for Al-gate devices.

IV. Conclusion

We presented in this paper a simple process for adjustment of the threshold voltage of depletion-type NMOS transistors. By this process we attained a high degree of control of the threshold voltage shift with electrical characteristics proper for high-speed digital circuits and for analog devices.

The drain characteristics obey the C_0 model as expected for devices with shallow channel junctions [9].

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