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Nano-Transistores de Porta Dupla em Silício Sobre Isolante
Simulação de FinFETs sub-20 nm

Double-Gate Nanotransistors in Silicon-on-Insulator
Simulation of sub-20 nm FinFETs

Tese de Doutorado como requisito parcial para a obtenção do grau de Doutor em Microeletrônica

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Dedico este trabalho

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LIST OF NOTATIONS

ρ	Charge density
ψ	Electrostatic potential of silicon
μ	Semiconductor mobility
α	Correction parameter for Whitfield method
α_{fb}	Variable that relates the interaction between the front and the back gates
$\alpha_{fb(d.a)}$	α_{fb} from depletion approximation
α_I	Ion implantation angle
ϕ_F	Fermi potential
ϕ_{Fn}	Quasi-Fermi level for electrons
ϕ_{Fp}	Quasi-Fermi level for holes
ψ_m	Minimum potential in the thin-film
ϕ_{ms}	Work-function difference
ϕ_{msb}	Back-gate to thin-film work-function difference
ϕ_{msf}	Front-gate to thin-film work-function difference
β_o	Transconductance factor ($\mu_o C_{ox} W/L$)
μ_o	Low-field mobility
θ	Mobility degradation parameter
ψ_{ob}	Potential drop across the back-gate oxide
ψ_{of}	Potential drop across the front-gate oxide
ε_{ox}	Silicon oxide permittivity
ε_{si}	Silicon permittivity
λ	Characteristic length
σ	Standard-deviation
ψ_{sb}	Back-gate surface potential
ψ_{sf}	Front-gate surface potential
ψ_{sfD}	Front-gate surface potential at the drain level in the channel

ψ_{sfS} Front-gate surface potential at the source level in the channel

A_v Voltage gain

BOX Buried oxide

C'_b Thin-film capacitance per unit area

C'_{bb} Total front to back capacitance per unit area

C_D Depletion oxide capacitance per unit area (ε_{si}/x_d)

C'_{ob} Back-gate oxide capacitance per unit area

C'_{of} Front-gate oxide capacitance per unit area

C_{ox} Oxide capacitance per unit area (ε_{ox}/t_{ox})

C_{ov} Parasitic or extrinsic overlap capacitance

C_{GDe} Parasitic or extrinsic gate-to-drain capacitance

C_{GSe} Parasitic or extrinsic gate-to-source capacitance

DG Double-gate

DIBL Drain Induced Barrier Lowering

DICE Drain Induced Conductivity Enhancement

DUT Device Under Test

dx Infinitesimally thick portion of the inversion layer in the position x_i

E_c Critic transversal Electric field

E_{sb} Back-gate electric field

$E_{sb(d.a)}$ E_{sb} from depletion approximation

E_{sf} Front-gate electric field

$E_{sf(d.a)}$ E_{sf} from depletion approximation

E Electric field

FD Fully-Depleted

g_d Output conductance

g_m Transconductance

G_m Complex transconductance

H_{fin} Silicon fin height

I_{DS} Total current in the inversion layer or Total source/drain current

I_{off} Turn-off current

I_{on} Turn-on current

L Effective channel length

L_d Modulation effective channel length

l_B Characteristic length

L_{Geff} Effective Gate length

L_{eff}	Modulated effective channel length
L_G	Gate length
L_{Gm}	Mask gate length
L_{SD}	S/D extension length
L_{SDmax}	maximum S/D extension length
M	Number of gate sections
n	Electron concentration
N	Number of channel sections
N_A	Silicon doping concentration
N_{fin}	Thin-film doping concentration
N_T	Numbers of parallel fins
N_o	Peak silicon doping concentration
n_i	Intrinsic-carrier concentration
n_o	Thermal-equilibrium electron concentration
p	Hole concentration
PD	Partially-Depleted
P_{fin}	Fin pitch
p_o	Thermal-equilibrium hole concentration
q	Electron charge
Q'_b	Thin-film depletion charge density per unit area
Q_b	Thin-film total charge
Q_D	Depletion charge per unit area
Q_{Df}	Front-channel drain total charge
Q'_{Gb}	Back-gate charge density per unit area
Q_{Gb}	Back-gate total charge
Q'_{Gf}	Front-gate charge density per unit area
Q_{Gf}	Front-gate total charge
Q'_{ib}	Back-channel charge density per unit area
Q'_{if}	Front-channel charge density per unit area
Q_{if}	Front-channel total charge
Q'_{ob}	Back-gate oxide charge per unit area
Q'_{of}	Front-gate oxide charge per unit area
Q_{ox}	Oxide charge per unit area
Q_{Sf}	Front-channel source total charge
R_{Ge}	Parasitic or extrinsic gate resistance

R_p	Projected range
ΔR_p	Standard-deviation or “straggle”
S	Subthreshold slope
SEM	Scanning Electron Microscopy
SG	Single-gate
SOI	Silicon-on-Insulator
t_b	Thin-film thickness
TEM	Transmission Electron Microscopy
T_{fin}	Silicon fin thickness
t_{ob}	Back-gate oxide thickness
t_{of}	Front-gate oxide thickness
t_{ox}	Oxide thickness
t_{ox_top}	Top-oxide thickness
t_{si}	Thin-film thickness
u_T	Thermal voltage
UTB	Ultra-Thin-Body
UTBB	Ultra-Thin-Body and Box
V_A	Early voltage
V_D	Drain voltage
V_{FBb}	Back-gate flatband voltage
V_{FBf}	Front-gate flatband voltage
V_G	Gate voltage
V_{Gb}	Back-gate voltage
V_{Gf}	Front-gate voltage
V_S	Source voltage
V_T	Threshold voltage
V_{TS}	Threshold voltage
W	Effective channel width
W_{eff}	Effective or equivalent FinFET channel width
W_G	Channel width
x_d	Space-charge region width
x_{dmax}	Maximum space-charge region width
x_i	Arbitrary position in the channel
ΔL	Effective channel length shortening

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RESUMO

Esta Tese apresenta os resultados da simulação do transporte eletrônico em três dimensões (3D) no nano dispositivo eletrônico conhecido como “SOI-FinFET”. Este dispositivo é um transistor MOS em tecnologia Silício sobre Isolante – “Silicon-on-Insulator”, SOI – com porta dupla e cujo canal e zonas de fonte e dreno são realizadas em uma estrutura nanométrica vertical de silício chamada de “finger” ou “fin”. Como introdução ao dispositivo em questão, é feita uma revisão básica sobre a tecnologia e transistores SOI e sobre MOSFETs de múltiplas portas. A implementação de um modelo tipo “charge-sheet” para o transistor SOI-MOSFET totalmente depletado e uma modelagem deste dispositivo em altas frequências também é apresentada. A geometria do “fin” é escalada para valores menores do que 100 nm, com uma espessura entre 10 e 20 nm. Um dos objetivos deste trabalho é a definição de parâmetros para o SOI-FinFET que o viabilizem para a tecnologia de 22 nm, com um comprimento efetivo de canal menor do que 20 nm. O transistor FinFET e uma estrutura básica simplificada para simulação numérica em 3D são descritos, sendo utilizados dados de tecnologias atuais de fabricação. São apresentados resultados de simulação numérica 3D (curvas I_D-V_G, I_D-V_D, etc.) evidenciando as principais características de funcionamento do FinFET.

É analisada a influência da espessura e dopagem do “fin” e do comprimento físico do canal em parâmetros importantes como a tensão de limiar e a inclinação de sublimiar. São consideradas e analisadas duas possibilidades de dopagens da área ativa do “fin”: (1) o caso em que esta pode ser considerada não dopada, sendo baixíssima a probabilidade da presença de dopantes ativos, e (2) o caso de um alto número de dopantes ativos (> 10 é provável). Uma comparação entre dois simuladores numéricos 3D de dispositivos é realizada no intuito de explicitar diferenças entre modelos de simulação e características de descrição de estruturas 3D. São apresentadas e analisadas medidas em dispositivos FinFET experimentais. Dois métodos de extração de resistência série parasita são utilizados em FinFETs simulados e caracterizados experimentalmente. Para finalizar, são resumidas as principais conclusões deste trabalho e são propostos os trabalhos futuros e novas diretivas na pesquisa dos transistores FinFETs.

Palavras-Chave: MOSFET, SOI, FinFET, dupla-porta, múltiplas-portas, nano-dispositivos, simulação numérica em 3D.

Nano-Transistores de Porta Dupla em Silício Sobre Isolante
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ABSTRACT

This thesis presents the results of 3D-numerical simulation of electron transport in double-gate SOI-FinFETs in the decanometer size range. A basic review on the SOI technology and multiple gates MOSFETs is presented. The implementation of a charge-sheet model for the fully-depleted SOI-MOSFET and a high frequency modeling of this device are first presented for a planar device topology. The second part of this work deals with FinFETs, a non-planar topology. The geometry of the silicon nano-wire (or "fin") in this thesis is scaled down well below 100 nm, with fin thickness in the range of 10 to 20 nm. This work addresses the parameters for a viable 22 nm CMOS node, with electrical effective channel lengths below 20 nm. The basic 3D structure of the FinFET transistor is described in detail, then it is simulated with various device structural parameters, and results of 3D-numerical simulation (I_D-V_G curves, I_D-V_D, etc.), showing the main features of operation of this device, are presented.

The impacts of varying silicon fin thicknesses, physical channel lengths, and silicon fin doping concentration on both the average threshold voltage and the subthreshold slope are investigated. With respect to the doping concentration, the discrete and highly statistical nature of impurity presence in the active area of the nanometer-range fin is considered in two limiting cases: (1) the zero-doping or undoped case, for highly improbable presence of active dopants, and (2) the many-dopants case, or high number (> 10 are probable) of active dopants in the device channel. A comparison between two 3D-numerical device simulators is performed in order to clarify differences between simulation models and features of the description of 3D structures. A structure for SOI-FinFETs is optimized, for the undoped fin, showing its applicability for devices with electrical effective channel lengths below 20 nm. SOI-FinFET measurements were performed on experimental devices, analyzed and compared to device simulation results. This thesis uses parasitic resistance extraction methods that are tested in FinFET simulations and measurements. Finally, the main conclusions of this work are summarized and the future work and new directions in the FinFETs research are proposed.

Keywords: MOSFET, SOI, FinFET, double-gate, multiple-gate, nano-device, 3D-numerical simulation.

1 INTRODUCTION

Silicon-on-Insulator (SOI) technology (Colinge, 1991), with single-gate (SG) SOI-MOSFETs, has become in the last years a serious competitor for traditional BULK technology (Flandre, 1996, 1999; Iñíguez, 1996; Ferreira, 1997). Double-gate (DG) SOI-MOSFETs have superior performance over single-gate ones (Doyle, 2003; Colinge, 2007; Kranti, 2007). SOI-FinFETs (Lindert, 2001), also called vertical SOI MOSFETs have demonstrated a good potential for circuit applications, in particular low-voltage analog applications (Pei, 2002; Giacomini, 2007; Pavanello, 2007a-b; Kranti, 2004, 2007). Geometry and process parameters optimization are a key factor to increase the performance of the SOI-FinFET for circuit design and fabrication. 3D-numerical simulation is a powerful tool to model and study the device characteristics and it has been extensive used (Pei, 2002; Dixit, 2005; Trivedi, 2005; Fossum, 2007; Zhao, 2008).

1.1 Objectives

The main goal of this work addresses the parameters for a viable 22 nm CMOS technology node, with electrical effective channel lengths below 20 nm. In order to achieve this goal a good understanding of the characteristics of the FinFET and the influence of process and geometry parameters on its behavior is fundamental. The dependence of important parameters such as threshold voltage V_T and subthreshold slope S on silicon fin thickness T_{fin} and silicon fin doping N_{fin} is addressed.

Due to the three-dimensional nature of the FinFET device, 3D-numerical simulation is a necessity. Thus a 3D-device structure based on technology standards and suitable for 3D-numerical simulation is defined and the results of a 3D-numerical simulation of the SOI-FinFET are presented and analyzed. Also SOI-FinFET measurements are presented and analyzed.

Two brief chapters about SOI technology and multi-gate MOSFETs are included as a basic introduction to the FinFET device and a chapter is dedicated to describe the implementation of a charge-sheet model for the fully-depleted SOI-MOSFET and a high frequency modeling of this device.

1.2 Organization of the Chapters

This thesis is organized as follows. Chapter 1 presents an introduction to this work. Chapter 2 presents an overview of SOI CMOS technology and SOI-MOSFETs. Chapter 3 presents a high frequency modeling of planar SOI-MOSFETs, with single active gate, that was developed by the author. Chapter 4 presents an overview of multi-gate MOSFETs, with emphasis on possible FinFET structures to be used in the 22 nm technology node and beyond. Chapter 5 presents the results and analysis of 3D-numerical simulation of the Double-Gate (DG) SOI-FinFET. These analyses have the goal of finding the structural double-gate FinFET parameters that are most suited for devices with effective channel length below 20 nm. Chapter 6 presents the results and analysis of measurements of experimental SOI-FinFETs manufactured at IMEC - Interuniversity Microelectronics Center in Belgium. Finally, Chapter 7 summarizes the conclusions of this thesis pointing out the most important goals and new directions in the FinFETs research.

2 SOI MOSFETS

In this chapter a brief overview of the Silicon-on-Insulator (SOI) CMOS technology and SOI MOSFET structures is presented.

2.1 SOI CMOS Technology

SOI technology (Colinge, 1991) is mentioned on the first description of an IGFET (Insulated-gate-field-effect-transistor) as far back as 1926, but unfortunately the technology of that time was unable to produce an operational device over a solid substrate. In the first half of the 1960's decade the MOSFET (metal-oxide-semiconductor field-effect-transistor) fabricated on "bulk" silicon substrates became available. Since 1982, CMOS (Complementary MOS) has been the driving technology for the microelectronics industry throughout the world. Integrated circuits fabricated on "bulk" silicon substrates represent the majority of commercial production today, with Silicon-on-Insulator over silicon substrates gaining ground on the commercial applications. The availability of electronic-grade silicon material and the excellent characteristics of silicon dioxide are key aspects aiding the predominant position of silicon devices in the industry.

SOI technology has been developed for over two decades and commercial circuits became available. Many techniques have been developed for producing a film of silicon on top of an insulator (see Figure 2.1). Some of the principal techniques are:

- SIMOX (Separation by Ion-Implanted Oxygen)
- BESOI (Bonding and Etch-back SOI)
- "Smart Cut" (Cut by Ion-Implanted Hydrogen)
- ZMR (Zone Melting Recrystalization)
- FIPOS (Full Isolation by Porous Oxidized Silicon)

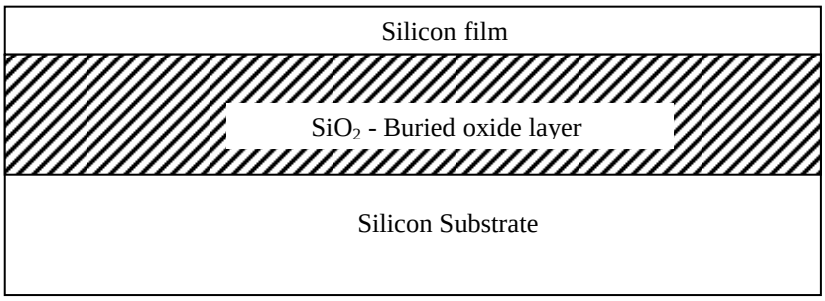


Figure 2.1: Cross section of an SOI wafer.

In fact the SOI technology has many advantages over the traditional bulk one. A simplified CMOS inverter structure in bulk and SOI technology is shown in Figure 2.2 and Figure 2.3 respectively, where the basic differences can be compared. First, the SOI structure is more compact offering a higher integration density; there is no need of wells in SOI and the direct contact between P+ and N+ junctions is possible. Second, the buried-oxide (SiO_2) layer prevents and/or reduces most of the parasitic effects verified in bulk silicon devices; also the known body effect is reduced. Third, the silicon film is thin enough for the junctions reach through the oxide layer, reducing the capacitances between these junctions and the substrate and virtually eliminating the possibility of latch-up; SOI offers also the ease control of making shallow junctions by controlling the thickness of the silicon film.

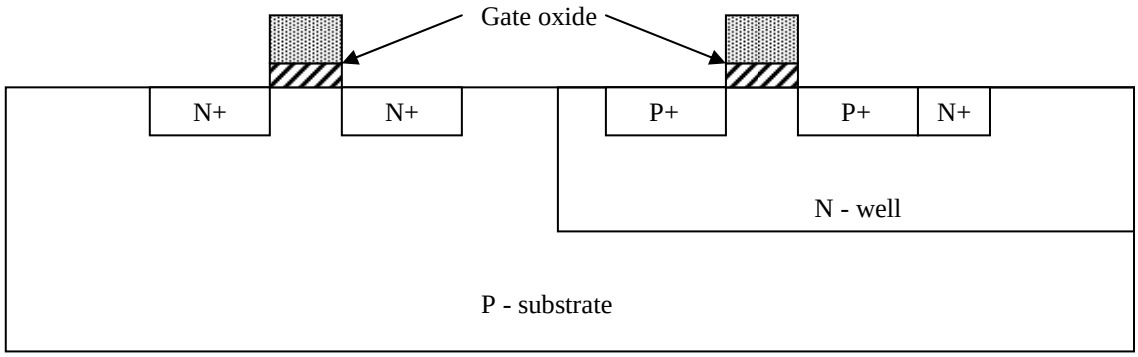


Figure 2.2: A simplified bulk CMOS inverter structure.

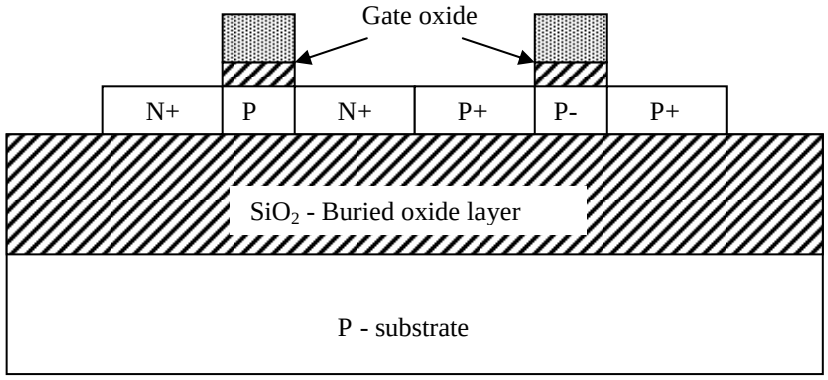


Figure 2.3: A simplified SOI CMOS inverter structure.

Some of basic advantages of SOI over bulk technology is summarize as follows:

- Higher integration density;
- Lower source and drain capacitances;
- Higher current capability;
- Virtual immune to latch-up;
- Better HF characteristics;
- Lower short channel effects;
- Better transconductance subthreshold slope;
- Better radiation hardness;

2.2 The SOI MOSFET

A previous description of SOI MOSFET structure and basic characteristics are presented as background to the Section 3.

2.2.1 Structure

The basic structure of the SOI MOSFET is shown in Figure 2.4. The NMOS transistor is used as reference hereafter. The basic necessary three terminals, source, drain and gate, and the forth called back-gate, are shown. The thickness of the silicon film t_{si} (or t_b) makes the distinction between thick-film and thin-film devices. The presence of the buried oxide layer acts as a second gate or back-gate. From now on the normal gate is called front-gate and the terminal voltages are name V_{Gf} (voltage of front-gate), V_{Gb} (voltage of back-gate), V_S e V_D, to avoid confusion.

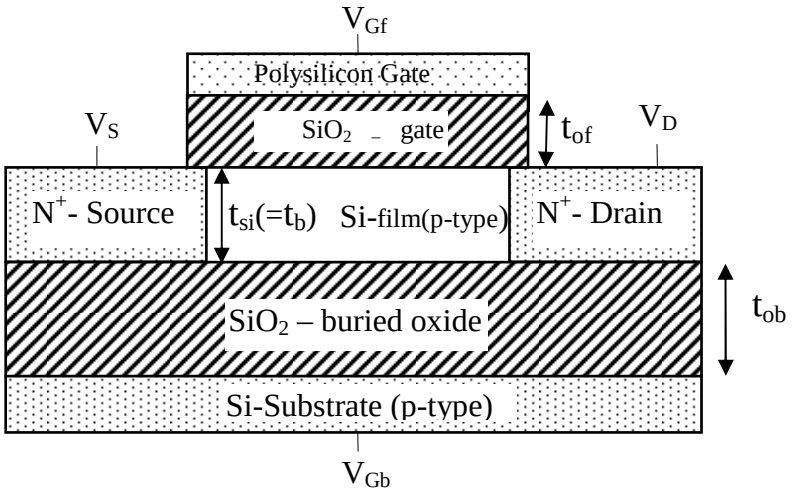


Figure 2.4: A simplified SOI NMOS transistor structure.

2.2.2 Basic Characteristics

As a result of the presence of the back-gate the SOI MOSFET offers many modes of operation depending on both terminal voltages (V_{Gf}, V_{Gb}, V_S, V_D) and thickness of the silicon film t_{si} (or t_b).

In thick-film devices the depletion zones from the front and back gates do not reach each other, resulting in a neutral zone in the middle of the silicon film. If this neutral zone is somehow connected to ground, the SOI MOSFET shows the same

characteristics of a bulk device; otherwise a floating neutral zone results in an effect on the I-V characteristics called kink effect and also in the presence of an open base parasitic bipolar transistor. Thick-film MOSFETs are not the subject of this overview and do not offer advantages over bulk counterparts.

In thin-film devices the depletion zones from the front and back gates reach each other, resulting in a fully-depleted silicon film. Depending on V_{Gf} and V_{Gb} the front and back interfaces can operate in depletion, inversion and accumulation, resulting in nine different modes of operation. However, most of these modes of operation are not practical, especially those with back-gate interface inverted or accumulated. Therefore fully-depleted (FD) SOI MOSFETs with back-gate interface depleted offer many advantages over bulk MOSFETs.

In the last decade the thickness of the silicon film t_{si} has been reduced by 10x and is nowadays around 10 nm or less. The buried oxide tchickness also has been reduced by 10x and is nowadays around 25 nm. Now the back-gate acts as an affective second gate and these devices are called UTBB or Ultra-Thin-Body-and-Box.

3 HIGH FREQUENCY MODELING OF SOI-MOSFETS

In this chapter a physical charge-sheet model for fully-depleted (FD) SOI MOSFETs is developed and used as a basic tool on a method to extend the validity of the quasi-static MOSFET models beyond the frequency on which these models fail.

3.1 A Charge-Sheet Model

The modeling of MOSFETs requires an accurate and continuous model for the transistor behavior. A numerical resolution of Poisson's and continuity equations in two-dimensions can achieve this goal, but imposes a burdensome numerical process. The problem have been made analytically tractable by means of certain approximations, two of which were first introduced in Brews (1978) and are the gradual channel and the charge-sheet approximations. Models based on these last two approximations and others ones have been developed, but many of them suffer of shortcomings (Tsividis, 1994), such as non-continuity in the MOSFET's regions of operation, non-conservation of charge, only quasi-statically validity, etc.

The purpose of this chapter is to presents a numerical charge-sheet model for thin-film SOI MOSFETs valid for back-channel in depletion from source to drain, based on the gradual channel and the charge-sheet approximations, that can predict the behavior of the transistor at high frequencies (microwave) with a good accuracy and be physically-based, with few fitting parameters. The basic model is only valid for long-channel devices so that short-channel effects such as velocity saturation, channel length modulation and drain-induced conductivity enhancement (DICE) are included. An effective front-gate voltage is used to link the velocity saturation effect to the drain saturation potential. The model is based on the front-gate surface potential that is computed with a newton-raphson method. The current and charge equations are derived from the model and integrated in Matlab routines.

3.1.1 Model Definitions

3.1.1.1 Poisson’s Equation

A four-terminal SOI nMOSFET structure is shown in Figure 3.1 as a reference to evaluate the Poisson’s equation inside the silicon thin-film. The front-gate, back-gate, source and drain voltages are represented by V_{Gf}, V_{Gb}, V_S, and V_D, respectively.

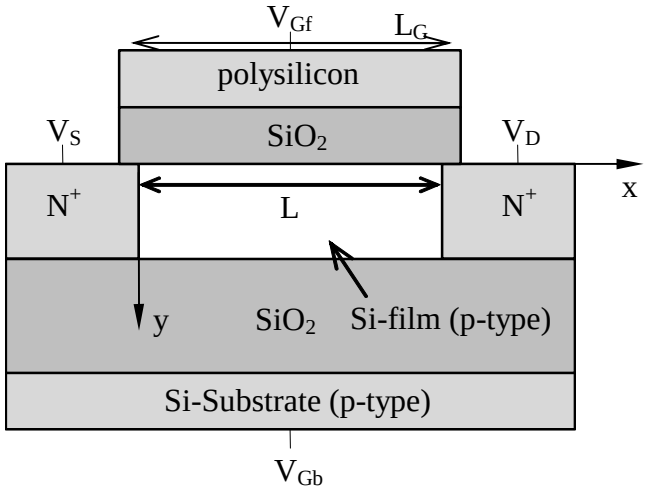


Figure 3.1: A simplified four-terminal SOI nMOSFET structure.

Inside the silicon thin-film the Poisson's equation can be written as

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=-\frac{\rho(x,y)}{\varepsilon_{si}} \tag{3.1}$$

where ψ is the electrostatic potential of silicon; ρ is the charge density; and ε_{si} is the silicon permittivity. Assuming a gradual channel approximation, which states that the longitudinal electrical field (*x*-direction) is much smaller than the transverse one (*y*-direction), leads to

$$\left|\frac{\partial^2\psi(x,y)}{\partial x^2}\right| << \left|\frac{\partial^2\psi(x,y)}{\partial y^2}\right| \tag{3.2}$$

Thus the x-direction dependence of ψ in (3.1) can be neglected and the Poisson's equation is then given by

$$\frac{d^2\psi}{dy^2}=-\frac{\rho}{\varepsilon_{si}} \qquad \text{or} \qquad \frac{d\mathsf{E}^2}{d\psi}=-\frac{2\rho}{\varepsilon_{si}} \tag{3.3}$$

where E is the electric field and the *y*-direction dependence is omitted for clarity. The charge density ρ can be defined as

$$\rho=-q\left[n-p+N_A\right] \tag{3.4}$$

where N_A is thin-film doping concentration; "*n*" and "*p*" are the electron and hole concentrations, respectively; and "*q*" is the electron charge. The condition of neutrality in the film implies that

$$N_A = [p_o - n_o] \tag{3.5}$$

where n_o and p_o are the thermal equilibrium electron and hole concentrations, respectively.

Thus, using (3.5) and (3.4) in (3.3), Poisson's equation can be rewritten as

$$\frac{d\mathsf{E}^2}{d\psi} = -\frac{2\rho}{\varepsilon_{si}} = \frac{2q}{\varepsilon_{si}}[n - p + p_o - n_o] \tag{3.6}$$

To clarify the conventions adopted Figure 3.2 shows an energy-band diagram at the surface of a p-type semiconductor, where the electrostatic potential ψ is measured with respect to the intrinsic Fermi level E_i and defined as zero in the bulk. At the oxide-semiconductor interface ψ is called the surface potential ψ_s. The quasi-Fermi level ϕ_F is define as $\phi_F = (E_F - E_i)/q$.

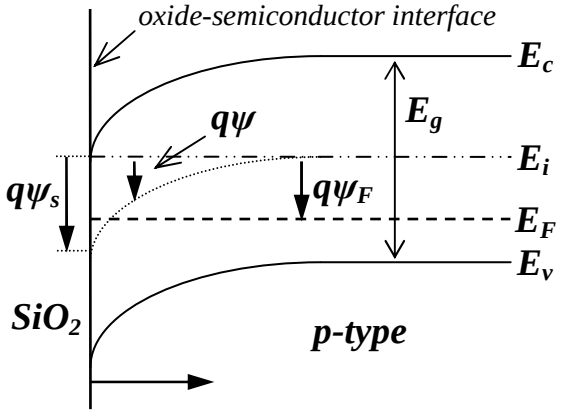


Figure 3.2: Energy-band diagram at the surface of a p-type semiconductor. The electrostatic potential ψ is measured with respect to the intrinsic Fermi level E_i and defined as zero in the bulk (the surface potential ψ_s is positive as shown).

Since the structure of Figure 3.1 is under non-equilibrium conditions (currents are flowing), quasi-Fermi levels for electrons and holes, ϕ_{Fn} and ϕ_{Fp}, respectively, should be introduced. The hole current is negligible and then ϕ_{Fp} can be set to ϕ_F, the latter taken in a region of the thin-film where $\psi=0$. In addition, ϕ_{Fn} can be considered constant in the *y*-direction since the vertical electron current is negligible, leading to the expression $\phi_{Fn} = \phi_F + V(x)$, where $V(x)$ is the potential in a position *x* along the channel that

represents the difference between ϕ_{Fn} in the channel and ϕ_{Fp}. Using these considerations, p_o, n_o, p and n are given by

$$\begin{aligned} p_o &= n_i e^{\phi_F/u_T} \\ n_o &= n_i e^{-\phi_F/u_T} = p_o e^{-2\phi_F/u_T} \\ p &= n_i e^{(\phi_F-\psi)/u_T} = p_o e^{-\psi/u_T} \\ n &= n_i e^{(\psi-\phi_F-V)/u_T} = p_o e^{(\psi-2\phi_F-V)/u_T} \end{aligned} \tag{3.7}$$

where n_i is the intrinsic-carrier concentration and u_T is the thermal voltage. Using (3.7) in (3.6) and considering that $p_o = N_A$, then finally the Poisson's equation takes the form below, in a region of the thin-film where $\psi = 0$.

$$\frac{d\mathcal{E}^2}{d\psi} = -\frac{2\rho}{\varepsilon_{si}} = \frac{2qN_A}{\varepsilon_{si}}\left[e^{(\psi-2\phi_F-V)/u_T} - e^{-\psi/u_T} + 1 - e^{-2\phi_F/u_T}\right] \tag{3.8}$$

An one-dimensional active portion of the structure of Figure 3.1, taken in *y*-direction at an arbitrary *x*-position, is shown in Figure 3.3 as a reference for the following considerations.

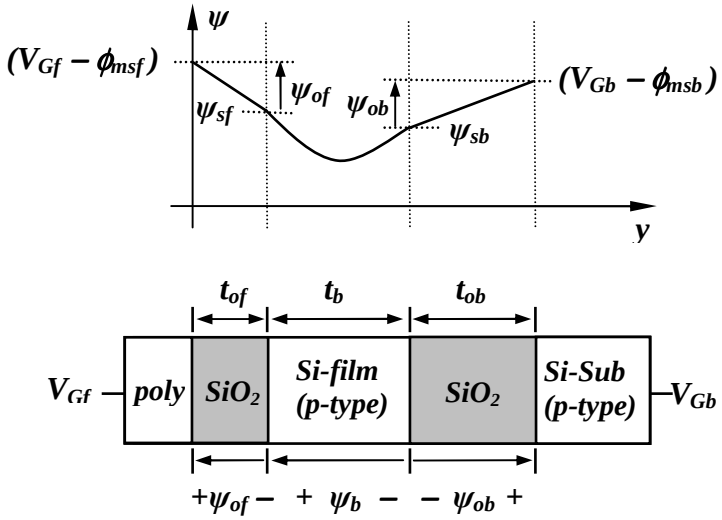


Figure 3.3: One-dimensional active portion of the structure of Figure 3.1, taken in *y*-direction at an arbitrary *x*-position.

The equations that express the coupling between front and back gates can be found integrating on both sides of (3.8) and using the front and back-gate surface potentials,

ψ_{sf} and ψ_{sb}, respectively, and the front and back-gate surface electric fields, E_{sf} and E_{sb}, respectively. Thus

$$\begin{aligned} \int_{E_{sf}}^{E} dE^2 &= G^2\Big|_{\psi_{sf}}^{\psi} \Rightarrow E^2 - E_{sf}^2 = G^2(\psi) - G^2(\psi_{sf}) \\ \int_{E_{sb}}^{E} dE^2 &= G^2\Big|_{\psi_{sb}}^{\psi} \Rightarrow E^2 - E_{sb}^2 = G^2(\psi) - G^2(\psi_{sb}) \end{aligned} \tag{3.9}$$

where G^2 is a function defined as

$$G^2 \equiv \int_0^{\psi}\left(-\frac{2\rho}{\varepsilon_{si}}\right)d\psi = \frac{2u_T^{\,2}}{l_B^2}\left[\left(e^{(\psi-2\phi_F-V)/u_T} - e^{(-2\phi_F-V)/u_T}\right) + \left(e^{-\psi/u_T} - 1\right) + F_{phf}\left(\frac{\psi}{u_T}\right)\right] \tag{3.10}$$

where $l_B \equiv \sqrt{\dfrac{u_T\varepsilon_{si}}{qN_A}}$ is the characteristic length and $F_{phf} \equiv \left(1 - e^{-2\phi_F/u_T}\right)$

A parameter α_{fb} that represents the interaction between front and back gates can now be defined. Thus combination of the equations (3.9) gives

$$\alpha_{fb} = E_{sf}^2 - G^2(\psi_{sf}) = E_{sb}^2 - G^2(\psi_{sb}) \tag{3.11}$$

It is important to note that α does not change significantly when the depletion approximation is applied (Ortiz-Conde, 1988; Mallikarjun, 1990).

The relations between the applied gate voltages, V_{Gf} and V_{Gb} respectively, and ψ_{sf} and ψ_{sb}, can be written taking into account the potential drops across the front and back-gate oxides, ψ_{of} and ψ_{ob}, respectively (Figure 3.3), and the front and back-gate to thin-film work-function differences, ϕ_{msf} and ϕ_{msb}, respectively. Thus

$$\begin{aligned} V_{Gf} - \phi_{msf} &= \psi_{sf} + \psi_{of} \\ V_{Gb} - \phi_{msb} &= \psi_{sb} + \psi_{ob} \end{aligned} \tag{3.12}$$

Application of Gauss's theorem to the front and back oxide-film surfaces gives

$$\psi_{of} = \frac{\varepsilon_{si}\mathsf{E}_{sf}}{C'_{of}} - \frac{Q'_{of}}{C'_{of}}$$
$$\psi_{ob} = -\frac{\varepsilon_{si}\mathsf{E}_{sb}}{C'_{ob}} - \frac{Q'_{ob}}{C'_{ob}} \tag{3.13}$$

where Q'_{of} and Q'_{ob} are the front and back-gate oxide charges per unit area, respectively; and C'_{of} and C'_{ob} are the front and back-gate oxide capacitances per unit area, respectively.

Combination of (3.12) and (3.13) yields two useful definitions, V_{gf} and V_{gb} that represent, respectively, the difference between V_{Gf} and the front-gate flatband voltage V_{FBf} and the difference between V_{Gb} and the back-gate flatband voltage V_{FBb}. Thus

$$V_{gf} \equiv V_{Gf} - V_{FBf} = \psi_{sf} + \frac{\varepsilon_{si}\mathsf{E}_{sf}}{C'_{of}}$$
$$V_{gb} \equiv V_{Gb} - V_{FBb} = \psi_{sb} - \frac{\varepsilon_{si}\mathsf{E}_{sb}}{C'_{ob}} \tag{3.14}$$

where

$$V_{FBf} \equiv -\frac{Q'_{of}}{C'_{of}} + \phi_{msf}$$
$$V_{FBb} \equiv -\frac{Q'_{ob}}{C'_{ob}} + \phi_{msb} \tag{3.15}$$

3.1.1.2 Poisson's Equation - Depletion Approximation

To find simple relations between front and back surface potentials and electric fields, the assumption that the film is completely depleted can be done, excepting narrow inversion or accumulation layers at the surfaces. Thus the charge density in (3.4) can be replaced by

$$\rho = -qN_A \tag{3.16}$$

and the Poisson's equation takes the simple form

$$\frac{d^2\psi}{dy^2} = \frac{qN_A}{\varepsilon_{si}} \quad \text{or} \qquad \frac{d\mathsf{E}}{dy} = -\frac{qN_A}{\varepsilon_{si}} \tag{3.17}$$

The coupling between front and back gates can be found integrating on both sides of (3.17), as in the rigorous analysis in Section 3.1.1.1, with the front and back-surface electric fields from depletion approximation, $\mathsf{E}_{sf(d.a)}$ and $\mathsf{E}_{sb(d.a)}$, respectively, being used in the place of E_{sf} and E_{sb}. Thus

$$\begin{aligned}
&\int_{\mathsf{E}_{sf}}^{\mathsf{E}} d\mathsf{E} = G_{(d.a)}\Big|_{o}^{y} \Rightarrow \mathsf{E} - \mathsf{E}_{sf(d.a)} = -\frac{qN_A y}{\varepsilon_{si}} \\
&\int_{\mathsf{E}_{sb}}^{\mathsf{E}} d\mathsf{E} = G_{(d.a)}\Big|_{t_b}^{y} \Rightarrow \mathsf{E} - \mathsf{E}_{sb(d.a)} = -\frac{qN_A y}{\varepsilon_{si}} + \frac{qN_A t_b}{\varepsilon_{si}}
\end{aligned} \tag{3.18}$$

where $G_{(d.a)}$ is a function defined as

$$G_{(d.a)} \equiv \int_{0}^{y} \left(-\frac{qN_A}{\varepsilon_{si}}\right) dy = -\frac{qN_A y}{\varepsilon_{si}}$$

Combination of the equations (3.18) gives

$$\left(\mathsf{E}_{sf(d.a)} - \mathsf{E}_{sb(d.a)}\right) = \frac{qN_A t_b}{\varepsilon_{si}} \quad \text{or} \quad \varepsilon_{si}\left(\mathsf{E}_{sf(d.a)} - \mathsf{E}_{sb(d.a)}\right) = -Q'_b \tag{3.19}$$

where $Q'_b = -qN_A t_b$ is the thin-film depletion charge density per unit area.

Eq. (3.18) can be rewritten as

$$\frac{d\psi}{dy} = -\mathsf{E} = -\mathsf{E}_{sf(d.a)} + \frac{qN_A y}{\varepsilon_{si}} \tag{3.20}$$

and its integration yields the relation between ψ_{sf} and ψ_{sb}.

Thus

$$\int_{\psi_{sf}}^{\psi} d\psi = H\Big|_{o}^{y} \Rightarrow \psi - \psi_{sf} = H(y)$$
$$\int_{\psi_{sb}}^{\psi} d\psi = H\Big|_{t_b}^{y} \Rightarrow \psi - \psi_{sb} = H(y) - H(t_b) \tag{3.21}$$

where H is a function defined as

$$H \equiv \int_0^y \left(-\mathsf{E}_{sf(d.a)} + \frac{qN_A y}{\varepsilon_{si}} \right) dy = -\mathsf{E}_{sf(d.a)} y + \frac{qN_A y^2}{2\varepsilon_{si}}$$

Combination of (3.21) gives

$$\left(\psi_{sf} - \psi_{sb}\right) = \mathsf{E}_{sf(d.a)} t_b - \frac{qN_A t_b^2}{2\varepsilon_{si}} \quad \text{or} \quad C'_b \left(\psi_{sf} - \psi_{sb}\right) = \varepsilon_{si} \mathsf{E}_{sf(d.a)} + \frac{Q'_b}{2} \tag{3.22}$$

where $C'_b = \dfrac{\varepsilon_{si}}{t_b}$ is the thin-film capacitance per unit area.

3.1.1.3 Numerical Solution for ψ_{sf} and ψ_{sb}

To calculate the drain current and the terminal charges of the structure of Figure 3.1, the surface potentials ψ_{sf} and ψ_{sb} have to be obtained. A numerical newton-raphson method has been employed.

Using a depletion approximation to the previous defined α, i.e., $\alpha_{(d.a)}$, Eq. (3.11) can be rewritten as

$$\alpha_{fb(d.a)} = \mathsf{E}_{sf}^2 - G^2(\psi_{sf}) = \mathsf{E}_{sb}^2 - G^2(\psi_{sb}) \tag{3.23}$$

and the following functions can be defined.

$$f = \mathsf{E}_{sf}^2 - G^2(\psi_{sf}) - \alpha_{fb(d.a)} = 0$$
$$g = \mathsf{E}_{sf}^2 - G^2(\psi_{sf}) - \left(\mathsf{E}_{sb}^2 - G^2(\psi_{sb})\right) = 0 \tag{3.24}$$

The parameter $\alpha_{fb(d.a)}$ can be derived (Ortiz-Conde, 1988; Mallikarjun, 1990), using the following expression to ρ:

$$\rho = q\left[p - N_A\right] \tag{3.25}$$

where p is accounted to avoid large errors in the charge sheet model.

Use of the same considerations that lead to (3.10), but taking (3.25) for ρ and neglecting the exponential term in ψ, results in

$$G^2(\psi_{sb}) = \frac{2u_T^{\,2}}{l_B^2}\left[F_{phf}\left(\frac{\psi_{sb}}{u_T}\right) - 1\right] (d.a) \tag{3.26}$$

Combination of (3.19) and (3.22) gives

$$C'_b\left(\psi_{sf} - \psi_{sb}\right) = \varepsilon_{si}\mathsf{E}_{sb(d.a)} - \frac{Q'_b}{2} \tag{3.27}$$

and use of the previous expressions for C'_b and Q'_b results in

$$\mathsf{E}_{sb(d.a)} = \frac{\left(\psi_{sf} - \psi_{sb}\right)}{t_b} - \frac{u_T}{2l_B^2}.t_b \tag{3.28}$$

Using (3.26) and (3.28) in (3.23), $\alpha_{fb(d.a)}$ can be expressed as

$$\alpha_{fb(d.a)} = \frac{2u_T^{\,2}}{l_B^2}\left[\left(\frac{\psi_{sf} - \psi_{sb}}{2u_T C} - \frac{C}{2}\right)^2 - \left(F_{phf}\left(\frac{\psi_{sb}}{u_T}\right) - 1\right)\right] \tag{3.29}$$

where $C \equiv \dfrac{t_b}{\sqrt{2}.l_B}$

The surface potentials ψ_{sf} and ψ_{sb}, required to calculate the drain current and the terminal charges of the structure of Figure 3.1, can be found solving (3.24), using (3.10), (3.14) and (3.29). This procedure of finding the surface potentials was implemented using a newton-raphson method in a matlab routine.

3.1.2 Model Formulation (Long-Channel)

3.1.2.1 Basic Equations

The charge sheet model (Brews, 1978), which assumes that the inversion layer is an infinitesimally thick layer at the interface between the gate oxide and silicon, leads to the approximation of the front and back-channel charge densities per unit area, Q'_{if} and Q'_{ib}, respectively. Thus

$$Q'_{if} = \varepsilon_{si}\mathsf{E}_{sf(d.a)} - \varepsilon_{si}\mathsf{E}_{sf}$$
$$Q'_{ib} = \varepsilon_{si}\mathsf{E}_{sb} - \varepsilon_{si}\mathsf{E}_{sb(d.a)} \tag{3.30}$$

This last approximation avoids the numerical solution of the integrals

$$Q'_{if} = -\int_{\psi_m}^{\psi_{sf}} \frac{q(n-n_o)}{\mathsf{E}} d\psi$$
$$Q'_{ib} = \int_{\psi_m}^{\psi_{sb}} \frac{q(n-n_o)}{\mathsf{E}} d\psi \tag{3.31}$$

where ψ_m is the minimum potential in the thin-film.

Use of (3.30) in (3.14) gives

$$V_{gf} = \psi_{sf} + \frac{\varepsilon_{si}\mathsf{E}_{sf(d.a)}}{C'_{of}} - \frac{Q'_{if}}{C'_{of}}$$
$$V_{gb} = \psi_{sb} - \frac{\varepsilon_{si}\mathsf{E}_{sb(d.a)}}{C'_{ob}} - \frac{Q'_{ib}}{C'_{ob}} \tag{3.32}$$

In the last equations, E_{sf} and E_{sb} can be replaced by the expressions derived from the depletion approximation analysis. Thus use of (3.22) and (3.27) in (3.32), results in

$$V_{gf} = \left(1 + \frac{C'_b}{C'_{of}}\right)\psi_{sf} - \frac{C'_b}{C'_{of}}\psi_{sb} - \frac{\left(\frac{Q'_b}{2} + Q'_{if}\right)}{C'_{of}}$$
$$V_{gb} = \left(1 + \frac{C'_b}{C'_{ob}}\right)\psi_{sb} - \frac{C'_b}{C'_{ob}}\psi_{sf} - \frac{\left(\frac{Q'_b}{2} + Q'_{ib}\right)}{C'_{ob}} \tag{3.33}$$

Expressions for Q'_{if} and Q'_{ib}, normalized to C'_{of} and C'_{ob}, respectively, can be found rearranging the terms of the last two equations. Thus

$$\frac{Q'_{if}}{C'_{of}} = -\left[V_{gf} + \frac{Q'_b}{2C'_{of}} - \left(1 + \frac{C'_b}{C'_{of}} \right) \psi_{sf} + \frac{C'_b}{C_{of}} \psi_{sb} \right]$$
$$\frac{Q'_{ib}}{C'_{ob}} = -\left[V_{gb} + \frac{Q'_b}{2C'_{ob}} - \left(1 + \frac{C'_b}{C'_{ob}} \right) \psi_{sb} + \frac{C'_b}{C'_{ob}} \psi_{sf} \right] \quad (3.34)$$

The previous assumption that the back-channel remains in depletion from source to drain implies that $Q_{ib} = 0$. Use of this condition in (3.34) results in an expression that gives the relation between ψ_{sb} and ψ_{sf}:

$$\psi_{sb} = Kl \frac{C'_{ob}}{C'_b} \left[V_{gb} + \frac{Q'_b}{2C'_{ob}} + \frac{C'_b}{C'_{ob}} \psi_{sf} \right] \quad (3.35)$$

where $Kl \equiv \dfrac{C'_b}{C'_b + C'_{ob}}$

This last expression (3.35) can be used to rewrite (3.34) that takes the simple form

$$\frac{Q'_{if}}{C'_{of}} = -\left[XG - K\psi_{sf} \right] \quad (3.36)$$

where $XG \equiv \left[V_{gf} + \dfrac{Q'_b}{2C'_{of}} + \dfrac{C'_{bb}}{C'_{of}} \left(V_{gb} + \dfrac{Q'_b}{2C'_{ob}} \right) \right]$ $C'_{bb} \equiv \dfrac{C'_b C'_{ob}}{C'_b + C'_{ob}}$ and $K \equiv \left(1 + \dfrac{C'_{bb}}{C'_{of}} \right)$

3.1.2.2 Current Equations

In Section 3.1.1.1 a four-terminal SOI nMOSFET structure, shown in Figure 3.1, was used as a reference to evaluate the Poisson's equation inside the silicon thin-film. Now, the same basic structure is shown in Figure 3.4 as a reference to find the current in the channel, where x_i represents an arbitrary position in the channel and L is the effective channel length. Also as a reference, an infinitesimally thick inversion layer that represents the channel shown in Figure 3.4 is depicted in Figure 3.5.

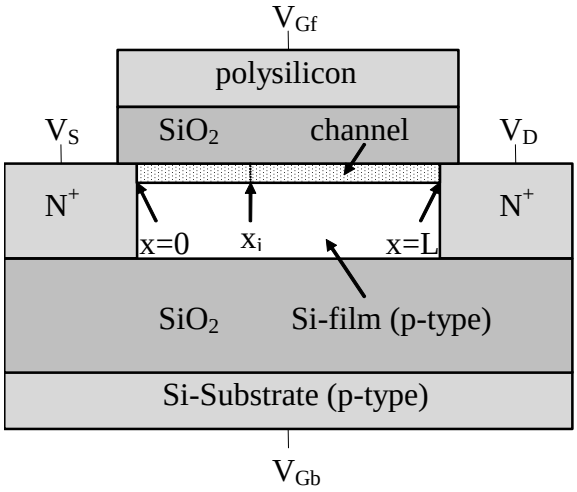


Figure 3.4: A simplified four-terminal SOI nMOSFET structure.

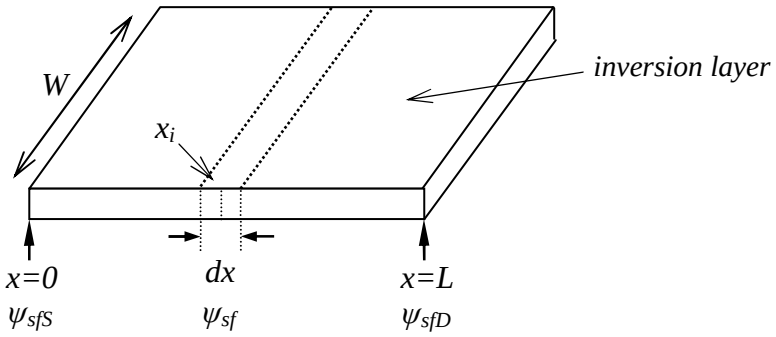


Figure 3.5: Infinitesimally thick inversion layer that represents the channel (Figure 3.4).

Taking Figure 3.5 as a reference, the current in the inversion layer (front-channel in this case) can be expressed as a sum of two components (Tsividis, 1987): *drift* and *diffusion*. The term due to drift is proportional to the longitudinal electric field in the layer, i.e., the derivative of ψ_{sf} in the *x*-direction, and the term due to diffusion is proportional to the derivative of Q'_{if} in the *x*-direction in the layer. Thus, an expression for the total current I_{DS} in the inversion layer can be written as

$$I_{DS} = \mu(x) C'_{of} W \left[-\left(\frac{Q'_{if}}{C'_{of}} \right) \frac{d\psi_{sf}}{dx} + u_T \frac{d\left(\frac{Q'_{if}}{C'_{of}} \right)}{dx} \right] \tag{3.37}$$

that can be rewritten as

$$\frac{I_{DS}}{\mu(x)C'_{of}\,W}dx=\left[-\left(\frac{Q'_{if}}{C'_{of}}\right)d\psi_{sf}+u_T d\left(\frac{Q'_{if}}{C'_{of}}\right)\right] \tag{3.38}$$

where dx represents one infinitesimally thick portion of the inversion layer in the position x_i (Figure 3.5); W is the effective channel width (Figure 3.5); $\mu(x)$ is the semiconductor mobility function of x; and u_T is the thermal voltage.

Use of (3.36) in (3.38) gives

$$\frac{I_{DS}}{\mu(x)C'_{of}\,W}dx=\left[XGT-K\psi_{sf}\right]d\psi_{sf} \tag{3.39}$$

where $XGT\equiv XG+u_T K$

Defining $\beta_o\equiv\mu_o C'_{of}\frac{W}{L}$, where μ_o is the low-field mobility, equation (3.39) can be rewritten as

$$\frac{I_{DS}}{\beta_o}\left(\frac{\mu_o}{\mu(x)}\right)\frac{dx}{L}=\left[XGT-K\psi_{sf}\right]d\psi_{sf} \tag{3.40}$$

For now it is assumed that $\mu(x)$ is constant along the channel and equal to μ_o. In the Section 3.1.4.3 it will be considered the problem of mobility degradation. Thus, equation (3.40) turns into

$$\frac{I_{DS}}{\beta_o}\frac{dx}{L}=\left[XGT-K\psi_{sf}\right]d\psi_{sf} \tag{3.41}$$

The normalized total current I_{DS}/β_o can be found integrating on both sides of (3.41), from $x=0$ to $x=L$. Thus

$$\frac{I_{DS}}{\beta_o}=\left[XGT\psi_{sf}-\frac{1}{2}K\psi_{sf}^2\right]_{\psi_{sfS}}^{\psi_{sfD}} \tag{3.42}$$

where ψ_{sfS} and ψ_{sfD} are the front-gate surface potentials at the source and drain levels in the channel, respectively.

It is useful for the next derivations to find expressions for dx and for the normalized distance along the channel x/L.

For *dx*, equation (3.41) can be simply rewritten, resulting in

$$dx = \frac{L}{\left(\frac{I_{DS}}{\beta_o}\right)}\left[XGT - K\psi_{sf}\right]d\psi_{sf} \tag{3.43}$$

For the normalized distance *x/L*, integration on both sides of (3.43), from *x=0* to x_i (Figure 3.5) and rearrange the terms, gives

$$\frac{x}{L} = \frac{1}{\left(\frac{I_{DS}}{\beta_o}\right)}\left[XGT\psi_{sf} - \frac{1}{2}K\psi_{sf}^2 - XS\right] \tag{3.44}$$

where $XS \equiv \left[XGT\psi_{sfS} - \frac{1}{2}K\psi_{sfS}^2\right]$

The expression (3.42) can be used directly to find the normalized total current if ψ_{sf} is evaluated first. A numerical method to find ψ_{sf} was outlined in the Section 3.1.1.3. Equations (3.43) and (3.44) will be used to derive the total charge expressions of the model.

3.1.2.3 Charge Equations

The total charge equations, associated to the terminals of the structure of Figure 3.4, can be found taking integrals of charge densities from source to drain. Thus for the front-channel total charge Q_{if}, front and back-gate total charges, Q_{Gf} and Q_{Gb}, respectively, the following integrals can be written

$$Q_{if} = -C'_{of}\,W\int_0^L\left(\frac{Q'_{if}}{C'_{of}}\right)dx \tag{3.45}$$

$$Q_{Gf} = C'_{of}\,W\int_0^L\left(\frac{Q'_{gf}}{C'_{of}}\right)dx \tag{3.46}$$

$$Q_{Gb} = C'_{ob}\,W\int_0^L\left(\frac{Q'_{gb}}{C'_{ob}}\right)dx \tag{3.47}$$

Use of (3.36) and (3.43) in (3.45) gives a normalized expression for Q_{if} as follows.

$$\frac{Q_{if}}{C'_{of}\,WL}=\frac{-1}{\left(\frac{I_{DS}}{\beta_o}\right)}\left[XG.XGT\psi_{sf}-\frac{1}{2}K\left(XG+XGT\right)\psi_{sf}^{2}+\frac{1}{3}K^{2}\psi_{sf}^{3}\right]_{\psi_{sfS}}^{\psi_{sfD}} \tag{3.48}$$

The potential drops across the front and back-gate oxides, ψ_{of} and ψ_{ob}, respectively (Figure 3.3), can be identified with the front and back-gate normalized charge densities per unit area, Q'_{gf} and Q'_{gb} normalized to C'_{of} and C'_{ob}, respectively. Thus use of (3.12) gives

$$\frac{Q'_{gf}}{C'_{of}}=\psi_{of}=V_{gmf}-\psi_{sf} \tag{3.49}$$

$$\frac{Q'_{gb}}{C'_{ob}}=\psi_{ob}=V_{gmb}-\psi_{sb} \tag{3.50}$$

where $V_{gmf}\equiv V_{Gf}-\phi_{msf}$ and $V_{gmb}\equiv V_{Gb}-\phi_{msb}$

Use of (3.43) and (3.49) in (3.46), and (3.35), (3.43) and (3.50) in (3.47), results in normalized expressions for Q_{Gf} and Q_{Gb}.

$$\frac{Q_{Gf}}{C'_{of}\,WL}=\frac{1}{\left(\frac{I_{DS}}{\beta_o}\right)}\left[V_{gmf}.XGT\psi_{sf}-\frac{1}{2}\left(K.V_{gmf}+XGT\right)\psi_{sf}^{2}+\frac{1}{3}K\psi_{sf}^{3}\right]_{\psi_{sfS}}^{\psi_{sfD}} \tag{3.51}$$

$$\frac{Q_{Gb}}{C'_{of}\,WL}=\frac{\left(\frac{C'_{ob}}{C'_{of}}\right)}{\left(\frac{I_{DS}}{\beta_o}\right)}\left[XGB.XGT\psi_{sf}-\frac{1}{2}\left(K.XGB+Kl.XGT\right)\psi_{sf}^{2}+\frac{1}{3}K.Kl\,\psi_{sf}^{3}\right]_{\psi_{sfS}}^{\psi_{sfD}} \tag{3.52}$$

where $XGB\equiv\left[V_{gmb}-Kl\frac{C'_{ob}}{C'_{b}}\left(V_{gb}+\frac{Q'_{b}}{2C'_{ob}}\right)\right]$

The charge balance and the neutrality condition can be used to find a normalized expression for the thin-film total charge Q_b. Thus

$$\frac{Q_b}{C'_{of}\,WL}=-\frac{Q_{if}}{C'_{of}\,WL}-\frac{Q_{Gf}}{C'_{of}\,WL}-\frac{Q'_{of}}{C'_{of}}-\frac{Q_{Gb}}{C'_{of}\,WL}-\frac{Q'_{ob}}{C'_{of}} \tag{3.53}$$

The source and drain total charges, Q_{Sf} and Q_{Df}, respectively, are representative partitions of Q_{If}. In the case the mobility is spacially dependent, such a partition is not obvious. In this work it is used a common partition scheme (Tsividis, 1987; Park, 1991; Veeraraghavan, 1988) and thus the following expressions can be written for Q_{Sf} and Q_{Df}:

$$Q_{Df} = -C'_{of} W \int_0^L \frac{x}{L}\left(\frac{Q'_{if}}{C'_{of}}\right)dx \tag{3.54}$$

$$Q_{Sf} = -C'_{of} W \int_0^L \left(1-\frac{x}{L}\right)\left(\frac{Q'_{if}}{C'_{of}}\right)dx \tag{3.55}$$

Use of (3.36), (3.43) and (3.44) in (3.54), gives a final normalized expression for Q_{Df}:

$$\frac{Q_{Df}}{C'_{of} WL} = \frac{-1}{\left(\frac{I_{DS}}{\beta_o}\right)^2}\left[\begin{array}{l}[\,XS.XG.XGT\,]\psi_{sf} + \frac{1}{2}\left[XG.XGT^2 - K.XS\left(XG+XGT\right)\right]\psi_{sf}^2 \\ +\frac{1}{3}\left[K^2 XS - \frac{1}{2}K.XG.XGT - K.XGT\left(XG+XGT\right)\right]\psi_{sf}^3 \\ +\frac{1}{4}\left[K^2 XGT + \frac{1}{2}K^2\left(XG+XGT\right)\right]\psi_{sf}^4 - \frac{1}{10}\left[K^3\right]\psi_{sf}^5\end{array}\right]_{\psi_{sfS}}^{\psi_{sfD}} \tag{3.56}$$

To avoid the solution of the integral of (3.55) that gives Q_{Sf}, an expression that take into account the charge conservation can be used. Thus, a normalized expression for Q_{Sf} can be written as

$$\frac{Q_{Sf}}{C'_{of} WL} = \frac{Q_{if}}{C'_{of} WL} - \frac{Q_{Df}}{C'_{of} WL} \tag{3.57}$$

3.1.3 High-Frequency Small-Signal Model

In the last section the current and charge equations of a charge-sheet model for the intrinsic SOI MOSFET were developed. These equations can be used to find the parameters of a complete high-frequency small-signal quasi-static model, i.e., transconductances and capacitances.

3.1.3.1 Transconductances and Capacitances

To clarify the analysis Figure 3.6 shows an NMOS transistor with terminal voltages, i.e., a DC voltage source plus a time-varying small signal voltage source. A complete quasi-static model requires that the transconductance and capacitance effect of each terminal be considered.

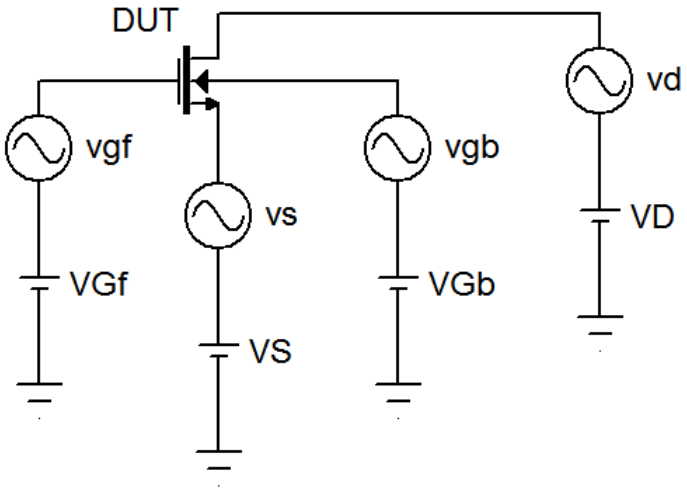


Figure 3.6: Schematic view of a NMOS transistor (DUT) with terminal voltages indicated (DC voltage source plus a time-varying small signal voltage source).

First, considering the transport of charges in the MOSFET channel, four transconductances can be define: g_{mG}, g_{mD}, g_{mS} and g_{mB}, which represent the partial derivative of the drain current I_D with respect to each terminal voltage V_{Gf}, V_D, V_S, and V_{Gb}, respectively, and can mathematically be expressed by

$$g_{mk} = +\frac{\partial I_D}{\partial V_k} \tag{3.58}$$

where $g_{mk}=\{g_{mG}, g_{mD}, g_{mS}, g_{mB}\}$ and $V_k=\{V_{Gf}, V_D, V_S, V_{Gb}\}$. Three of these transconductances are independents and the other can be omitted, i.e., $g_{mG} + g_{mD} + g_{mS} + g_{mB} = 0$.

Second, considering the variation of charges Q_{Gf}, Q_D, Q_S, and Q_{Gb} with respect to each terminal voltage V_{Gf}, V_D, V_S, and V_{Gb}, sixteen capacitances can be define or, in the strict sense, transcapacitances. These capacitances can mathematically be expressed by

$$C_{kk} = +\frac{\partial Q_k}{\partial V_k}$$
$$C_{kl} = -\frac{\partial Q_k}{\partial V_l}, l \neq k \tag{3.59}$$

where $Q_k=\{Q_{Gf}, Q_D, Q_S, Q_{Gb}\}$ and $V_l,V_k=\{V_{Gf}, V_D, V_S, V_{Gb}\}$. Nine of these transcapacitances are independents and the other three can be omitted, i.e., $C_{GG} - C_{GD} - C_{GS} - C_{GB} = 0$, and so on.

3.1.3.2 A General y-Parameter Model

Now a complete high-frequency small-signal quasi-static model can be define using the y-parameters. The compact matrix representation is used to simplify the expressions. Then the small-signal terminal currents i_{Gf}, i_D, i_S, and i_{Gb}, in terms of the small-signal terminal voltages v_{Gf}, v_D, v_S, and v_{Gb}, are expressed by

$$\begin{bmatrix} i_{Gf} \\ i_D \\ i_S \\ i_{Gb} \end{bmatrix} = \begin{bmatrix} y_{GG} & y_{GD} & y_{GS} & y_{GB} \\ y_{DG} & y_{DD} & y_{DS} & y_{DB} \\ y_{SG} & y_{SD} & y_{SS} & y_{SB} \\ y_{BG} & y_{BD} & y_{BS} & y_{BB} \end{bmatrix} \times \begin{bmatrix} v_{Gf} \\ v_D \\ v_S \\ v_{Gb} \end{bmatrix} \tag{3.60}$$

or using the transconductances and transcapacitances, results in

$$\begin{bmatrix} i_{Gf} \\ i_D \\ i_S \\ i_{Gb} \end{bmatrix} = \left[\begin{bmatrix} 0 & 0 & 0 & 0 \\ +g_{mG} & +g_{mD} & +g_{mS} & +g_{mB} \\ -g_{mG} & -g_{mD} & -g_{mS} & -g_{mB} \\ 0 & 0 & 0 & 0 \end{bmatrix} + j.\omega. \begin{bmatrix} +C_{GG} & -C_{GD} & -C_{GS} & -C_{GB} \\ -C_{DG} & +C_{DD} & -C_{DS} & -C_{DB} \\ -C_{SG} & -C_{SD} & +C_{SS} & -C_{SB} \\ -C_{BG} & -C_{BD} & -C_{BS} & +C_{BB} \end{bmatrix} \right] \times \begin{bmatrix} v_{Gf} \\ v_D \\ v_S \\ v_{Gb} \end{bmatrix} \tag{3.61}$$

From the y-parameter definitions of (3.60) and (3.61) a small-signal equivalent circuit of three or two ports can be found. Using the substrate terminal - the back-gate terminal V_{Gb} in the SOI case - as the reference, only nine (independents) small-signal parameters are necessary. Then a general three-port y-parameter model can be defined and is shown in Figure 3.7. This model will be used in the analysis of the next section.

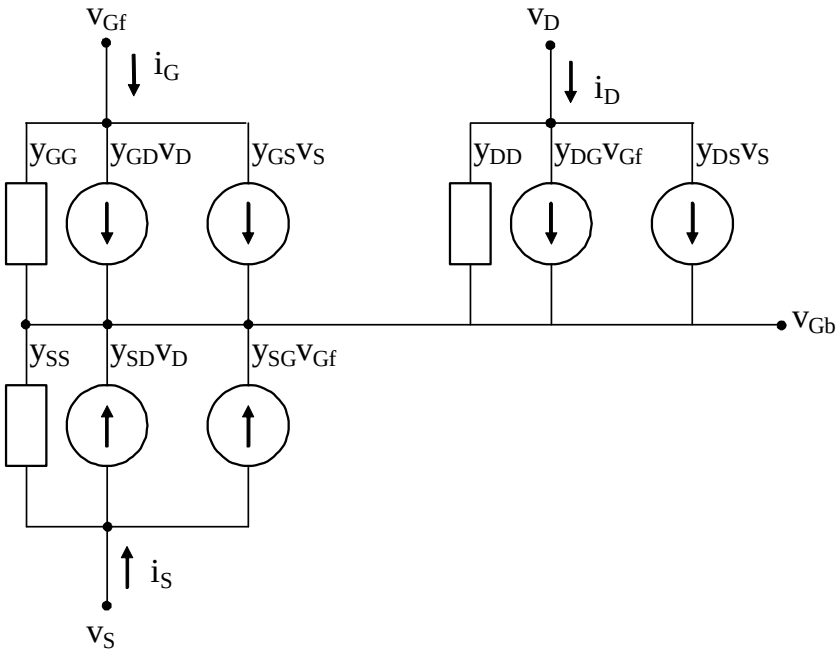


Figure 3.7: A general three-port y-parameter model with the substrate terminal (the back-gate terminal V_{Gb} in the SOI case) used as the reference.

3.1.3.3 Experimental Results

To verify the accuracy of the model simulated results were compared to measurements on SOI NMOS transistors and a good agreement between experimental and simulated data was verified.

The data was measured for SOI-MOSFETs with the following structural parameters (see Figure 3.3):

t_{of} = 30 nm

t_b or t_{si} = 80 nm

t_{ob} = 400 nm

The DC, AC, and high frequency measurements were carried out by the staff of the Microelectronics and Microwave Laboratories of UCL University , Belgium.

Figure 3.8 shows a plot of the transconductance over the drain current g_m/I_D versus the normalized drain current I_D/β_o, for a L_G = 3 µm (W/L = 30) SOI NMOS transistor in the saturation region (V_D = 2.5 V), and Figure 3.9 shows a plot of small-signal capacitances C_{GD} and C_{GS} versus the front-gate voltage V_{Gf} for a L_G = 20 µm (W/L = 1) edgeless SOI NMOS transistor, and for different values of drain-voltage (V_D = 0.05, 1.05, 2.05, and 3.05 V).

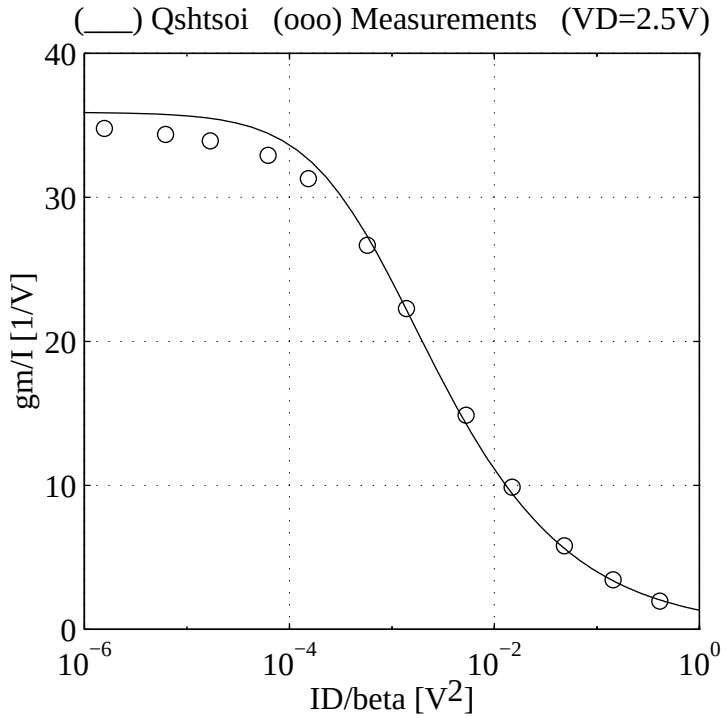


Figure 3.8: Transconductance over the drain current g_m/I_D versus the normalized drain current I_D/β_o of a SOI NMOS transistor (L_G = 3 µm, W/L = 30).

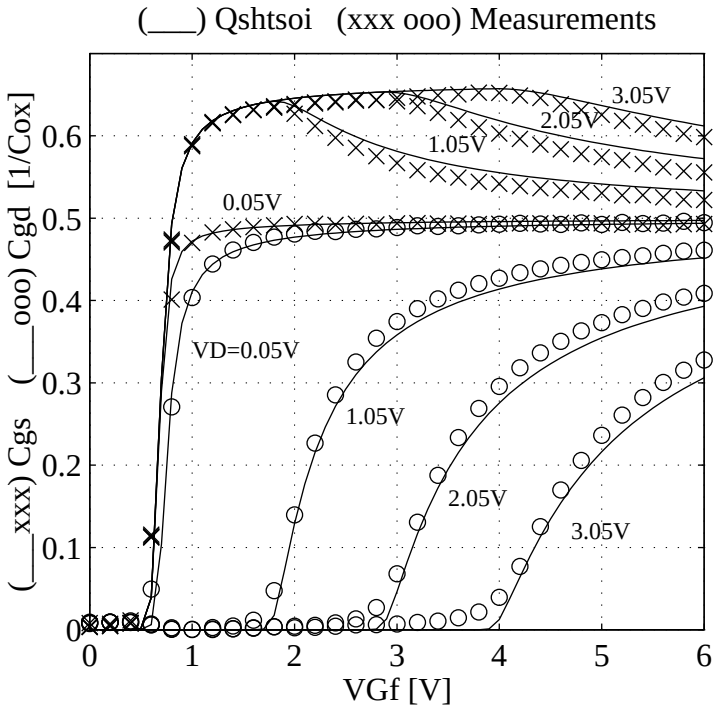


Figure 3.9: Small-signal capacitances C_{GD} and C_{GS} versus the front-gate voltage V_{Gf} of an edgeless SOI NMOS transistor for different values of drain-voltage V_D (L_G = 20 µm, W/L = 1).

3.1.4 Second-Order Effects

To improve the model some important second-order effects were introduced. These effects are: drain-Induced conductivity enhancement (DICE), channel-length modulation, mobility degradation and velocity saturation.

3.1.4.1 Drain-Induced Conductivity Enhancement Effect

The SOI MOSFET is affected by the Drain Induced Conductivity Enhancement (DICE) effect due to charge sharing between the gate and the junctions, similarly to the Drain Induced Barrier Lowering (DIBL) effect in the standard bulk technology. This effect has been included in the SOI charge sheet model by means of a coefficient that multiplies the thin-film total charge Q_b. It increases the output conductance g_d in the saturation region, but it is less important than channel length modulation.

3.1.4.2 Channel-Length Modulation

The channel-length modulation has also been included in the model for the accuracy, but it is not so important to simulate the SOI MOSFET in saturation. As the DICE (DIBL) effect it causes a non-zero value of g_d in the saturation region. It has been included by means of a modulated effective channel length $L_{eff} = L - L_d$, L_d being called modulation channel parameter and calculated as a function of $V_{DSeff} = (\psi_{sfD} - \psi_{sfS})$, V_D, μ_{eff}, v_{sat} and geometric factors. For the reason mentioned before, neither DICE (DIBL) nor channel-length modulation effects have been used in the simulations and analysis of the high-frequency behavior of the SOI MOSFET with the output conductance g_d in the saturation region being included as an extrinsic parameter by means of the early-voltage V_A.

3.1.4.3 Mobility Degradation and Velocity Saturation

The normal component of the electric field E_y in the inversion layer degrades the mobility in the transistor channel. A common approach to model this effect is to define an effective mobitilty μ_{eff} (Tsividis, 1987), i.e., a low-lateral field mobility that is affected by E_y. The following relation has been used to take into account the dependence of mobility on normal fields (Veeraraghavan, 1988).

$$\mu_{eff} = \frac{\mu_o}{1 + \frac{E_{yeff}}{E_c}} \tag{3.62}$$

where E_{yeff} is an average of E_y on the front-gate inversion layer surface, using the electric fields at source and drain, E_{sfS} and E_{sfD} respectively; and E_c is a fitting parameter.

When the channel length decreases and the lateral electric field E_x increases the assumption that the carrier velocity varies linearly with the E_x may be no longer valid. With the increase of E_x, the carrier velocity tends to reach a saturation value, called

saturation velocity v_{sat}, following a non-linear relation that implies in the reduction of the mobility. This phenomenon is called velocity saturation effect.

To take into account the effects of lateral electric field, it is used a mobility expression (Tsividis, 1987) that also includes the degradation by normal electric field expressed in the previous equation. This expression is

$$\mu(x) = \frac{\mu_{eff}}{1 + \left(\frac{\mu_{eff}}{v_{sat}}\right)\frac{d\psi_{sf}}{dx}} \tag{3.63}$$

where $\frac{d\psi_{sf}}{dx}$ represents the lateral electric field E_x or E_{sfx}.

Figure 3.10 shows the dependence of carrier velocity v_c on longitudinal (lateral) electric field E_x for three different vales of normal (vertical) electric field E_y. The curves saturate at a value called saturation velocity v_{sat}.

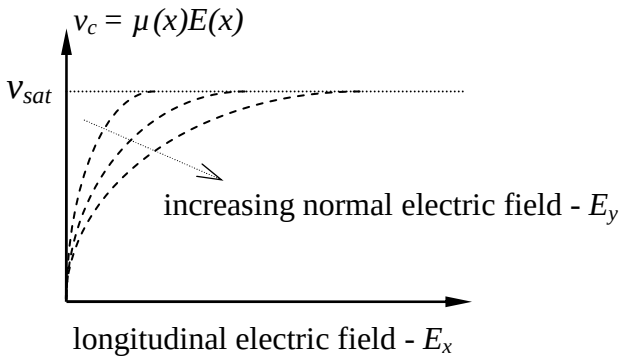


Figure 3.10: Carrier velocity v_c versus longitudinal (lateral) electric field E_x for three different vales of normal (vertical) electric field E_y. The curves saturate at a value called saturation velocity v_{sat}.

Now it can be assumed that μ varies along the channel and (3.63) can be used in the current and charge equations of Section 3.1.2.2 to include mobility reduction effects.

Thus the use of (3.63) in (3.40) gives

$$\frac{I_{DSeff}}{\beta_o}\left(\frac{\mu_o}{\mu_{eff}}\right)\left[1 + \left(\frac{\mu_{eff}}{v_{sat}}\right)\frac{d\psi_{sf}}{dx}\right]\frac{dx}{L} = \left[XGT - K\psi_{sf}\right]d\psi_{sf} \tag{3.64}$$

where I_{DSeff} is the total current that includes second order effects. The integration of both sides of (3.64) from source to drain and the relocation of terms finally gives

$$\frac{I_{DSeff}}{\beta_o} = \frac{\left(\frac{\mu_{eff}}{\mu_o}\right)\left[XGT\psi_{sf} - \frac{1}{2}K\psi_{sf}^2\right]_{\psi_{sfS}}^{\psi_{sfD}}}{\left[1+\left(\frac{\mu_{eff}}{v_{sat}L}\right)\Delta\psi_{sfDS}\right]} \tag{3.65}$$

where $\Delta\psi_{sfDS} \equiv \left(\psi_{sfD} - \psi_{sfS}\right)$

The term in the brackets in the numerator of (3.65) can be identified as the normalized total current of (3.42). Thus, it can be written for the normalized total current a simplify expression that is simply the total current without second-order effects multiplied by a factor that includes such effects, i.e.

$$\frac{I_{DSeff}}{\beta_o} = \left(\frac{F_{eff}}{F_{sat}}\right)\frac{I_{DS}}{\beta_o} \tag{3.66}$$

where $F_{eff} \equiv \left(\frac{\mu_{eff}}{\mu_o}\right)$ is a factor to include the mobility degradation by normal fields; and $F_{sat} \equiv \left[1+\left(\frac{\mu_{eff}}{v_{sat}L}\right)\Delta\psi_{sfDS}\right]$ is a factor to include the velocity saturation effect.

The expressions for dx and x/L can be found in the same manner as in Section 3.1.2.2. For dx, (3.64) can be rewritten as

$$dx = F_{eff}\frac{L}{\left(\frac{I_{DSeff}}{\beta_o}\right)}\left[XGTl - K\psi_{sf}\right]d\psi_{sf} \tag{3.67}$$

where $XGTl \equiv XGT - \left(\frac{\mu_o}{v_{sat}L}\right)\frac{I_{DSeff}}{\beta_o}$

The integration on both sides of (3.67) from source to some point x_i in the inversion layer (Figure 3.5), results in an expression for x/L:

$$\frac{x}{L} = F_{eff}\frac{1}{\left(\frac{I_{DSeff}}{\beta_o}\right)}\left[XGTl\psi_{sf} - \frac{1}{2}K\psi_{sf}^2 - XSl\right] \tag{3.68}$$

where XSl can be defined as $XSl \equiv \left[XGTl\psi_{sfS} - \frac{1}{2}K\psi_{sfS}^2\right]$

The equations (3.67) and (3.68) are more general expressions for dx and x/L that include second-order effects, while equations (3.43) and (3.44) are particular expressions when mobility degradation and velocity saturation can be neglected.

The effect of velocity saturation is clearly noted on the saturation current I_{DSsat}, reducing its value. As a result a V_{DSsat}, i.e., a V_{DS} where the drain current reaches its maximum, can be derived as follows.

First , (3.64) is rewritten as

$$\frac{I_{DSeff}}{\beta_o} = \frac{L}{\mu_o}\mu(x)\frac{d\psi_{sf}}{dx}\left[XGT - K\psi_{sf}\right] \qquad \text{and}$$

$$\frac{I_{DSeff}}{\beta_o} = \frac{L}{\mu_o}v(x)\left[XGTS - K\Delta\psi_{sf}\right] \tag{3.69}$$

where $v(x) = \mu(x)\dfrac{d\psi_{sf}}{dx}$ $\qquad XGTS \equiv \left(XGT - K\psi_{sfS}\right)$ $\qquad$ and $\qquad \Delta\psi_{sf} \equiv \left(\psi_{sf} - \psi_{sfS}\right)$

The equation (3.69) expresses the normalized total drain current resulting directly from the considerations of *drift* and *diffusion* components of the current in the inversion layer. It is equivalent to (3.65) but uses the carrier velocity as a parameter. This equivalence can be used to find V_{DSsat}. Thus considering v(x) = v(L) and $\Delta\psi_{sf} = \Delta\psi_{sfDS}$ at the end of the channel (x=L in Figure 3.5), equations (3.65) and (3.69) can be rewritten as

$$\frac{I_{DSeff}}{\beta_o} = \frac{\left(\dfrac{\mu_{eff}}{\mu_o}\right)\left[XGTS\Delta\psi_{sfDS} - \dfrac{1}{2}K\Delta\psi_{sfDS}^2\right]}{\left[1 + \left(\dfrac{\mu_{eff}}{v_{sat}L}\right)\Delta\psi_{sfDS}\right]} \tag{3.70}$$

$$\frac{I_{DSeff}}{\beta_o} = \frac{L}{\mu_o}v(L)\left[XGTS - K\Delta\psi_{sfDS}\right] \tag{3.71}$$

The last two equations can be equalized and the resultant expression solved to $\Delta\psi_{sfDS}$. When the drain current saturates, the carrier velocity reaches its saturation value v_{sat} at the end of the channel and also $\Delta\psi_{sfDS}$ reaches its maximum and can be identified to V_{DSsat}, i.e., v(L) = v_{sat} and $\Delta\psi_{sfDS}$ = V_{DSsat}.

Thus

$$V_{DSsat} = -\left(\frac{v_{sat}L}{\mu_{eff}}\right) + \sqrt{\left(\frac{v_{sat}L}{\mu_{eff}}\right)^2 + 2\frac{XGTS}{K}\left(\frac{v_{sat}L}{\mu_{eff}}\right)} \tag{3.72}$$

When mobility degradation and velocity saturation can be neglected the last equation simplifies to

$$V_{DSsat} = \frac{XGTS}{K} = \frac{XG - K\psi_{sfS}}{K} + u_T = \frac{V_{Gf} - V_{TS}}{K} + u_T \tag{3.73}$$

where V_{TS} is the threshold voltage at the source level.

Figure 3.11 shows the velocity saturation effect on the drain current I_D, greatly reducing its value and the saturation voltage V_{DSsat}. It is observed a *"bump"* for values of V_D greater than V_{DSsat}. It is an undesirable effect that finds explanation on the manner by which the front-gate surface potential ψ_{sf} is evaluated. In Figure 3.11 is also plotted ψ_{sf} as a reference and to stress that I_D saturates when ψ_{sf} saturates. The introduction of the velocity saturation effect reduces V_{Dssat} (when the carrier velocity tends to v_{sat}), but ψ_{sf} continues to grow and saturates a little further (when Q_{if} tends to zero) causing the "bump" in I_D. A simple solution will be consider $I_D = I_{Dsat}$ from V_{DSsat} and beyond, clamping the current, but it results in a discontinuity in the curve. The solution implemented in the model and that preserves its continuity is: an effective V_{Gf} voltage V_{Gfeff} is used to evaluate ψ_{sf} generating an effective ψ_{sf} or ψ_{sfeff} that saturates when V_D reaches V_{Dsat}, solving the problem.

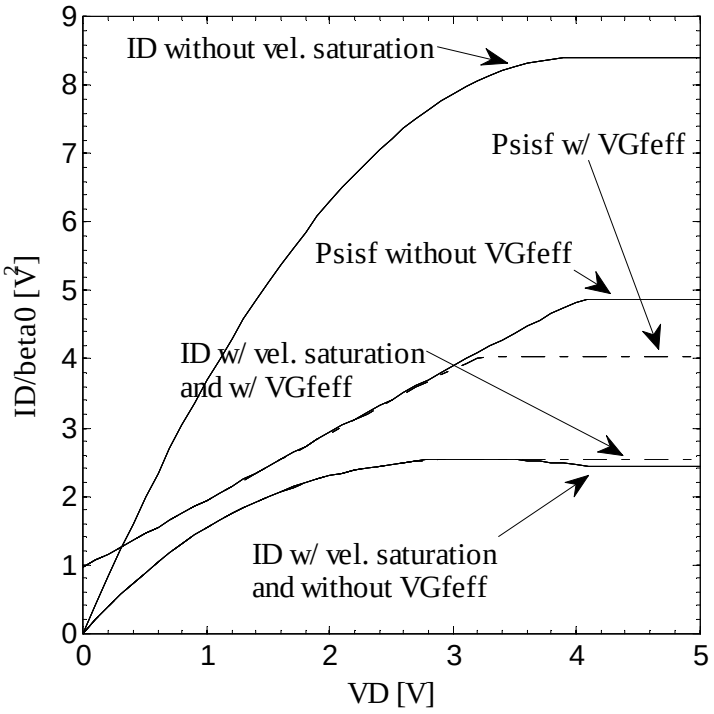


Figure 3.11: The velocity saturation effect on the drain current (L_G = 1 µm).

To demonstrate the effect of velocity saturation on the small-signal capacitances Figure 3.12 and Figure 3.13 show plots with normalized capacitances C_{GG}, C_{GD}, C_{GS}, C_{DD}, and C_{DG} versus V_{Gf} and V_D, respectively, and for a L_G = 1 µm SOI NMOS transistor. These capacitances were chosen because they are useful in a two-port small-signal lumped model. Solid lines represent the model virtually without velocity saturation effect, setting the parameter v_{sat}=1x10^{12} cm/s; dashed lines represent the model with a finite parameter v_{sat}=1x10^{7} cm/s. It can be seen a great influence of this effect on the drain saturation voltage V_{Dssat} and producing a different distribution of charge in the linear and saturate zones.

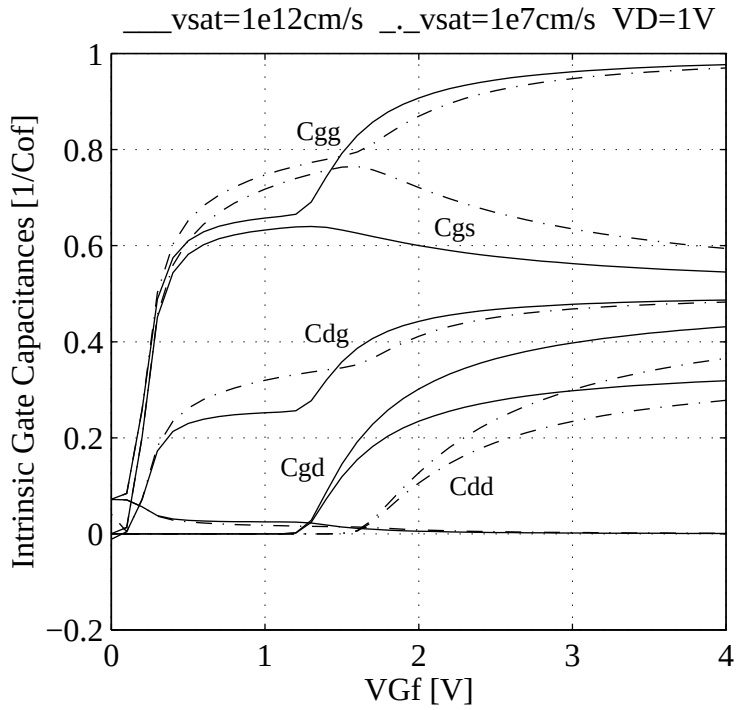


Figure 3.12: Normalized small-signal capacitances C_{GG}, C_{GD}, C_{GS}, C_{DD}, and C_{DG} versus V_{Gf} for an SOI NMOS transistor with two different values of v_{sat} (L_G = 1 µm).

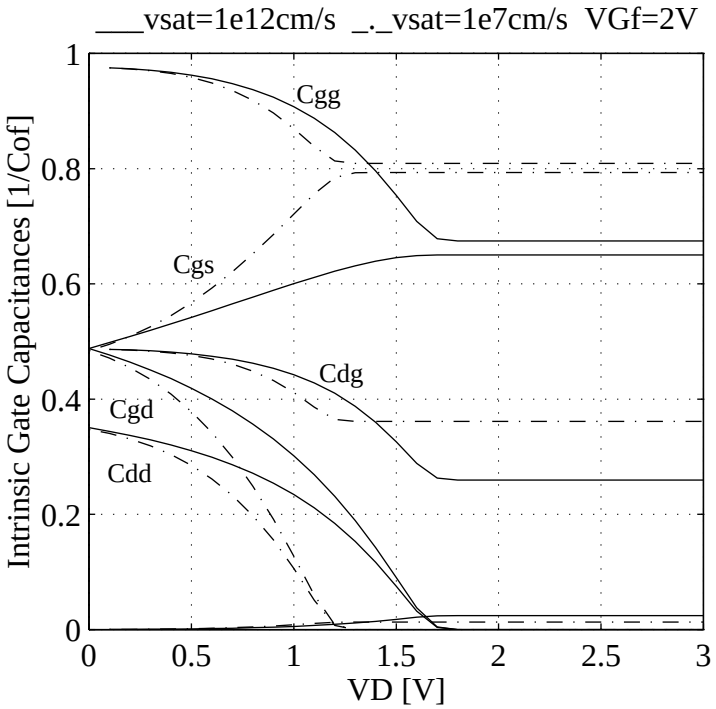


Figure 3.13: Normalized small-signal capacitances C_{GG}, C_{GD}, C_{GS}, C_{DD}, and C_{DG} versus V_D for an SOI NMOS transistor with two different values of v_{sat} (L_G = 1 µm).

3.1.4.4 Experimental Results

Figure 3.14 and Figure 3.15 show the normalized drain current I_D/β_o versus V_{Gf} and V_D, respectively, and for a L_G = 1 µm SOI NMOS transistor. Model and measurements are compared in terms of velocity saturation and mobility reduction effects. It can be seen from that the inclusion of an extrinsic source-drain resistance improves the fitting (dashed line). In Figure 3.15, three curves of I_D/β_o were generated (solid lines) with different values for the critical electrical field parameter E_C and v_{sat}. In the first curve, with E_C and v_{sat} tending to infinity, neither mobility reduction nor velocity saturation is present. In the second curve, with a finite E_C, only the mobility reduction by vertical electrical field is present. In the third curve, with a finite v_{sat}, all effects are present. The "bump" mentioned before is present in the curve with velocity saturation effect (the solution with an effective V_{Gf} were not active in this case) but the value of the saturation current agrees with the measurements.

Figure 3.16 and Figure 3.17 also show the normalized drain current I_D/β_o versus V_{Gf} and V_D, respectively, and for a L_G = 2 µm SOI NMOS transistor, but here the model and measurements comparison is more in terms of the mobility reduction by vertical electrical field (Figure 3.16) and channel-length modulation (Figure 3.17). With an appropriate critical field parameter E_C, a good agreement between model and measurements is found. Considering the channel-length modulation effect, it can be seen from Figure 3.17 that the effect is taking into account by the model but the agreement is not so good.

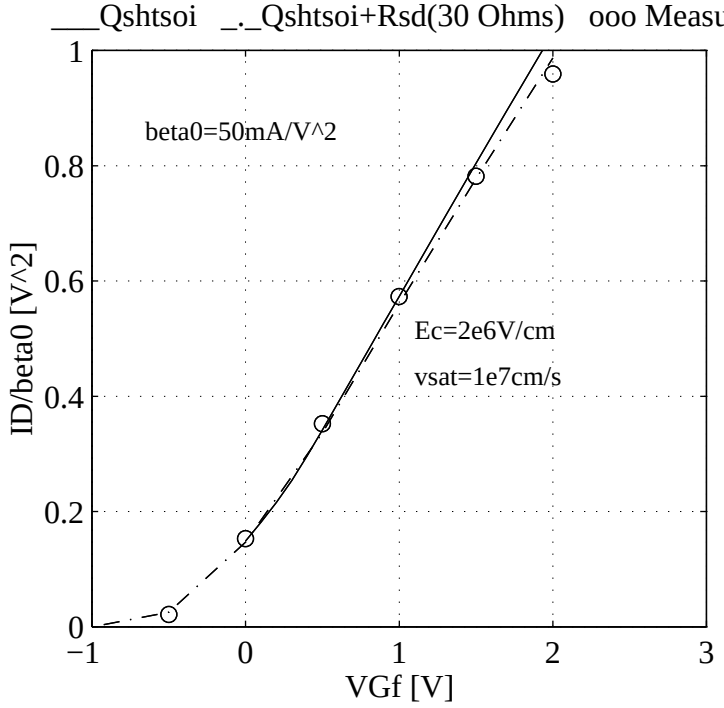


Figure 3.14: Normalized drain current I_D/β_o versus front-gate voltage V_{Gf} for an SOI NMOS transistor comparing model and measurements in terms of velocity saturation effect (L_G = 1 µm).

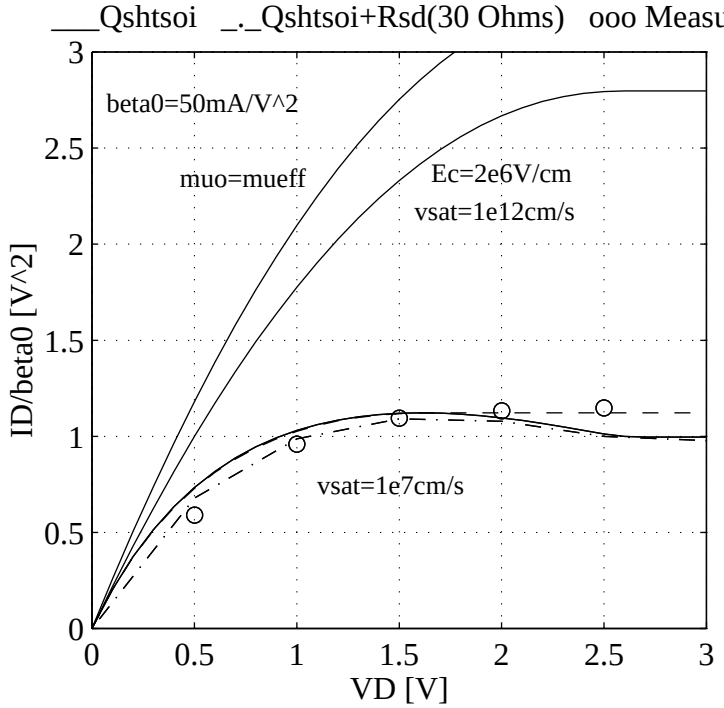


Figure 3.15: Normalized drain current I_D/β_o versus drain voltage V_D for an SOI NMOS transistor comparing model and measurements in terms of velocity saturation and mobility reduction effects (L_G = 1 µm).

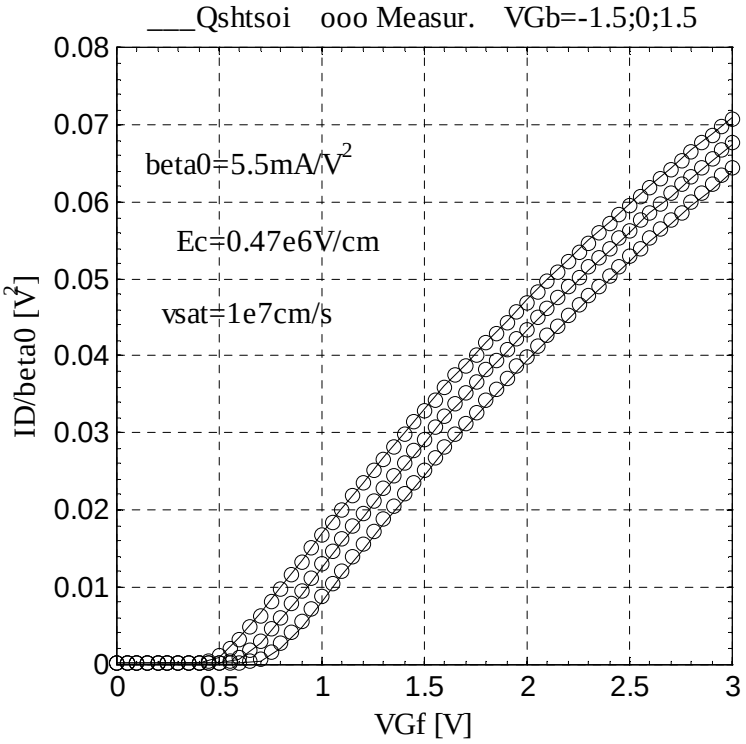


Figure 3.16: Normalized drain current I_D/β_o versus front-gate voltage V_{Gf} for an SOI NMOS transistor and for different values of the back-gate voltage V_{Gb} (L_G = 2 µm).

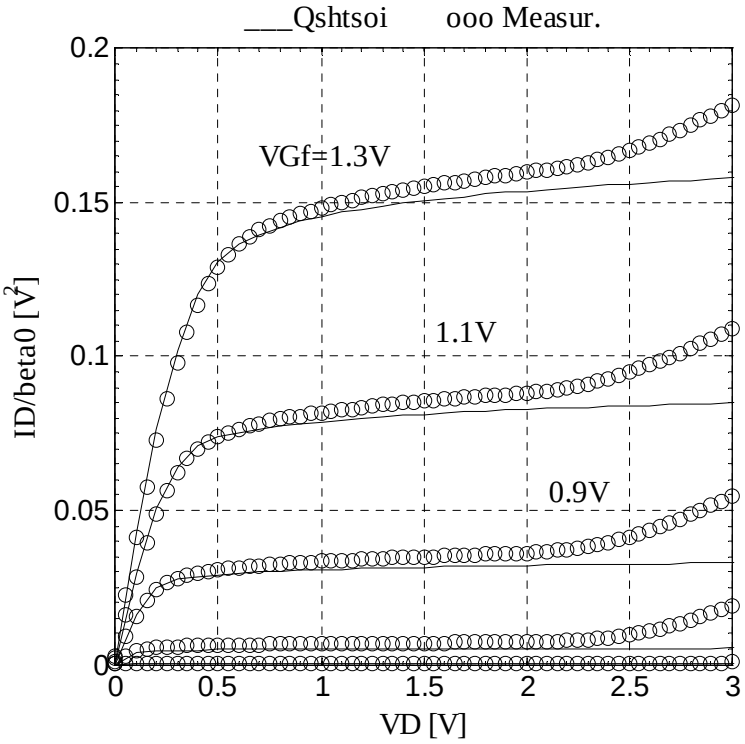


Figure 3.17: Normalized drain current I_D/β_o versus drain voltage V_D for an SOI NMOS transistor and for different values of the front-gate voltage V_{Gf} (L_G = 2 µm).

3.2 A Method to Extend the Validity of the Quasi-Static MOSFET Model

Quasi-static MOSFET models are largely used, but there is a limit frequency beyond which these models fail to predict the real characteristics of the transistor. On the other hand, non-quasi-static models result in complicated mathematical expressions. Special cases in which the transistor is assumed to operate and simple MOS models are usually considered to simplify the analysis.

In this Section, a method to extend the validity of the quasi-static MOSFET model that has been suggested in (Tsividis, 1987) is presented. This chapter deeply investigates the conditions required for the method to work properly, especially in the case of short-channel devices, and leads to the direct evaluation of the small-signal parameters without running a complete circuit simulation. Furthermore, although this method can be applied to an nMOS transistor, it focuses on SOI technology, in particular fully-depleted (FD) nMOSFETs, which feature very promising performance for microwave applications. This technique has been implemented in MATLAB routines starting from an accurate FD SOI charge-sheet model. This model follows the basic numerical procedure proposed in (Ortiz-Conde, 1988). To account for second-order effects, mobility degradation and velocity saturation have been included in this particular charge-sheet model. The basic goal is to have a good physical model, in the case, based in a charge sheet model, from which simpler models capable to predict the MOSFET behavior at high frequencies can be validated.

3.2.1 Distributed Channel Analysis

Quasi-static models are no longer valid when the charge distribution in the channel can not follow the temporal variation of the terminal voltages. The actual distribution of the charges has to be considered in order to model the transistor when it operates at this limit and beyond.

One way to deal with this problem is to divide the transistor in a cascade of several elementary transistors (Tsividis, 1987), as shown in Figure 3.18, each section being short enough to be legitimately represented by the quasi-static model. The sub-transistors are intrinsic with the exception of the first and last ones.

To model this cascade of "N" sub-transistors (N channel sections), the general y-parameters are used. The principle of this method is as follows. The first two sub-transistors, shown in the area marked with a dashed line in Figure 3.18, are taken first and the y-parameters of each individual sub-transistor are combined. The resulting y-parameters are combined once again with the y-parameters of the third sub-transistor and so on. This procedure is repeated until the last sub-transistor is reached and finally the global y-parameter matrix is obtained.

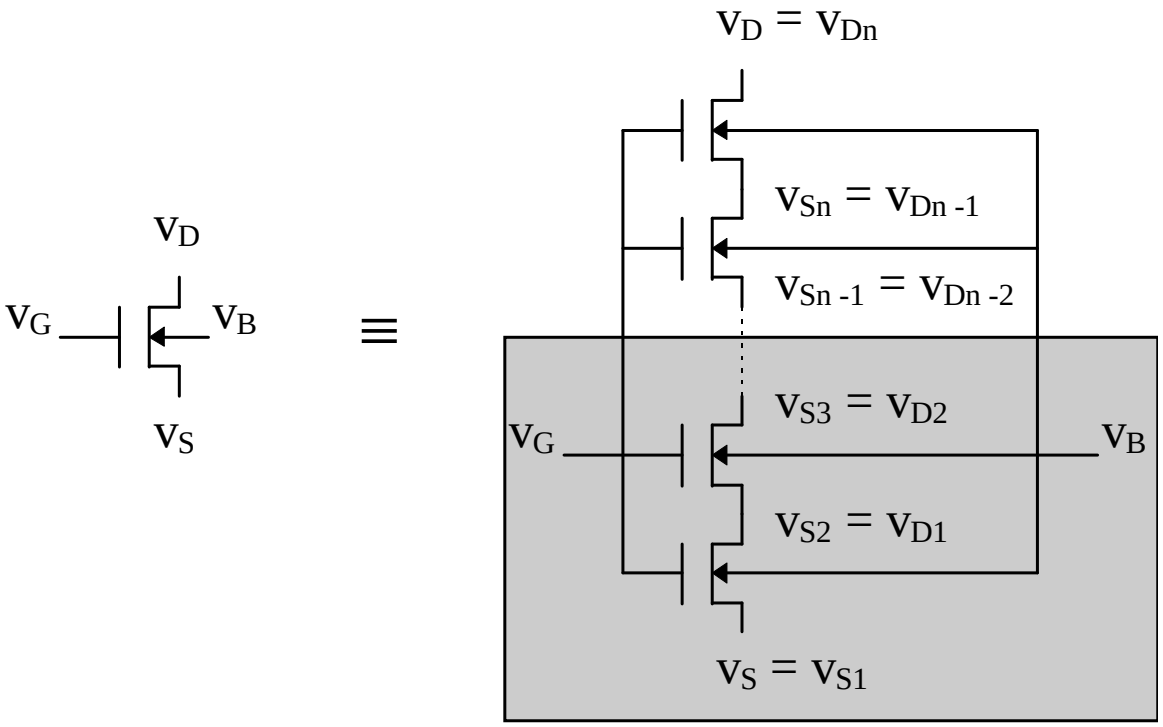


Figure 3.18: Schematic nMOSFET considered as a cascade of several elementary transistors (N channel sections); the subscript "n" represents the number of sections.

To explain this method in more detail, Figure 3.19 shows a general y-parameter model using the substrate terminal (the back-gate terminal in the SOI case) as the reference.

This model represents the first two sub-transistors in the area marked with a dashed line in Figure 3.18. A set of equations which represents the currents in the terminals of Figure 3.19 is written using the y-parameters of each sub-transistor.

$$\begin{aligned} i_{G1} &= y_{GG1}v_{Gf} + y_{GD1}v_{D1} + y_{GS1}v_{S1} \\ i_{D1} &= y_{DG1}v_{Gf} + y_{DD1}v_{D1} + y_{DS1}v_{S1} \\ i_{S1} &= y_{SG1}v_{Gf} + y_{SD1}v_{D1} + y_{SS1}v_{S1} \end{aligned} \tag{3.74}$$

$$\begin{aligned} i_{G2} &= y_{GG2}v_{Gf} + y_{GD2}v_{D2} + y_{GS2}v_{S2} \\ i_{D2} &= y_{DG2}v_{Gf} + y_{DD2}v_{D2} + y_{DS2}v_{S2} \\ i_{S2} &= y_{SG2}v_{Gf} + y_{SD2}v_{D2} + y_{SS2}v_{S2} \end{aligned} \tag{3.75}$$

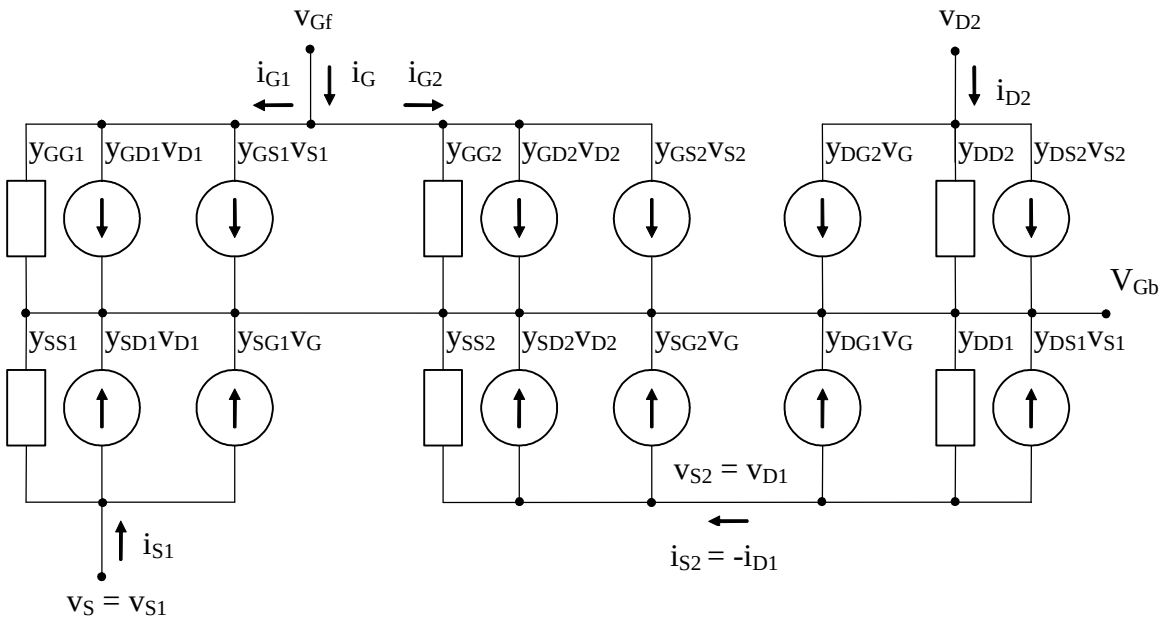


Figure 3.19: A general y-parameter model for the first two elementary transistors in the area marked with a dashed line in Figure 3.18. The substrate terminal (the back-gate terminal V_{Gf} in the SOI case) is used as the reference.

Using the fact that $i_G = i_{G1} + i_{G2}$, $i_{S2} = -i_{D1}$ and $v_{S2} = v_{D1}$ in (3.74) and (3.75), results in

$$i_G = (y_{GG1} + y_{GG2})v_{Gf} + y_{GD2}v_{D2} + (y_{GD1} + y_{GS2})v_{D1} + y_{GS1}v_{S1} \tag{3.76}$$

$$v_{S2} = v_{D1} = -K_1 v_{Gf} - K_2 v_{D2} - K_3 v_{S1} \tag{3.77}$$

where $K_1 = \dfrac{(y_{DG1} + y_{SG2})}{(y_{DD1} + y_{SS2})}$ $\qquad K_2 = \dfrac{y_{SD2}}{(y_{DD1} + y_{SS2})}$ $\qquad K_3 = \dfrac{y_{DS1}}{(y_{DD1} + y_{SS2})}$

Now using (3.77) to eliminate v_{D1} and v_{S2} from (3.74), (3.75) and (3.76), a new set of equations that represents the terminal currents of the first two sub-transistors can be written.

$$\begin{aligned} i_G &= y_{GG}v_{Gf} + y_{GD}v_{D2} + y_{GS}v_S \\ i_{D2} &= y_{DG}v_{Gf} + y_{DD}v_{D2} + y_{DS}v_S \\ i_S &= y_{SG}v_{Gf} + y_{SD}v_{D2} + y_{SS}v_S \end{aligned} \tag{3.78}$$

where each y-parameter of the two combined sub-transistors are given by

$$\begin{aligned} y_{GG} &= (y_{GG1} + y_{GG2}) - (y_{GD1} + y_{GS2})K_1 \\ y_{GD} &= y_{GD2} - (y_{GD1} + y_{GS2})K_2 \\ y_{GS} &= y_{GS1} - (y_{GD1} + y_{GS2})K_3 \end{aligned} \tag{3.79}$$

$$\begin{aligned} y_{DG} &= y_{DG2} - y_{DS2}K_1 \\ y_{DD} &= y_{DD2} - y_{DS2}K_2 \\ y_{DS} &= -y_{DS2}K_3 \end{aligned} \tag{3.80}$$

$$\begin{aligned} y_{SG} &= y_{SG1} - y_{SD1}K_1 \\ y_{SD} &= -y_{SD1}K_2 \\ y_{SS} &= y_{SS1} - y_{SD1}K_3 \end{aligned} \tag{3.81}$$

All y-parameters are determined in the quasi-static mode (Section 3.1.3).

As already stated, the procedure is repeated considering the third sub-transistor and so on, to find the global y-parameter matrix that represents the whole transistor. This method requires that the y-parameters of each sub-transistor be known. To determine these y-parameters all intermediate voltages along the channel, from source to drain, have to be known too.

The interest is in the intrinsic transistor, i.e., from x=0 to x=L (see Figure 3.4). The front-gate surface electrostatic potential $\psi_{sf}(x)$ and the potential V(x) are related to an intermediate point "x" along the channel. V(x) represents the difference between the quasi-fermi potential for electrons in the channel ϕ_{fn} and the quasi-fermi potential for holes ϕ_{fp}. V(x) is either a drain or source voltage of a sub-transistor. Assuming that the current in each sub-transistor has to be the same, an expression which relates “x”, ψ_{sf} and a “V” voltage, or in other words, $x=f_1(\psi_{sf})$ and $\psi_{sf}=f_2(V)$, can be obtained.

Two different ways of dividing the channel have been implemented: the first procedure consist in choosing a set of “V” voltages and finding “x” along the channel, so the functions f_1 and f_2 can be used directly; the second consist in choosing values of “x”, i.e., setting each section length Δx and finding “V” voltages along the channel. This second procedure needs to invert the functions f_1 and f_2 and is computationally slower than the first one. The two methods were implemented but the first one gives better results since the front-gate surface electrostatic potential $\psi_{sf}(x)$ and the potential V(x) are nonlinear functions of “x”.

Another problem is to include expressions for mobility degradation due to normal electric fields and velocity saturation at higher lateral electric fields which remain valid in each short sub-transistor. These effects are taken into account in the FD SOI charge-sheet model presented in Section 3.1.4. The former effect is included using an effective mobility μ_{eff}, i.e., a low-lateral field mobility affected by the normal electric field E_y – or equation (3.62) rewritten below.

$$\mu_{eff} = \frac{\mu_o}{1 + \frac{E_{yeff}}{E_c}}$$

Velocity saturation effect has been included as well using a mobility expression - equation (3.63) - which also combines the last relation for μ_{eff}, or

$$\mu(x) = \frac{\mu_{eff}}{1 + \left(\frac{\mu_{eff}}{v_{sat}}\right)\frac{d\psi_{sf}}{dx}}$$

where $\frac{d\psi_{sf}}{dx}$ represents the lateral electric field E_x or E_{sfx}.

3.2.2 Distributed Gate Analysis

Another important effect to be considered is the propagation time along the gate. The poly-silicon gate of a transistor can be treated as an RC network since, in general, the poly-silicon resistance cannot be neglected and the RC network delays the signal that arrives at the gate. The result is that the elements under the gate, intrinsic and extrinsic ones, respond at different times to the signal. Similar to the distributed channel analysis, one-way to deal with this problem is to consider several gate sections short enough to minimize the propagation effects.

To illustrate the analysis explained later in this section, Figure 3.20 shows a simplified layout of an NMOSFET putting in evidence parasitic capacitances and resistances along the gate and how y-parameters are taking into account; Figure 3.21 shows a schematic NMOSFET considered as a cascade of several elementary transistors along the gate (M gate sections). The substrate terminal (the back-gate terminal in the SOI case) is omitted for simplicity and the subscript "m" represents the number of sub-transistors. R_{Ge1}, R_{Ge2} ... R_{Gem-1}, and R_{Gem} represent elementary gate resistances each one equal to the total gate resistance R_{Ge} divided by the number of gate sections “M”; C_{GDe1}, C_{GDe2} ... C_{GDem-1}, and C_{GDem}, and C_{GSe1}, C_{GSe2} ... C_{GSem-1}, and C_{GSem} represent elementary capacitances each one equal, respectively, to the total gate-to-drain C_{GDe} and gate-to-source C_{GSe} extrinsic or parasitic capacitances divided by the number of gate sections.

To model this cascade of sub-transistors along the gate, the y-parameters and a matrix analysis are used. The principle is as follows. The y-parameters that represent the whole transistor are determined and extrinsic elements such as g_{de}, C_{GDe}, and C_{GSe} are added. The resulting y-parameters are divided by the number of gate sections yielding an elementary set of y-parameters called Y_{e1} which represents the first sub-transistor T_1 plus C_{GDe1} and C_{GSe1} (at the end of the gate) show in Figure 3.21. Now the elementary gate resistance R_{Ge1} can be added. The set Y_{e1} is transformed in the corresponding z-parameters, R_{Ge1} is added and the resulting z-parameters are retransformed in y-parameters. The procedure is repeated using the second sub-transistor and so on, until the last sub-transistor is reached and finally the global y-parameter matrix is obtained.

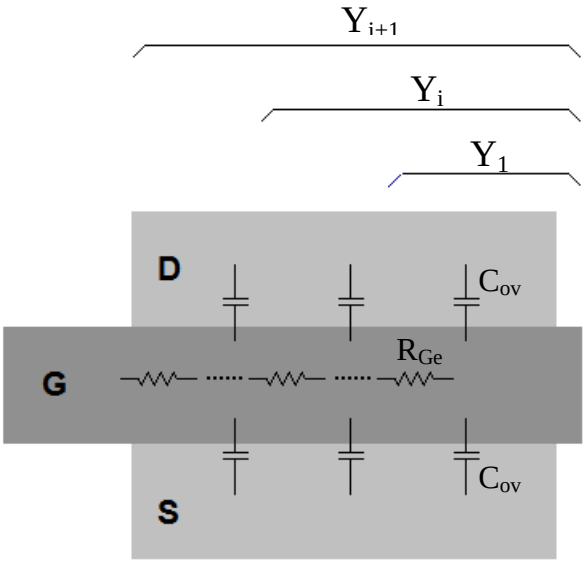


Figure 3.20: A simplified layout of an NMOSFET putting in evidence parasitic capacitances and resistances along the gate and how y-parameters are taking into account.

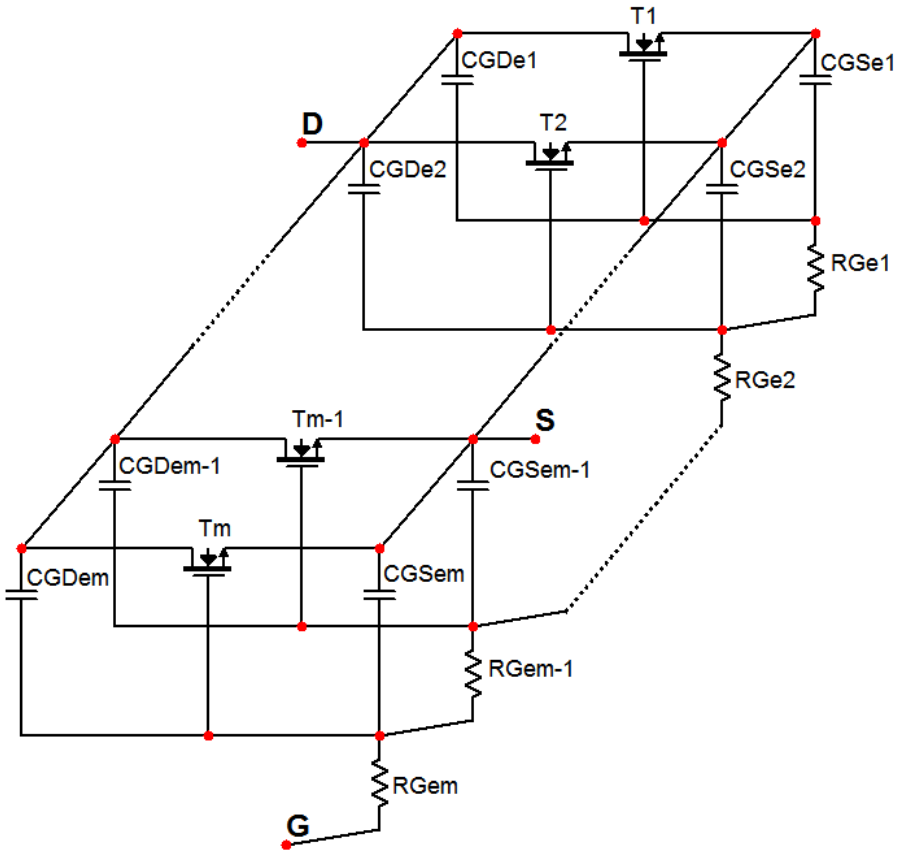


Figure 3.21: Schematic nMOSFET considered as a cascade of several elementary transistors along the gate (M gate sections). The substrate terminal (back-gate terminal) is omitted for simplicity and the subscript "m" represents the number of sections.

3.2.3 Results and Model Comparison

Some results are illustrated in Figure 3.22 for a $L_G = 0.75\mu m$ SOI nMOS transistor with $V_{Gf} = V_D = 3V$ and $V_S = V_{Gb} = 0V$. Ten channel sections (N=10) based on a set of "V" voltages have been considered, which have been evaluated to be a good trade-off between accuracy and complexity. In Figure 3.22, four subplots are shown representing the lateral electric field E_{sfx}, the carrier velocity "vel", the normalized mobility μ/μ_{eff}, and the front-channel charge density normalized to the front-gate oxide capacitance Q_{if}/C_{of} versus normalized distance along the channel x/L. Each subplot shows two curves with either $v_{sat} = 1.1x10^7$ cm/s or v_{sat} tending to infinity.

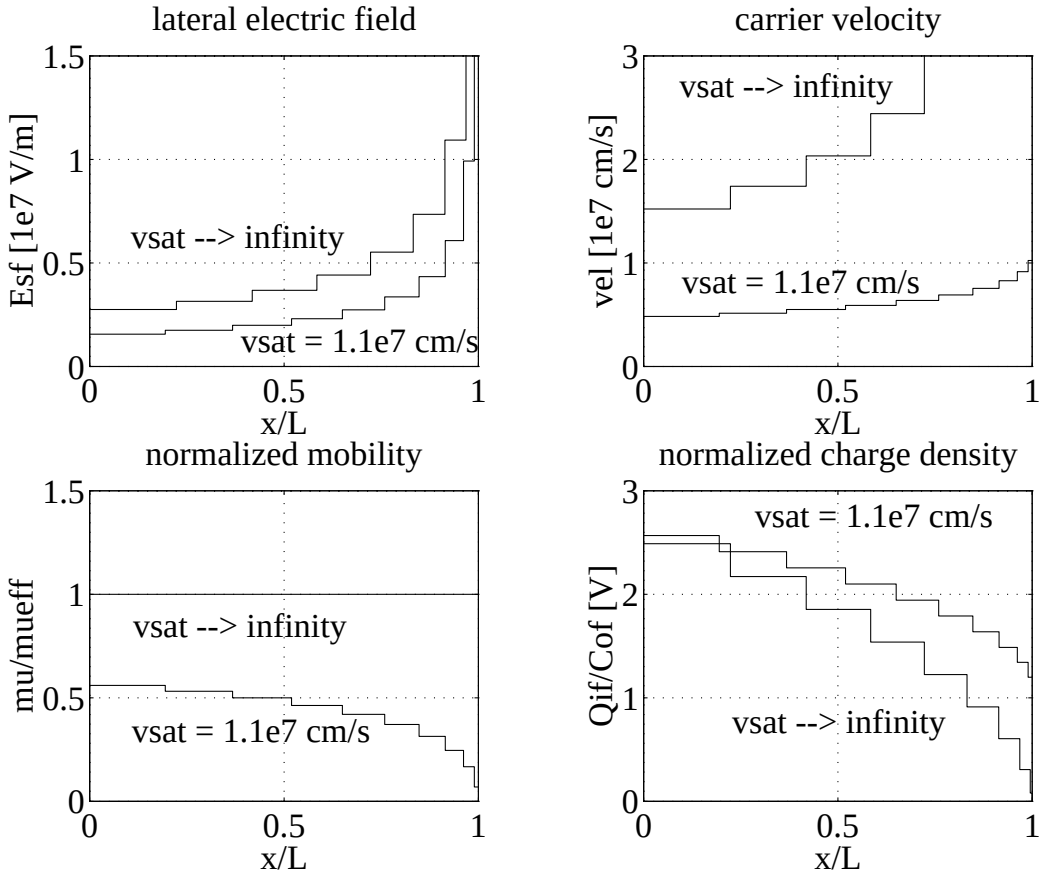


Figure 3.22: E_{sf}, vel, μ/μ_{eff} (mu/mueff) and Q_{if}/C_{of} vs. x/L for a $L_G = 0.75\ \mu m$ SOI nMOS transistor with $V_{Gf} = V_D = 3V$, $V_S = V_{Gb} = 0V$, 10 channel sections (N = 10) and with either $v_{sat} = 1.1x10^7$ cm/s or v_{sat} tending to infinity.

The effect of the finite v_{sat} is quite clear. At the end of the channel, the carrier velocity tends to equal v_{sat} and the charge density Q_{if} tends to a non-zero value. Since the carrier velocity saturates, a non-zero Q_{if} is essential to assure the current continuity. Also the mobility tends to zero as the lateral electric field increases. With an infinite v_{sat}, Q_{if} at the end of the channel tends to zero since the carrier velocity becomes infinite and the mobility remains constant being affected only by the normal electric field.

Figure 3.23 shows the magnitude of Y_{21} normalized to its low-frequency value $Y_{21(LF)}$ and the phase of Y_{21} vs. frequency for a L_G = 0.75 µm SOI nMOS transistor in the common source configuration with $V_{Gf} = V_D = 3$ V and $V_S = V_{Gb} = 0$V. The curves with solid lines (—) are for the model using the method described in this work, with 10 channel sections (N = 10) and 20 gate sections (M =20); the curves with dashed lines (- - -) are for the single transistor complete quasi-static model. The limit of validity of the latter model corresponds to the point where $|Y_{21}|$ goes upward.

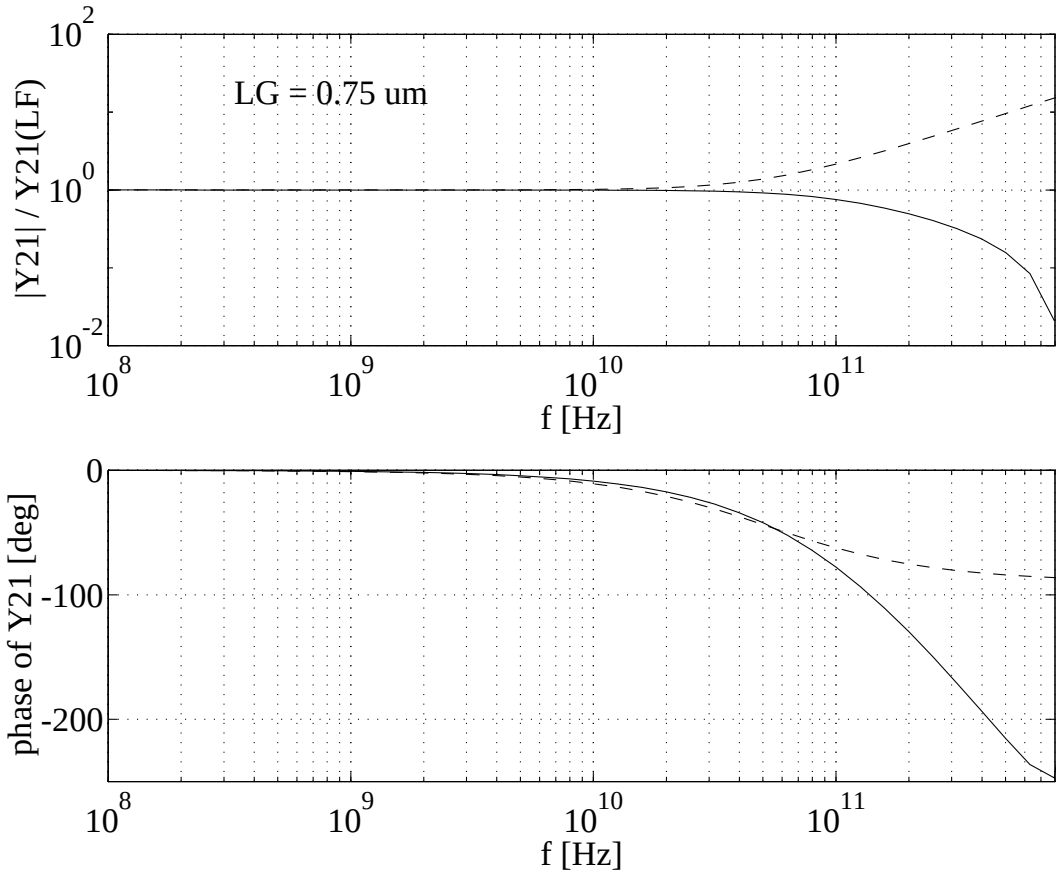


Figure 3.23: $|Y_{21}|/Y_{21(LF)}$ and the phase of Y_{21} vs. frequency for a L_G = 0.75 µm SOI nMOS transistor in common source configuration with $V_{Gf} = V_D = 3$V and $V_S = V_{Gb} = 0$V. The model (—) corresponds to the subdivided transistor, 10 channel sections (N = 10) and 20 gate sections (M =20), and the model (- - -) corresponds to the single transistor.

In the common source configuration, $y_{DG} = g_{mG} - j.\omega.C_{DG}$ is equivalent to Y_{21}, a complex transconductance G_m. Figure 3.24 shows the transconductance G_m vs. frequency (magnitude and phase) for a L_G = 0.75 µm SOI nMOS transistor in common source configuration. The model (- - -) corresponds to the single transistor. The other curves represent the transistor subdivided into several channel (N) and gate (M) sections. The influence of multiple gate sections is quite visible on magnitude and phase of G_m, as well as the inclusion of a parasitic overlap capacitance C_{ov}. Figure 3.25 shows the dependence of the S-parameters on carrier saturation velocity v_{sat}, S21 and S22 being the most affected.

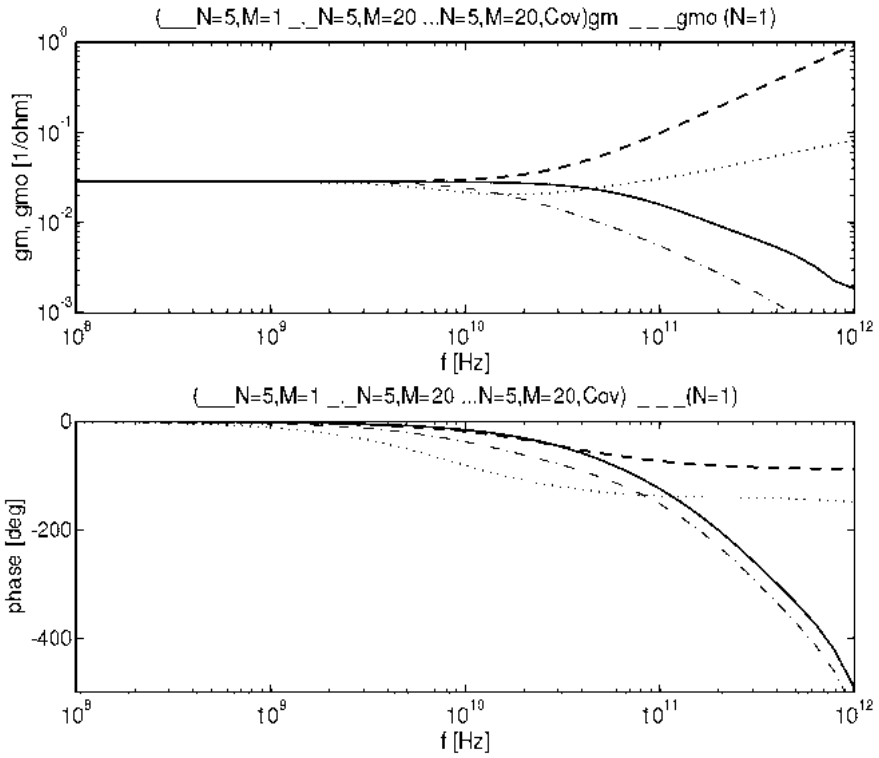


Figure 3.24: Transconductance G_m vs. frequency (magnitude and phase) for a L_G = 0.75 µm SOI nMOS transistor in common source configuration. The model (- - -) corresponds to the single transistor.

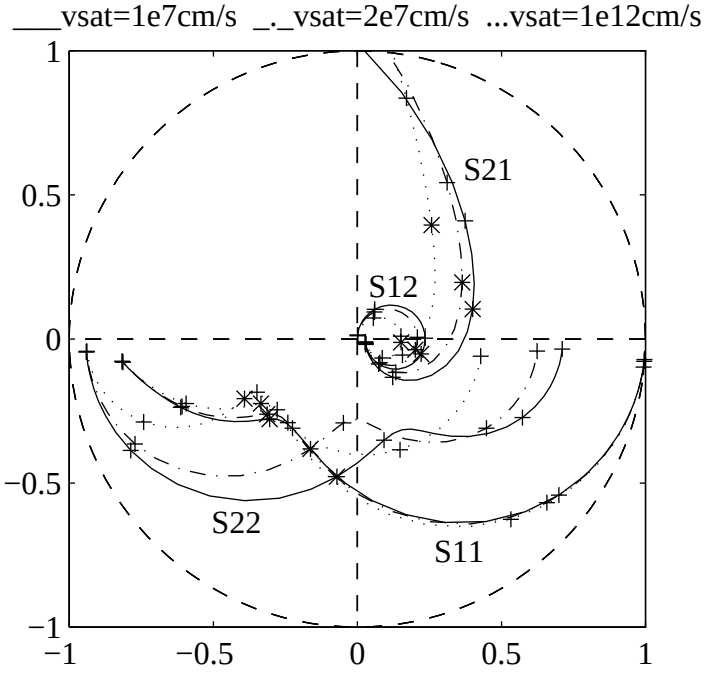


Figure 3.25: S-parameters (model) for a for a 20x(25/0.75) SOI nMOS transistor in the common source configuration with different values of v_{sat} (from 0.1 to 1000 GHz, N = 10, M = 20).

Figure 3.26 shows the S-parameters measurements (ooo) and the predicted parameters (—) for a SOI nMOS transistor in common source configuration, consisting of 20 parallel fingers each with W = 25 µm, L_G = 0.75 µm, and with $V_{Gf} = V_D$ = 3V and $V_S = V_{Gb}$ = 0V. Measurements have been performed in the 0.1-24 GHz frequency range with a cross (+) marking each decade. The modeled S-parameters are shown in the 0.1-1000 GHz frequency range with a star (*) marking each decade. It can be seen that the agreement between the model using the method presented in this work and the measurements is quite good.

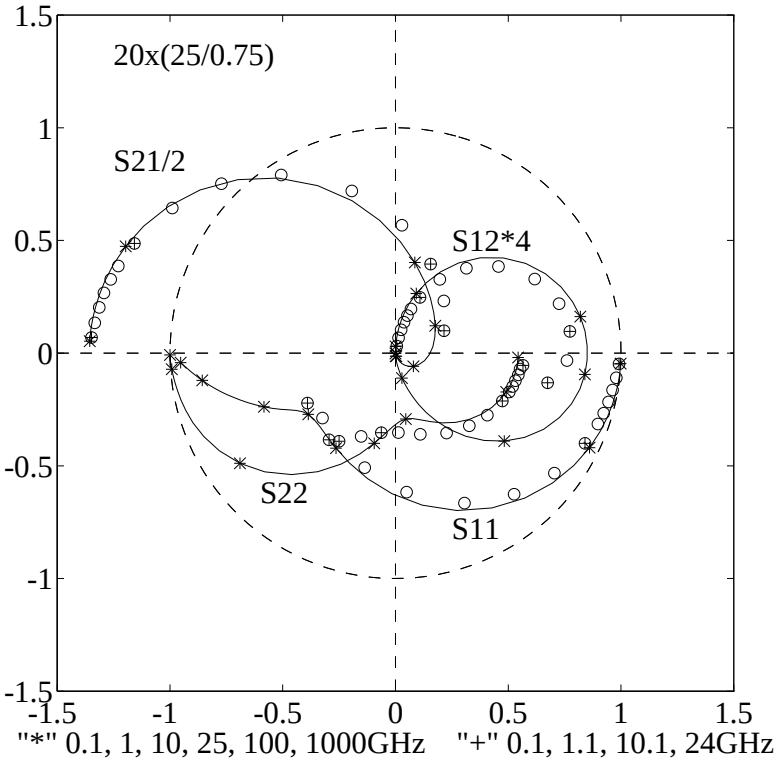


Figure 3.26: S-parameters for a 20x(25/0.75) SOI nMOS transistor in the common source configuration with $V_{Gf} = V_D$ = 3V and $V_S = V_{Gb}$ = 0V. Model (—) from 0.1 to 1000 GHz (N = 10, M = 20) and measurements (ooo) from 0.1 to 24 GHz.

3.3 Conclusions

A numerical charge-sheet model for thin-film fully-depleted (FD) silicon-on-insulator (SOI) MOSFETs valid for back-channel in depletion from source to drain, based on the *"gradual channel"* and the *"charge-sheet"* approximations, has been presented. Short-channel effects such as velocity saturation, channel length modulation and drain-induced conductivity enhancement (DICE) are included. The model is physivally-based and has only a few fitting parameters such as the critic transversal electric field E_c, saturation velocity v_{sat}, low-field mobility μ_o, and flat-band voltages of front and back gates. The formal definition of V_T is not needed nor a related fitting parameter.

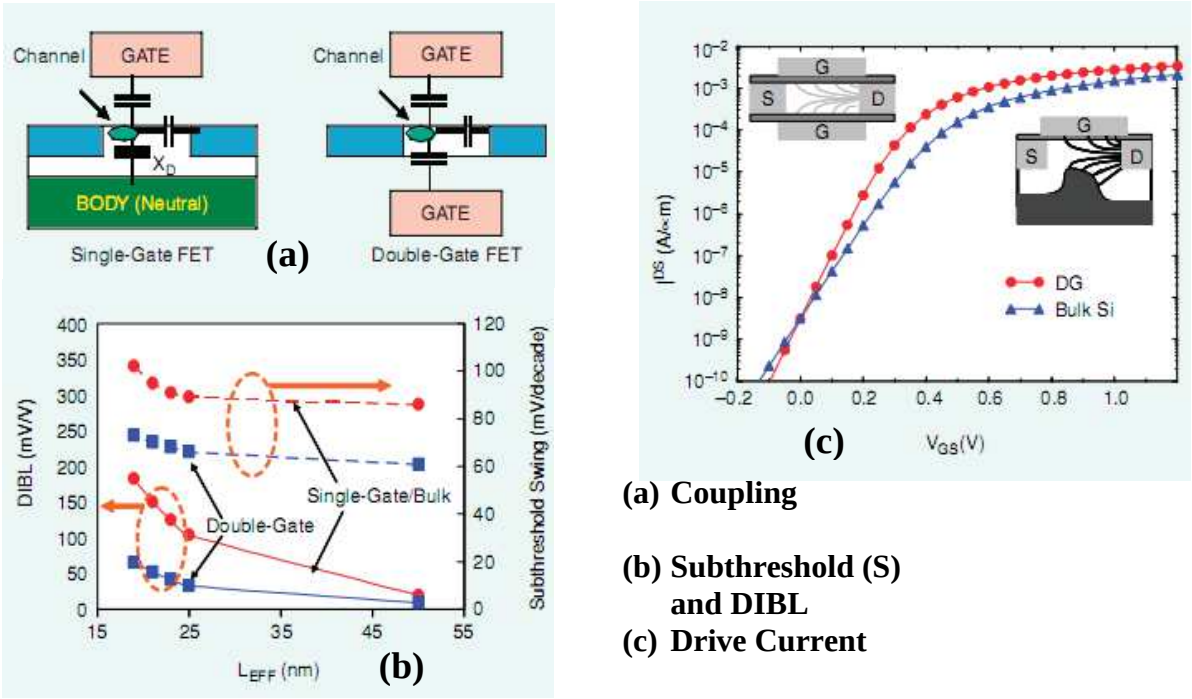
A method to model thin-film fully-depleted SOI-MOSFETs at frequencies where the quasi-static model is no longer valid has been presented. The methodology is based on a distributed channel model. The approach based on a choice of voltages along the channel followed by the determination of each channel section length is more suitable in terms of computational procedure. The influence of the mobility degradation and velocity saturation effects has been stressed and a good agreement between the model and the measurements has been found. The basic methodology can be applied to multi-gate MOSFETs, but the numerical charge-sheet model used has to be changed or substituted by other model to incorporate very important details of the physics of multi-gate devices.

4 MULTI-GATE MOSFETS

In this chapter a brief overview of Multi-Gate MOSFETs is presented. The general concepts of alternative 3D structures are summarized.

4.1 Multi-Gate Devices

The continuous necessity for increasing the circuits performance, for example, in terms of current drive and better short-channel effects, has driven the development of MOS transistors and technology. Silicon-on-Insulator (SOI) technology (Colinge, 1991) has evolved as a need of better performance of BULK traditional counterpart. In the same manner, single-gate devices have evolved into very three-dimensional multi-gate devices, achieving a better gate control over the channel (Lindert, 2001; Chau, 2002; Doyle, 2003; Colinge, 2007; Cristoloveanu, 2007). Figure 4.1 shows a comparison between single-gate (SG) and double-gate (DG) MOSFETs in terms of coupling, subthreshold slope S, drive current and DIBL - Drain Induced Barrier Lowering (Tsividis, 1987).



(a) Coupling

(b) Subthreshold (S) and DIBL

(c) Drive Current

Figure 4.1: Comparison between Single-Gate and Double-Gate MOSFETs (IEEE Circuits & Devices Magazine, 2004).

Figure 4.1 schematically shows the coupling between the gate, channel and drain. The drain potential influence on the channel potential increase as the channel length is reduced, degrading the control of the channel current by the gate. This short-channel effect can be weakened by reducing the gate oxide thickness t_{ox} and the depletion region x_d. Unfortunately, the decrease in t_{ox} can lead to an increase in power consumption due to gate leakage and became a serious problem. For example, at 90 nm BULK technology this parasitic consumption is comparable to the power used for switching circuits. A double-gate control can alleviate some of these short-channel effects, acting in the potential channel in a more efficient way and reducing the coupling with the drain. In particular, DIBL effect is reduced and the subthreshold slope S is decreased. Figure 4.1(b) shows simulation results comparing predicted values of these two important parameters (figures of merit) on single and double gate MOSFETs. It is noted the improving of S and DIBL on DG-MOSFETs. Subthreshold slope affects the drive and turn-off current of the transistor and consequently the threshold voltage V_T. Figure 4.1(c) shows simulation results that illustrate the improvement of the drive current on DG-MOSFETs when compare to BULK SG MOSFETs. It is clear that on DG one can use a lower voltage for a given off-current.

These so called multi-gate MOSFET devices can be classified in: double, triple (or tri) and quadruple (or quad) gate devices. In most cases these multiple gates are all connected together, wrap around silicon channel area, but they can be independent. In Figure 4.2 the basic difference in the structures of Ultra-Thin-Body (UTB) MOSFETs can be seen. Figure 4.2(a) shows a UTB SOI-MOSFET structure, similar to those shown briefly in Chapter-2, and Figure 4.2(b) shows a DG SOI-MOSFET. Although these devices have a three-dimensional (3D) structure, normally they have a strong symmetry in one axis that allows a two-dimensional (2D) analysis. On the other hand, Figure 4.2(c) shows a multi-gate MOSFET called FinFET that have a strong 3D-structure where a 3D-analysis is a must.

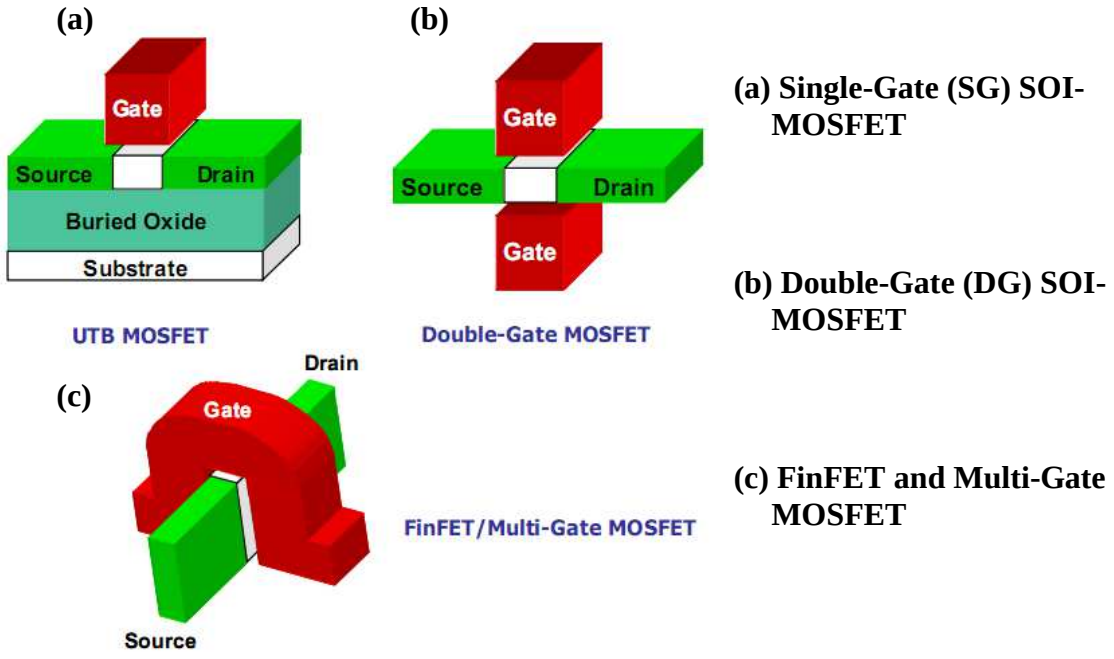
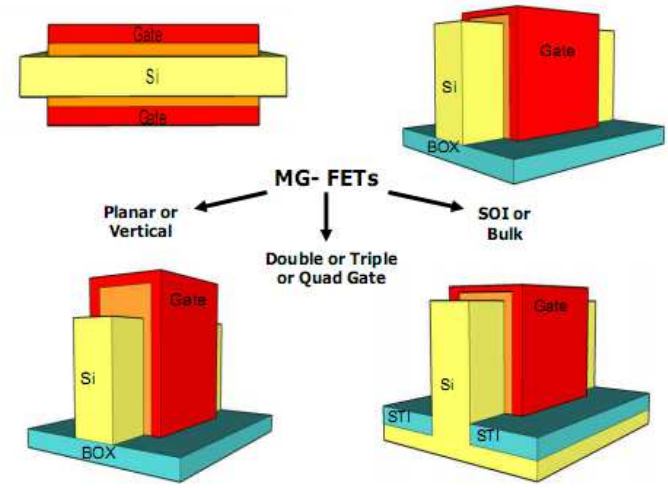


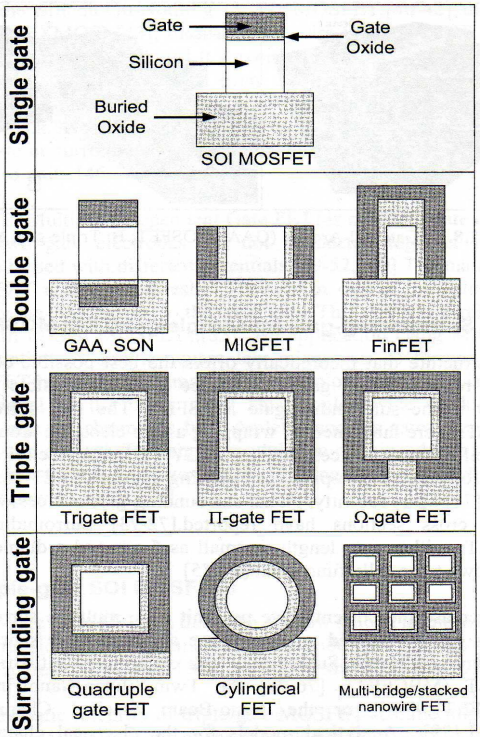
Figure 4.2: Ultra-thin-body MOSFET structures (LIN, 2007).

Figure 4.2 focus only the multiple gates aspect regardless of technology. Although SOI technology is very well suited and have many advantages over BULK , the last one can also be used to perform multi-gate devices. Figure 4.3 shows a summary of possible configurations of multi-gate MOSFETs, regarding technology. They can be performed either on SOI or on BULK, either on planar technology or on vertical and, of course, with double, triple or quadruple gate. Figure 4.4 shows many possible multi-gate SOI MOSFET structures. These figures are very interesting to avoid confusion with the terminology.



- **Planar or Vertical**
- **SOI or BULK**
- **Double, Triple or Quaduple**

Figure 4.3: Summary of possible configurations of Multi-Gate MOSFETs (DUNGA, 2008).



(a) Single-Gate (SG)

(b) Double-Gate (DG)

(c) Triple-Gate, etc

(d) Quaduple-Gate, etc

Figure 4.4: Multi-Gate SOI MOSFET structures (COLINGE, 2007).

In Figure 4.5 is shown a schematic view of an Ultra-Thin-Body nano-device structure, a FinFET (Lindert, 2001), in more details. The channel, source and drain regions are performed in a silicon vertical nanostructure called “finger” or “fin”. The gate wraps around the silicon fin inducing electrostatic control from opposite sides. This is a great advantage in terms of reducing short-channel effects as was discussed earlier. Drain and source pads (enlarged silicon areas) are patterning to contact and low resistance.

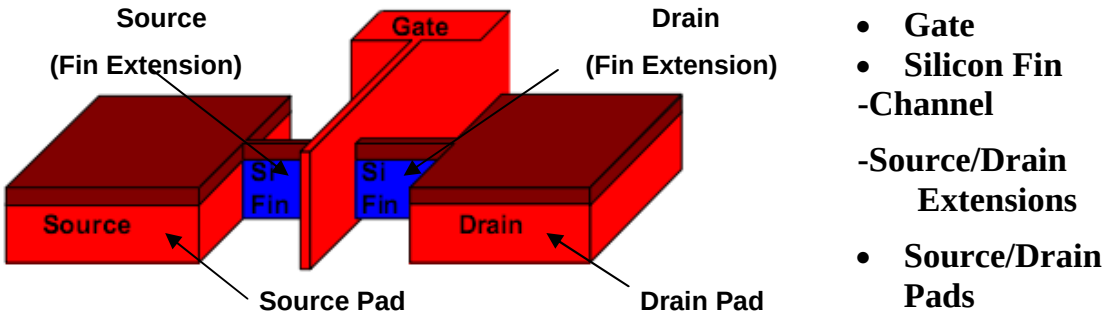


Figure 4.5: Schematic view of a FinFET structure (Dunga, 2008).

4.2 FinFET Fabrication

In the same way SOI CMOS process flow (Colinge, 1991) can be very close to the traditional BULK CMOS, with the basic difference on the starting wafers, SOI-FinFET (double-gate or triple-gate) process flow (Colinge, 2007) is also very closely related to SOI process flow. Moreover, the starting wafers for SOI-FinFETs can be the same standard SOI material.

Figure 4.6 shows the basic geometry features of a FinFET structure layout with five parallel fins ($N_T = 5$). The critical dimensions are indicated:

- mask channel length (L_{Gm});
- silicon fin thickness (T_{fin});
- the maximum S/D extension length (L_{SDmax}), which is the spacing between the gate mask and the silicon pad that connects all fins;
- and the fin pitch (P_{fin}), which is the spacing between fins plus fin thickness.

Considering only one fin and for a double-gate FinFET, the effective or equivalent width is $W_{eff} = 2H_{fin}$. The fin pitch has to scale down appropriately, while the third-dimension (fin height, H_{fin}) needs to scale up, in order to have an effective multi-fin FinFET width ($W_{eff}.N_T$) larger than that of a planar SOI-MOSFET laid down in the same direction ($P_{fin}.N_T$). This way, $2H_{fin}$ has to be larger than P_{fin}, for providing advantages in terms of density over planar SOI-MOSFETs.

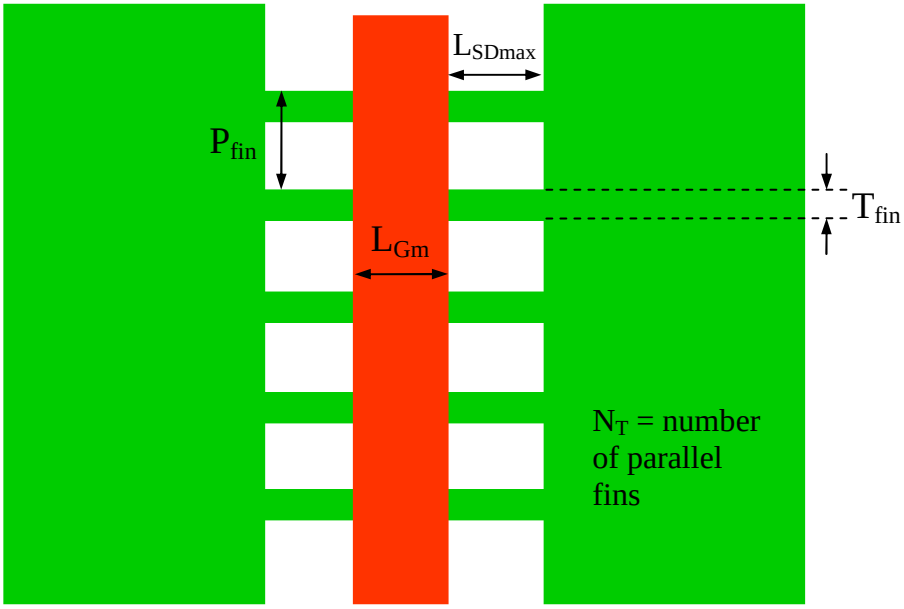


Figure 4.6: FinFET device structure layout with five parallel fins ($N_T = 5$). Critical dimensions indicated: mask channel length L_{Gm}, silicon fin thickness T_{fin}, maximum S/D extension length L_{SDmax}, and the fin pitch P_{fin}.

In Figure 4.7(a) and Figure 4.7(b) a comparison of process flows of SOI-FinFET and conventional SOI is illustrated in very simplified steps.

The basic process flow steps depicted in Figure 4.7 are: fin formation; gate stack deposition and planarization and gate etch; source/drain extension implantation and halos; spacer formation; epitaxial raised source/drain formation; deep source/drain implantation and anneal. The fin formation step defines the fin height H_{fin} and fin thickness T_{fin}, two important transistor dimensions that will be defined in the next chapter. It is similar to trench isolation, with nitride/oxide films deposition, etch fin and source/drain regions, very similar to the conventional SOI process.

Considering starting wafers with (100) surface orientation, patterning fins at 0^o or 90^o with respect to the (110) notch results in (110) sidewall surface fins, while patterning fins at 45^o results in (100) sidewall surface fins. The (100) surface is the higher mobility surface for electrons and the lowest mobility surface for holes. On the other hand, the (110) surface is the higher mobility surface for holes and the lowest mobility surface for electrons (Colinge, 2007).

The aspect ratio H_{fin}/T_{fin} are very important too and high ratios are a device design goal and also a challenge. The transistor current drive increases with the increase of H_{fin} and the decrease of fin pitch (distance between adjacent fins). There is a trade-off between H_{fin}, T_{fin}, fin pitch and gate patterning. Aspect ratio and fin pitch can be improved beyond optical lithography by using a spacer-defined fin formation (Colinge, 2007) (Choi, 2002). Gate etch is also very similar with less severe demands on the selectivity. On the other hand, implantations and halos differ for geometrical reasons, but in the essence they are similar.

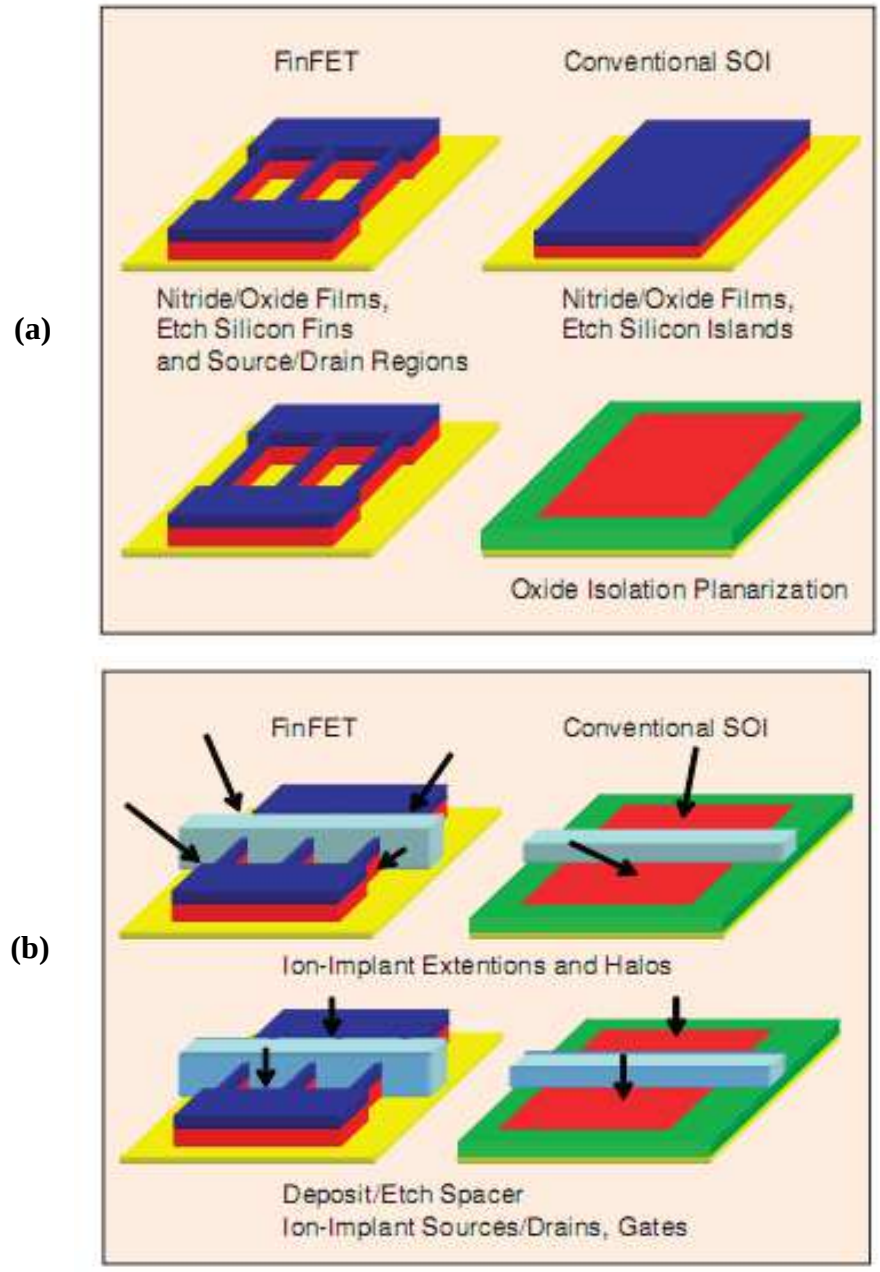


Figure 4.7: Simplified FinFET and conventional SOI process flow (IEEE Circuits & Devices Magazine, 2004; Nowak, 2003).

In Figure 4.8 and Figure 4.9 are shown a few pictures of real FinFET transistors that exhibit the very three-dimensional (3D) nature of this device. Figure 4.8 shows a cross section of a nickel-silicide gate FinFET and Figure 4.9 shows a multi-finger SOI-FinFET.

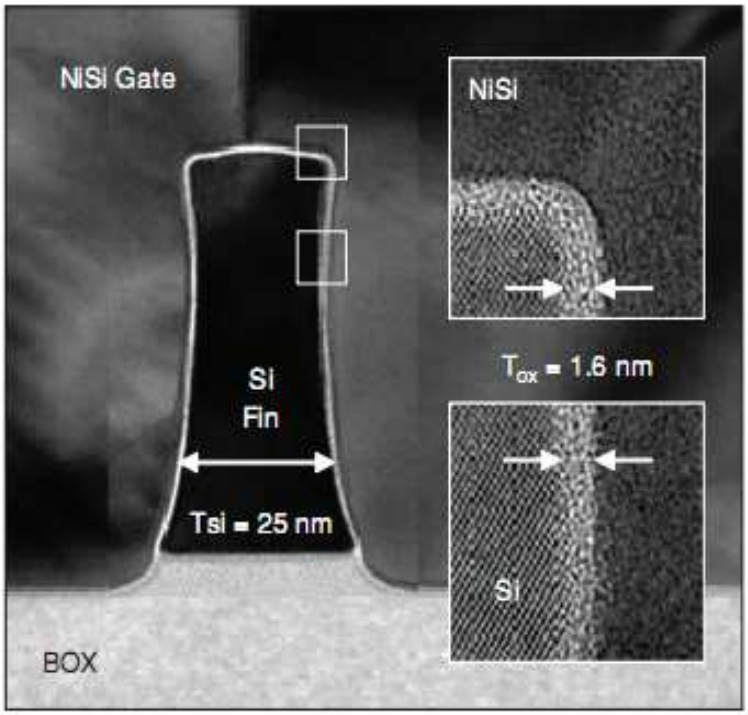
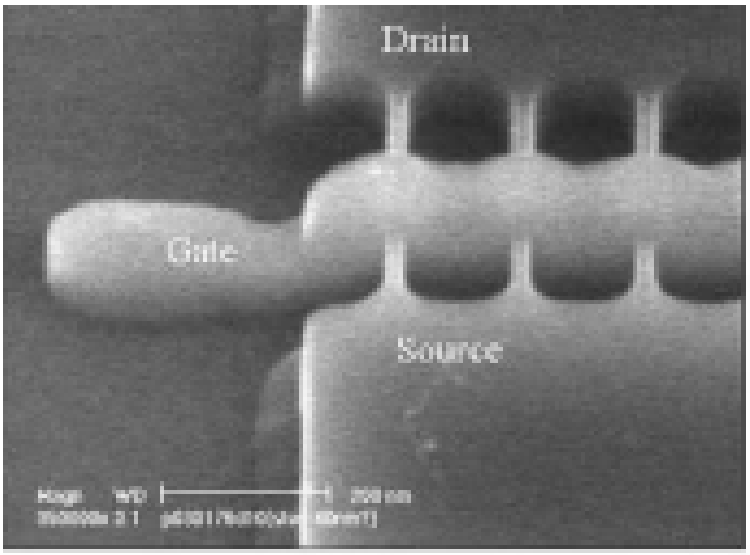


Figure 4.8: Cross section of a nickel-silicide gate FinFET (TEM) (IEEE CIRCUITS & DEVICES MAGAZINE, 2004; Kedzierski, 2002).



t_{ox}= 2 nm

H_{fin} = 75 nm

(W_{eff}= 150 nm)

T_{fin} = 35 nm

Figure 4.9: Picture of a multi-finger SOI-FinFET device (SEM) (Lederer, 2005).

4.3 Bulk FinFET

In the previous Section 4.1 a brief overview of multi-gate MOSFETs structures was presented. Vertical structures called FinFETs can be manufactured on SOI or BULK substrates. Although the present work addresses the SOI technology and SOI-FinFETs it is important to stress that Bulk-FinFETs can be a viable option at 22 nm CMOS technology node and beyond. Figure 4.10 shows simplified cross-sections of a Bulk-FinFET and a SOI-FinFET. At this level of simplicity the major difference, in the case of Bulk-FinFET, is the contact of the silicon fin with the substrate body. On SOI-FinFET the silicon fin is isolated from the substrate body by the buried-oxide (BOX). But considering the complete 3-D device there are many other differences concerning doping and isolation.

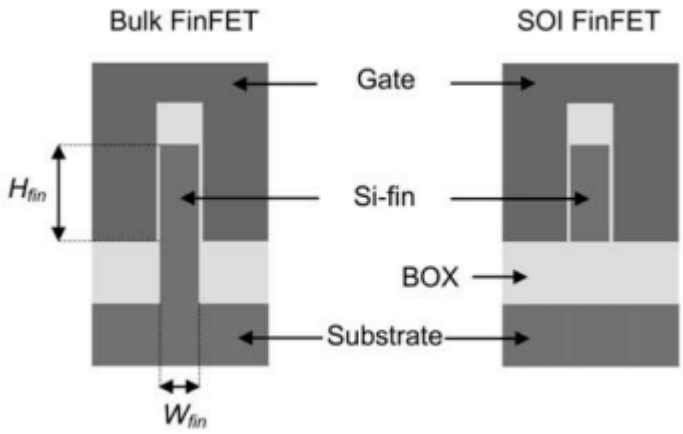


Figure 4.10: Cross-sections of a Bulk-FinFET and a SOI-FinFET.

FinFETs characteristics (Bulk or SOI) such as very good short channel effects control, high integration density and near ideal subthreshold slope (≈ 60 mV/dec, 300K) have made these devices very attractive to implement advanced node technology applications (like 22 nm down to about 10 nm), particularly analog circuits and SRAMs.

Comparative studies have been made stressing advantages of one type of FinFET over another (Chiarella, 2009; Poljak, 2009). Some advantages of Bulk-FinFETs over SOI-FinFETs are pointed out in (Poljak, 2009): cost of the starting material, heat transfer from the channel and compatibility with planar Bulk CMOS devices. On the other hand, (Chiarella, 2009) pointed out that SOI-FinFETs may offer a better choice in terms of voltage gain and mismatch for analog applications, as well as speed of the device.

4.4 Ultra-Thin Body and BOX

In Chapter 2 a brief overview of the Silicon-on-Insulator (SOI) CMOS technology was presented and its differences and advantages over bulk technology were emphasized. The SOI technology has been developed for over two decades and commercial and very complex digital circuits became available in the 1990's.

Although the SOI technology is inherently dual-gate, the more effective control of the front-gate over the back-gate makes the technology very competitive as single-gate. Recently the use of FD-SOI with ultra-thin body and ultra-thin BOX (UTBB) has made the technology competitive with Bulk-FinFETS and SOI-FinFETs. Figure 4.11 shows a simplified UTBB MOSFET structure.

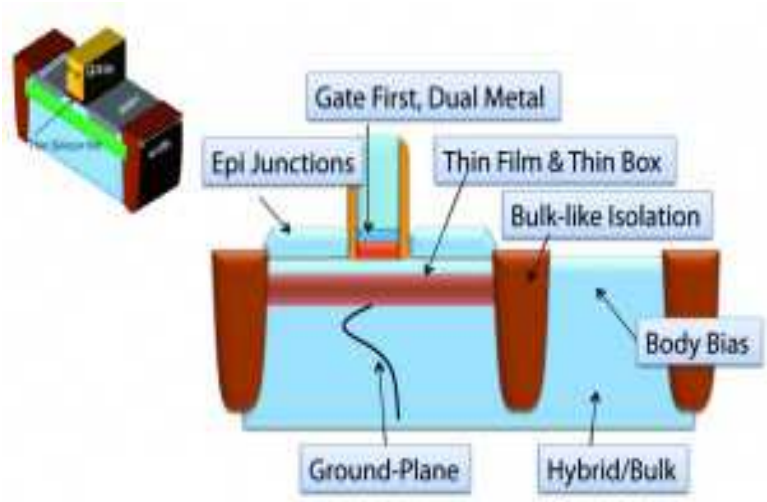


Figure 4.11: Ultra-thin-body and Box (UTBB) MOSFET structure (STMicroelectronics, IEEE SOI Conference 2011).

One example is pointed out in (Skotnicki, 2011) where results have indicated that fully depleted (FD) SOI UTBB could be as good as the FinFETs for mobile multimedia systems-on-chips (SOC) and could be competitive at 28 nm technology node and beyond. Devices with 7 nm thin silicon film thickness and 25 nm buried oxide thickness demonstrate manufacturability.

The following characteristics of FD-SOI UTBB are very attractive when compared to FinFETs: powerful body biasing and efficient multiple V_T control in contrast of no body biasing on FinFETs; simple process and easy SOC migration from traditional Bulk technology, while FinFETs are a new technology and represent a more complex process. A comparison between FinFETs and an extremely-thin FD-SOI (ETSOI) devices is presented in (Lammers, 2011) showing that IBM researchers believe today that the ETSOI are a serious competitor for FinFETs.

4.5 Conclusions

Multi-gate MOSFETs are considered as key to the continuing development of CMOS technologies to meet the targets set by the semiconductor industry. The devices called FinFETs has gained momentum in recent years as a way to relax the complexities required in manufacturing state-of-the-art CMOS devices for advanced node technology like 22 nm down to about 10 nm.

FinFETs are multi-gate MOSFETs with vertical structures and can be manufactured on SOI or BULK substrates. The process flow of SOI-FinFETs (double-gate or triple-gate) is very close related to SOI process flow and the starting wafers can be the same standard SOI material. SOI-FinFETs rely on the SOI technology that has evolved as a need of better performance of BULK technology, but is important to note that Bulk-FinFETs are a viable option.

Both alternatives, SOI-FinFETs and Bulk-FinFETs, show better scalability than planar MOSFETs and have advantages and disadvantages relative to one another. As (Chiarella, 2009) pointed out, in terms of voltage gain and mismatch for analog applications the SOI-FinFET may offer a better choice but in terms of cost of wafers, heat transfer from the channel and compatibility with planar Bulk CMOS devices, the Bulk-FinFET has advantage.

Recently another option has been considered as an alternative to improve the trade-off between complexity-performance and compatibility-cost. The use of FD-SOI with Ultra-Thin Body and Ultra-Thin BOX (UTBB) has made the planar SOI technology competitive with SOI-FinFETS and Bulk-FinFETs.

5 DOUBLE-GATE SOI-FINFET SIMULATION

This chapter describes a basic double-gate n-type SOI-FinFET structure (Chau, 2002) as a reference device and presents the results and analysis of a 3D-numerical simulation of this device. The effects of varying key technological parameters of the FinFET are investigated in this chapter. In the first part of this simulation study only the influence of the variation of the silicon fin thickness and the silicon fin doping on the SOI-FinFET I-V characteristics are investigated. The second part addresses the influence of the variation of the physical gate length and the silicon fin doping. In the third part, several improvements on the 3D structure of the FinFET are implemented and only an undoped fin is used. Finally, the last part presents comparative results between different 3D numeric device simulators, namely Davinci (Synopsys, 2006) and Sentaurus (Synopsys, 2009), and simulation results of the effects of S/D extension implantation methods.

5.1 Basic SOI-FinFET Structure

In the last chapter the basic structure of the single and multi-finger SOI-FinFET was shown and some aspects of his fabrication were put in evidence. In order to perform a 3D-numerical simulation study of this ultra-thin-body nano-device, a basic SOI-FinFET structure, based on technology standards, was defined. This structure and its principal geometric characteristics are shown in Figure 5.1. Figure 5.1(a) shows the gate, gate oxide, silicon fin and silicon fin extensions (source and drain), buried oxide (called "BOX" for short) and silicon substrate; Figure 5.1(b) shows the top-gate, two lateral-gates, lateral-gate extension, top-gate oxide, lateral-gate oxide (both sidewalls of the fin) and fin extension (e.g., drain). The source and drain pads, that can be seen in Figure 4.5 of Chapter 4, were omitted for the sake of simplicity and reasonable computational times.

The SOI-FinFET structure shown in Figure 5.1 is, in fact, a triple-gate device for the gate acts on both lateral and top sides of silicon fin (Chau, 2002; Doyle, 2003). A double-gate control is obtained setting the top-gate oxide much thicker than the lateral-gate oxide, avoiding the influence of the top-gate surface on device characteristics. This top-gate (cap) oxide acts like a "hard mask" before the etching of the silicon fin and avoids the formation of parasitic inversion regions at the top of the fin, particularly in the top corners, called "corner effects" (Burenkov, 2003; Xiong, 2003). Parasitic corner effects are not investigated in this work.

The critical dimensions of this basic SOI-FinFET structure and the values used in the simulations are shown in Figure 5.2. They are: the physical gate length L_G, the source or drain (S/D) extension length L_{SD}, the lateral-gate oxide thickness t_{ox}, the top-gate oxide thickness t_{ox_top}, the buried oxide thickness T_{Box}, the silicon fin height H_{fin},

and the silicon fin thickness T_{fin}. T_{fin} sometimes is referred to as W_{fin} or silicon fin width. In this work, however, T_{fin} is used instead of W_{fin} to avoid confusion with the gate and effective or equivalent gate width (e.g., $W_{eff} = 2.H_{fin}$ for the double-gate SOI-FinFET).

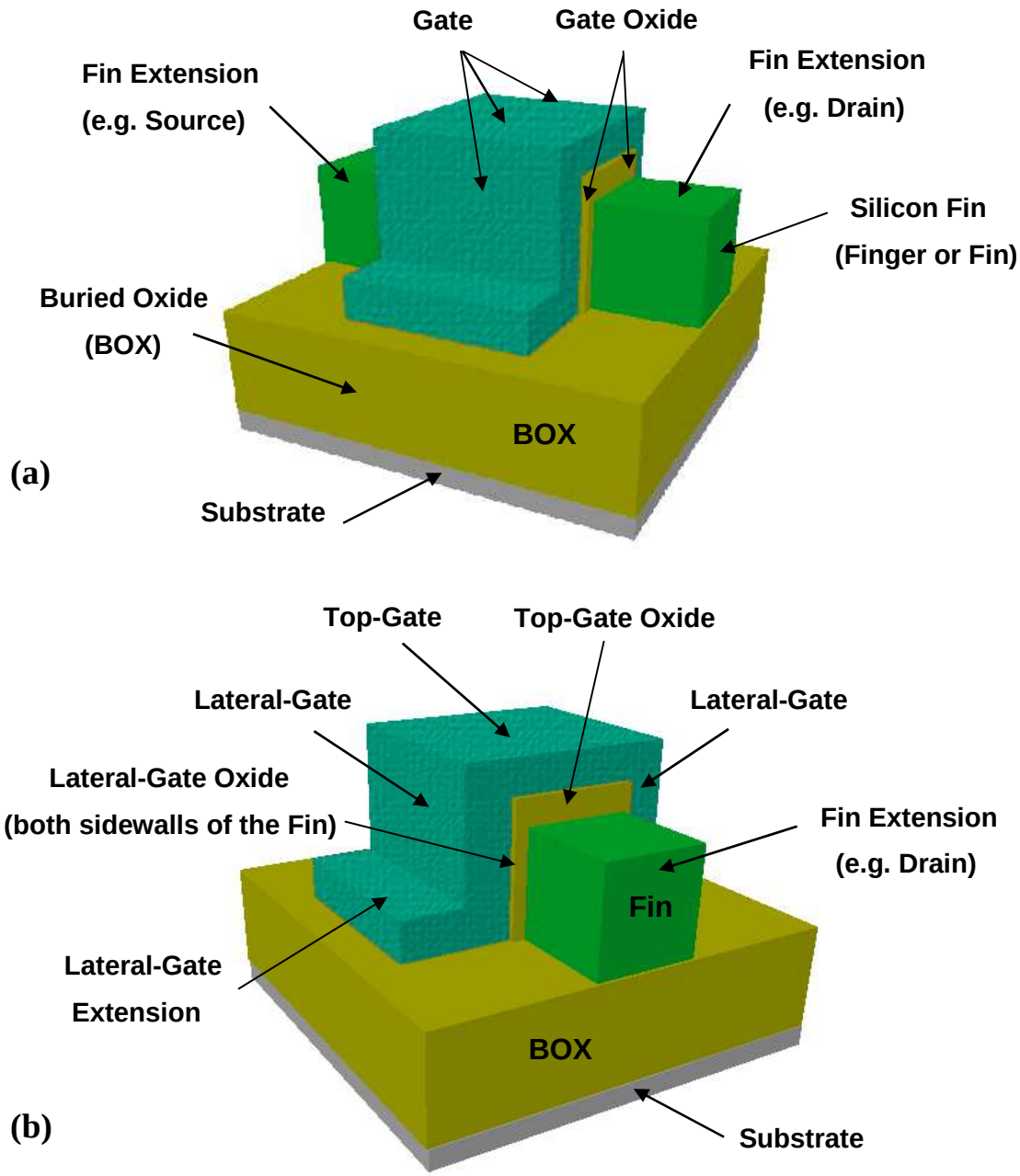
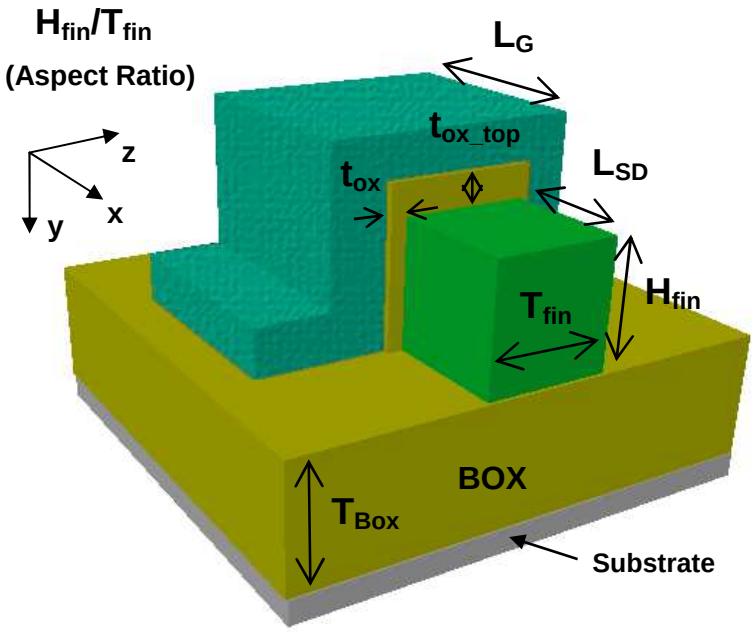


Figure 5.1: Basic SOI-FinFET structure: (a) the gate, gate oxide, silicon fin ("finger" or "fin"), silicon fin extensions (source and drain), buried oxide and silicon substrate; (b) the top-gate, two lateral-gates, lateral-gate extension, top-gate oxide, lateral-gate oxide (both sidewalls of the fin) and fin extension (e.g., drain).

The values of the critical dimensions used in the first part of the simulations are explained next.



Critical Dimensions:

- **t_{ox} = 2 nm (t_{ox_top} → ∞)**
- **H_{fin} = 60 nm**
- **T_{fin} from 20 to 200 nm**
- **T_{Box} = 150nm**
- **L_G = 1µm**
- **L_{SD} = 0.25µm**
- **W_{eff} = 2xH_{fin} (double-gate)**

Figure 5.2: Basic SOI-FinFET structure with critical dimensions indicated and the values used in the simulations.

Since only T_{fin} variations are now considered, T_{Box} is set at 150 nm, H_{fin} is set at 60 nm, t_{ox} is set at 2 nm and t_{ox_top} is consider much thicker than t_{ox}. In fact, in the simulation structure described in the next section, the top-gate and top-gate oxide are deleted. These values are currently used in SOI-FinFET fabrication. For now, second-order effects such as the gate-leakage current and short-channel effects are avoided. L_G is set at 1 µm (long-channel device) and L_{SD} is set at 0.25 µm. T_{fin} ranges from 20 to 200 nm, which means an aspect ratio H_{fin}/T_{fin} from 0.3 to 3. The aspect ratio of the fin is an important geometric parameter and is depicted in Figure 5.2. For a double-gate SOI-FinFET $W_{eff} = 2H_{fin}$ what defines, in principle, the basic drive current capability.

5.2 Double-Gate Structure Simulation

5.2.1 Description of the Structure

Based on the 3D SOI-FinFET structure and critical dimensions defined in the last section, a simplified 3D simulation structure of a double-gate SOI-FinFET was defined. This structure, herein referred to as “Structure-I”, is shown in Figure 5.3 and is simplified for the sake of simplicity and reasonable computational times. The lateral-gate extensions were omitted and only areas located below silicon fin were considered. The top-gate that connects the two lateral-gates was removed and the connection between gates is set by boundary conditions set in the simulation software tool. Also the

top-gate oxide was removed since it is supposed to be much thicker than the lateral-gate oxide.

After determining the simulation structure to be used, the initial simulation grid is specified according the chosen dimensions of the last section. For each value of T_{fin} a different grid is obtained. The type of materials is specified and the silicon fin area and oxide (gate and BOX) areas are defined along with the positions of the electrodes of source, drain, gate and substrate. The doping concentrations are defined now. Considering first the doping of the active area of the silicon fin N_{fin}, which has to be p-type ($N_{fin} = N_A$) for an n-type SOI-FinFET, three cases are initially analyzed: $N_{fin} = 6x10^{17}\ cm^{-3}$, $N_{fin} = 2x10^{18}\ cm^{-3}$ and $N_{fin} = 6x10^{18}\ cm^{-3}$. The doping concentrations are the large-area average doping of the silicon film over the buried oxide.

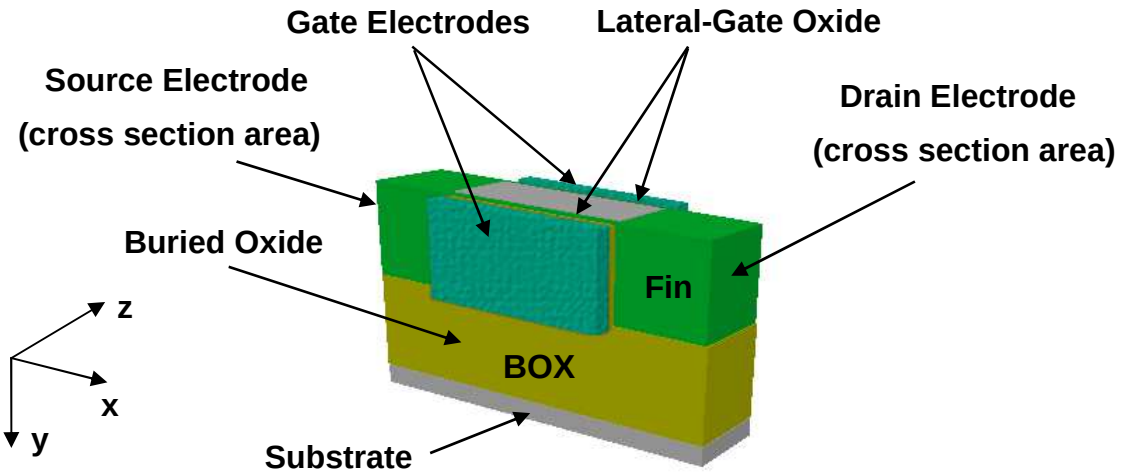


Figure 5.3: SOI-FinFET structure used to define the simulation grid - Structure-I.

The source-drain (S/D) extensions of the fin (nano-wire) need very accurate modeling since this portion of the device is very important to the final I-V characteristics and represents one main challenge for nanoscale FinFETs. Avoid non-uniformities of dopants across the fin height is a goal, but difficult to achieve in real and practical ion implantation (I/I) conditions. In real process, tilted I/I with an angle (α_I) with respect to the perpendicular of fin top surface (y-axis) are used in practice. An ideal case of S/D extension doping using an ion implantation angle (α_I) of 90º on both sidewalls of the fin is considered in the simulations and is depicted in Figure 5.4. Also ideal Gaussian and complementary error function (Erfc) profiles are considered.

Considering then these ideal conditions, the S/D extensions are doped with two Gaussian profiles with the typical expression: $N(z)=N_o.\exp(-[(z-R_p)/\lambda_z]^2)$, perpendicular to the sidewalls of the silicon fin (z-axis), where N_o, R_p and λ are the peak concentration, the projected range, and the characteristic length, respectively. The characteristic length is related to the standard-deviation σ or ΔR_p "straggle" by $\lambda = \sqrt{2}\,\Delta R_p$.

A peak concentration $N_o = 1x10^{19}\ cm^{-3}$ at the interface of silicon ($R_p = 0$) is used with a characteristic length $\lambda_z = 6.5$ nm, resulting in an initial 10 nm/dec ratio. The

doping along z-axis results in a lateral profile along x-axis. To describe this lateral profile, an Erfc function is used with a characteristic length λ_x = 2 nm, resulting in an initial 2.33 nm/decade ratio and an effective channel length shortening ΔL of approximately 5.4 nm, 3.6 nm and 1.5 nm, respectively for $N_{fin} = 6x10^{17}$ cm^{-3}, $N_{fin} = 2x10^{18}$ cm^{-3} and $N_{fin} = 6x10^{18}$ cm^{-3}.

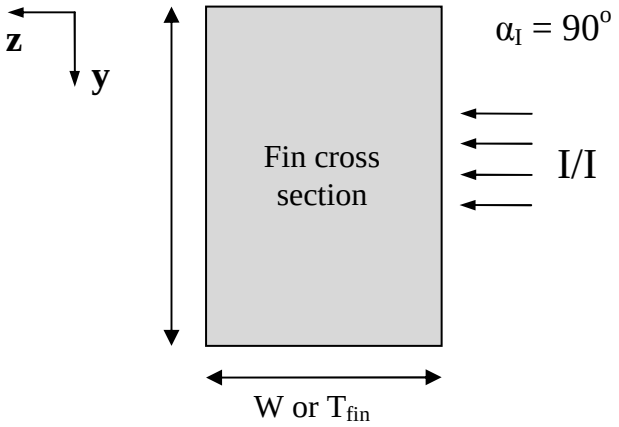


Figure 5.4: Silicon fin cross-section considering an ideal case of ion implantation (I/I) angle α_I of 90º.

The final 3D simulation structure with grid (for a given value of T_{fin}), doping profiles and electrodes definition are shown in Figure 5.5. The typical doping profiles used in the S/D extensions are shown in Figure 5.6, using the left one (e.g., source) as example.

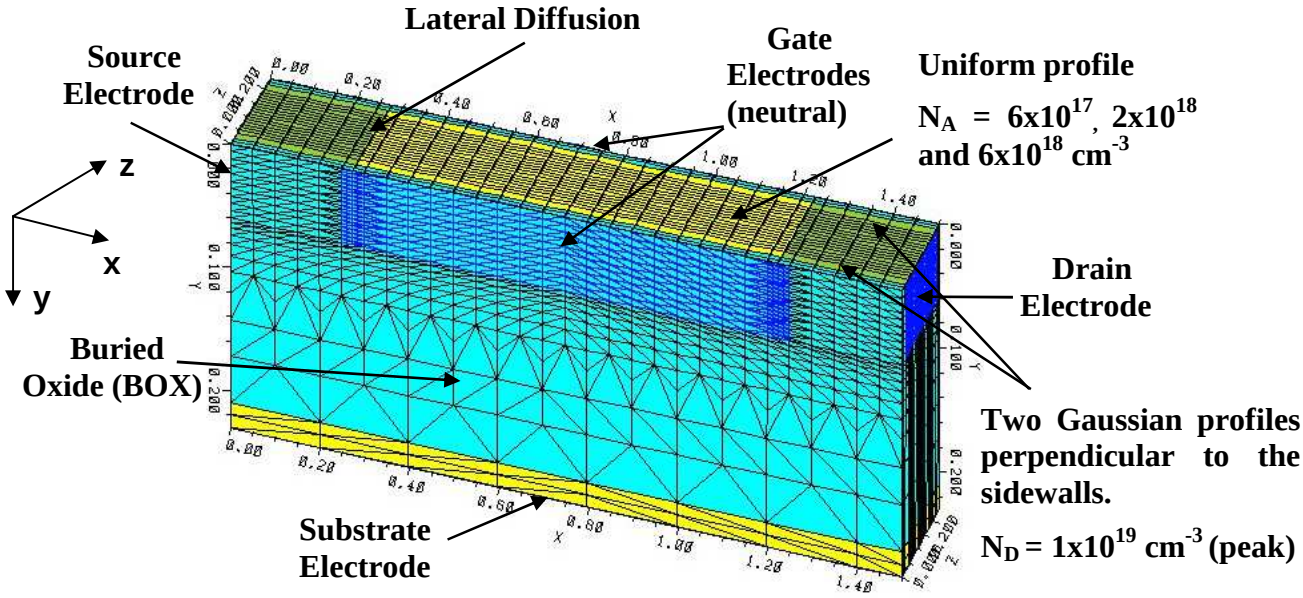


Figure 5.5: Simulation grid for the double-gate SOI-FinFET structure. Doping profiles and terminal electrodes are indicated.

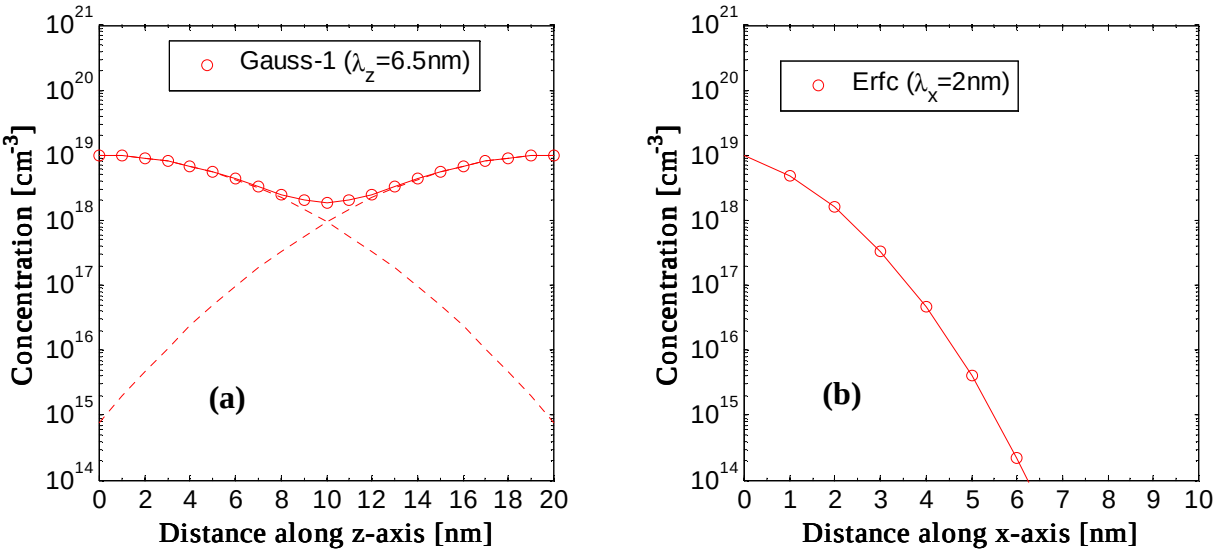


Figure 5.6: Doping profiles for the S/D extensions (e.g., left one): (a) Two Gaussian profiles along z-axis (T_{fin} = 20 nm), with left and right limits at gate-oxide/silicon fin interface; (b) Erfc profile along x-axis with zero reference point set at the beginning of gate-electrode.

The source, drain, gate and substrate (below BOX) contacts are defined as neutral. By setting the gate contact to neutral in the simulator, the gate electrode work-function is set to mid-gap. This is an ideal structure, since the materials complexity of the metallurgy of a specific metal gate is not within the scope of our work. The definition of gate electrode work-function is a key to the achievement of controlled enhancement-mode complementary devices.

The grid is refined two times following a refinement criterion of include a new grid point where a particular variable exceed some value. The first refinement is achieved considering the doping concentration variation and the second, after a preliminary zero voltage solution (all terminal electrodes are grounded), is achieved considering the electrostatic potential variation.

5.2.2 Davinci Simulation Models

The simulator Davinci provides several mobility model choices that can be classified into three categories:

• Low Field Mobility

• Transverse Field Mobility Degradation

• High Parallel Field Mobility

The following models were used in the simulations referred herein:

- Concentration-dependent Mobility Model (CONMOB): A low field mobility model that includes the effect of impurity scattering by using mobility values from tables which depend on the local total impurity concentration. The table values may be modified by the simulator user. The default values were used in the simulations herein presented.

- Surface Mobility Model (SRFMOB): This is a transverse field mobility model. Due to surface scattering along insulator-semiconductor interfaces the carrier mobility is substantially lower than in the bulk of the semiconductor. Davinci allows surface mobility degradation factors and the selection of an effective-field based surface mobility model that is applied only at insulator-semiconductor interfaces. It is important to note that a low-field mobility model should be selected to properly model current flow away from the surface.

- Field-dependent Mobility Model for High Electrical Fields (FLDMOB): A parallel field mobility model that accounts for effects due to high field in the direction of current flow, such as carrier heating and velocity saturation effects. Davinci uses analytic expressions for the drift velocity as a function of the electric field in the direction of current flow.

Quantum mechanical effects are very important for deep submicron devices, especially FinFETs with a extremely narrow silicon fin, in which quantum confinement causes distortion of the electron waves with respect to the bulk silicon band structure. Silicon wires with thickness around 10 nm and below ($T_{fin} \leq 10$ nm) are at the scale of the thermal electrons/holes wavelengths, and the wave nature of electrons and holes can no longer be neglected. The quantization of electron motion in the inversion layer affects carrier distribution and also all the relevant electrical model parameters, like the threshold voltages, terminal currents, C-V characteristics, etc. The solution of Schrödinger's equation is needed to correctly account for such effects, but it is extremely time consuming and approximate methods are useful in many situations. Davinci program has basically two options regarding quantum mechanical effects in MOSFET inversion layers: (1) using the van Dort's bandgap widening approach (van DORT, 1994) and (2) an alternative model based in the modified local density approximation (MLDA) that is capable of calculating the confined carrier distributions that occur near Si/SiO_2 interfaces (Paasch, 1982). The first option was used in the simulations:

- Quantum Mechanical Effects in Inversion Layer (QM.PHILI): An approximate method of accounting for quantum mechanical effects in the inversion layer using the van Dort's bandgap widening approach (van DORT, 1994).

5.2.3 Simulation Results

After the definition of both the basic n-type double-gate SOI-FinFET structure and the simplified simulation structure, a set of simulations were carried out under several terminal voltage conditions. For now, only I_D-V_G characteristics in the linear region are addressed. The drain electrode voltage V_D is set at 100 mV. Since L_G is very long (1 μm channel length) a condition of low longitudinal electrical field is also achieved. The voltages of the source and substrate electrodes V_S and V_B are grounded. Once a particular solution is obtained for a given set of terminal voltages, important quantities in the device structure such as electrostatic potential, electric field, electron and hole concentration can be analyzed. The terminal currents of each electrode are also available for analysis. A good qualitative analysis tool is the 3D contours of a chosen variable, although this tool of Davinci has many limitations in the manipulation of the 3D object view. For example, Figure 5.7 shows electrostatic potential contours obtained from a simulation solution for $V_G = 0.5$ V and $V_D = 100$ mV (other terminal voltages grounded) for the n-type double-gate SOI-FinFET structure. In this work, however, the

focus will be in the analysis of the terminal currents, which lead to the I-V characteristics of the device.

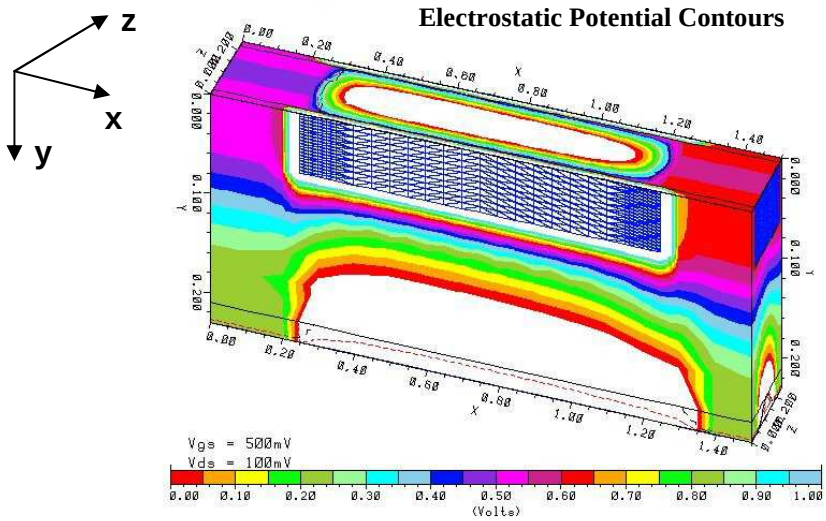


Figure 5.7: Potential contours obtained from a simulation solution for V_G = 0.5 V and V_D = 100 mV for the n-type double-gate SOI-FinFET structure.

In the first run of simulations, N_{fin} is set at $6x10^{17}$ cm^{-3} with T_{fin} of 20, 50, 100, 150 and 200 nm, H_{fin} = 60 nm and t_{ox} = 2 nm. The simulated I_D-V_G characteristics in the linear region are shown in Figure 5.8 (linear scale) and Figure 5.9 (log scale) for different values of T_{fin}. The currents are normalized by the effective FinFET (double-gate) channel width (W_{eff} = $2H_{fin}$) to facilitate the comparison with single-gate MOSFETs.

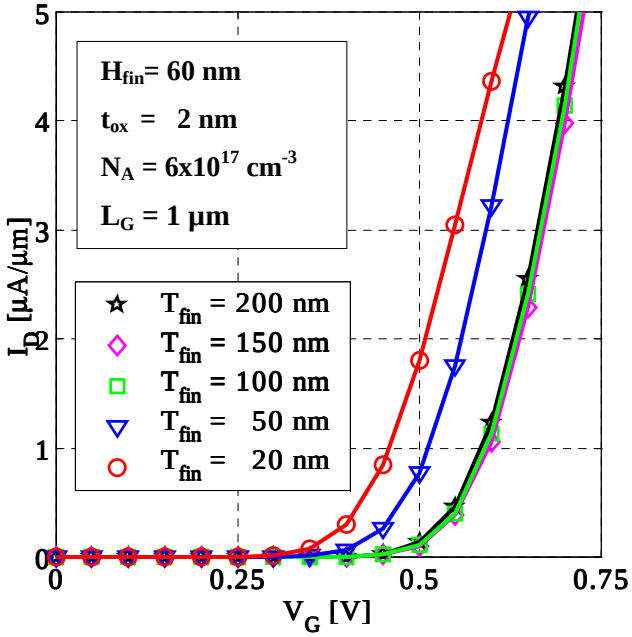


Figure 5.8: I_D-V_G characteristics (long-channel FinFET) for different values of silicon fin thickness T_{fin} (L_G = 1 µm).

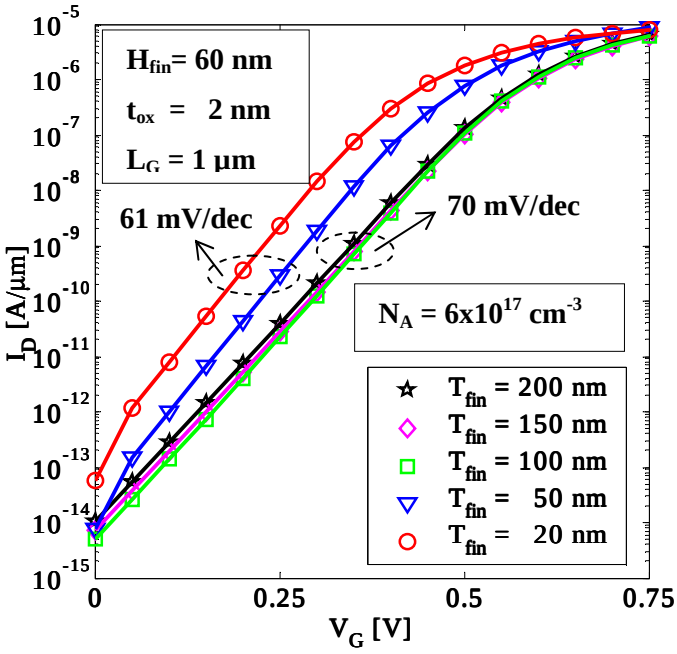


Figure 5.9: I_D-V_G characteristics (long channel FinFET - log scale) for different values of silicon fin thickness T_{fin} (L_G = 1 µm).

The threshold voltages V_T were extracted by three different methods, named methods "LE", "SD", and "GMLE" for short, and explained in Appendix A. For now only the values obtained by method "GMLE" are presented. The subthreshold slopes S were extracted by linear fitting of the log(I_D)-V_G curves in the linear portion of the subthreshold. The values of V_T and S for "Structure-I" were extracted from Figure 5.8 and Figure 5.9 and are shown in Figure 5.10 and Figure 5.11, respectively, as a function of T_{fin}. These results are summarized in Table 5.1.

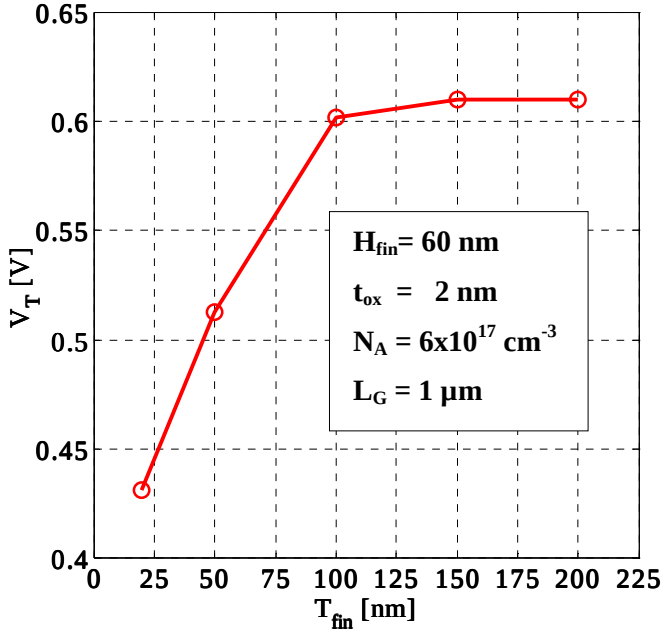


Figure 5.10: Threshold voltage V_T vs. silicon fin thickness T_{fin} (method "GMLE").

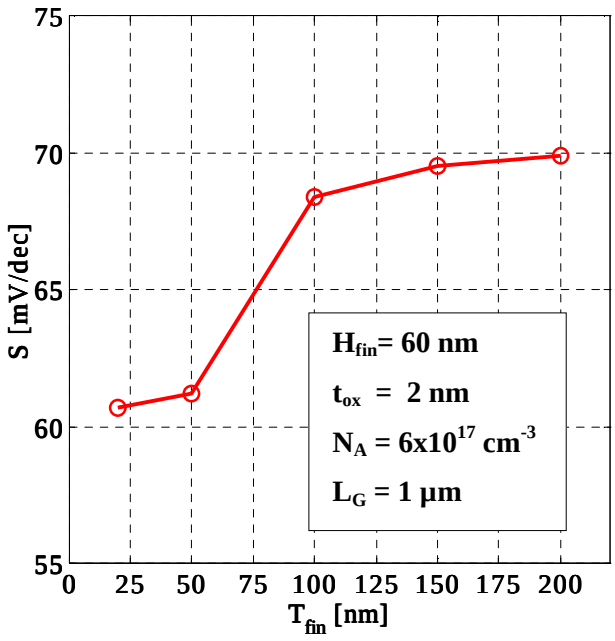


Figure 5.11: Subthreshold slope S vs. silicon fin thickness T_{fin}

Considering first the threshold voltage V_T, it is observed that V_T increases as T_{fin} increases and tends to saturate in the transition from fully-depleted (FD) to partially-depleted (PD) fins. The transition occurs around $T_{fin} = 100$ nm (see Figure 5.8 and Figure 5.10). As T_{fin} decreases the total depletion charge Q_D contribution to V_T decreases and becomes small compared to the contribution of the gate electrode to silicon work-function difference ϕ_{ms} and tends to be negligible. This dependence of V_T can be better understood regarding the following expression (Tsividis, 1987) which is normally used for a long-channel MOSFET.

$$V_T = \phi_{ms} + 2\phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{5.1}$$

where ϕ_f is the Fermi potential; C_{ox} is the oxide capacitance per unit area; and Q_{ox} is the gate oxide charge per unit area.

This agrees with a depletion approximation analysis of a SG-MOS structure where the maximum width of the semiconductor space-charge region x_{dmax} is taken at the onset of strong inversion. However, for fins thin enough a quantum effect of electron quantization energy has to be considered (Colinge, 2007). In fact, this effect can lead to an opposite behavior, with an increase of V_T as T_{fin} decreases, and an additional term in equation (5.1). These quantum-mechanical effects are not subject of this work. The gate oxide charge contribution to V_T can be considered small and in this case negligible. For large T_{fin} and high $N_A(=N_{fin})$ equation (5.1) tends to be more accurate.

Regarding now the subthreshold slope, S is greatly affected in the transition from FD to PD fins (see Figure 5.9 and Figure 5.11). This behavior can be expected since partially-depleted thin-film SOI-MOSFETs exhibit a BULK behavior with a greater S value.

Now considering the dependence of V_T on N_A (N_{fin}), Figure 5.12 and Figure 5.13 show the I_D-V_G characteristics (L_G = 1µm, long-channel FinFET) for different N_A, with T_{fin} = 20 nm, t_{ox} = 2 nm. The values of V_T are show in Figure 5.14 as a function of N_A.

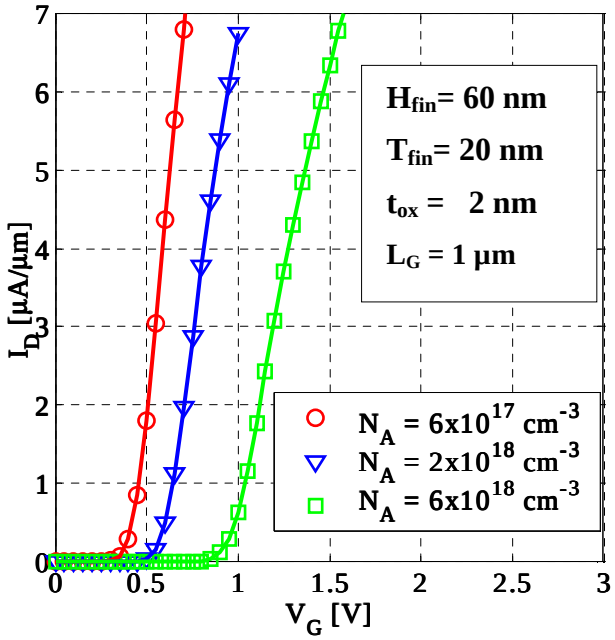


Figure 5.12: I_D-V_G characteristics (lin. scale) for different values of N_A.

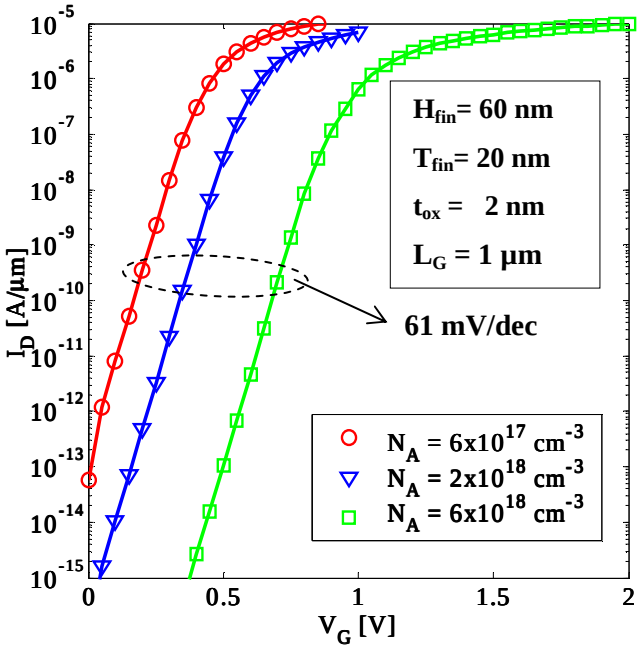


Figure 5.13: I_D-V_G characteristics (log. scale) for different values of N_A.

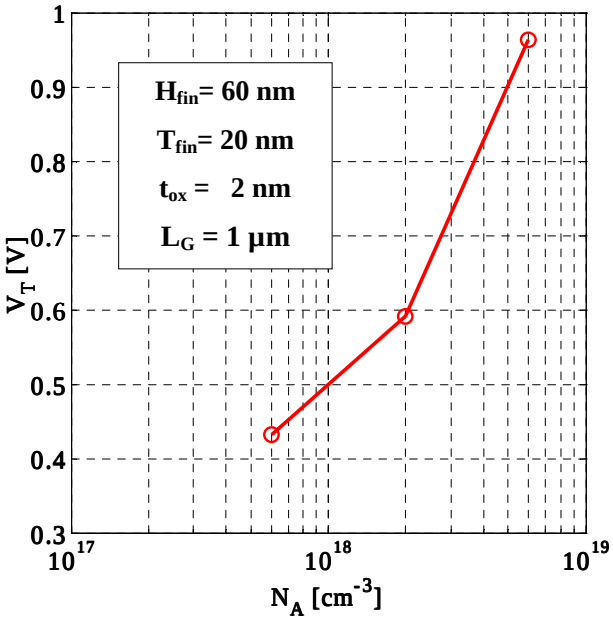


Figure 5.14: Threshold voltage V_T vs. silicon fin doping N_A (method "GMLE").

As N_A increases the total depletion charge Q_D contribution to V_T increases. The subthreshold slope S is not significantly affected as the fin remains FD (see Figure 5.13). An analysis of the electrostatic potential has shown that a fin doping around $1x10^{19}$ cm^{-3}, for the structure to which Figure 5.12 refers to, appears to be the limit between a FD and a PD fin of 20 nm width. A depletion approximation analysis of a SG-MOS structure where the maximum width of the semiconductor space-charge region (x_{dmax}) is taken at the onset of strong inversion can also be used to predict this limit, as in the case of dependence of V_T on T_{fin} mentioned earlier in this section.

The results of the 3D-numerical simulation done with Davinci simulator tool for the SOI-FinFET are summarized in Table 5.1. It is clear that for CMOS applications with low V_{DD} (less than 1.0 V) the V_T is too high (0.5 V or higher) and in the next simulations it will be consider an effectively thinner SiO_2 equivalent oxide, by using higher-k insulator around the fin (see section 5.4).

The effects of random dopants fluctuations are very important. The results above do not consider an important effect that, in practical terms, may render the mid-range doping of 10^{17} to 10^{18} cm^{-3} unsuitable for circuits on which T_{fin} is below 20 nm and channel length is aggressively scaled below 20 nm. Table 5.2 shows the ideal average number of dopants in a silicon fin volume of 20 nm x 60 nm x L_G of a FinFET transistor.

The results indicate that, for FinFET technologies below 22 nm, the undoped case is the most practical, since the actual threshold voltage will depend mostly on the gate work-function and silicon fin width only. Random-doping problems and corner-effects can be neglected in undoped FinFETs (Fossum, 2003, 2007). In the next section, it will be consider very lightly doped silicon fins, with typical doping on the order of $1x10^{15}$ cm^{-3}. The many-dopants case will have doping densities of $6x10^{17}$ cm^{-3}, which

will be far worse for the reason of doping atom fluctuation in the fin, both in random numbers and random positioning within the fin.

Table 5.1: Threshold voltage V_T (method "GMLE") and Subthreshold slope S for different values of silicon fin thickness T_{fin} and fin doping N_A or N_{Fin}. Bold figures are related to the dependence of V_T and S on N_A (L_G = 1 µm).

V_T (V)	S (mV/dec)	T_{fin} (nm)	t_{ox} (nm)	N_A (cm^{-3})
0.61	70	200	2	$6x10^{17}$
0.61	69	150	2	$6x10^{17}$
0.60	68	100	2	$6x10^{17}$
0.51	61	50	2	$6x10^{17}$
0.43	**61**	20	2	**$6x10^{17}$**
0.59	**61**	20	2	**$2x10^{18}$**
0.96	**61**	20	2	**$6x10^{18}$**

Table 5.2: Ideal average number of dopants in a silicon fin volume of 60 nm x 20 nm x L_G of a FinFET transistor (e.g., H_{fin} = 60nm, T_{fin} = 20nm).

N_{fin} [cm^{-3}] \ L_G [nm]	10	20	50	1000
$1x10^{15}$	0.012	0.024	0.061	1.212
$6x10^{17}$	7.212	14.42	36.06	721.2
$2x10^{18}$	24.12	48.24	120.6	2412

5.3 Improvements on the Double-Gate Structure - Simulation for Ultra-Short Gate Lengths

In this section, several improvements on the 3D modeling of the FinFET are shown. A new 3D FinFET structure is defined, similar to Figure 5.3, herein referred to as "Structure-II". Figure 5.15 shows this new simulation structure. The top-gate that connects the two lateral-gates is not removed and a top-gate oxide t_{ox_top} of 20 nm is considered. Now there is a gate electrode covering the top of the fin, which is the realistic case for production double-gate devices in practice and renders the structure a de-facto double-gate device. The effects of longitudinal channel length reduction are also considered and simulated. It is important to consider that, for ultra-short FinFETs,

the device characteristics are also influenced by the extrinsic regions (outside the gate region) of the drain and source of the FinFET.

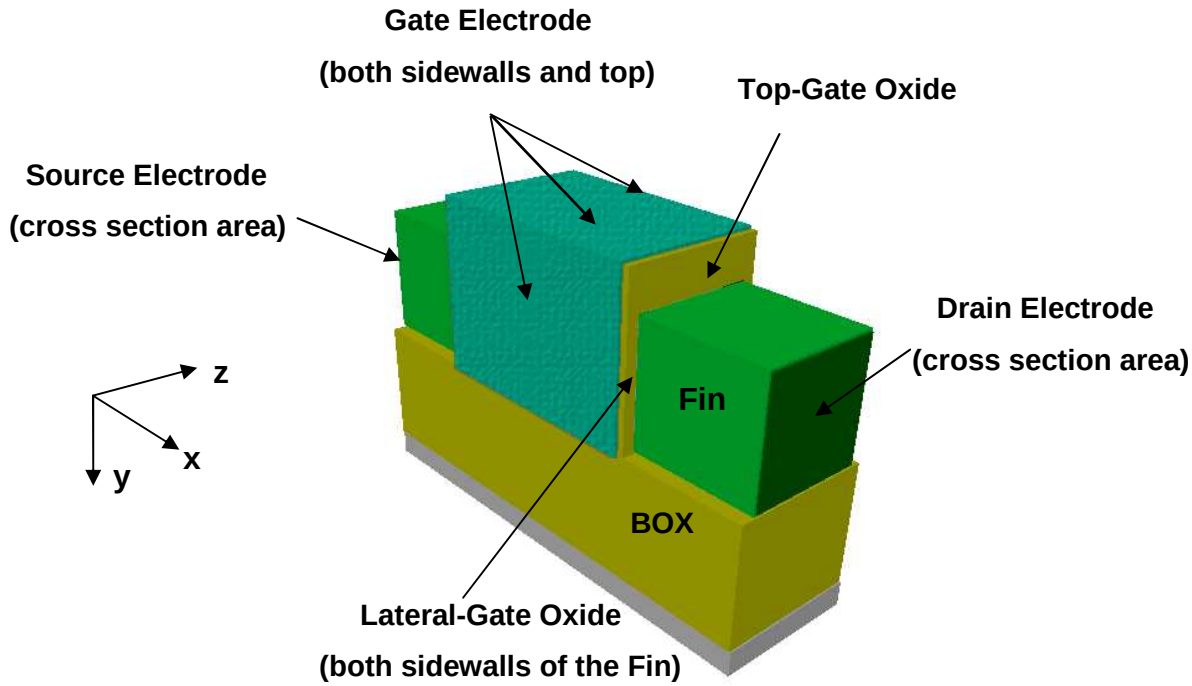


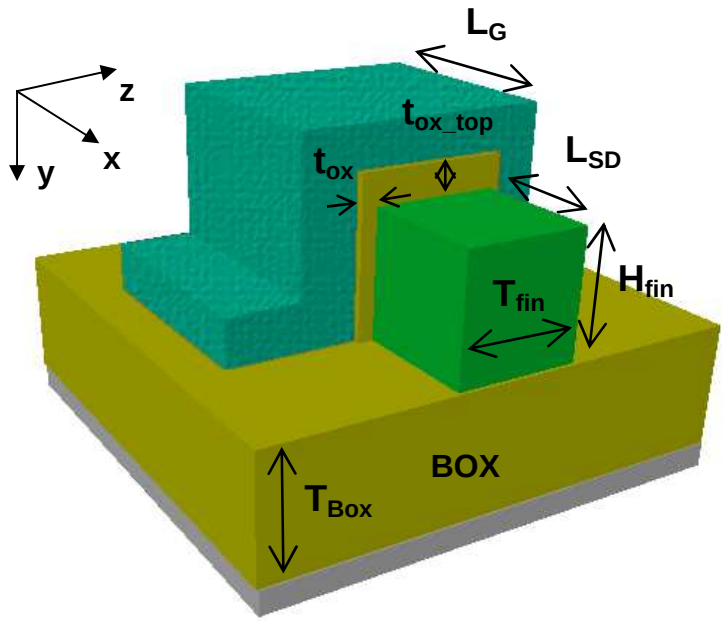
Figure 5.15: SOI-FinFET structure used to define the simulation grid - Structure-II. The top-gate that connects the two lateral-gates is shown.

The values of the critical dimensions used in this section are indicated in Figure 5.16 and are explain next:

The buried oxide thickness T_{Box} and the silicon fin height H_{fin} are 150 nm and 60 nm, respectively, the same as initially defined. The S/D extension length L_{SD} is 25 nm long, compatible with gate lengths around 20 nm; two values of silicon fin thickness T_{fin}, 20 nm and 15 nm, were considered in different device simulations; the lateral-gate oxide t_{ox} is 2 nm and the top-gate oxide t_{ox_top} is ten times (10x) thicker to minimize the influence of the top gate surface on device characteristics; the physical gate length was simulated with L_G from 1000 nm (long-channel FinFET) to 20 nm (short-channel FinFET).

Considering the process parameters and in particular the doping concentration of the active area of the silicon fin N_{fin}, which has to be p-type ($N_{fin}=N_A$) for an n-type SOI-FinFET, two limiting cases are took into account: the zero-doping case, for highly improbable presence of active dopants in the fin, N_{fin} set at $1x10^{15}$ cm^{-3}, and the many-dopants case, or high number (> 10 are highly probable) of dopants present in the active fin, N_{fin} set at $6x10^{17}$ cm^{-3}.

Note that after the actual fabrication of the silicon nano-wire (i.e., fin) the average number of dopants fluctuates over the length of the wire due to its narrow T_{fin} and ultra-thin H_{fin}.



Critical Dimensions:

- **t_{ox} = 2 nm (t_{ox_top} > 10 x t_{ox})**
- **H_{fin} = 60 nm**
- **T_{fin} = 15 and 20 nm**
- **T_{Box} = 150nm**
- **L_G from 20 to 1000 nm**
- **L_{SD} = 25nm**
- **W_{eff} = 2xH_{fin} (double-gate)**

Figure 5.16: Basic SOI-FinFET structure with critical dimensions indicated and the values used in the simulations.

Consider the Table 5.2 presented in the last section (H_{fin}=60nm, T_{fin}=20nm). For the zero-doping case (N_{fin}=1x10^{15} cm^{-3}) and a gate length of 1 µm, there is an average of 1.2 active dopants; with a gate length of 50 nm, there is an average of only 0.06 active dopants. On the other hand, for the many-dopants case (N_{fin}=6x10^{17} cm^{-3}) and a gate length of 1µm, there is an average of 721 active dopants; with a gate length of 50 nm, there is an average of 36 active dopants. Regarding the doping atom fluctuation in the fin, the doping concentration N_{fin} for the many-dopants case could have been set at a higher level than 6x10^{17} cm^{-3}. This particular doping level, however, was used to help the comparison with previous results. A more accurate transport simulation for the intermediate doping cases needs to consider the exact location of the dopant atomic position within the active region. This is a capability that the Davinci tool does not support. As in the previous section, the S/D extensions of the fin are doped with two Gaussian profiles perpendicular to the sidewalls of the silicon fin (z-axis). A peak concentration N_D = 1x10^{19} cm^{-3} is used with λ_z = 6.5 nm, resulting in an initial 10 nm/dec ratio. To describe the lateral profile, an Erfc function is used with λ_x = 2 nm, resulting in an initial 2.33 nm/decade ratio and an effective channel length shortening ΔL of approximately 5.4 nm and 11 nm, respectively for N_{fin} = 6x10^{17} cm^{-3} and 1x10^{15} cm^{-3}.

As differences with respect the previous simulations with the Structure-I, simulations with Structure-II have:

- undoped fin case (N_{fin}=1x10^{15} cm^{-3});
- only two (high) aspect ratios H_{fin}/T_{fin} = 3 and 4 (T_{fin} = 20 nm and 15 nm);
- shorter S/D extension length L_{SD} of 25 nm;
- physical gate lengths L_G from 20 to 1000 nm;

5.3.1 Simulation Results

5.3.1.1 I_D-V_G Characteristics

The following figures in this section show the simulated I_D-V_G characteristics of the SOI-FinFET with improvements on the structure. The bias applied in the simulations was: V_D = 100 mV in the linear region and V_D = 1V in saturated region, with V_S and V_B grounded.

The comparison between the two doping regimes can be seen directly in figures below. Plots "a" depict the many-dopants case ($N_{fin} = 6x10^{17}cm^{-3}$) and plots "b" depict the zero-doping case ($N_{fin} = 1x10^{15}cm^{-3}$). Figure 5.17 and Figure 5.19 show I_D-V_G characteristics in the linear region (linear and log scales, respectively) and Figure 5.18 and Figure 5.20 show I_D-V_G characteristics in saturated region (linear and log scales, respectively). Each plot has four curves for different gate lengths (L_G of 20, 50, 100 and 1000 nm) and T_{fin} = 20 nm.

The degradation of device characteristics for gate lengths below 50 nm is clearly noted in subthreshold regime (log scale), with a sharp increase in subthreshold slope S and DIBL (drain-induced barrier lowering for the electron transport in the fin). A poor I-V characteristic, resulting from large DIBL effect, is observed in I_D-V_G curves (comparing linear and saturated regimes). The devices with L_G of 20 nm, which have effectives L_G (=L) of approximately 14.6 nm and 9 nm, for the many-dopants case and zero-doping case, respectively, due to lateral diffusion ($\Delta L \approx 5.4$ and 11nm), shows very poor off-characteristics. The FinFET for ultra-deep sub-100nm gate length needs to consider thinner t_{ox} and narrower T_{fin} to improve the off-characteristics and make this device circuit-worthy. The reduction of t_{ox} and T_{fin} can alleviate the DIBL problem.

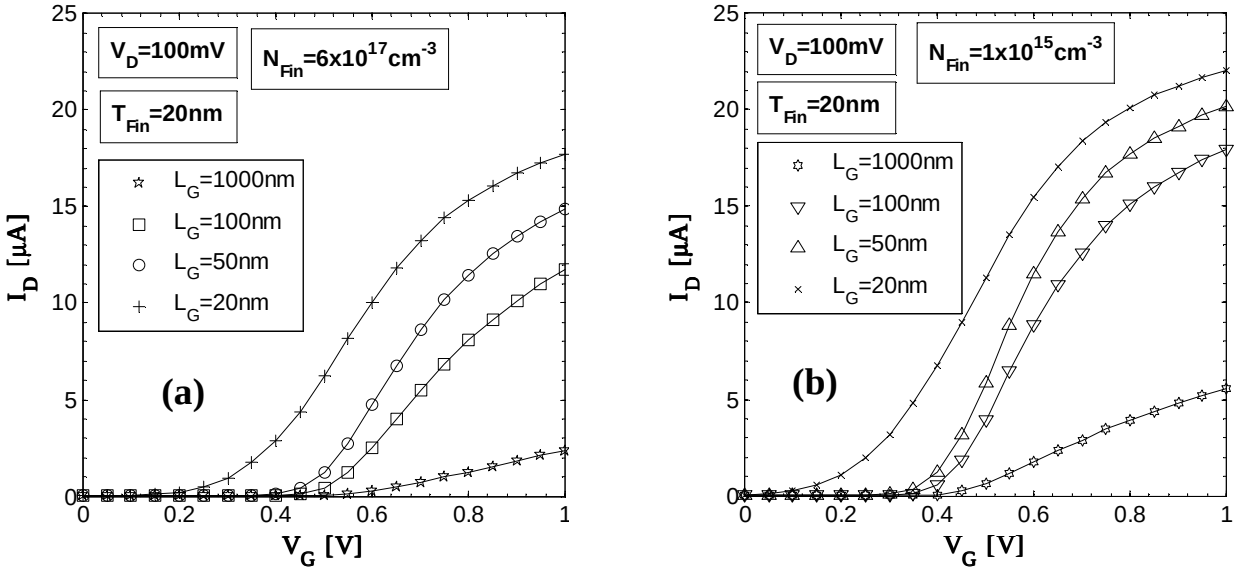


Figure 5.17: I_D-V_G characteristics in the linear region (V_D=100mV) for different values of L_G and T_{fin}=20 nm. (a) $N_{fin}=6x10^{17}cm^{-3}$ and (b) $N_{fin}=1x10^{15}\,cm^{-3}$.

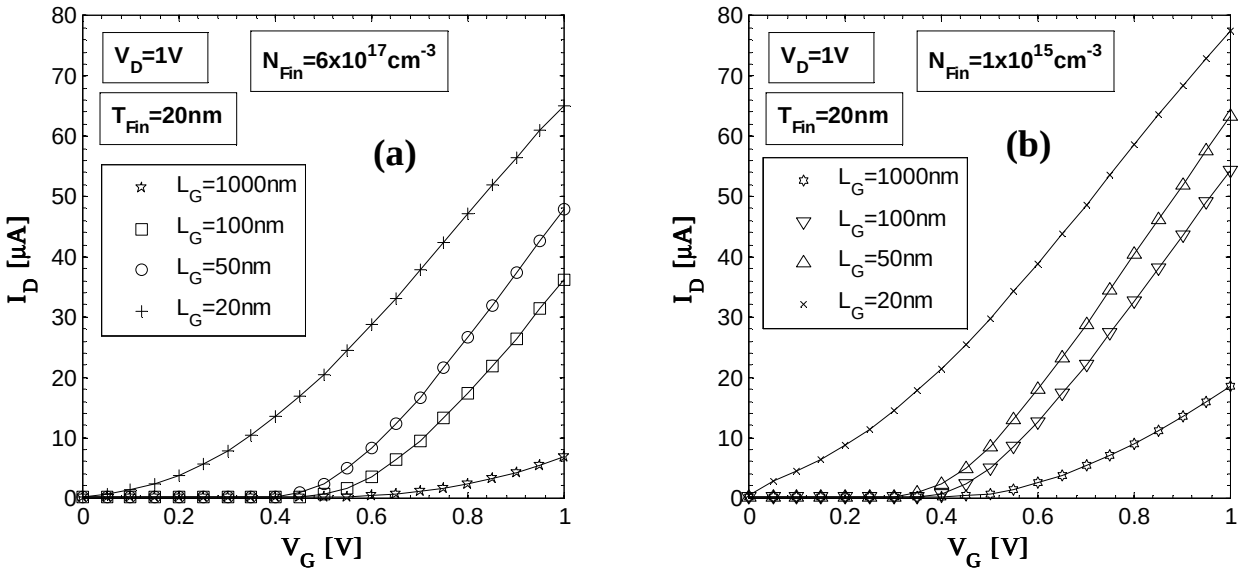


Figure 5.18: I_D-V_G characteristics in the saturated region (V_D=1V) for different values of L_G and T_{fin}=20 nm. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15} cm^{-3}.

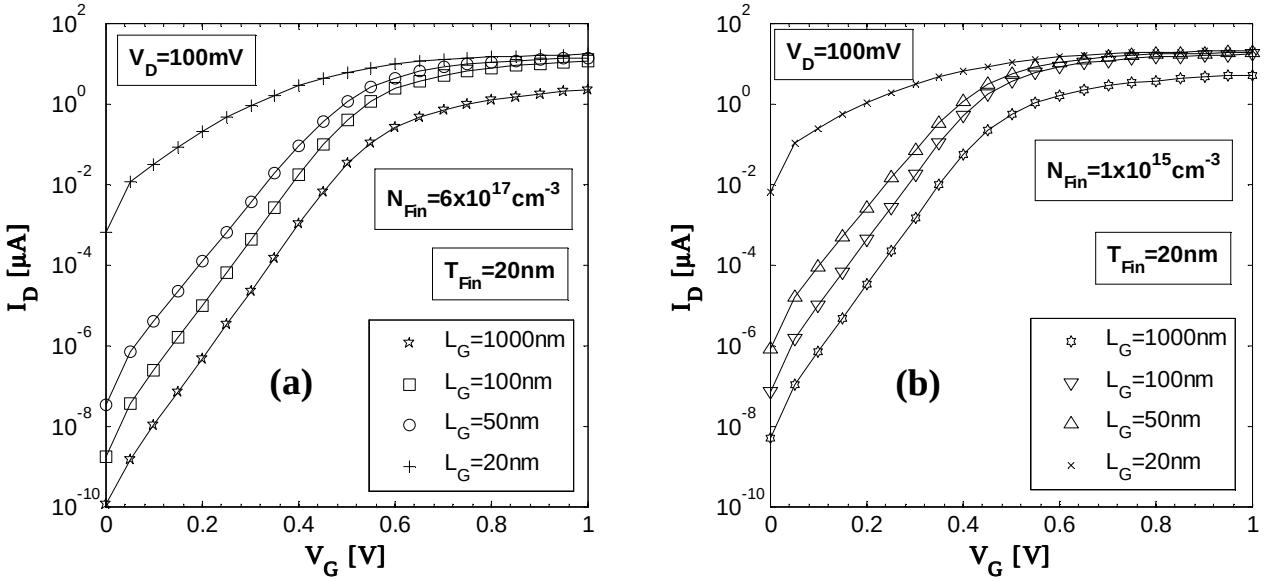


Figure 5.19: I_D-V_G (log) characteristics in the linear region (V_D=100mV) for different values of L_G and T_{fin}=20 nm. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15} cm^{-3}.

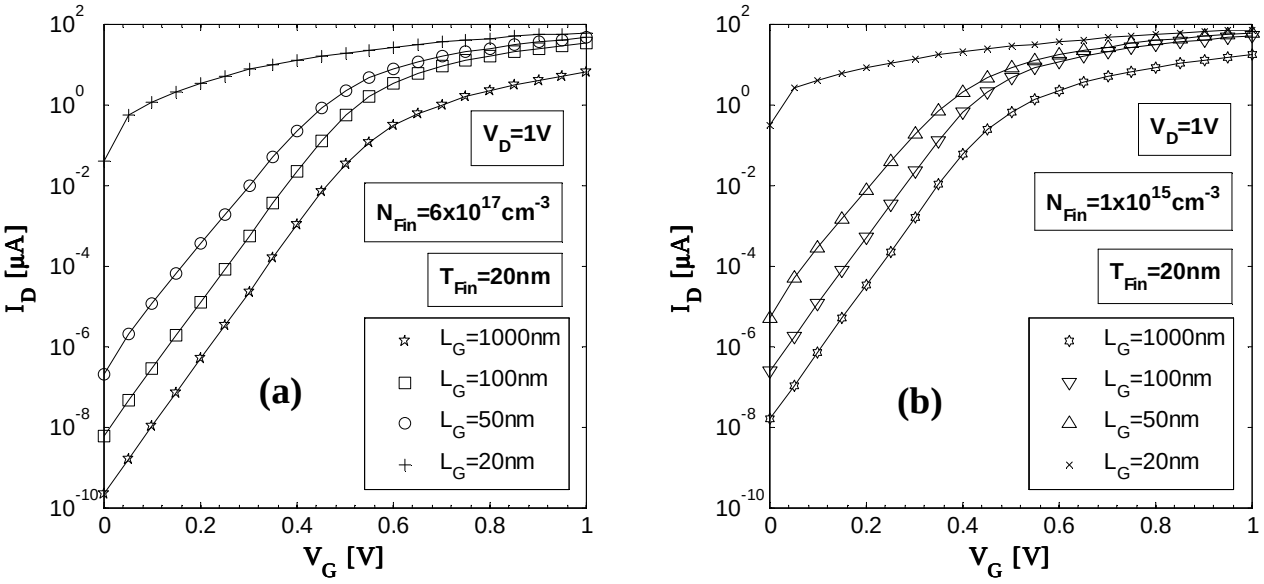


Figure 5.20: I_D-V_G (log) characteristics in the saturated region (V_D=1V) for different values of L_G and T_{fin}=20 nm. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15} cm^{-3}.

The influence of a silicon fin thickness reduction, from T_{fin} of 20 nm to 15 nm, on I_D-V_G characteristics (linear and saturated regions) of the FinFET devices, is shown from Figure 5.21 to Figure 5.24. I_D-V_G characteristics for gate lengths of 50 nm and 20 nm are plotted.

The I-V characteristics for L_G of 50 nm are slightly improved, especially in the zero-doping case. For L_G of 20 nm a good improvement in I-V characteristics is observed. The improvements are noted in subthreshold regime (log scale), with a decrease in subthreshold slope S.

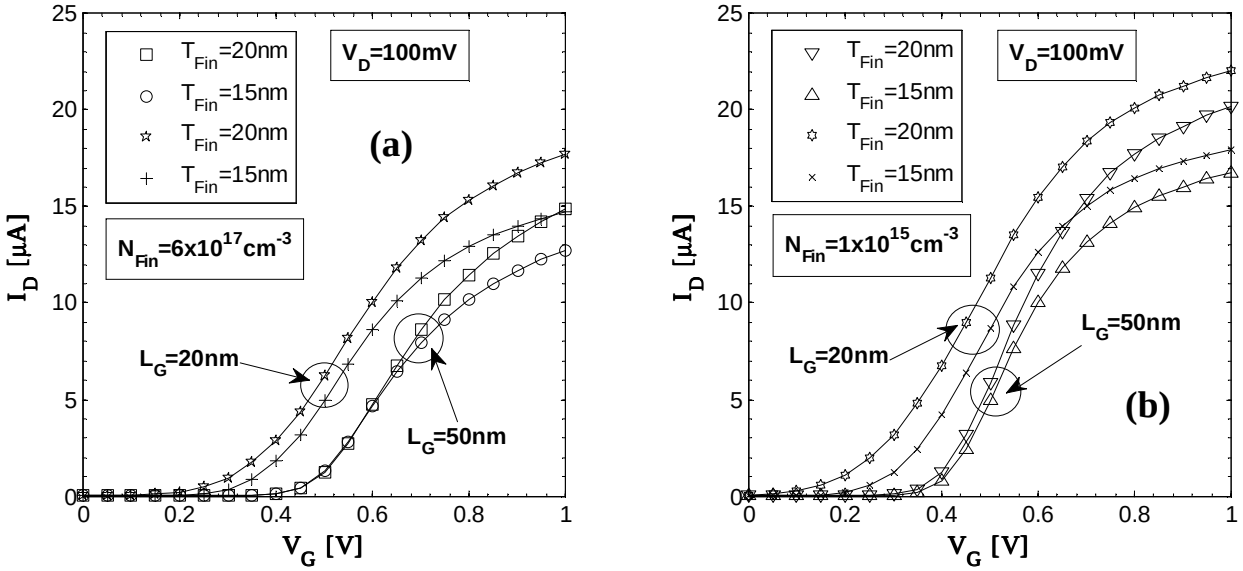


Figure 5.21: I_D-V_G characteristics in the linear region (V_D=100mV) for different values of T_{fin} and L_G. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15}cm^{-3}.

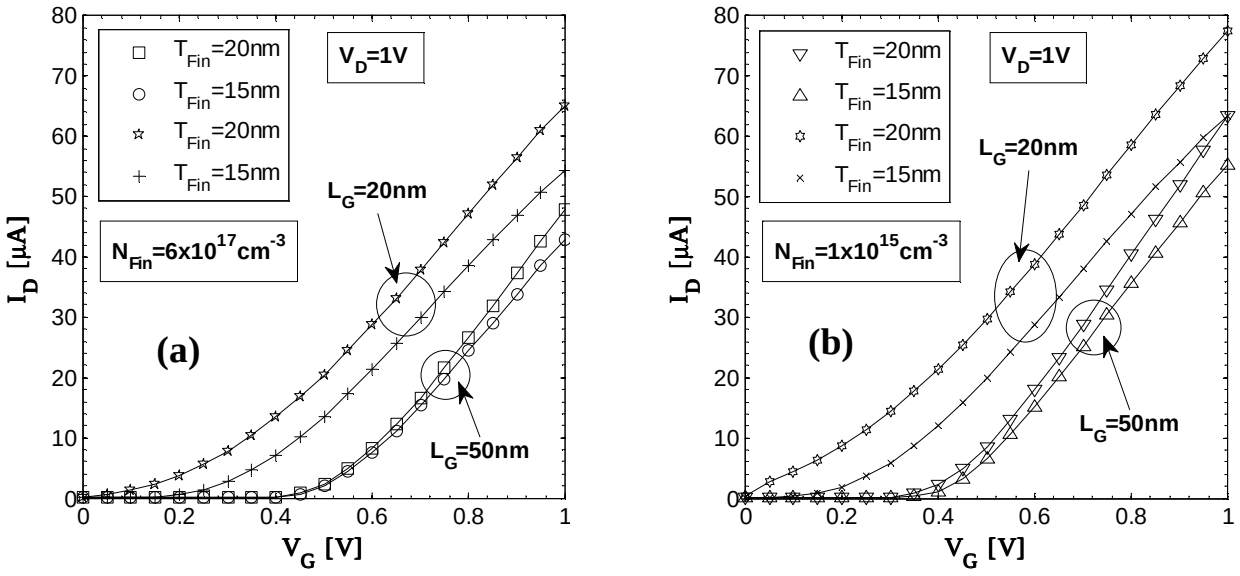


Figure 5.22: I_D-V_G characteristics in the saturated region (V_D=1V) for different values of T_{fin} and L_G. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15}cm^{-3}.

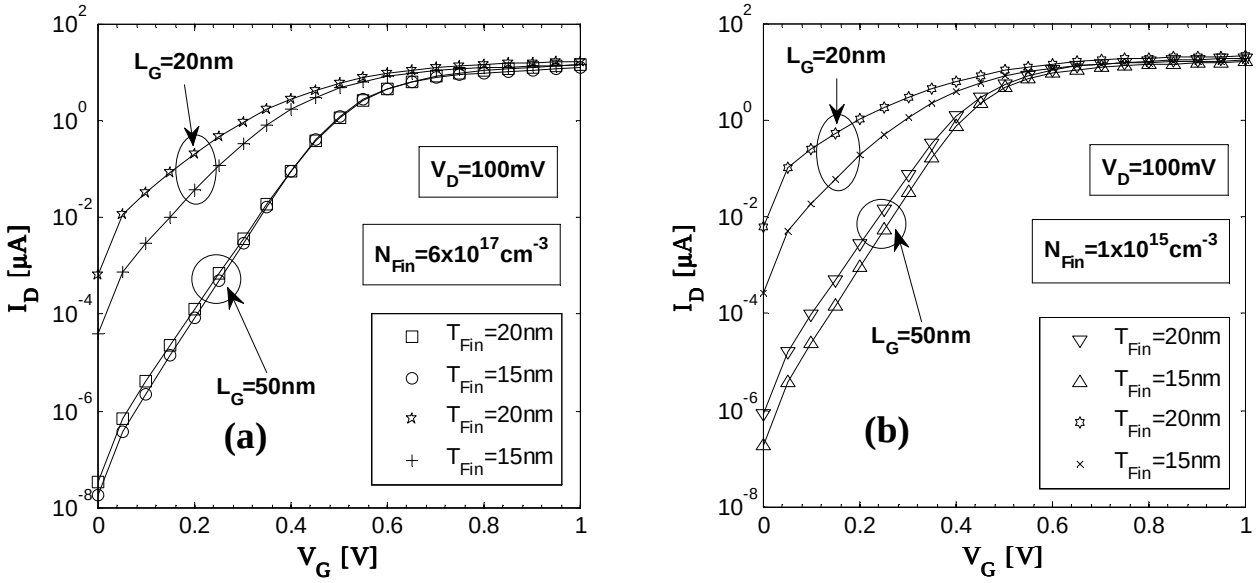


Figure 5.23: I_D-V_G (log) characteristics in the linear region (V_D=100mV) for different values of T_{fin} and L_G. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15}cm^{-3}.

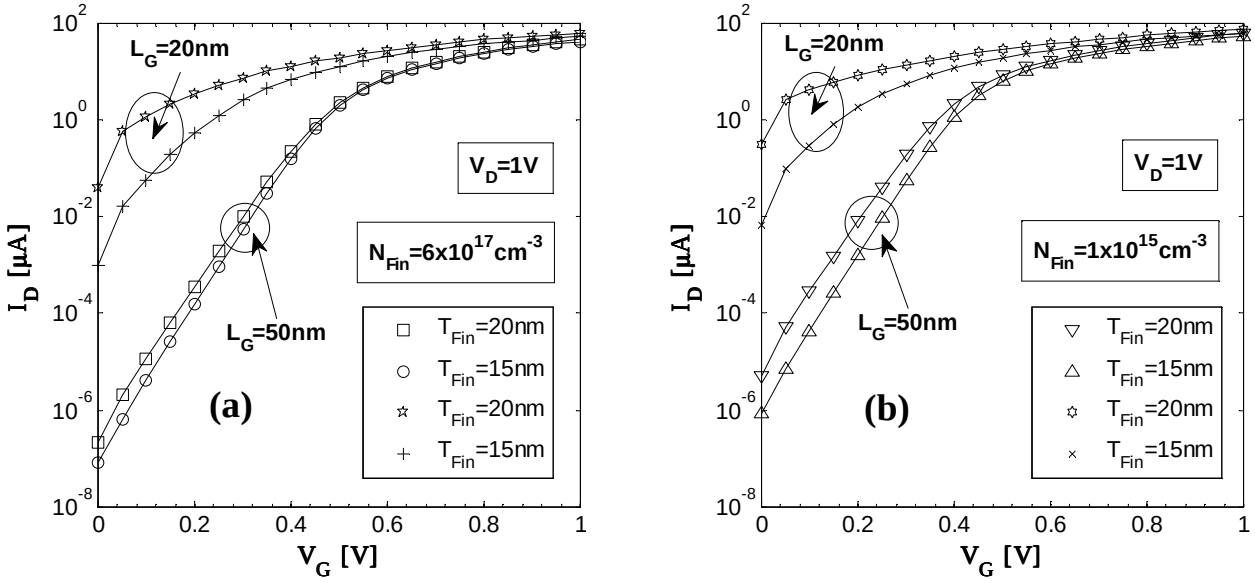


Figure 5.24: I_D-V_G (log) characteristics in the saturated region (V_D=1V) for different values of T_{fin} and L_G. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15}cm^{-3}.

5.3.1.2 Transconductance

The transconductance g_m versus gate voltage V_G for different values of T_{fin} (20 nm and 15 nm) and L_G (50 nm and 20 nm) are shown in Figure 5.25 and Figure 5.26. In the linear regime (V_D=100mV), the peak g_m decreases with the narrowing of the fin. This characteristic is probably the result of series resistances of source and drain. The g_m curves for the zero-doping and many-dopants case show that the parasitic fin regions outside the gate control is of utmost importance to be designed to reduce the parasitic resistance, and thus render this device worthy for circuit design.

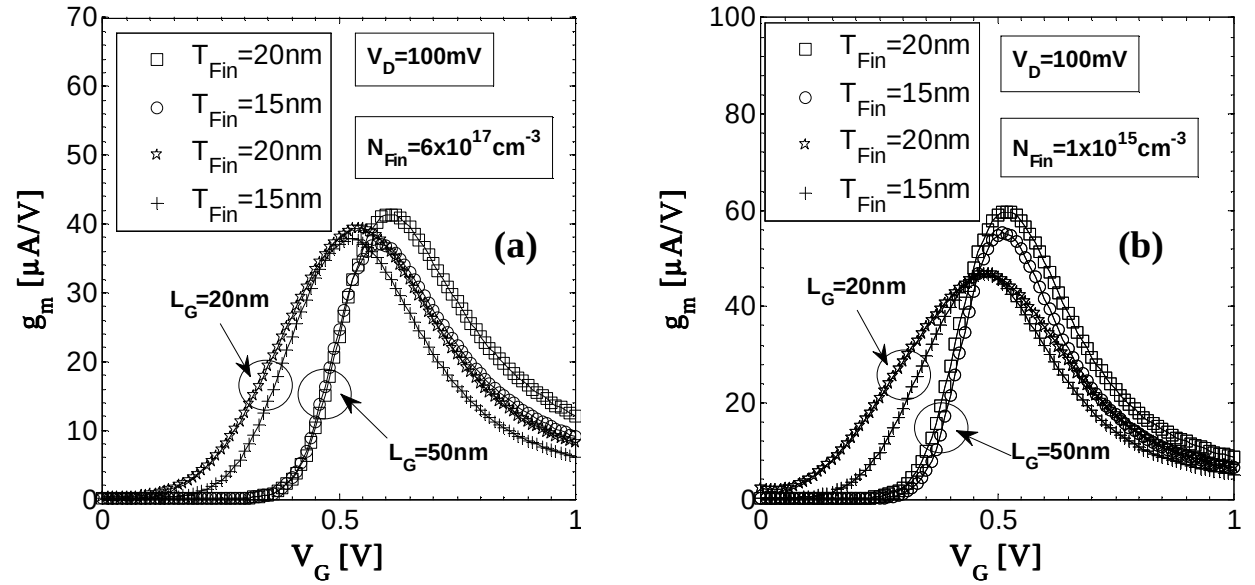


Figure 5.25: Transconductance g_m vs. gate voltage V_G in the linear region (V_D=100mV) for different values of T_{fin} and L_G. (a) N_{fin}=6x10^{17}cm^{-3} and (b) N_{fin}=1x10^{15}cm^{-3}.

Comparing Figure 5.25(a) and (b) one can see the higher g_m peak (about 40% higher) for the zero-doping case when compared to the many-dopants case.

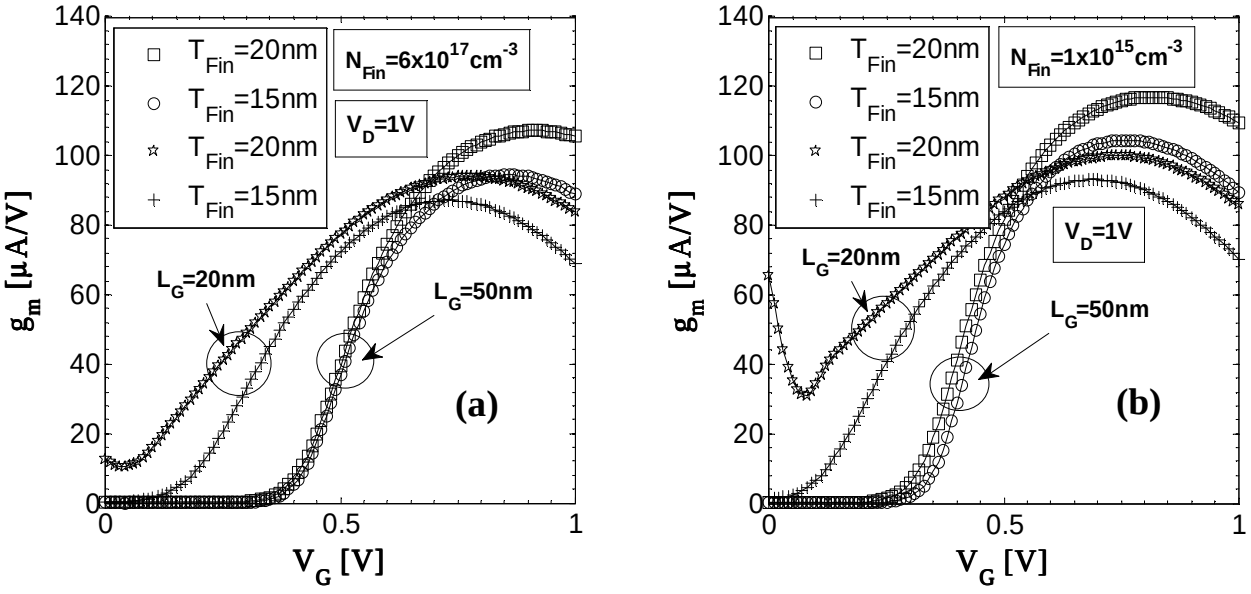


Figure 5.26: Transconductance g_m vs. gate voltage V_G in the saturated region (V_D=1V) for different values of T_{fin} and L_G. (a) $N_{fin}=6x10^{17}cm^{-3}$ and (b) $N_{fin}=1x10^{15}cm^{-3}$.

5.3.1.3 Threshold Voltage, Subthreshold Slope and DIBL

Threshold voltages V_T and subthreshold slopes S for V_D=100mV, and DIBL are shown in Figure 5.27, Figure 5.28, and Figure 5.29, respectively, and were extracted from I_D-V_G curves (linear region) of Section 5.3.1.1.

DIBL effect was extracted as follows: first, V_T is extracted from the I_D-V_G curve in the linear region (e.g. $V_D = V_{Dlin}$ = 100 mV); second, I_D (= I_{Do}) for $V_G = V_T$ is found; third, using I_{Do} in the I_D-V_G curve in the saturated region (e.g. $V_D = V_{Dsat}$ = 1V), V_G (= V_{Go}) is found; forth, DIBL effect is calculated by $(V_T - V_{Go})/(V_{Dsat} - V_{Dlin})$

The variations of V_T, S and DIBL with respect to L_G and are presented for two silicon fin thicknesses and two silicon fin doping concentrations. The V_T roll-off is present below gate lengths of 100 nm, what further indicates that the significant drop in V_T below 50 nm gate length calls for a thinner gate oxide and a narrower fin, in the range of 10 to 15 nm. On both doping concentrations, the reduction of T_{fin} of 20 nm to 15 nm reduces the V_T roll-off and improves S and DIBL. Acceptable values will be below 80 mV/dev for S and below 100 mV/V for DIBL.

However, a t_{ox} reduction below 2 nm is also mandatory to improve the device characteristics. Further reduction of gate oxide below 2 nm causes significant tunneling through the gate oxide. Hence, for this device to work below L_G of 20 nm it is mandatory to use effectively high-k dielectric gate material to minimize the gate tunneling current and to provide also good control of the fin conductance by the metal gate.

For circuit reasons, to provide both n- and p-type FinFETs with symmetrical thresholds and reasonable circuit performance in moderate to strong inversion, it is also necessary to use metal gate with mid-bandgap work function (mig-gap gate material). This is the more adequate gate structure being investigate to provide both n-type and p-type complementary I-V behavior.

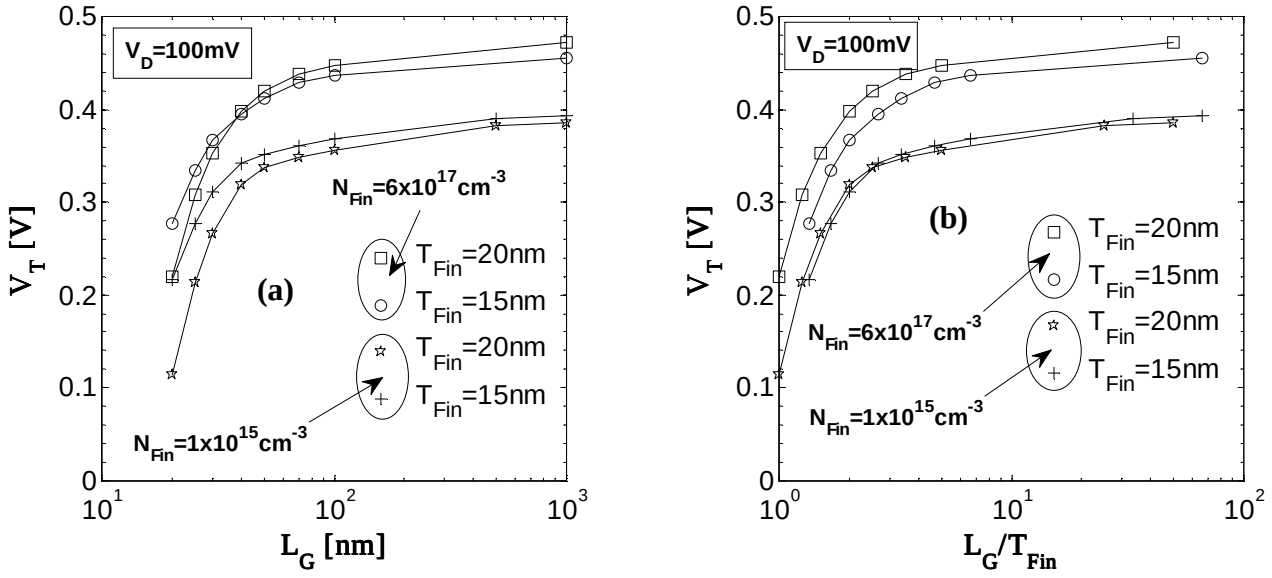


Figure 5.27: Threshold voltage V_T (method "GMLE") for different values of T_{fin} and N_{fin} (V_D = 100 mV). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

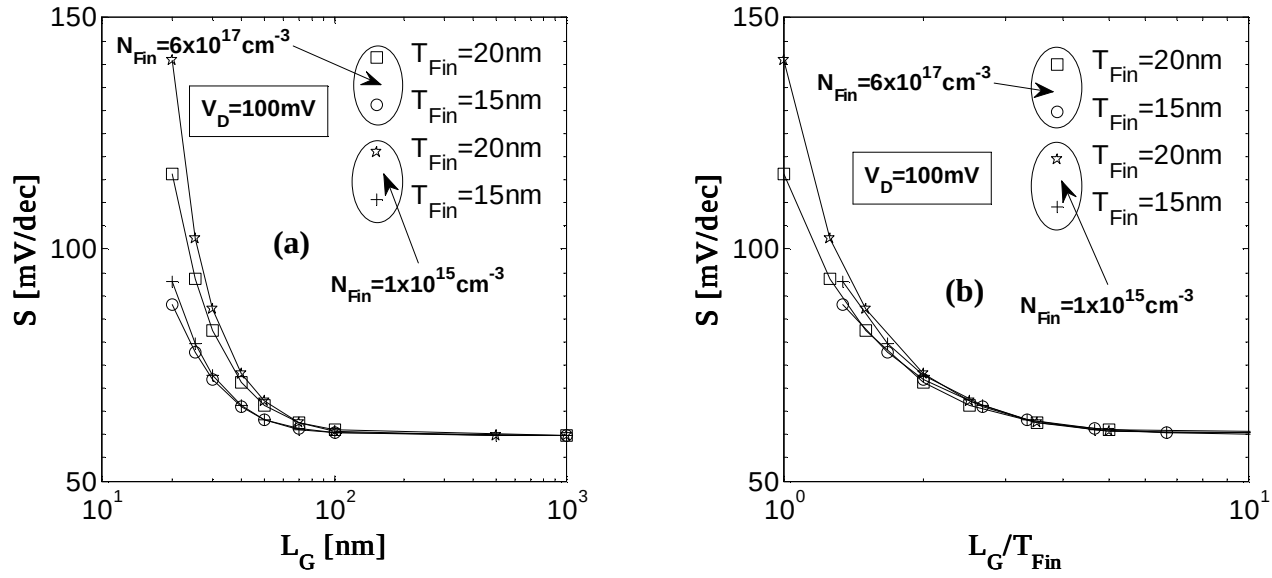


Figure 5.28: Subthreshold slope S for different values of T_{fin} and N_{fin} (V_D = 100 mV). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

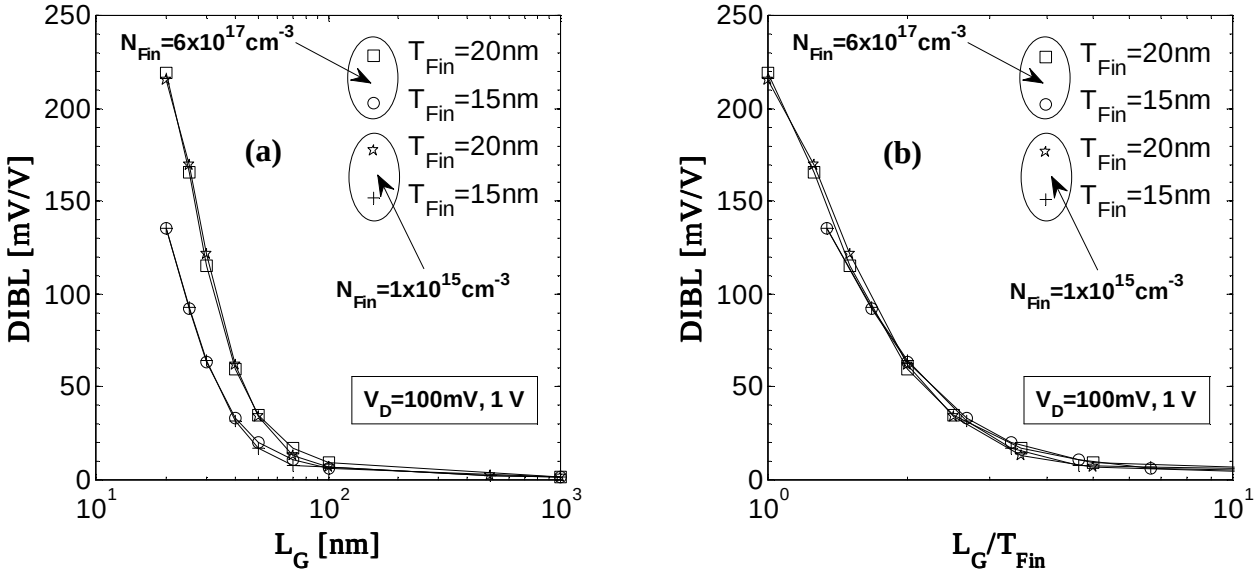


Figure 5.29: DIBL for different values of T_{fin} and N_{fin}. (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

5.4 Improvements on S/D Extensions and high-K dielectrics

In order to improve the V_T roll-off, subthreshold slope S, and DIBL, incremental changes in the FinFET structure parameters were made and simulated. A new device structure, herein referred to as "Structure-III" and shown in Figure 5.30, was used to simulate both high-K and SiO_2 dielectrics.

The values of the critical dimensions used in this section are indicated in Figure 5.31 and are explain next:

A structure with T_{fin} = 15 nm was simulated but with a higher gate oxide dielectric constant (e_{ox} = 7.2 instead e_{ox} = 3.9), similar to high-K materials, keeping t_{ox} = 2 nm and avoiding a thinner gate oxide and higher parasitic tunneling oxide currents, with an effective oxide thickness (EOT) of 1.1 nm. The oxide dielectric constant e_{ox} or K is also called relative permittivity ($e_r = e_s/e_o$). Previous simulation results for V_T roll-off, S, and DIBL behavior, show in Figure 5.27, Figure 5.28, and Figure 5.29, respectively, indicate that the ratio L_G/T_{fin} (or normalized gate length) has to be larger than approximately 1.5 to 2. Hence, a narrower fin, of about 10 nm is needed for $L_G \approx 15$ nm.

A structure with the previous modifications but with a narrower fin with T_{fin} = 10 nm was simulated with the standard S/D contact areas and with a new S/D contact areas (on both sidewalls and top of the last portion of the S/D extensions). These new contact areas are shown in Figure 5.30, a 3D simulation structure similar to Figure 5.15. A structure with previous modifications but with H_{fin} = 40 nm (H_{fin}/T_{fin} ratio of 4) was simulated. Only the zero-doping case ($N_{fin} = 1x10^{15}$ cm^{-3}), or undoped case, was considered, and only for a gate length of 20 nm.

As in the previous section, the S/D extensions of the fin are doped with two Gaussian profiles perpendicular to the sidewalls of the silicon fin (z-axis). A peak

concentration $N_D = 1x10^{19}\ cm^{-3}$ is used with $\lambda_z = 6.5$ nm, resulting in an initial 10 nm/dec ratio. A complementary error function (Erfc) is used to describe the lateral profile with $\lambda_x = 2$ nm, resulting in an initial 2.33 nm/decade ratio and a ΔL of approximately 11 nm (5.5 nm of each side).

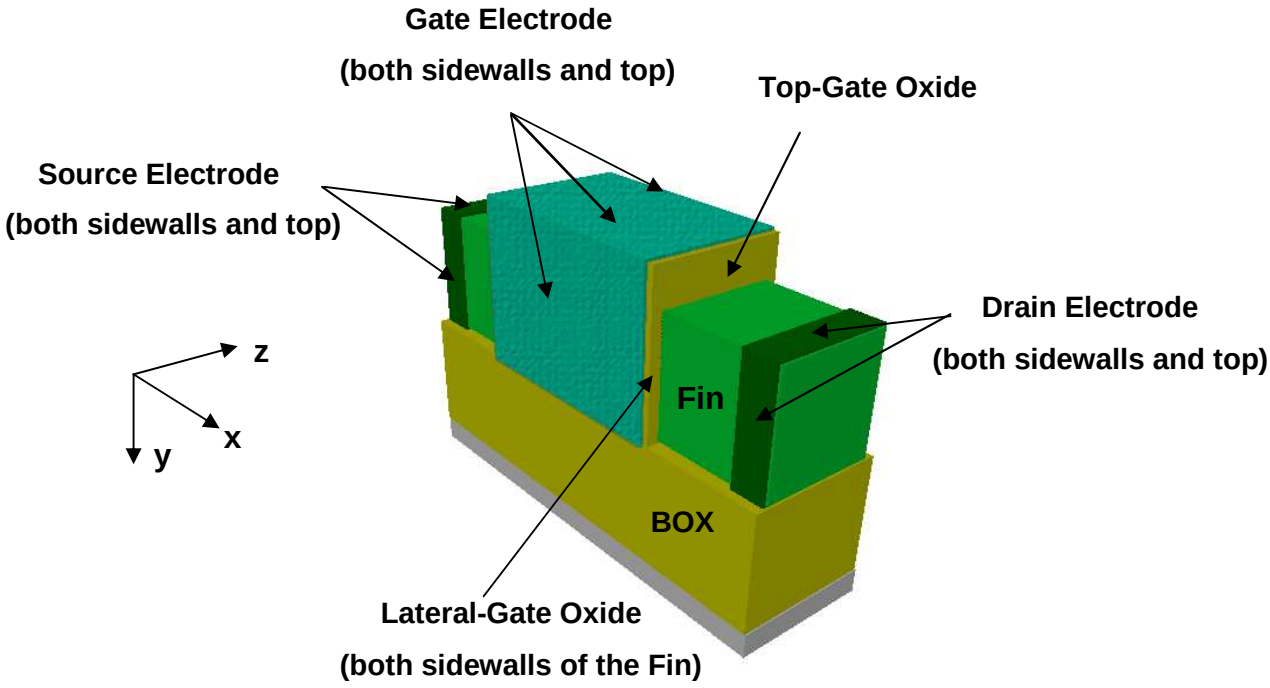
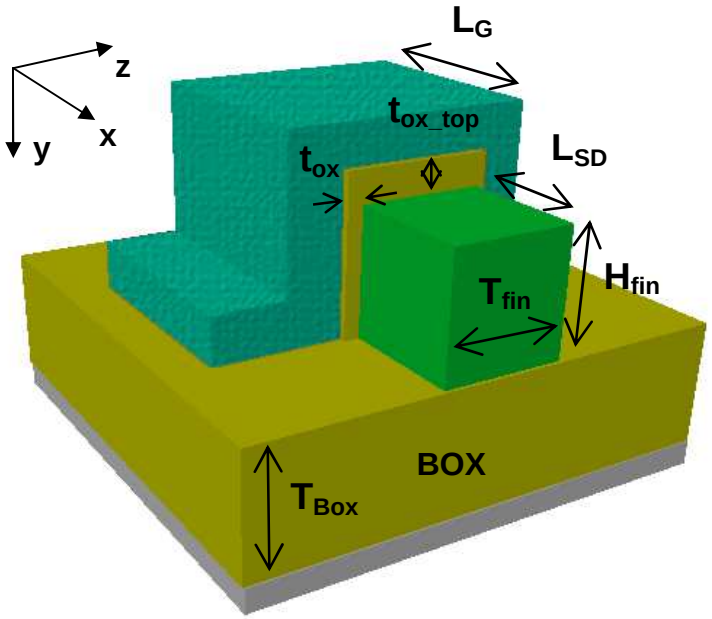


Figure 5.30: SOI-FinFET structure used to define the simulation grid - Structure-III. A new source and drain contact areas (electrodes) are shown.



Critical Dimensions:

- **t_{ox} = 2 nm (t_{ox_top} > 10 x t_{ox})**
- **H_{fin} = 40 and 60 nm**
- **T_{fin} = 10 and 15 nm**
- **T_{Box} = 150nm**
- **L_G = from 20 to 500 nm**
- **L_{SD} = 25nm**
- **$W_{eff} = 2xH_{fin}$ (double-gate)**

Figure 5.31: Basic SOI-FinFET structure with critical dimensions indicated and the values used in the simulations.

As differences with respect the previous simulations with the Structure-II, simulations with Structure-III have:

- new source and drain contact areas (electrodes);
- only the undoped fin case is considered (N_{fin}=1x10^{15} cm^{-3});
- physical gate lengths L_G from 20 to 500 nm;
- simulation cases with e_{ox} = 7.2, (instead e_{ox} = 3.9);
- simulation cases for T_{fin} = 10 nm;
- a simulation case for H_{fin} = 40 nm;

5.4.1 Simulation Results

5.4.1.1 I_D-V_G Characteristics

Figure 5.32 and Figure 5.33 show the simulated I_D-V_G characteristics of the SOI-FinFET with the last improvements on the structure. The bias applied in the simulations was the same as in the previous section, i.e., V_D = 100 mV in the linear region and V_D = 1 V in saturated region, with V_S and V_B grounded. I_D-V_G characteristics for devices with T_{fin} = 20 nm and 15 nm, but without the last improvements on the structure (see Section 5.3), are plotted for comparison. Each plot has three curves for T_{fin} = 10 nm, all with high-k (e_{ox} = 7.2). The plot marks are explained next:

– "*" for T_{fin} = 20 nm, H_{fi} = 60 nm;

– "x" for T_{fin} = 15 nm, H_{fi} = 60 nm;

– "o" for T_{fin} = 10 nm, H_{fi} = 60 nm, high-k;

– "□" for T_{fin} = 10 nm, H_{fin} = 60 nm, high-k, new S/D contact structure;

– "Δ" for T_{fin} = 10 nm, H_{fin} = 40 nm, high-k, new S/D contact structure;

Considering the three structures with T_{fin}=10 nm and high-k ("o", "□", "Δ"), a good improvement on I-V characteristics is observed with a decrease of the subthreshold slope to around 70 mV/dec. The turn-off current I_{off} (I_D for V_G = 0 V) was reduced by two orders of magnitude. The use of high-k and the reduction of EOT (1.1 nm) and T_{fin} alleviated the DIBL problem.

Considering the structures with T_{fin}=10 nm and H_{fi} =60 nm ("o", "□"), an increase on turn-on current I_{on} (I_D for V_G = 1 V) of 18% and 7%, respectively for V_D = 100 mV and V_D = 1V, is observed when the new S/D structure is used. The use of new S/D contact areas has reduced the parasitic resistance (R_{SDE}) of the S/D extensions regions. On the other hand, a decrease on I_{on} of 20% and 27%, respectively for V_D = 100 mV and V_D = 1V, is observed for the structure with T_{fin} = 10 nm and H_{fin} = 40 nm ("Δ"). The impact of the reduction of H_{fin} by 33% and the consequent increase in the fin resistance compensates the reduction of R_{SDE}.

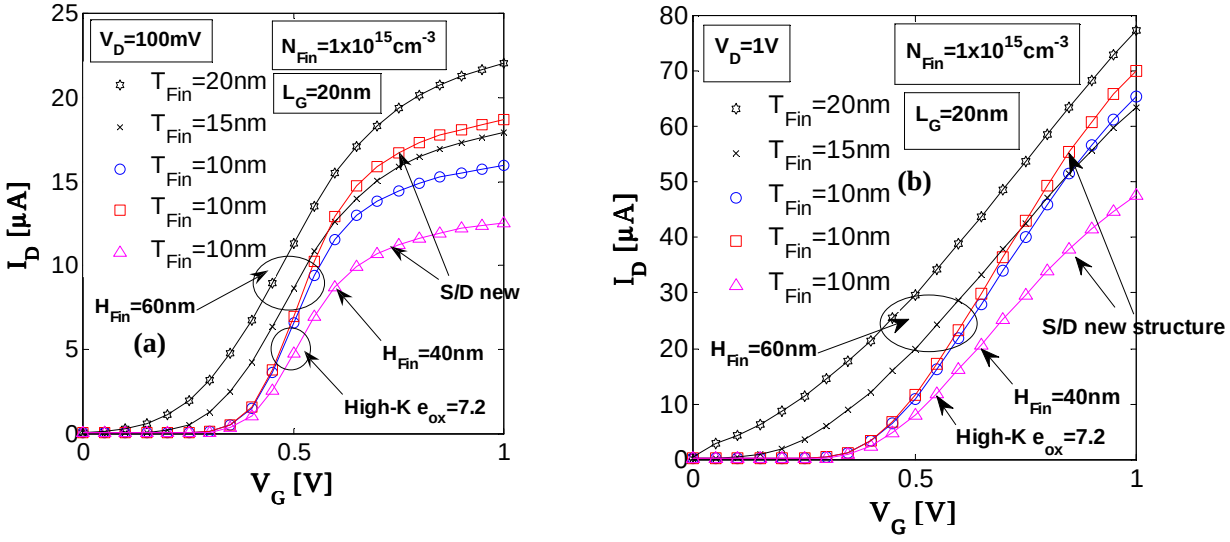


Figure 5.32: I_D-V_G characteristics for different values of T_{fin} and L_G of 20 nm. (a) linear region (V_D=100mV) (b) saturated region (V_D = 1V).

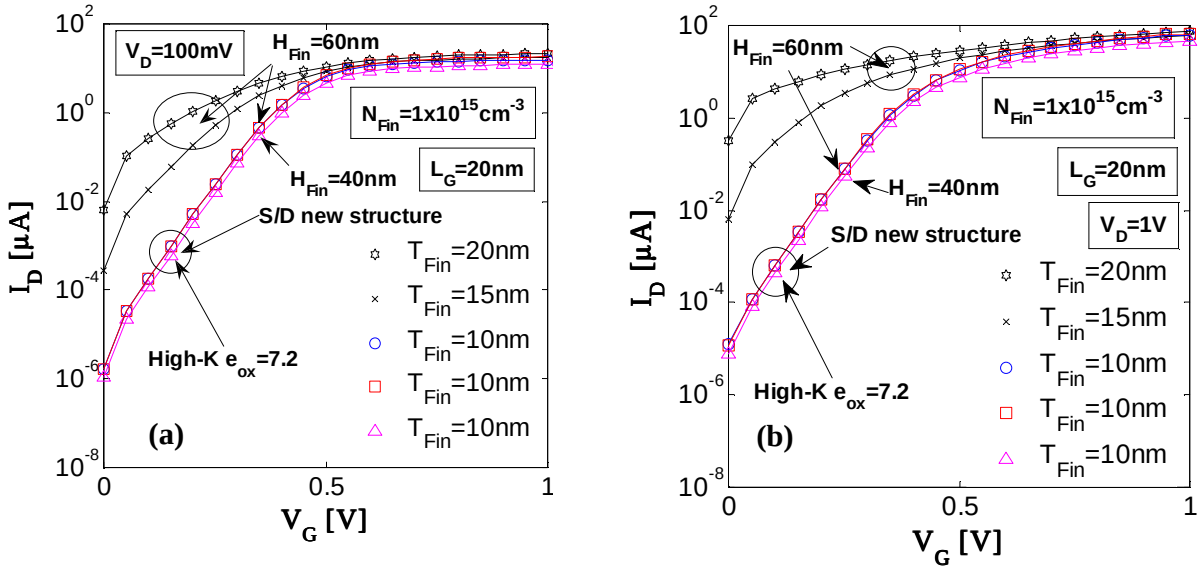


Figure 5.33: I_D-V_G (log) characteristics for different values of T_{fin} and L_G of 20 nm. (a) linear region (V_D=100mV) (b) saturated region (V_D=1V).

A particular method that accounts for a quantum mechanical (QM) effect in the inversion layer was used in the simulations to estimate the influence of such effect on the SOI-FinFET I-V characteristics (see Section 5.2.2). Figure 5.34 and Figure 5.35 show I_D-V_G curves in the linear and saturated regions, with and without a QM effect in the inversion layer. Considering the nanometric dimensions of the fin, i.e., H_{fin} = 40 nm and T_{fin} = 10 nm, this particular QM effect made little difference, with a reduction of around 5% in the final drain current (saturated region) and a slight shift in the threshold voltage.

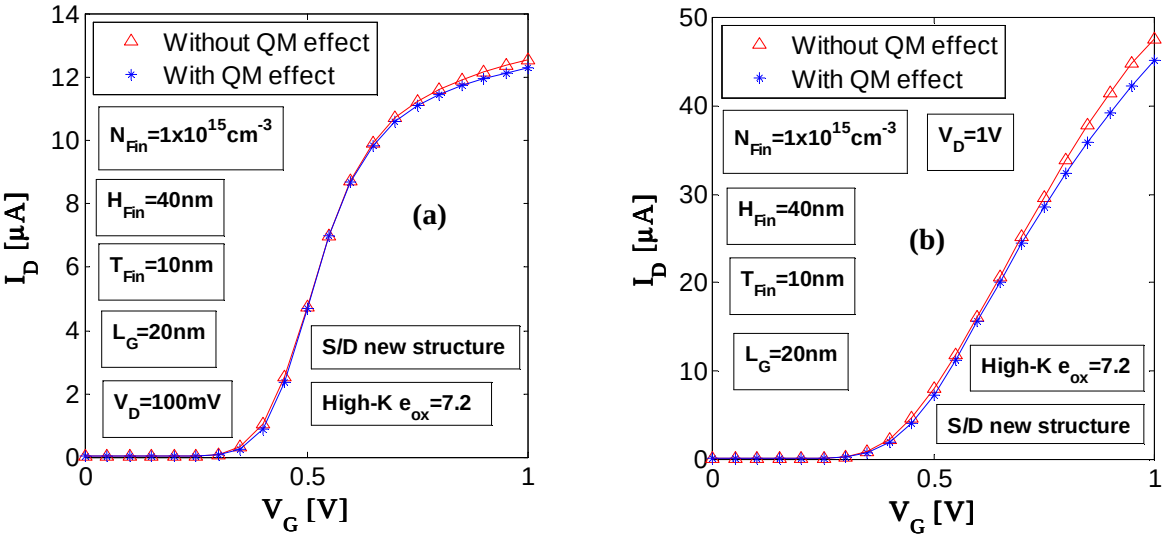


Figure 5.34: I_D-V_G characteristics with and without a quantum mechanical (QM) effect in the inversion layer. (a) linear region (V_D=100mV) (b) saturated region (V_D=1V).

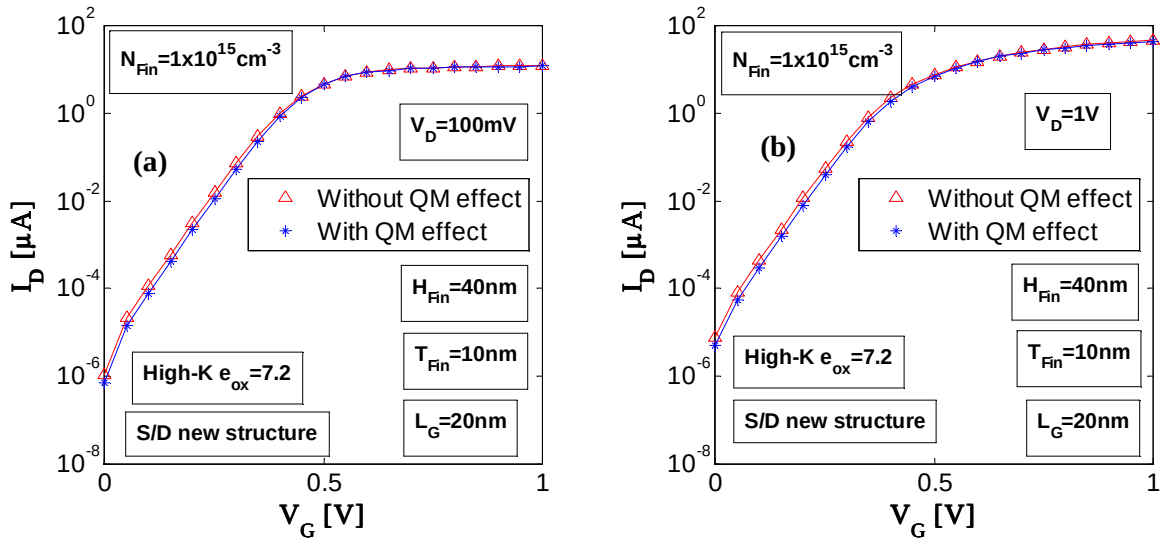


Figure 5.35: I_D-V_G (log) characteristics with and without a quantum mechanical effect (QM) in the inversion layer. (a) linear region (V_D = 100 mV) (b) saturated region (V_D = 1 V).

5.4.1.2 Transconductance

The transconductance g_m and the transconductance over drain current g_m/I_D, both versus gate voltage V_G, and the g_m/I_D versus normalized drain current $I_D/(W/L)$ are show from Figure 5.36 to Figure 5.41 for different values of T_{fin}. For each figure, curves for structures with T_{fin} = 20 nm and 15 nm, but without the last improvements on the structure (see Section 5.3), are plotted for comparison. As in the previous section, each plot has three curves for T_{fin} = 10 nm, all with high-k (e_{ox} = 7.2), but has also a curve for T_{fin} = 15 nm and high-k (e_{ox} = 7.2). The plot marks are explained next:

– "*" for T_{fin} = 20 nm, H_{fi} = 60 nm;

– "x" for T_{fin} = 15 nm, H_{fi} = 60 nm;

– "+" for T_{fin} = 15 nm, H_{fi} = 60 nm, high-k;

– "o" for T_{fin} = 10 nm, H_{fi} = 60 nm, high-k;

– "□" for T_{fin} = 10 nm, H_{fin} = 60 nm, high-k, new S/D contact structure;

– "Δ" for T_{fin} = 10 nm, H_{fin} = 40 nm, high-k, new S/D contact structure;

As in the case of I_D-V_G characteristics of the previous section, considering the three structures with T_{fin} = 10 nm and high-k ("o", "□", "Δ"), a good improvement on g_m and g_m/I_D is observed. An increase on g_m/I_D in the subthreshold regime can be noted, first with the use of high-k (g_m/I_D around 28 V^{-1}) and second with a new S/D contact structure (g_m/I_D around 34 V^{-1}).

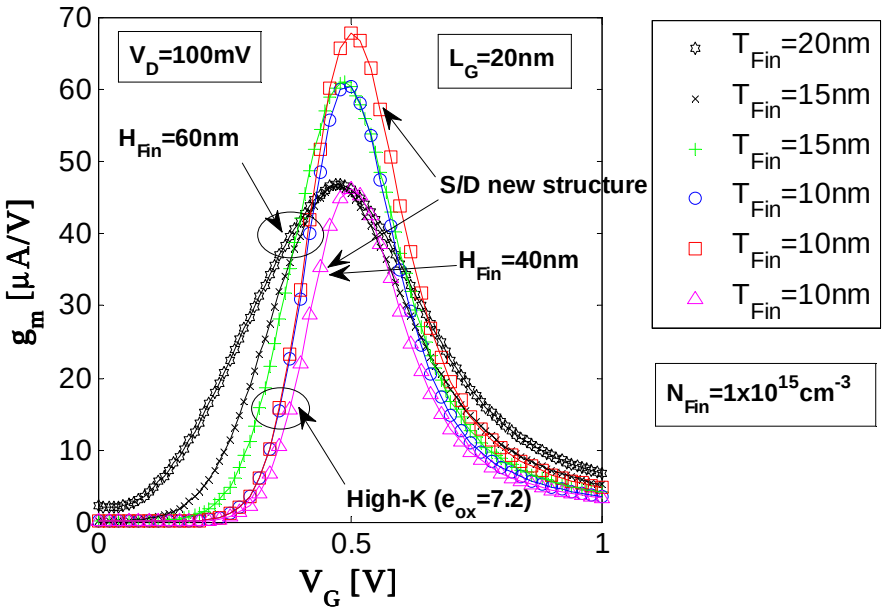


Figure 5.36: Transconductance g_m versus gate voltage V_G for different values of T_{fin} (L_G = 20 nm, N_{fin} = 1x10^{15}cm^{-3} and V_D = 100 mV).

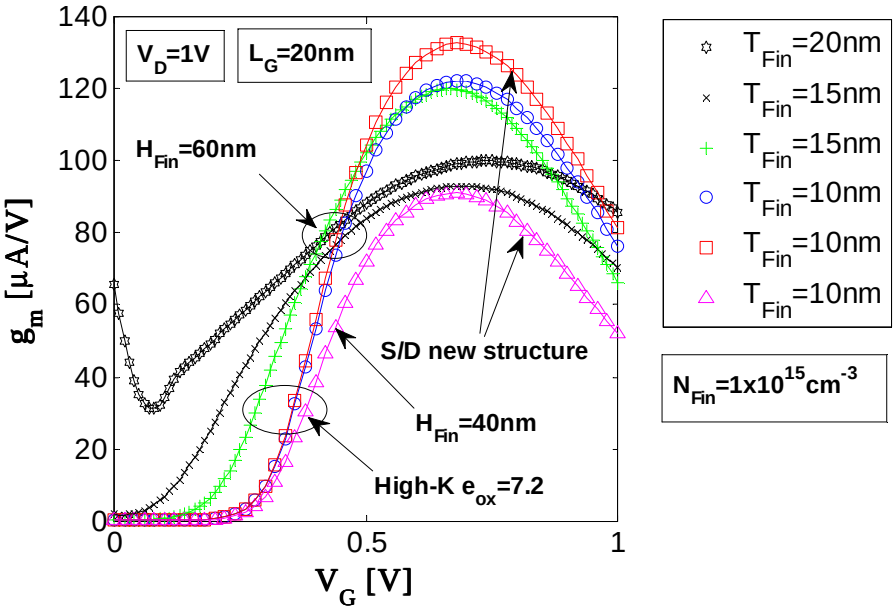


Figure 5.37: Transconductance g_m versus gate voltage V_G different values of T_{fin} (L_G = 20 nm, N_{fin} = 1x10^{15}cm^{-3} and V_D = 1V).

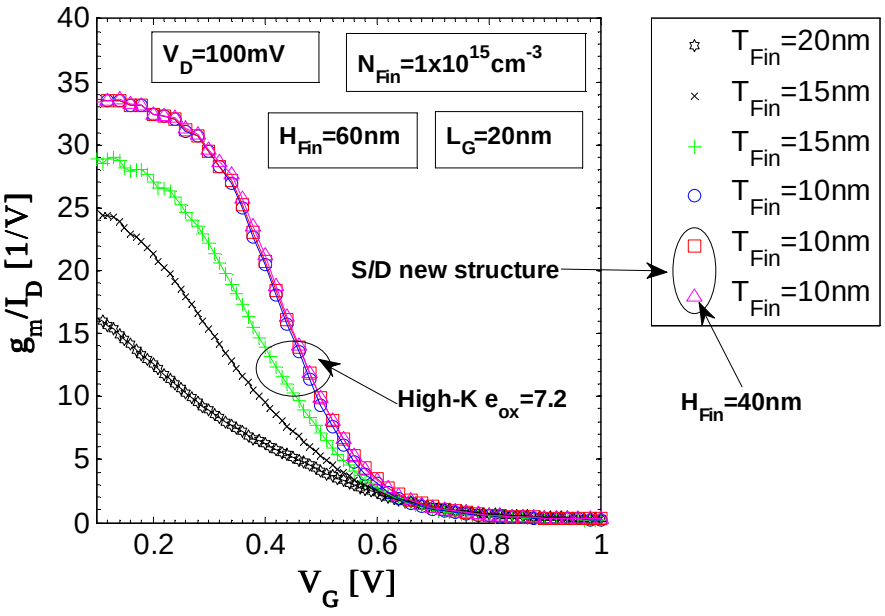


Figure 5.38: Transconductance over drain current g_m/I_D versus gate voltage V_G for different values of T_{fin} (L_G = 20 nm, N_{fin} = 1x10^{15}cm^{-3} and V_D = 100 mV).

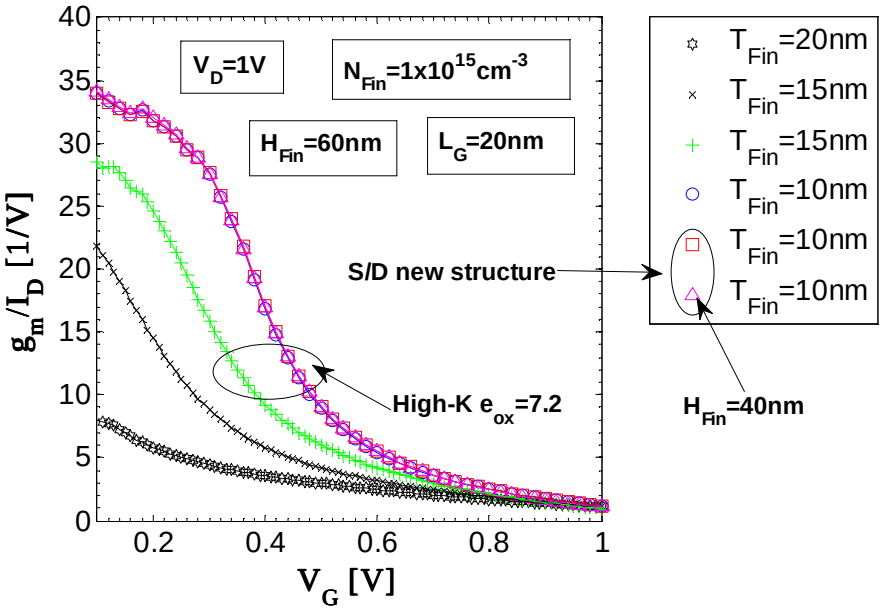


Figure 5.39: Transconductance over drain current g_m/I_D versus gate voltage V_G for different values of T_{fin} (L_G = 20 nm, N_{fin} = 1x10^{15}cm^{-3} and V_D = 1V).

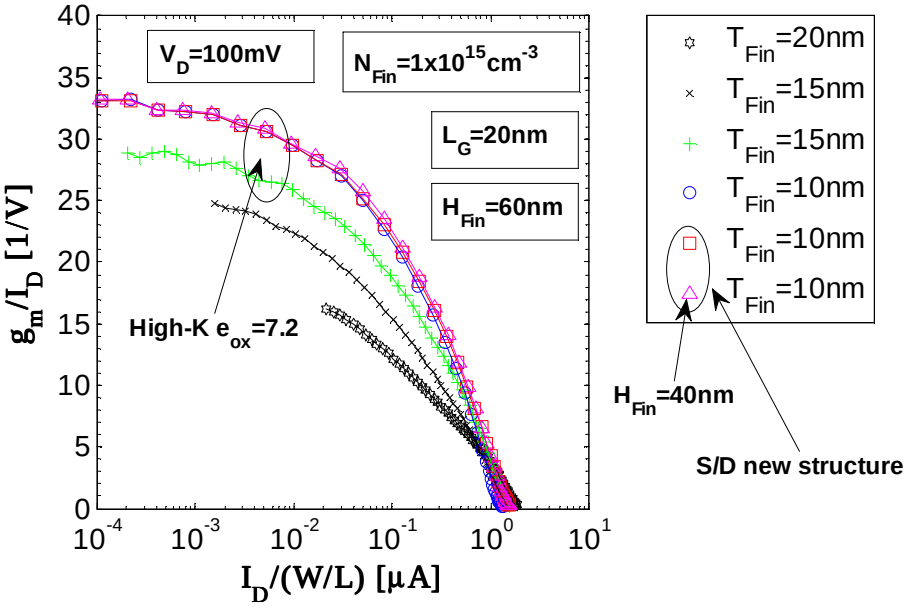


Figure 5.40: Transconductance over drain current g_m/I_D versus normalized drain current $I_D/(W/L)$ for different values of T_{fin} (L_G = 20 nm, N_{fin} = 1x10^{15}cm^{-3} and V_D = 100 mV).

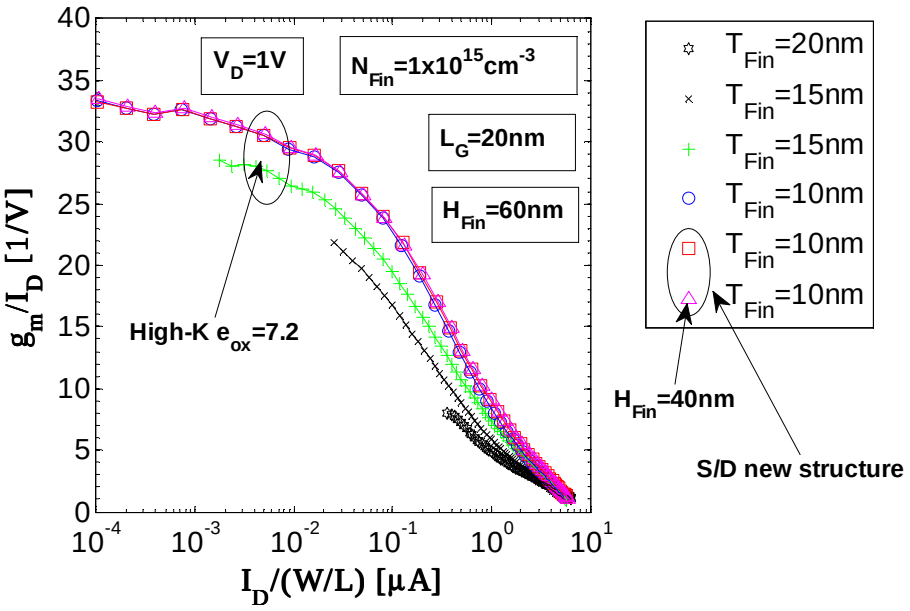


Figure 5.41: Transconductance over drain current g_m/I_D versus normalized drain current $I_D/(W/L)$ for different values of T_{fin} (L_G = 20 nm, N_{fin} = 1x10^{15}cm^{-3} and V_D = 1V).

5.4.1.3 Threshold Voltage, Subthreshold Slope and DIBL

Threshold voltages V_T are shown in Figure 5.42 and Figure 5.43, respectively extracted by method "GMLE" and "SD". Subthreshold slope S is shown in Figure 5.44. DIBL is shown in Figure 5.45 and Figure 5.46, respectively using V_T from Figure 5.42 and Figure 5.43.

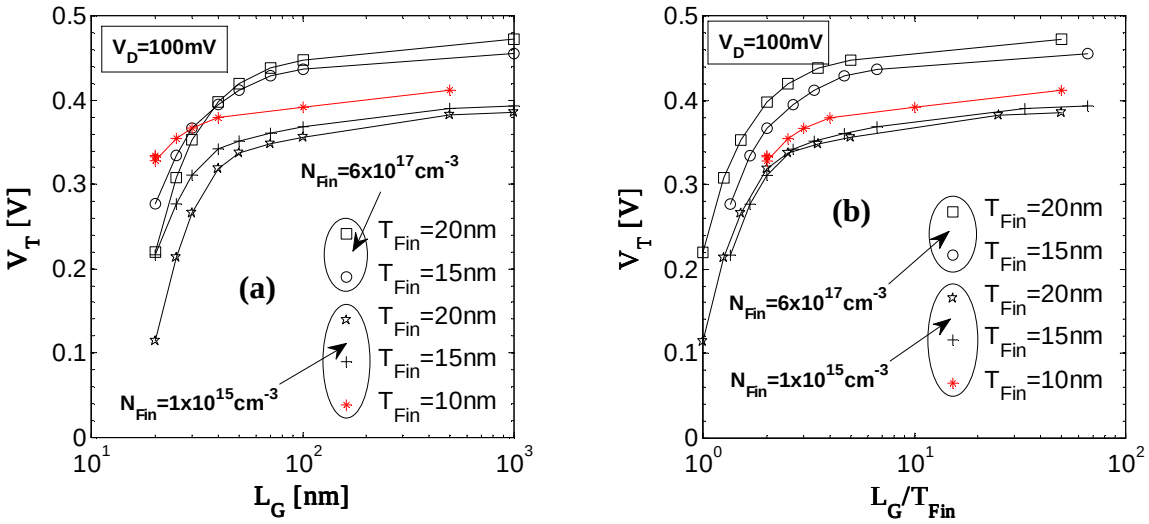


Figure 5.42: Threshold voltage V_T (method "GMLE") for different values of T_{fin} and N_{fin} (V_D = 100 mV). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

Along with the values of V_T, S and DIBL shown in Section 5.3.1.3, new curves ("*") are presented, for T_{fin} = 10 nm, H_{fin} = 60 nm, high-k and new S/D contact structure. Considering these new curves, one can note a better V_T roll-off, present now below gate lengths of 50 nm.

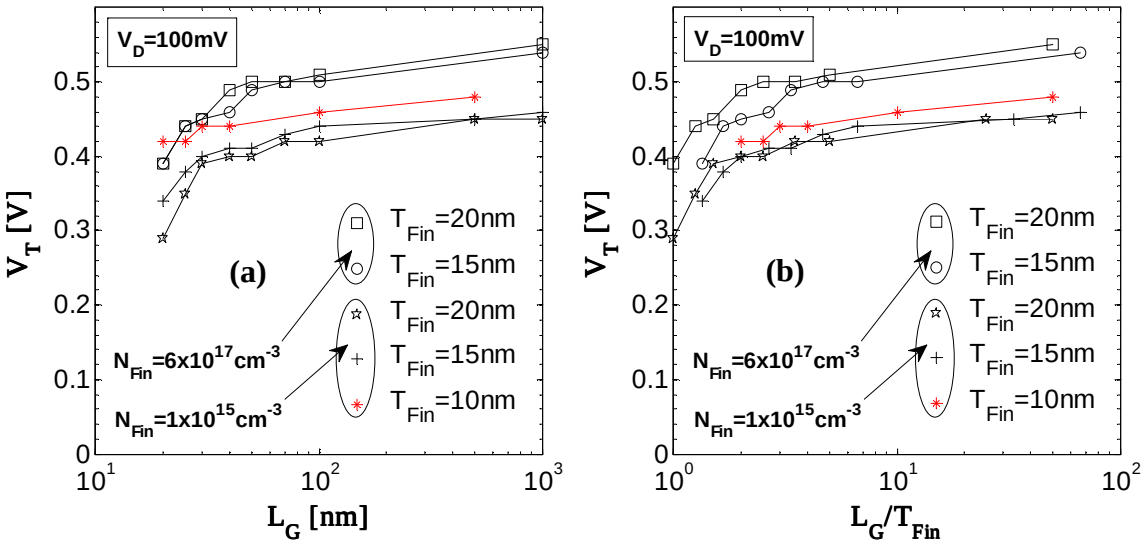


Figure 5.43: Threshold voltage V_T (method "SD") for different values of T_{fin} and N_{fin} (V_D = 100 mV). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

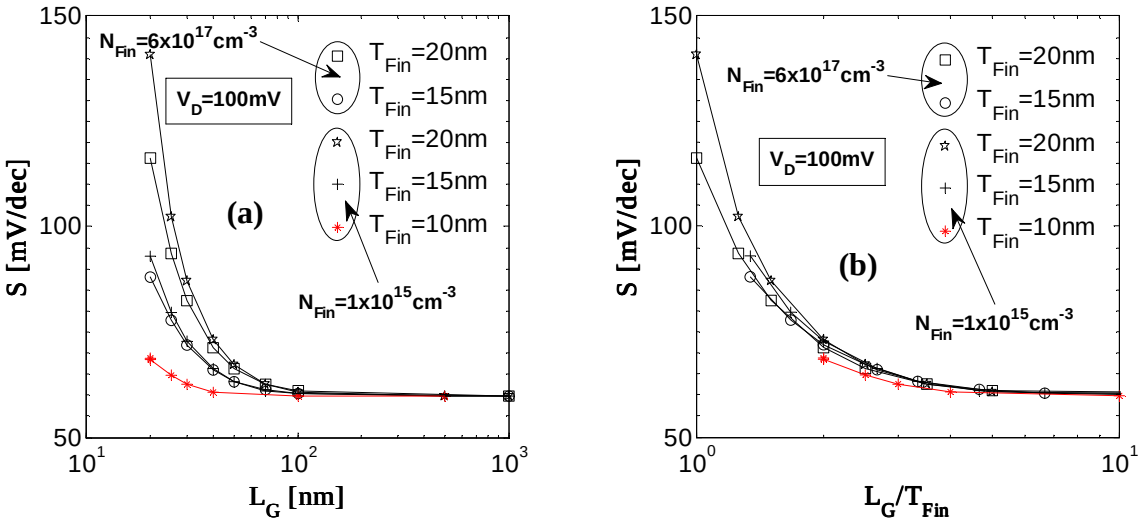


Figure 5.44: Subthreshold slope S for different values of T_{fin} and N_{fin} (V_D = 100 mV). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

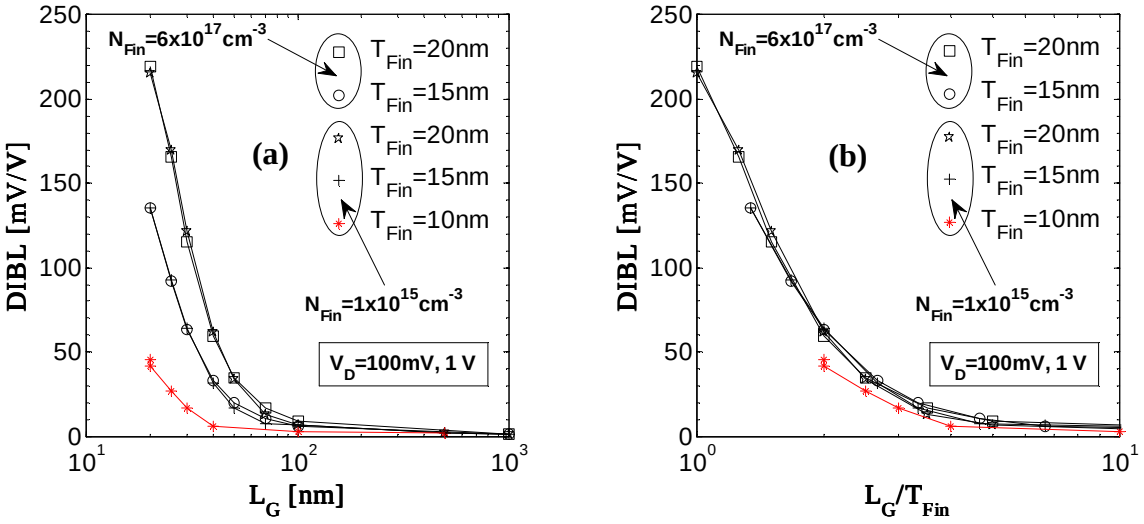


Figure 5.45: DIBL for different values of T_{fin} and N_{fin}. (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}. Using V_T from Figure 5.42.

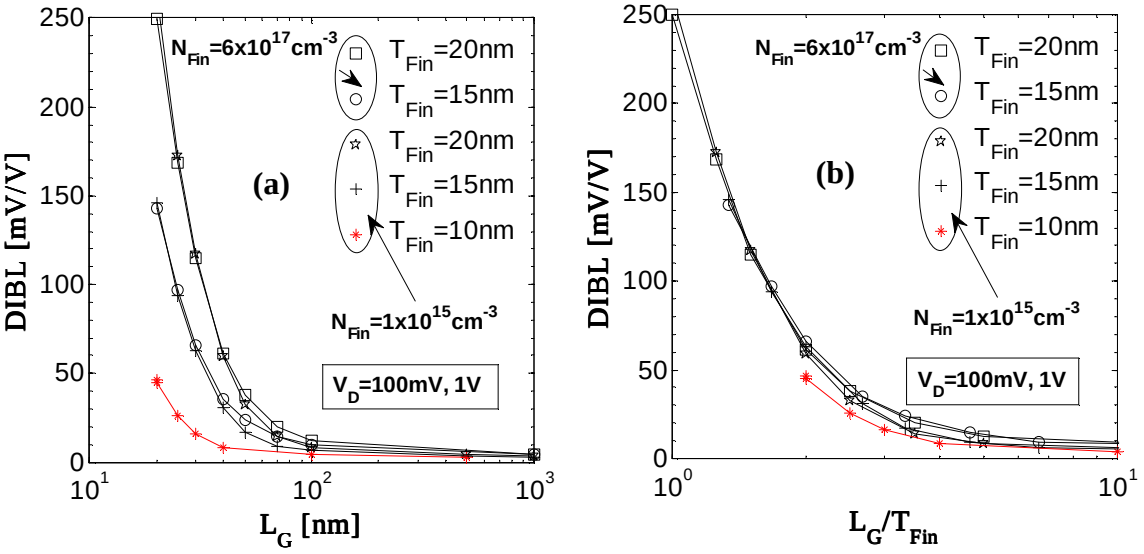


Figure 5.46: DIBL for different values of T_{fin} and N_{fin}. (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}. Using V_T from Figure 5.43.

5.4.1.4 Turn-on and Turn-off currents

Turn-on current I_{on} is extracted taking I_D (= I_{on}) for the maximum values of V_G and V_D (e.g. V_G = 1V, V_D = 1V). Turn-off current I_{off} is extracted by extrapolation of the log(I_D)-V_G curve in the linear portion of the subthreshold for the maximum value of V_D (e.g. V_D = 1V), V_G = 0, and taking I_D (= I_{off}).

Figure 5.47, Figure 5.48, and Figure 5.49 show extracted values of, respectively, I_{on}, I_{off}, and turn-on/turn-off ratio I_{on}/I_{off}, versus gate length L_G and versus normalized gate

length L_G/T_{fin}. Along with the values of I_{on}, I_{off} and I_{on}/I_{off} for the devices without the last improvements on the structure (see Section 5.3), new curves ("*") are presented, for T_{fin} = 10 nm, H_{fin} = 60 nm, high-k and new S/D contact structure.

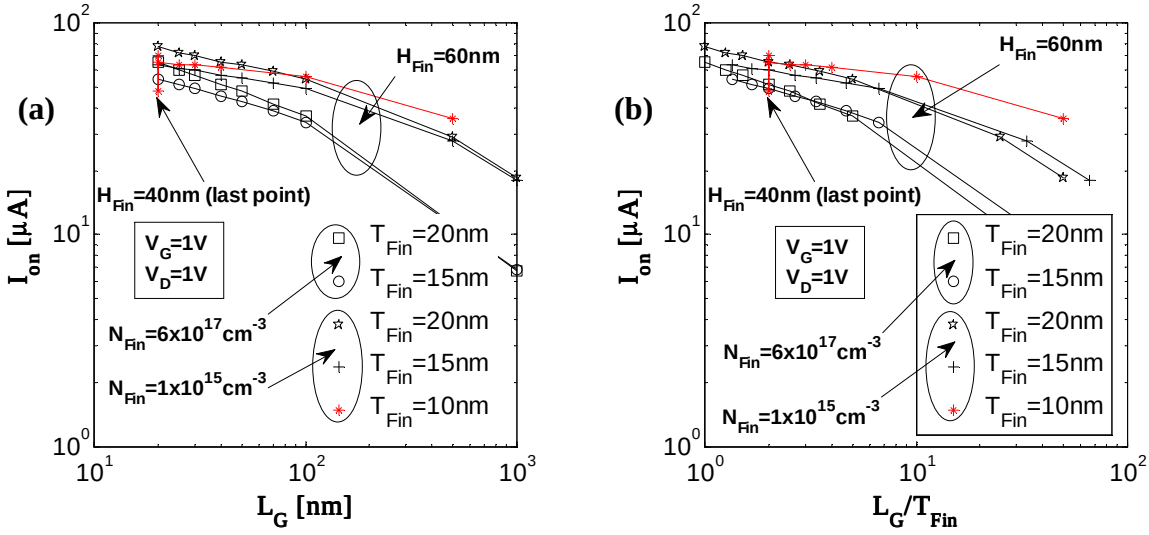


Figure 5.47: Turn-on current I_{on} for different values of T_{fin} and N_{fin} (V_G = 1V, V_D = 1V). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

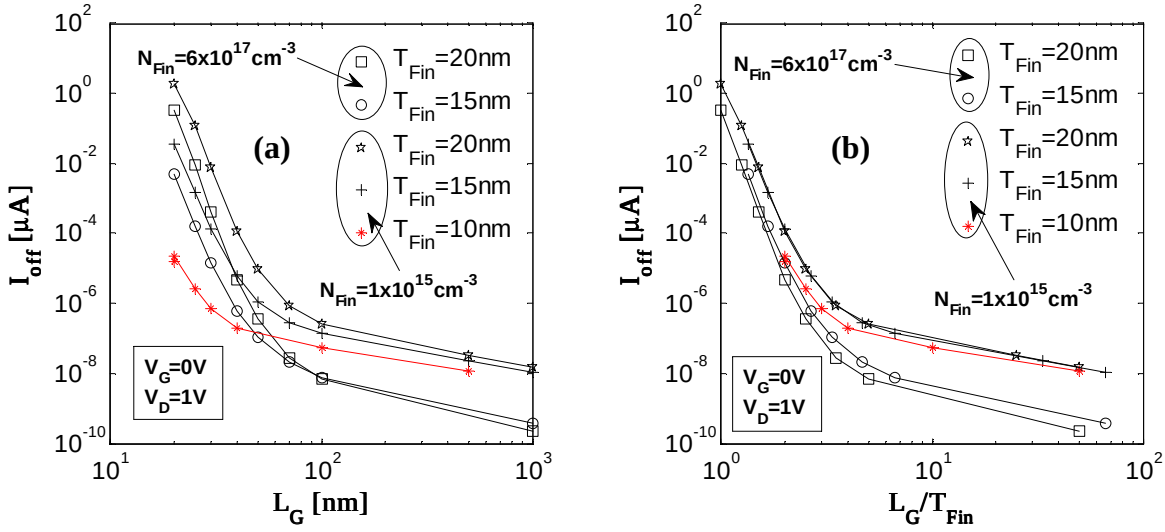


Figure 5.48: Turn-off current I_{off} for different values of T_{fin} and N_{fin} (V_G = 0 V, V_D = 1 V). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

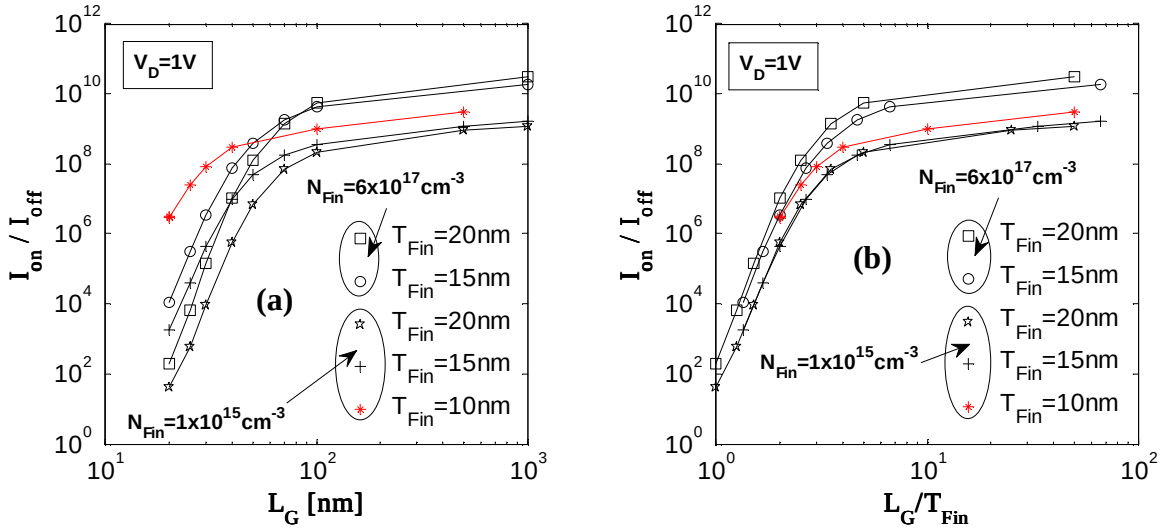


Figure 5.49: Turn-on/turn-off ratio I_{on}/I_{off} for different values of T_{fin} and N_{fin} (V_D = 1V). (a) versus gate length L_G and (b) versus normalized gate length L_G/T_{fin}.

5.4.1.5 I_D-V_D Characteristics

Figure 5.50, Figure 5.51, Figure 5.52, and Figure 5.53 show I_D-V_D characteristics for different gate voltages. Figure 5.54, Figure 5.55, and Figure 5.56 show, respectively, the output conductance g_d, the output resistance $1/g_d$ and the early voltage V_A, versus drain voltage V_D. These figures show the impact of the improvements on S/D extension regions, use of high-k dielectrics and reduction of T_{fin}.

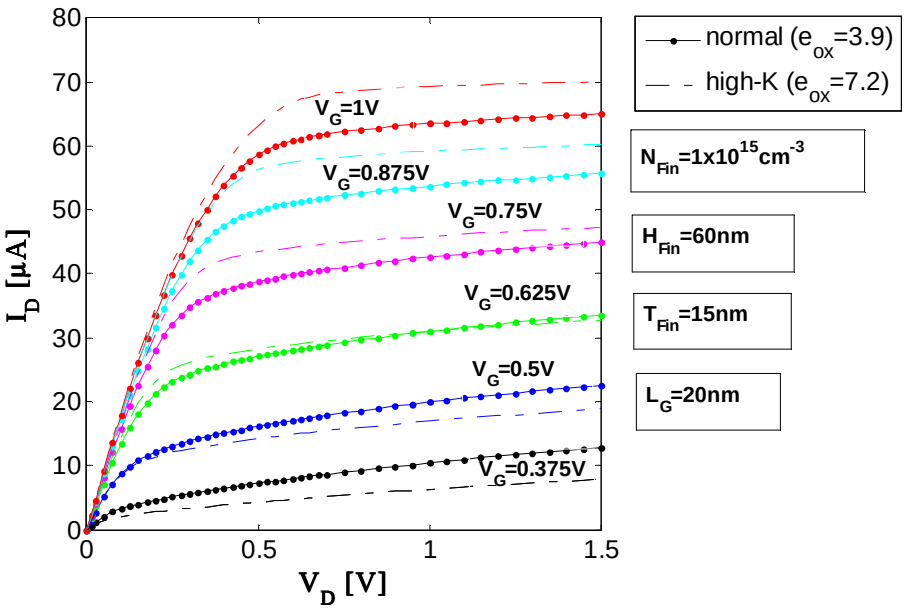


Figure 5.50: I_D-V_D characteristics for different gate voltages. FinFETs with gate oxide with (—) e_{ox}=3.9 and (–.–) e_{ox}=7.2 (N_{fin} = 1x10^{15}cm^{-3}, H_{fin} = 60 nm, T_{fin} = 10 nm, L_G = 20 nm).

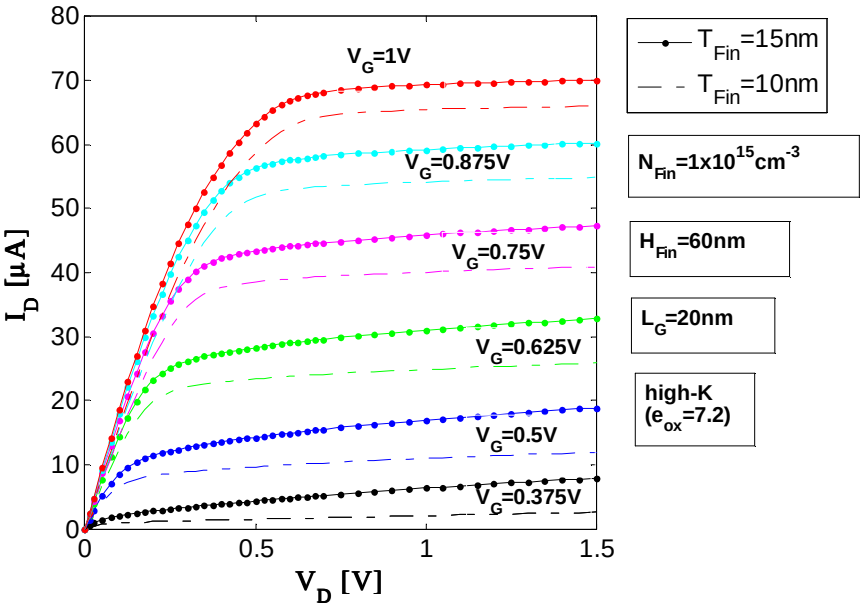


Figure 5.51: I_D-V_D characteristics for different gate voltages. FinFETs with (—) T_{fin}=15nm and (–.–) T_{fin}=10nm (N_{fin} = 1x10^{15}cm^{-3}, H_{fin} = 60 nm, e_{ox} = 7.2, L_G = 20 nm).

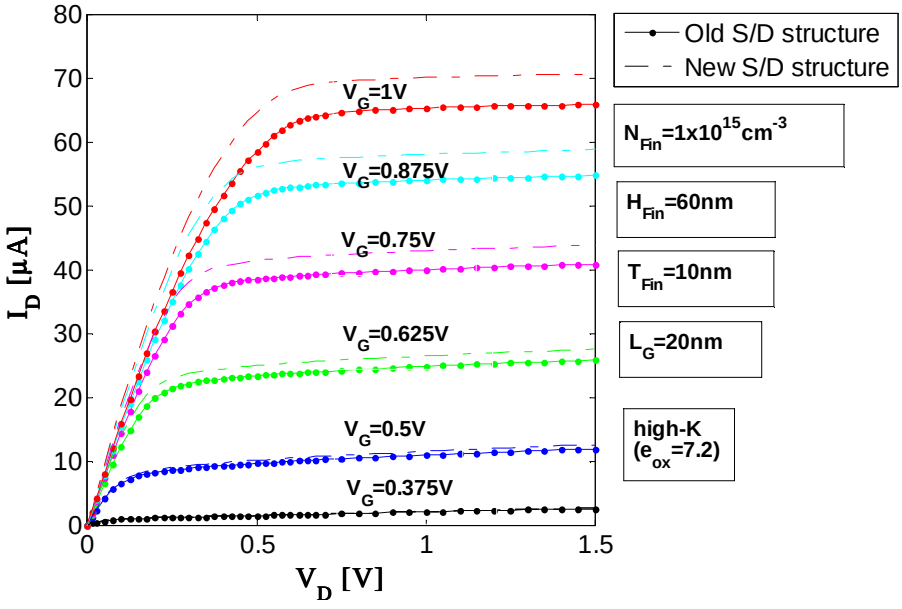


Figure 5.52: I_D-V_D characteristics for different gate voltages. FinFETs with (—) old S/D structure and (–.–) new S/D structure (N_{fin} = 1x10^{15} cm^{-3}, H_{fin} = 60 nm, e_{ox} = 7.2, L_G = 20 nm).

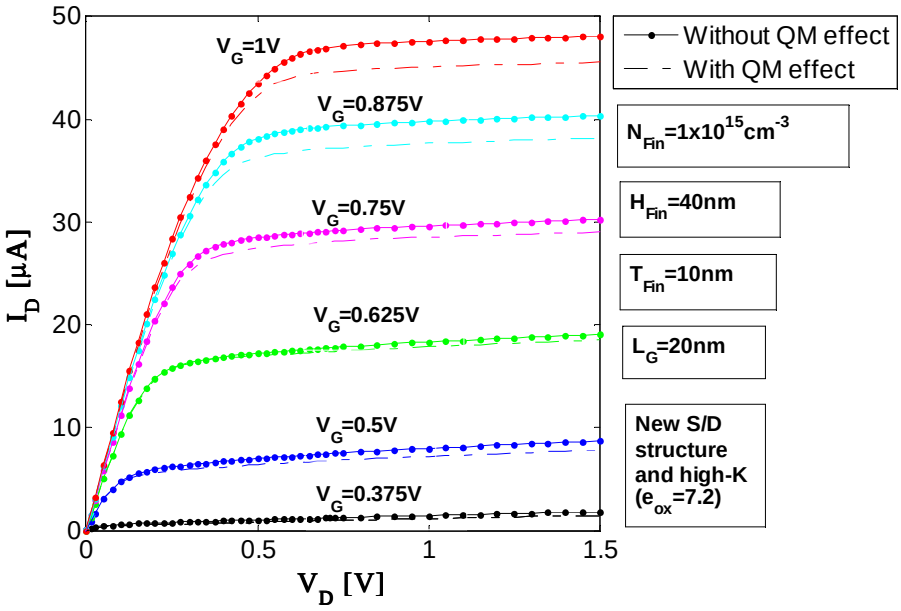


Figure 5.53: I_D-V_D characteristics for different gate voltages. Simulation without (—) QM effects and (–.–) with a QM effect (N_{fin} = 1x10^{15} cm^{-3}, H_{fin} = 60 nm, e_{ox} = 7.2, L_G = 20 nm).

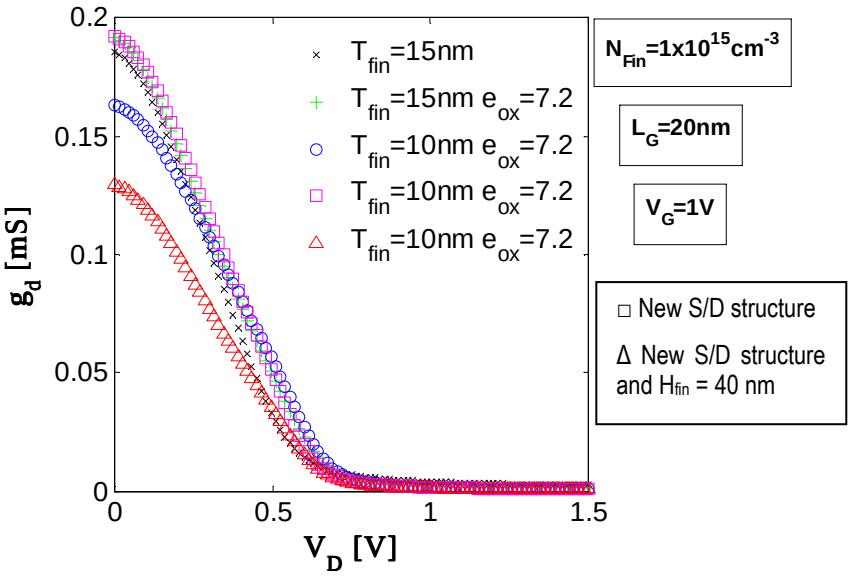


Figure 5.54: Output conductance g_d versus drain voltage V_D for different values of T_{fin}, H_{fin}, e_{ox} and structure of S/D (N_{fin} = 1x10^{15} cm^{-3}, L_G = 20 nm, V_G = 1V).

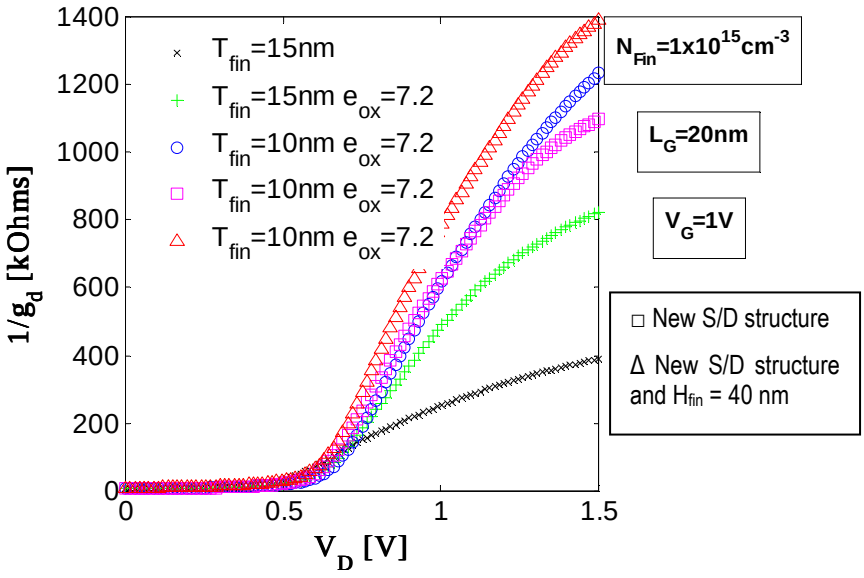


Figure 5.55: Output resistance $1/g_d$ versus drain voltage V_D for different values of T_{fin}, H_{fin}, e_{ox} and structure of S/D ($N_{fin} = 1x10^{15}$ cm^{-3}, $L_G = 20$ nm, $V_G = 1V$).

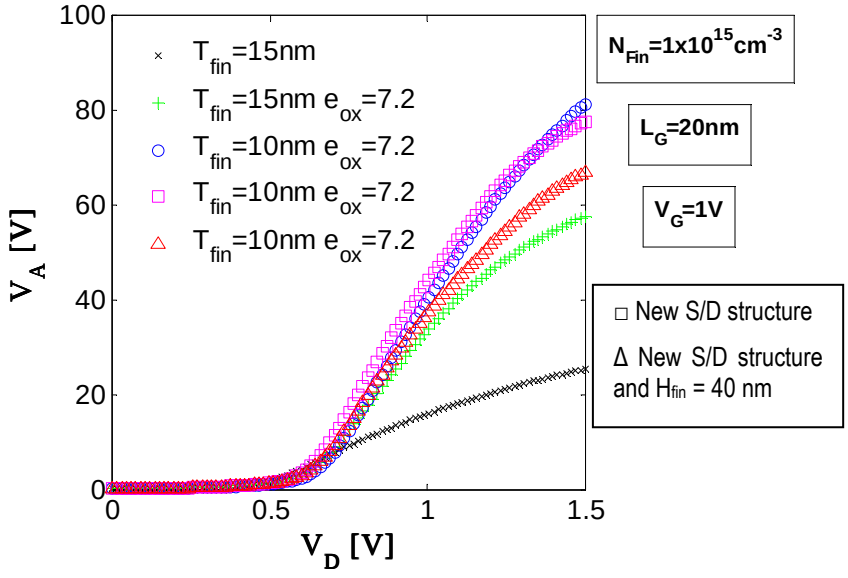


Figure 5.56: Early voltage V_A versus drain voltage V_D for different values of T_{fin}, H_{fin}, e_{ox} and structure of S/D ($N_{fin} = 1x10^{15}$ cm^{-3}, $L_G = 20$ nm, $V_G = 1V$).

5.5 Method of Extraction of R_{SDE}

The series S/D resistance play a significant role on the worth of FETs circuits. It is, therefore, of great importance to have a quantitative measure of the parasitic resistance (R_{SDE}) of the S/D extensions regions, often referred to as S/D parasitic resistance. Considering the source voltage V_S grounded, the effective drain voltage V_{Def} applied do the transistor channel is the drain voltage V_D minus the voltage drop in R_{SDE} or $V_{Def} = V_D - R_{SDE}I_D$. Dividing the last expression by I_D, results in the resistance relation $R_{CH} = R_{SD} - R_{SDE}$, where R_{CH} is the channel resistance and R_{SD} is source-drain total resistance. Many methods of extraction of R_{SDE} have been proposed (Terada, 1979; Suciu, 1980; de la Moneda, 1982; Whitfield, 1985).

In the Whitfield method, I-V characteristics in the linear region of two transistors with the same gate widths ($W_{G2} = W_{G1}$) and different gate lengths ($L_{G2} > L_{G1}$) can be used to extract an approximation for R_{SDE}. Thus, considering the last resistance relation expression for two transistors (with sub-indexes 1 and 2) and considering that the parasitic resistance R_{SDE} of the source-drain extrinsic regions does not change with bias, the difference of the S/D total resistances (R_{SD2}-R_{SD1}) is equal to the difference of the channel resistances ($R_{CH2} - R_{CH1}$). Then with the increase of bias in linear region, ($R_{SD2} - R_{SD1}$) tends to zero since ($R_{CH2} - R_{CH1}$) does the same, and R_{SD1} (or R_{SD2}) tends to R_{SDE}. This dependence can be approximated by a linear relation. The ratio of the channel resistances is approximated by

$$\frac{R_{CH2}}{R_{CH1}} = \frac{(R_{SD2} - R_{SDE})}{(R_{SD1} - R_{SDE})} \cong \frac{L_{Geff\,2}}{L_{Geff\,1}} . \frac{1}{\alpha} \tag{5.2}$$

where $\alpha \equiv \dfrac{(V_{G2} - V_{T2})}{(V_{G1} - V_{T1})}$, and L_{Geff2} and L_{Geff1} are the effective gate lengths $L_{Geff} = L_G - \Delta L$.

The parameter "α" is a correction introduced to account for a difference in the threshold voltages between devices and it was not in the Whitfield method. Other corrections to account for other effects, such as mobility differences, or the modulation of the effective channel length by the gate voltage (Torres-Torres, 2002), are not considered in this work. Considering that

$$\left(\frac{L_{Geff\,2}}{L_{Geff\,1}} - \alpha\right) \cong \left(\frac{L_{Geff\,2}}{L_{Geff\,1}} - 1\right) \tag{5.3}$$

$$\left(L_{Geff\,2} - L_{Geff\,1}\right) = \left(L_{G2} - L_{G1}\right) \tag{5.4}$$

the expression (5.2). is manipulated to result in

$$\alpha.\left(R_{SD2} - R_{SD1}\right) \cong \left(\frac{L_{G2} - L_{G1}}{L_{Geff\,1}}\right).\left(R_{SD1} - R_{SDE}\right) \tag{5.5}$$

The expression (5.5) represents a linear relation and can be plotted from I-V characteristics in the linear region of two transistors. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis.

5.6 Simulation Comparisons and S/D Extensions Effects

This section presents comparative results between 3D numeric device simulators Davinci (Synopsys, 2006) and Sentaurus (Synopsys, 2009). Variations on the S/D extensions profiles are addressed, as well as results with varying device models that are used to adjust the transport in the devices are also presented.

5.6.1 SOI-FinFET Structures

The first step was the description of the SOI-FinFET structures, double-gate, to be simulated with Sentaurus. These structures were described for the simulator Davinci. It is necessary to get great similarity between structures, both geometric and in terms of process parameters, thus allowing a better comparison between simulations and the differences resulting from the different models used.

Two structures with $T_{fin} = 20$ nm were used: a long-channel and a short channel structure with gate lengths of $L_G = 1000$ nm and $L_G = 50$ nm. Two others structures with $t_{ox\_top} = 2$ nm (tri-gate) were used to compare the I-V characteristics of the double-gate and tri-gate devices. One structure with $T_{Box} = 100$ nm, instead of $T_{Box} = 150$ nm, was also simulated. Figure 5.57 shows the basic simulation structure defined for Sentaurus and, in this case, with $t_{ox\_top} = 20$ nm (double-gate). Figure 5.58 and Figure 5.59 show the doping profiles of S/D extension regions (Gaussian and Erfc) with the characteristic length λ_z along z-axis (transversal) and λ_x along x-axis (lateral), i.e., parallel or along current flow. Contacts are at the end of S/D extensions for all structures.

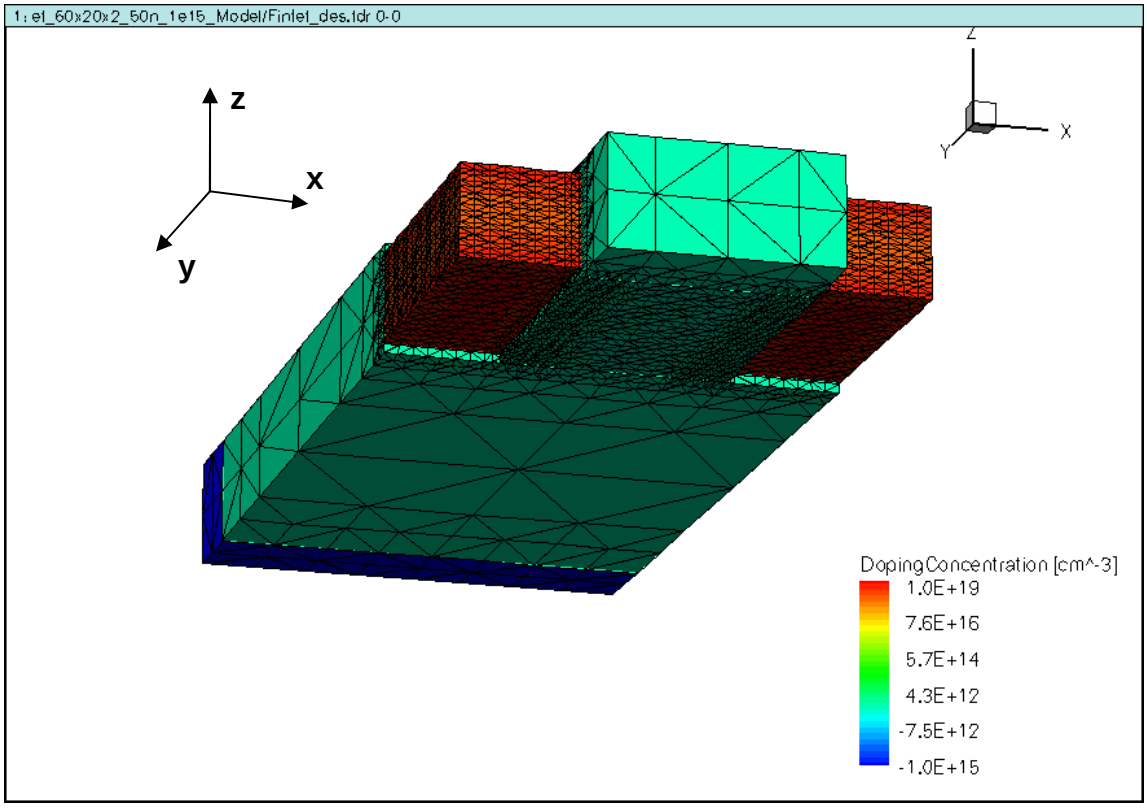


Figure 5.57: Basic 3D simulation structure defined with Sentaurus.

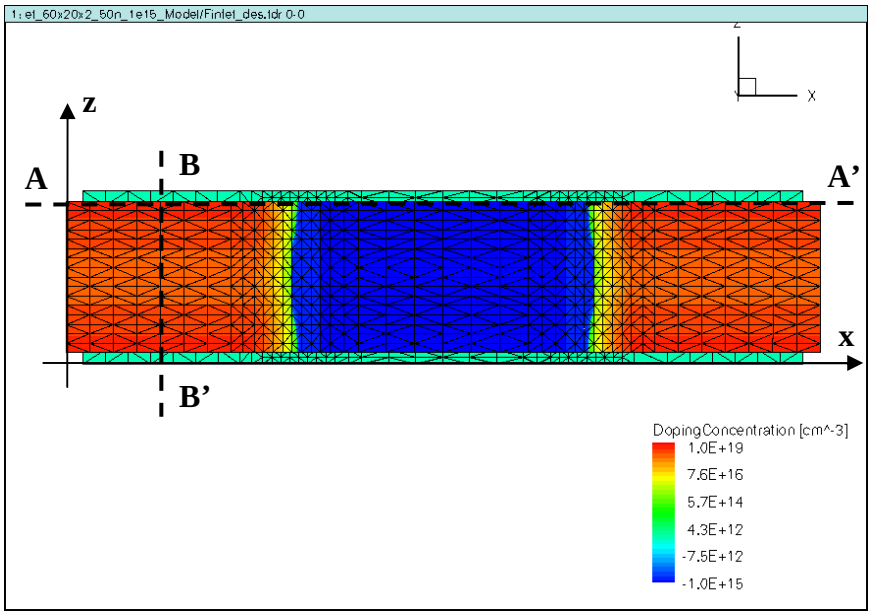


Figure 5.58: Cross-section at the middle of the silicon fin in the xz-plane showing the doping profile of the S/D extensions. Gaussian profile in the z-axis (λ_z = 6.5 nm) and Erfc in the x-axis (λ_x = 2 nm). The 1D doping profiles for cuts B-B' and A-A' are shown in the Figure 5.60.

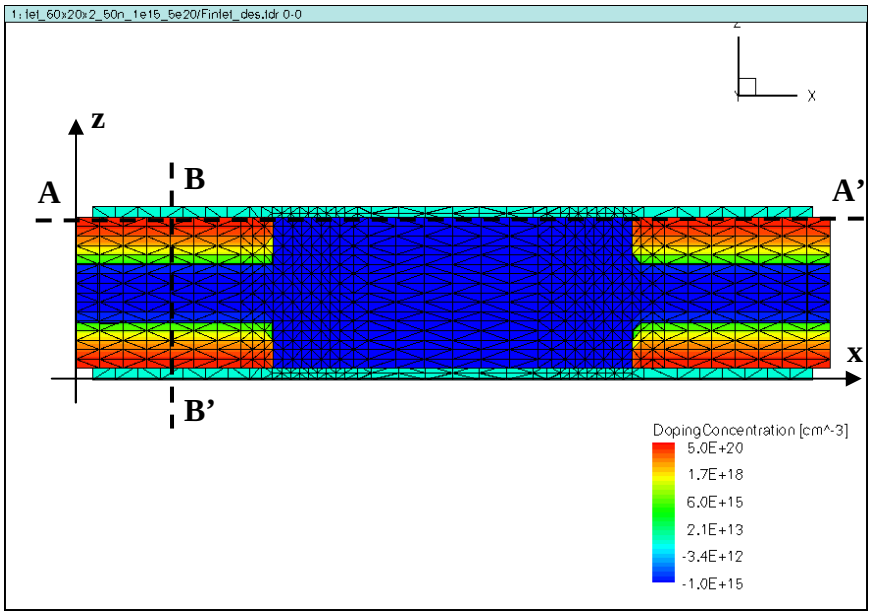


Figure 5.59: Cross-section at the middle of the silicon fin in the xz-plane showing an alternative doping profile of the S/D extensions. A shallow Gaussian profile in the z-axis (λ_z = 1.5 nm) and an abrupt Erfc in the x-axis (λ_x = 0 nm). The 1D doping profiles for cuts B-B' and A-A' are shown in the Figure 5.60.

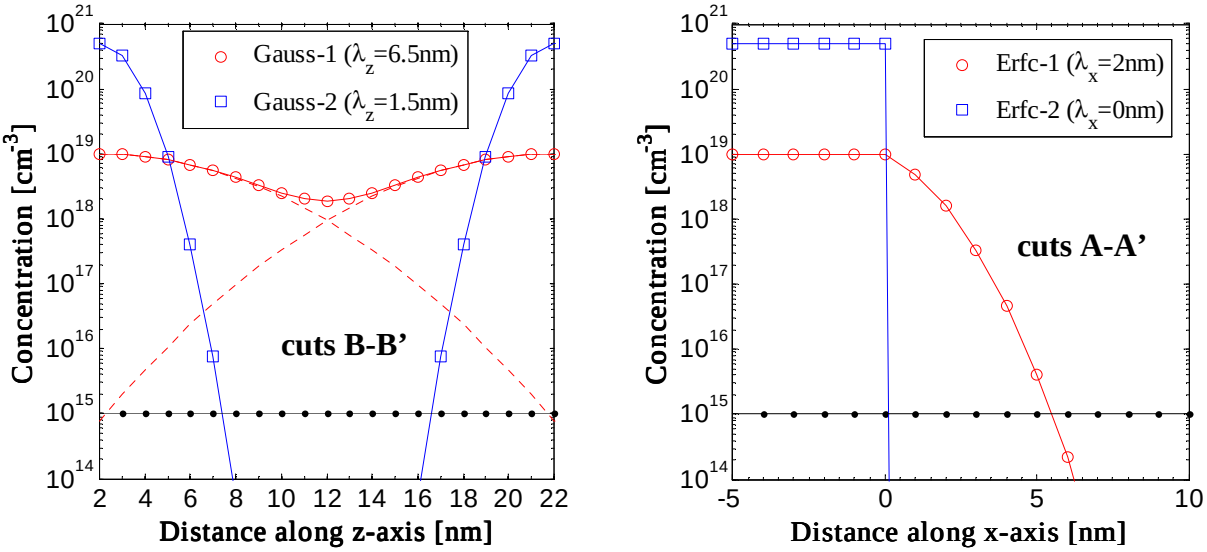


Figure 5.60: Doping profiles for cuts B-B' and A-A' of the cross-sections of Figure 5.58 and Figure 5.59.

5.6.2 Simulation Models - Comparing Simulators and Their Models

Previous in Section 5.2.2, the mobility models and a quantum mechanical model that were used in the simulations with Davinci were briefly described. These models are listed below:

- Concentration-dependent Mobility Model (CONMOB): A low field mobility model that includes the effect of impurity scattering by using mobility values from tables which depend on the local total impurity concentration.

- Surface Mobility Model (SRFMOB): A transverse field mobility model. Davinci allows surface mobility degradation factors and the selection of an effective-field based surface mobility model that is applied only at insulator-semiconductor interfaces.

- Field-dependent Mobility Model (FLDMOB): A parallel field mobility model that accounts for effects due to high field in the direction of current flow, such as carrier heating and velocity saturation effects.

- Quantum Mechanical Effects (QM.PHILI): An approximate method of accounting for quantum mechanical effects in the inversion layer using the van Dort's bandgap widening approach (van DORT, 1994).

The following models were used in the simulations with Sentaurus:

- Doping Dependence Model (DOPINGDEP): A model for the mobility degradation due to impurity scattering. Several model options are available. The default is the Masetti model (Masetti, 1983).

- Lombardi Mobility Model (ENORMAL): A transverse field mobility model that accounts for effects of mobility degradation at interfaces where carriers under high transverse electric field are subjected to scattering by acoustic surface phonons and surface roughness (Lombardi, 1988).

High-k gate dielectrics are being considered as an alternative to SiO_2 to reduce unacceptable leakage currents as transistor dimensions become smaller. One obstacle when using high-k gate dielectrics is that degraded carrier mobility is often observed for such devices. Although the causes of high-k mobility degradation are not completely understood, two possible contributors are remote Coulomb scattering (RCS) and remote phonon scattering (RPS).

- Canali Model (HIGHFIELDSAT): A saturation mobility model that accounts for effects due to high electric fields in the direction of current flow, where the carrier drift velocity is no longer proportional to the electric field and the velocity saturates to a finite speed (Canali, 1975).

- Philips Unified Mobility Model (PHUMOB): A low field mobility model that includes acceptor, donor, and carrier-carrier. The Philips unified mobility model (Klaassen, 1992), unifies the description of majority and minority carrier bulk mobilities. The model describes the temperature dependence of the mobility and takes into account electron–hole scattering, screening of ionized impurities by charge carriers and clustering of impurities.

- Generation-Recombination model (SRH(DopingDep)): A Shockley–Read–Hall Recombination (SRH) model in which the evaluation of the SRH lifetimes is done according to the Scharfetter model (Fossum, 1982).

- Intrinsic carrier concentration model (EffectiveIntrinsicDensity (BandGapNarrowing (OldSlotboom))): This is the silicon bandgap narrowing model that determines the intrinsic carrier concentration. In this case, using the Slotboom model (Slotboom, 1976).

Sentaurus implements four quantization models to account for quantum mechanical effects: the van Dort model (van DORT, 1994), the 1D Schrödinger equation, the density gradient model (Ancona, 1987) and the modified local-density approximation (Paasch, 1982). These models are based on a potential-like quantities introduced in the classical density formulas for electrons and holes. They differ in numeric expense and in physical sophistication. The following model was used in the simulations with Sentaurus:

- Quantum Potential Model (QUANTUMPOTENTIAL): A density gradient quantization model (Ancona, 1987) (Ancona, 1989). A keyword has to be specified if only one carrier is considered. For example, eQUANTUMPOTENTIAL for electrons.

The conventional drift-diffusion transport model tends to lose its full validity in the deep submicron regime and fails to predict effects such as velocity overshoot and often overestimates the impact ionization generation rates. The solution of the Boltzmann kinetic equation using the Monte Carlo Method is a better approach. However, it is

normally very expensive in computational time. The energy balance model (Roberts, 1990) or the so called hydrodynamic model offers a very good trade-off between numeric expense and physical sophistication. The following model was used in the simulations with Sentaurus:

- Hydrodynamic Transport Model (HYDRODYNAMIC): An energy balance model that solves the temperature equations for electrons and holes. If only one carrier equation is to be solved an argument or keyword has to be specified. For example, HYDRODYNAMIC (eTemperature), for electrons.

5.6.3 Comparison of Simulators and Models

In this section, Davinci and Sentaurus simulations are compared under several model conditions. I_D-V_G characteristics in linear region (V_D = 100 mV) were simulated. In the first part of the simulations, the FinFET structures have the same doping profiles and only the simulator and models were changed for each gate length. The exception is the curve market with the legend "Sent(trig)", on which the top-gate oxide (t_{ox_top}) is reduced to 2 nm, making the structure a tri-gate FinFET. In the second part of the simulations (next sections), the FinFET structures have different doping profiles for the S/D extensions. In Table 5.3 are summarized the conditions under which each curve was obtained. It is necessary to give a few explanations about the models used in the simulations.

In the case of Davinci device simulator (SYNOPSYS, 2006), mobility for low, transversal, lateral and high electrical fields stands for: a mobility model for low fields that includes the effect of impurity scattering, using mobility values from tables, which depend on the local total impurity concentration; a transverse field mobility model that allows surface mobility degradation factors and the selection of a surface mobility model (based on effective-field) that is applied only at insulator-semiconductor interfaces; a lateral field mobility model that accounts for effects due to high field in the direction of current flow, such as carrier heating and velocity saturation effects.

In the case of Sentaurus device simulator (SYNOPSYS, 2009), mobility for low, transversal, lateral and high electrical fields stands for: a model for the mobility degradation due to impurity scattering (default Masetti model is used); a transverse field mobility model that accounts for effects of mobility degradation at interfaces, where carriers under high transverse electric field are subjected to scattering by acoustic surface phonons and surface roughness (default Lombardi model is used); a saturation mobility model that accounts for effects due to high electric fields in the direction of current flow, where the carrier drift velocity is no longer proportional to the electric field and the velocity saturates to a finite speed (the Canali model is used).

Other models used: a low field mobility model that includes acceptor, donor, and carrier-carrier, is the Philips unified mobility model; a Shockley–Read–Hall Recombination (SRH) model in which the evaluation of the SRH lifetimes is done according to the Scharfetter model; a silicon bandgap narrowing model that determines the intrinsic carrier concentration (Slotboom model is used); a density gradient quantization model by Ancona; and an energy balance model that solves the temperature equations for electrons and holes, or an hydrodynamic model.

Table 5.3: Conditions under which each simulated I-V characteristic curve of the SOI-FinFET structure was obtained.

#	**Caption (curves)**	**Simulator**	**Models (keywords)**	**N_D , λ_z, λ_x, t_{ox}, t_{ox_top}, T_{Box}**
1	Davinci	Davinci	conmob srfmob fldmob	N_D=1x10^{19} cm^{-3} (peak), λ_z=6.5 nm, λ_x=2 nm, t_{ox}=2 nm, t_{ox_top}=20 nm, T_{fin}=20nm T_{Box}=150 nm
2	Sentaurus	Sentaurus	DopingDep HighFieldsat Enormal **PhuMob SRH(DopingDep) OldSlotboom**	Idem, as #1
3	Sent(basic)	Sentaurus	DopingDep HighFieldsat Enormal	Idem, as #1
4	Sent(hydro)	Sentaurus	Idem, as #2, plus: **Hydrodynamic (eTemperature)**	Idem, as #1
5	Sent(trig)	Sentaurus	Idem, as #2	Idem, as #1, but **t_{ox_top}=2 nm**
6	Sent(quant)	Sentaurus	Idem, as #2, plus: **eQuantumPot**	Idem, as #1
7	Sent(2e19)	Sentaurus	Idem, as #2	Idem, as #1, but **N_D=2x10^{19} cm^{-3}** (peak)
8	Sent(1e20)	Sentaurus	Idem, as #2	Idem, as #1, but **N_D=1x10^{20} cm^{-3}** (peak)
9	Sent(5e20)	Sentaurus	Idem, as #2	**N_D=5x10^{20} cm^{-3}** (peak), **λ_z=1.5 nm, λ_x=0nm**, t_{ox}=2 nm, t_{ox_top}=20 nm, T_{fin}=20nm T_{Box}=150 nm
10	Sent(tbox100)	Sentaurus	Idem, as #2	Idem, as #9, but **T_{Box}=100 nm**
11	Sent(lmob)	Sentaurus	Idem, as #2, but: **Enormal with increase in mobility degradation**	Idem, as #9
12	Sent(lmob2)	Sentaurus	Idem, as #11	Idem, as #1

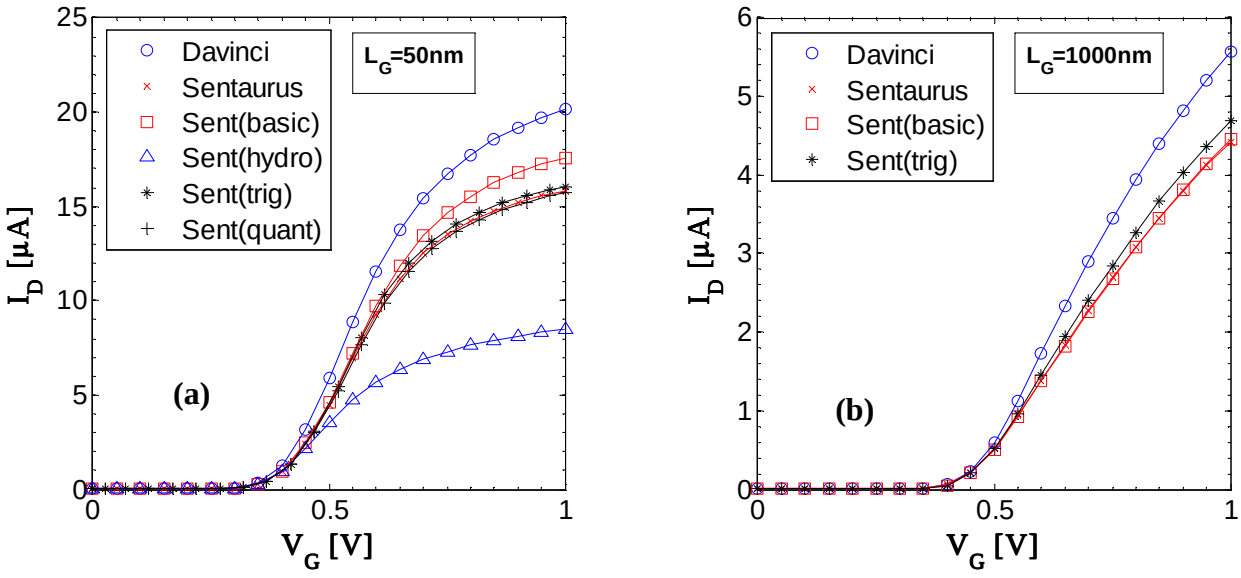


Figure 5.61: I_D-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

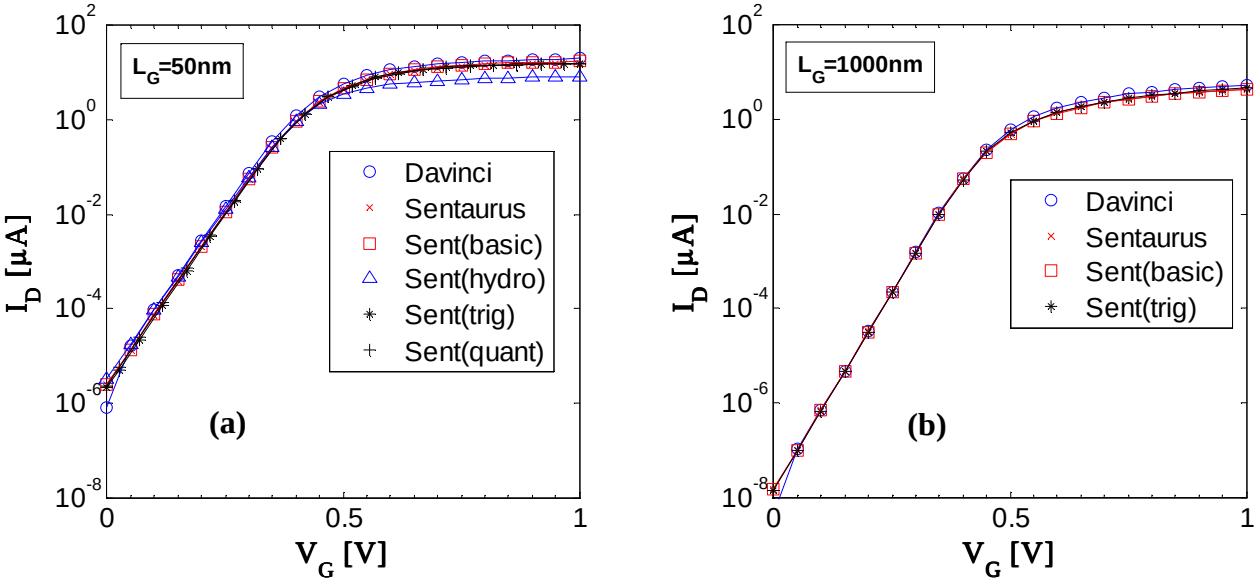


Figure 5.62: I_D-V_G characteristics (log. scale) (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

Figure 5.61 and Figure 5.62 show the simulated I_D-V_G characteristics in linear region (V_D = 100 mV) for the SOI-FinFET devices, in linear and log. scale respectively. A good agreement was obtained in the sub-threshold region, for both short and long-channel devices, where the difference in models is not very significant. However, in the moderate and strong inversion regions, significant differences appear (±25% in final

current), suggesting a probable over estimation of drain current by the simulator Davinci (see Table 5.3).

Little difference is noted between Sentaurus simulations, especially for the long-channel FinFET, even when a quantization model is used. The top-gate of the tri-gate structure contributes only with approximated 5% for the final current due to the aspect ratio H_{fin}/T_{fin} of 3. Great differences are apparent with the hydrodynamic model, indicating the need for a better set of coefficients in this case.

The contribution of the series resistance of the S/D extension regions R_{SDE} for the final current is certainly very important, especially for the short-channel FinFET.

In Table 5.4 are summarized the extracted threshold voltages V_T, subthreshold slopes S, turn-on currents I_{on} (for $V_G = 1$ V) and source-drain total resistances R_{SD}. The V_T voltages were extracted with the method "GMLE".

Table 5.4: Threshold voltages V_T (method "GMLE"), subthreshold slopes S, I_{on} and R_{SD} from I_D-V_G simulated data ($V_D = 100$ mV).

Caption (curves)	**V_T (mV)** L_G		**S (mV/dec)** L_G		**I_{on} (µA)** (V_G=1V) L_G		**R_{SD} (kΩ)** (V_G=1V) L_G	
	50nm	1µm	50nm	1µm	50nm	1µm	50nm	1µm
Davinci	334.7	382.6	67.1	59.8	20.2	5.57	5.0	18.0
Sentaurus	332.6	375.8	68.0	59.7	15.8	4.42	6.3	22.6
Sent(basic)	332.9	375.7	68.0	59.7	17.6	4.46	5.7	22.4
Sent(hydro)	322.9	-----	69.0	-----	8.49	-----	11.8	-----
Sent(trig)	333.6	379.7	67.7	59.7	16.0	4.70	6.2	21.3
Sent(quant)	329.2	-----	67.9	-----	15.7	-----	6.4	-----
Sent(2e19)	328.1	376.5	69.6	59.7	22.2	4.73	4.5	21.1
Sent(1e20)	326.3	377.8	72.6	59.7	42.4	5.26	2.4	19.0
Sent(5e20)	332.4	377.9	70.4	59.7	41.7	5.25	2.4	19.0
Sent(tbox100)	332.9	379.4	70.5	59.8	41.5	5.21	2.4	19.2
Sent(lmob)	332.0	372.7	70.4	59.6	36.4	4.00	2.7	25.2

Figure 5.63, Figure 5.64, and Figure 5.65 show, respectively, the extracted g_m vs. V_G, g_m/I_D vs. V_G, and g_m/I_D vs. $I_D/(W/L)$, from I_D-V_G characteristics of Figure 5.61.

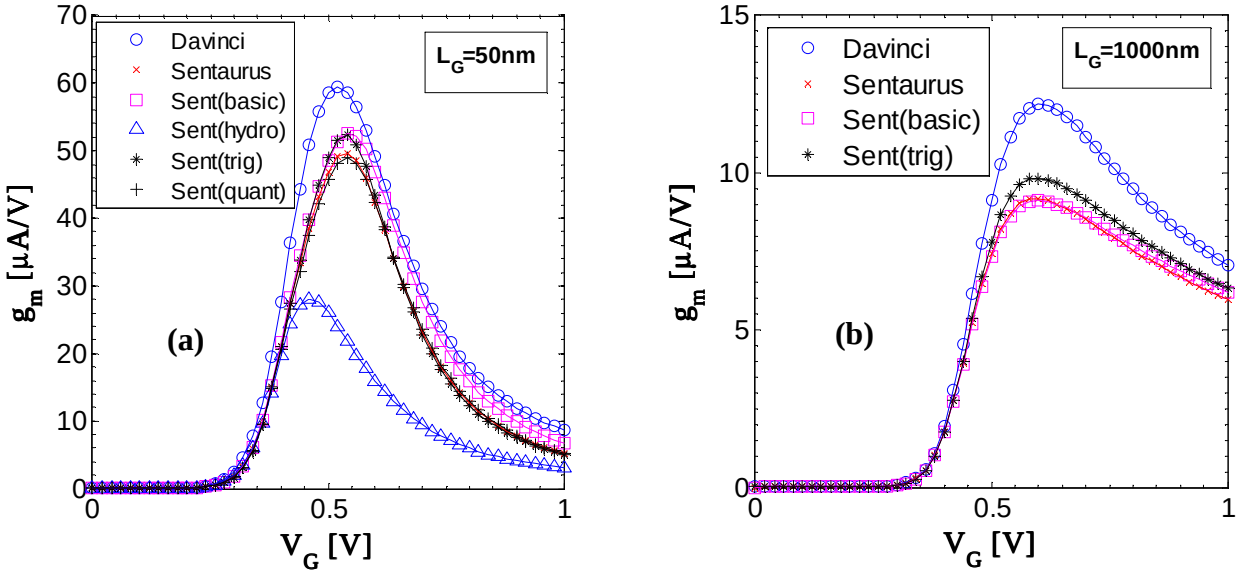


Figure 5.63: g_m-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

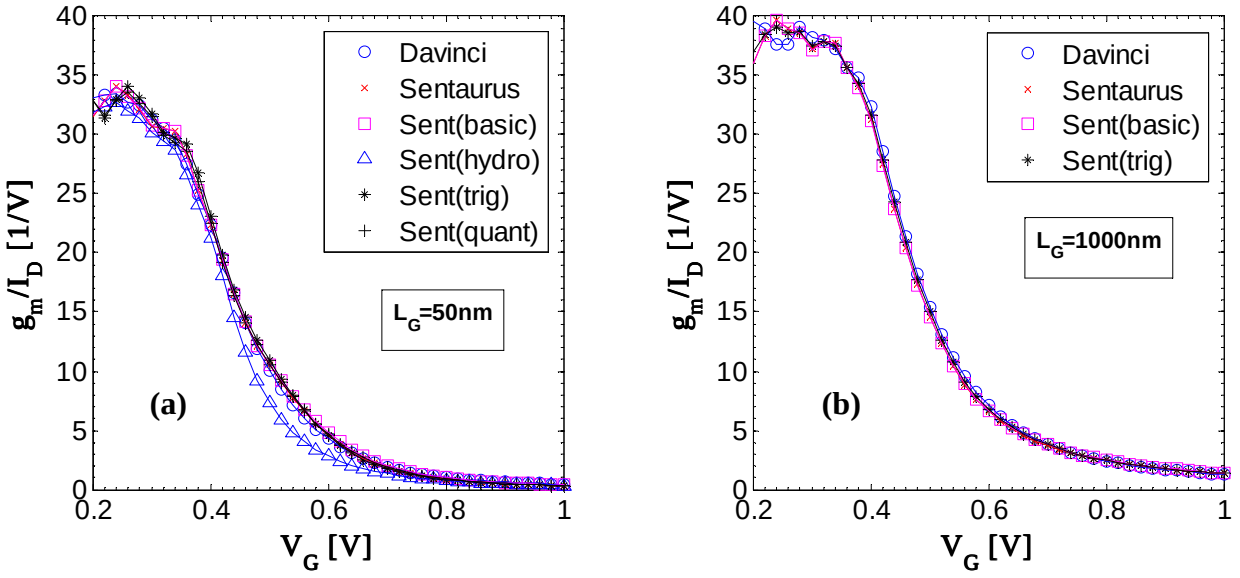


Figure 5.64: g_m/I_D-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

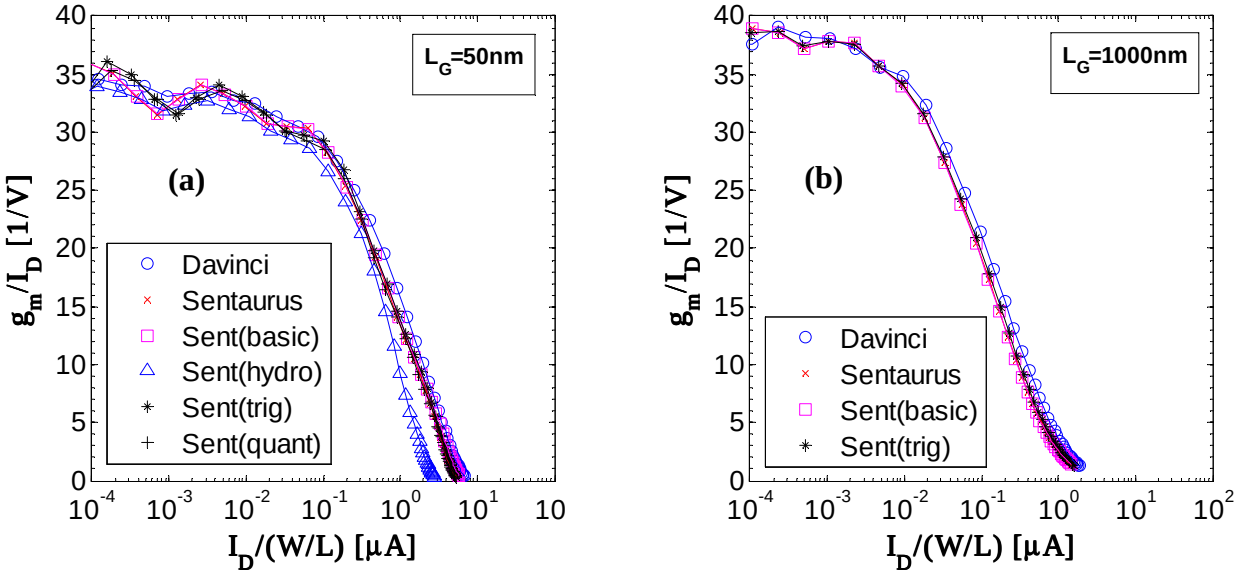


Figure 5.65: g_m/I_D-$I_D/(W/L)$ characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

5.6.4 Comparison of FinFET Structures and Extraction of R_{SDE}

In this section, the FinFET structures simulated with Sentaurus have different doping profiles for the S/D extensions (see Figure 5.59 and Table 5.3). Figure 5.66 and Figure 5.67 show simulated I_D-V_G characteristics in linear region (V_D = 100 mV) for the SOI-FinFET devices. The over estimation of drain current by the simulator Davinci is more evident. For the long-channel case, even the FinFET structures with the highest doping concentration for the S/D extensions give approximated 6% less final current.

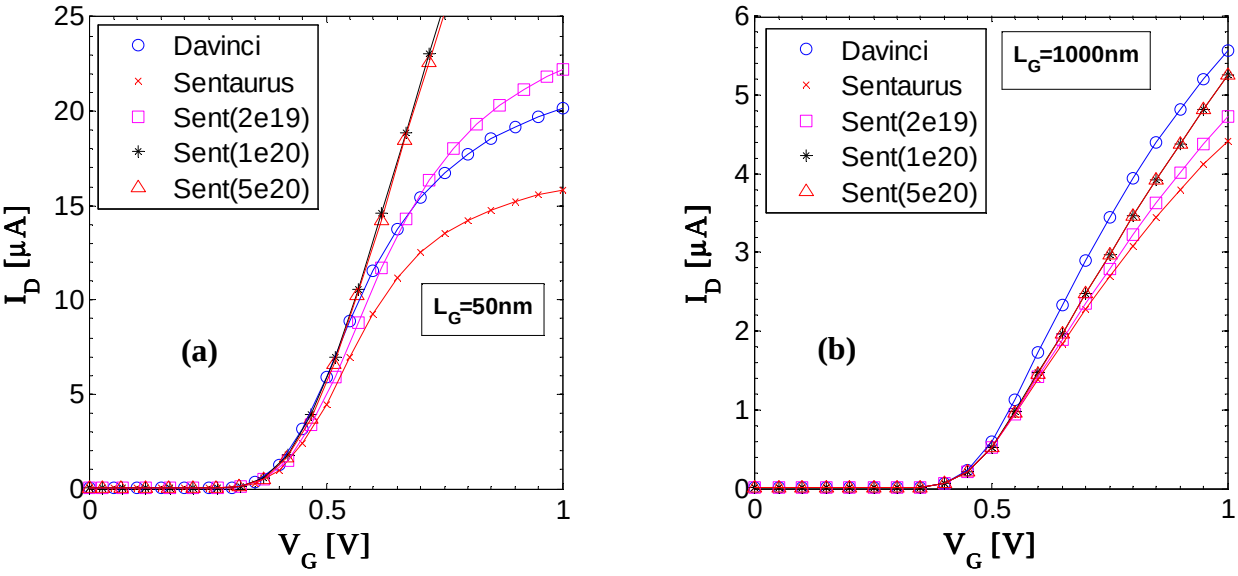


Figure 5.66: I_D-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

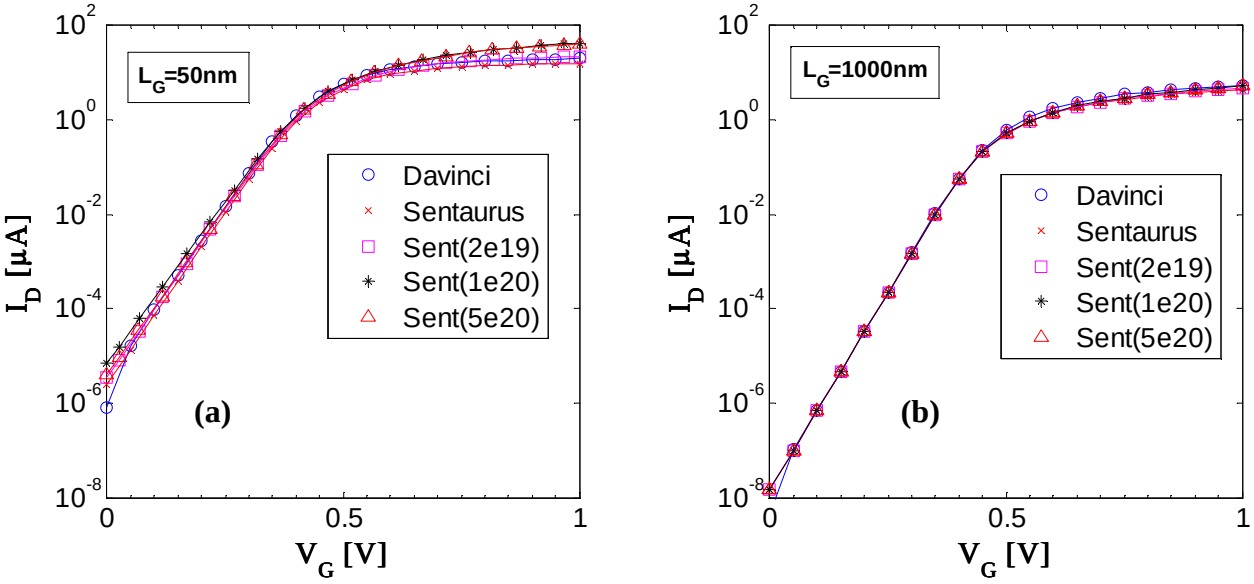


Figure 5.67: I_D-V_G characteristics (log. scale) (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

Figure 5.68, Figure 5.69, and Figure 5.70 show, respectively, the extracted g_m vs. V_G, g_m/I_D vs. V_G, and g_m/I_D vs. $I_D/(W/L)$, from I_D-V_G characteristics of Figure 5.66.

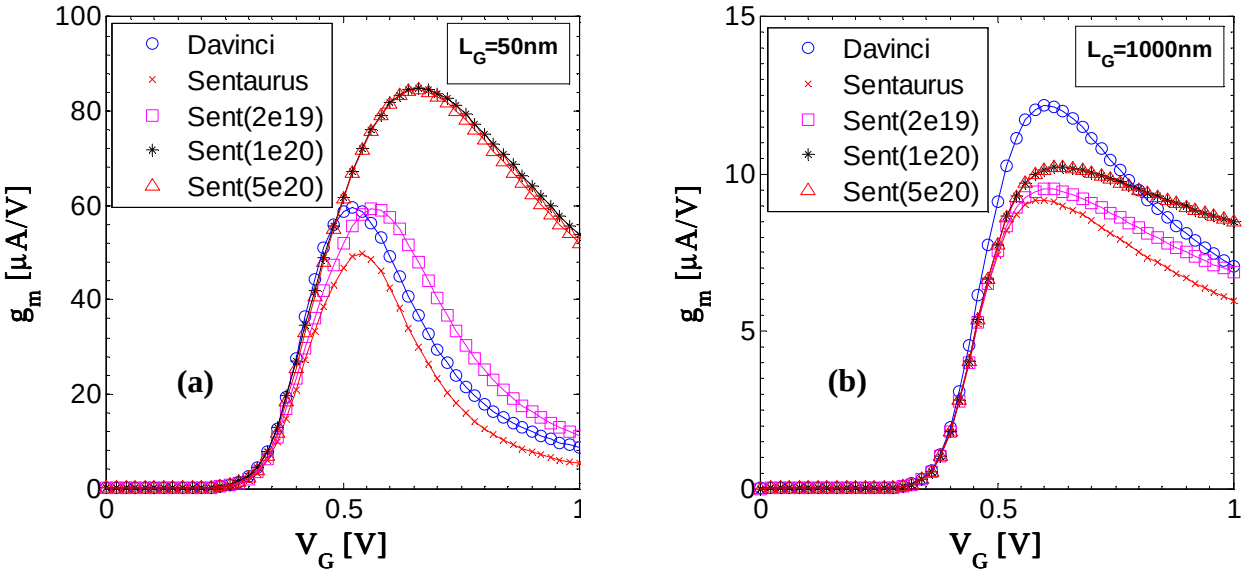


Figure 5.68: g_m-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

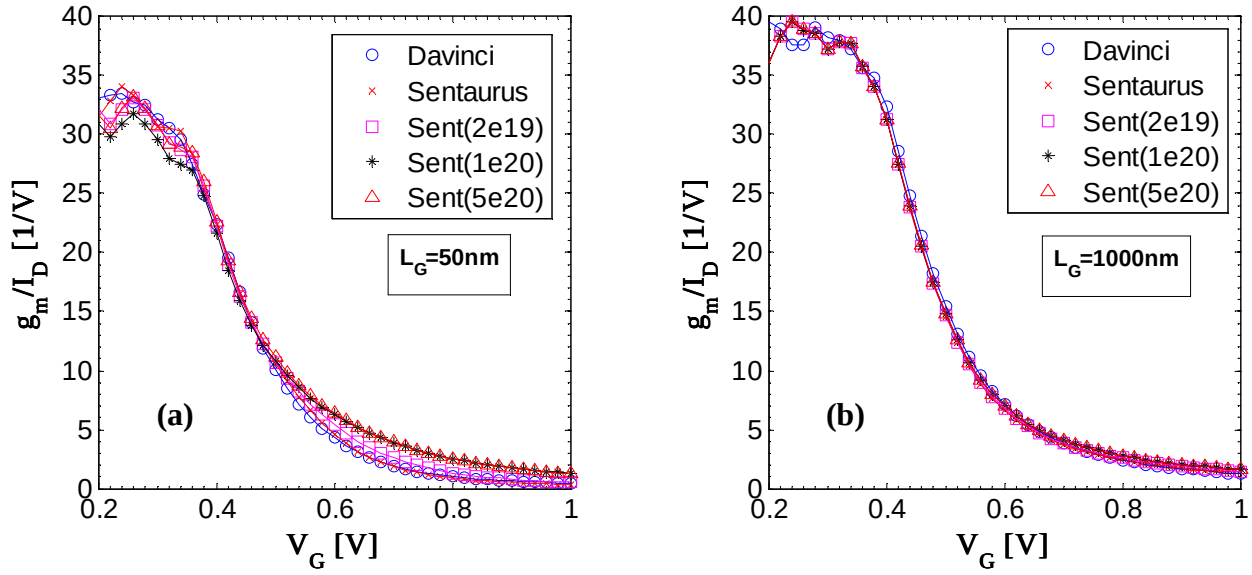


Figure 5.69: g_m/I_D-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

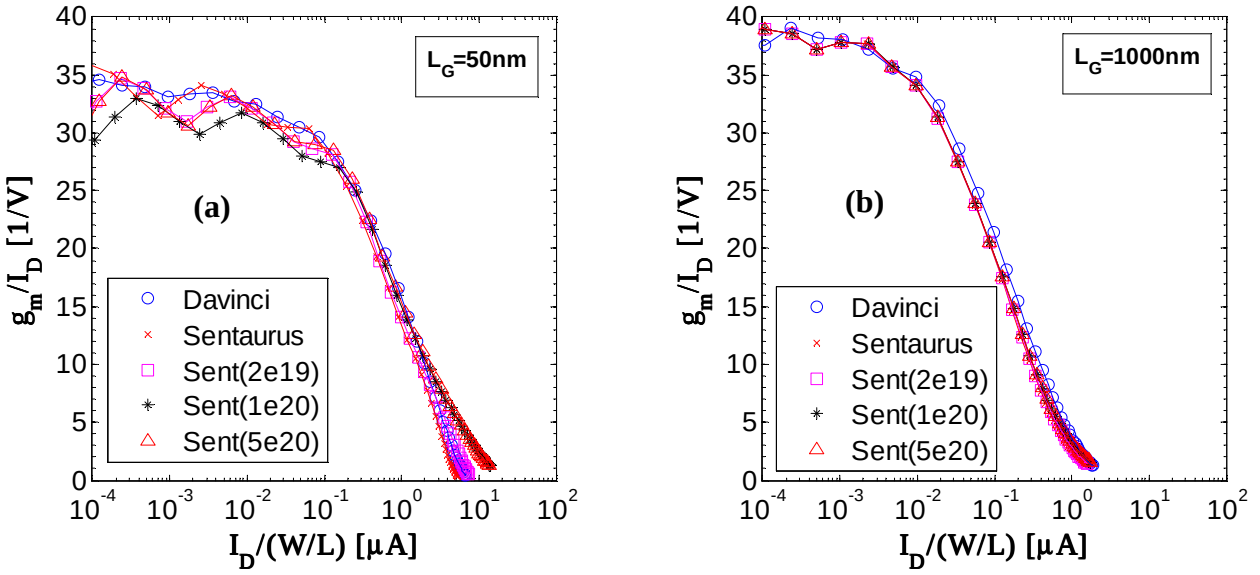


Figure 5.70: g_m/I_D-$I_D/(W/L)$ characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

The simulated data for two SOI-FinFET devices of Figure 5.66 were used for the extraction of the parasitic resistance R_{SDE} of the S/D extension region. Figure 5.71 shows these data from pairs of FinFET devices (a short and a long-channel SOI-FinFET) plotted as in expression (5.5), in Section 5.5. The data were selected to be in strong inversion but with a gate voltage overdrive of only a few hundreds of milivolts to avoid that expression (5.5) lose its validity. The parameter "α" is a correction introduced to account for a difference in the threshold voltages.

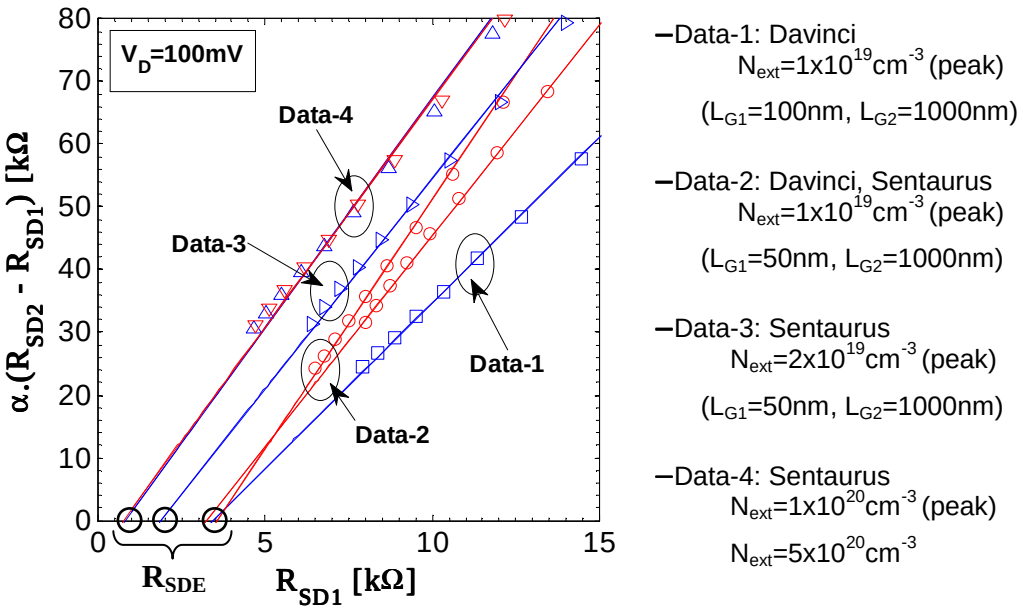


Figure 5.71: Simulated data from pairs of FinFET devices (a short- and a long-channel FinFET) plotted as the difference of the source-drain total resistances (R_{SD2}-R_{SD1}) versus the source-drain total resistance R_{SD1} of the short-channel FinFET.

Data set "Data-1" are from simulations with Davinci (L_{G1} = 100 nm, L_{G2} = 1 µm). The simulated data for the SOI-FinFET of gate length 100 nm are not plotted in Figure 5.66. Data set "Data-2" are from simulations from Davinci and Sentaurus (L_{G1} = 50 nm, L_{G2} = 1 µm). These two data sets share the same doping and geometry for the source-drain extrinsic regions and the results point to the same S/D parasitic resistance R_{SDE} as expected. The values extracted for R_{SDE} are around 3.5 kΩ. Data set "Data-3" are from simulations with Sentaurus but with an increased peak doping concentration of the S/D extrinsic regions of two times (2x). The value extracted for R_{SDE} is around 2 kΩ, a reduction of 43%. Data set "Data-4" are also from simulations with Sentaurus but for two doping of the S/D extrinsic regions: a ten times (10x) increased peak concentration and a fifty times increased (50x) peak concentration but with shallow doping (see Figure 5.59 and Table 5.3). Both values extracted for R_{SDE} are less than 1 kΩ. A further reduction of more than 50% is verified. Considering the error generated by the method in the extracted values of R_{SDE}, this values are in agreement with the values of R_{SD} listed in Table 5.4.

5.6.5 Comparison of FinFET Structures and Models Parameters

In this section, the FinFET structures simulated with Sentaurus have the same doping profile for the S/D extensions, a fifty times increased (50x) peak concentration but with shallow doping (see Figure 5.59 and Table 5.3). One can compares the impact of the reduction of T_{Box} and the increase in mobility degradation. Considering the Sentaurus structures, the reduction of 33 % in T_{Box} has produced negligible effect in the drain current I_D while the increase in mobility degradation has caused a reduction in I_D of 14 % (short-channel device) and 23 % (long-channel device).

Figure 5.72 and Figure 5.73 show simulated I_D-V_G characteristics in linear region (V_D = 100 mV) for the FinFET devices.

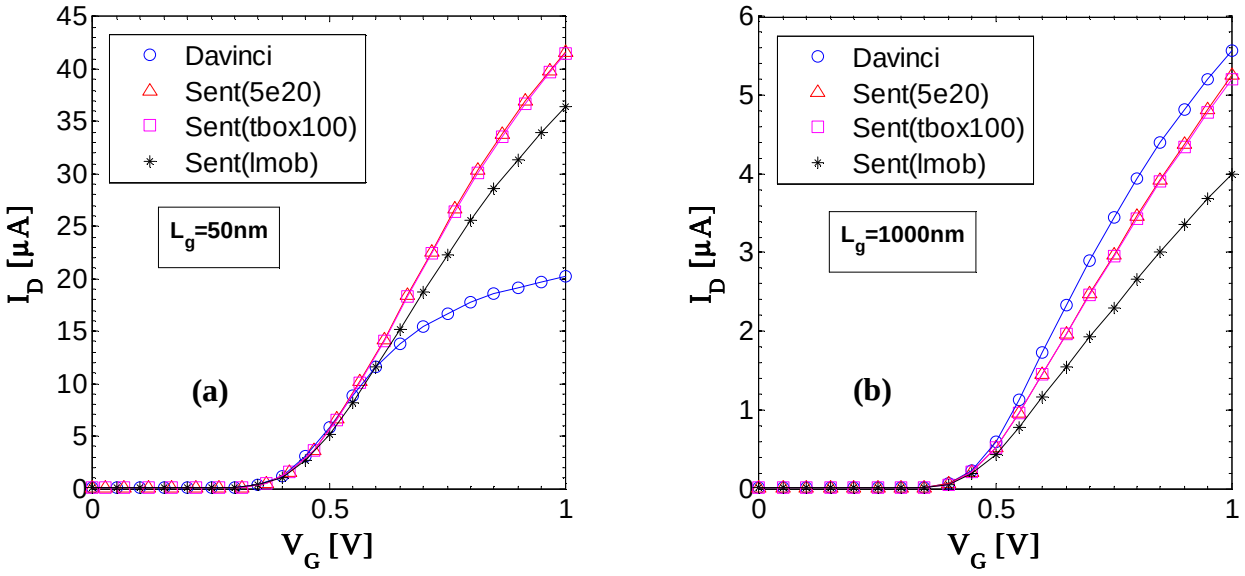


Figure 5.72: I_D-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

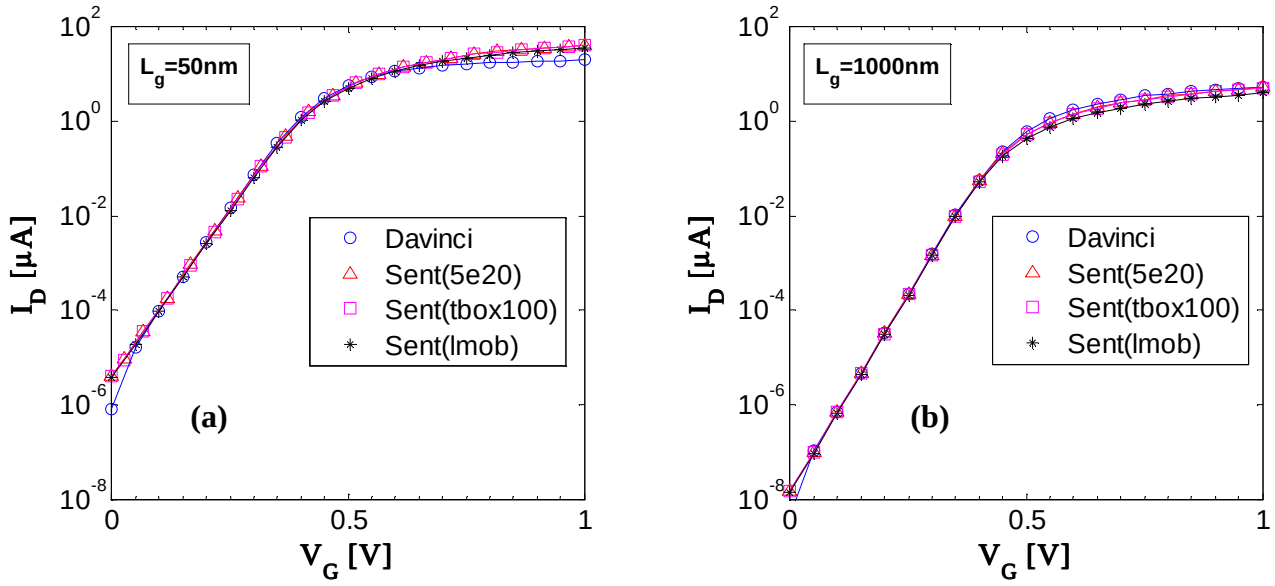


Figure 5.73: I_D-V_G characteristics (log. scale) (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

Figure 5.74, Figure 5.75, and Figure 5.76 show, respectively, the extracted g_m vs. V_G, g_m/I_D vs. V_G and g_m/I_D vs. $I_D/(W/L)$, from I_D-V_G characteristics of Figure 5.72.

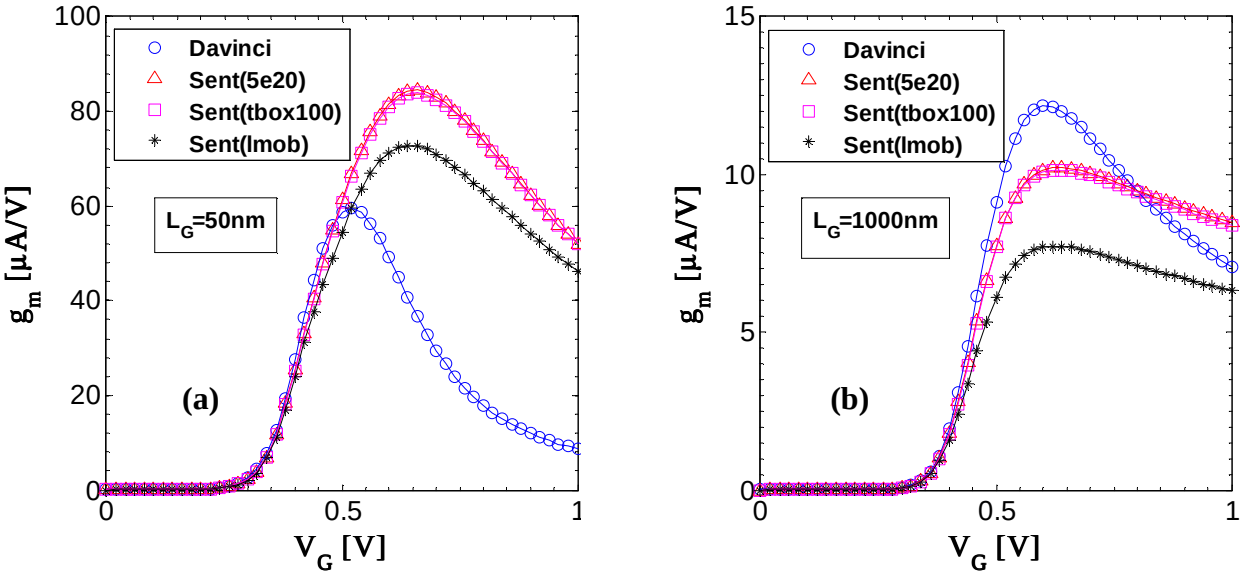


Figure 5.74: g_m-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

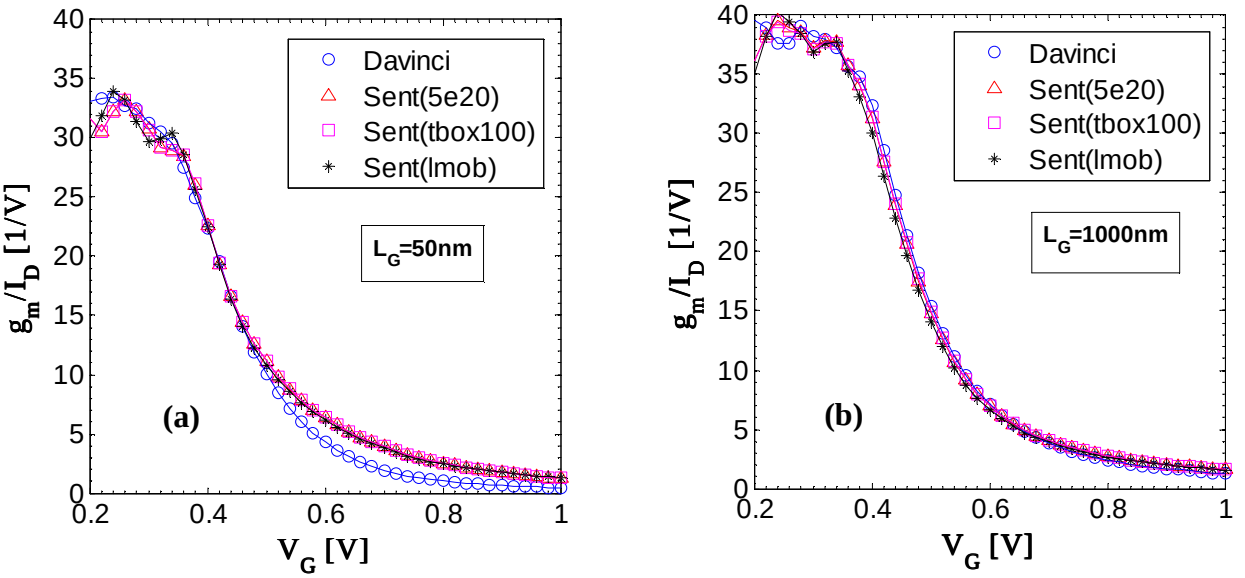


Figure 5.75: g_m/I_D-V_G characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

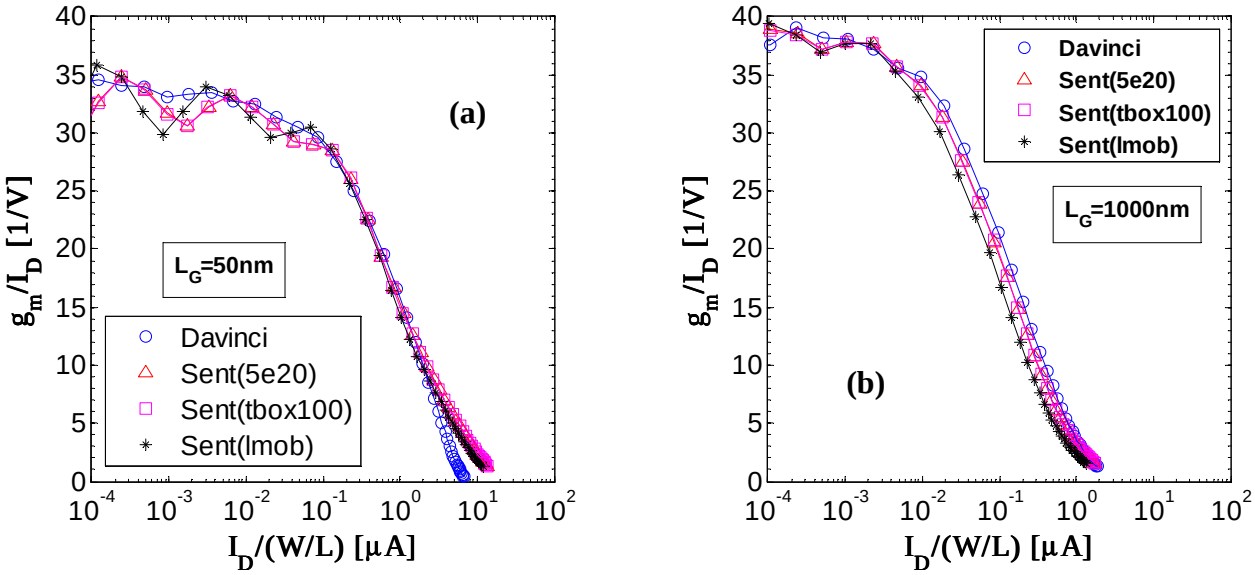


Figure 5.76: g_m/I_D-$I_D/(W/L)$ characteristics (V_D = 100 mV) for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

5.6.6 I_D-V_D Characteristics

Figure 5.77 show I_D-V_D characteristics for different gate voltages. Figure 5.78, Figure 5.79, and Figure 5.80 show, respectively, the output conductance g_d, the output resistance $1/g_d$, and the early voltage V_A, all parameters versus drain voltage V_D. These figures show the impact of the increase in mobility degradation (see Table 5.3).

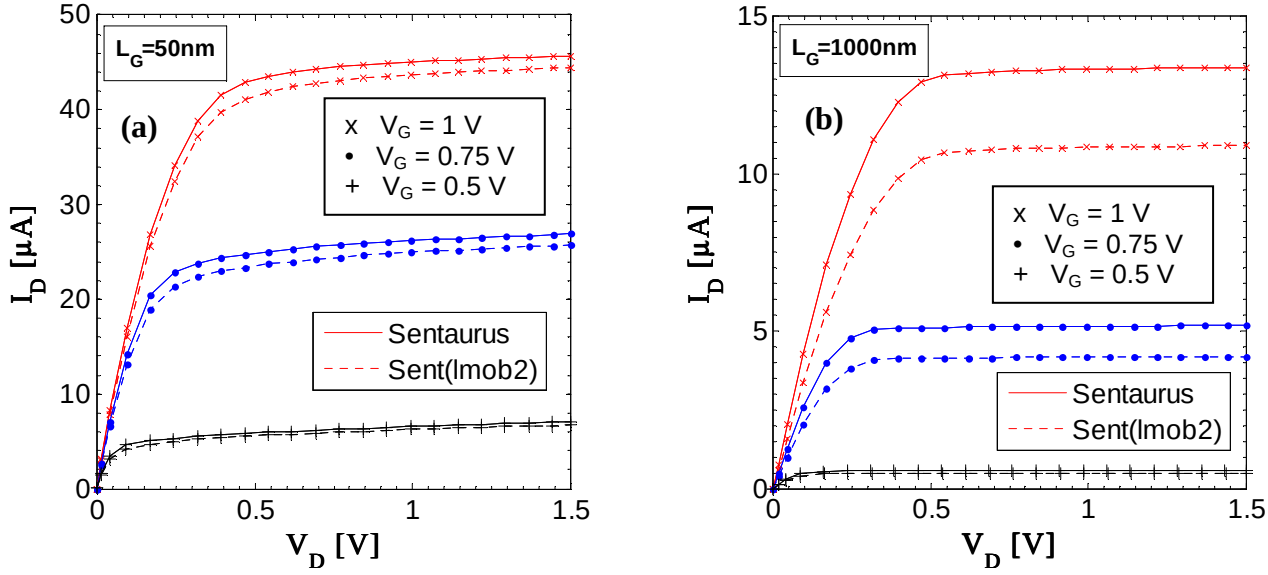


Figure 5.77: I_D-V_D characteristics for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

The two mobility models disagree by up to 10% to 20% in saturation current calculation. For the incremental $g_{d,}$ agreement is very good even for L_G = 50 nm.

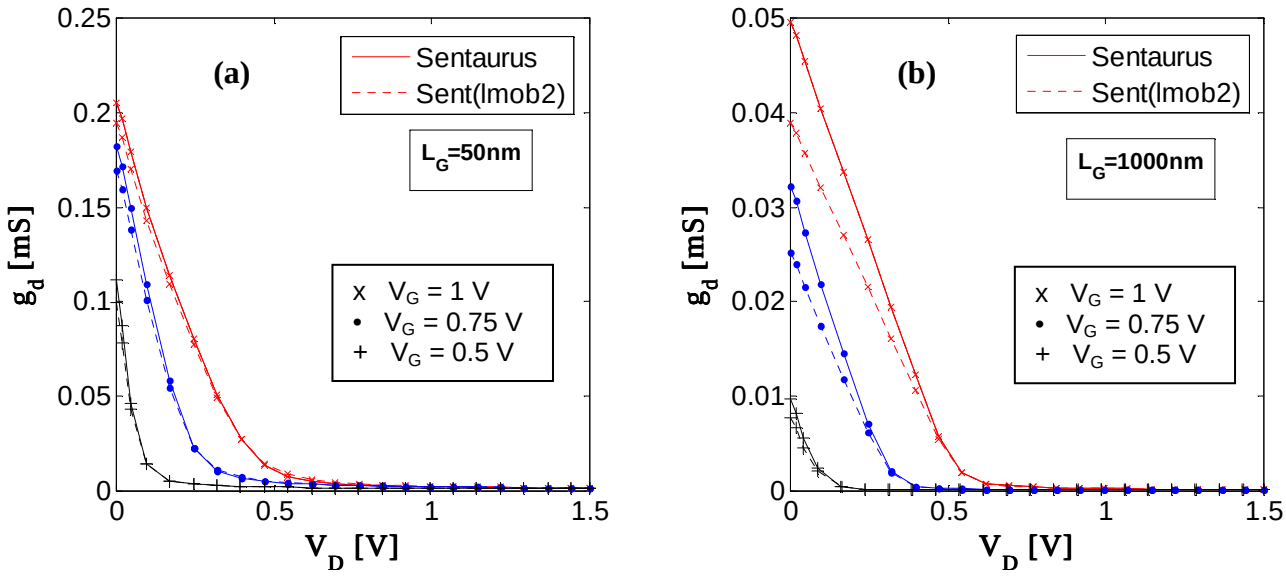


Figure 5.78: g_d-V_D characteristics for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

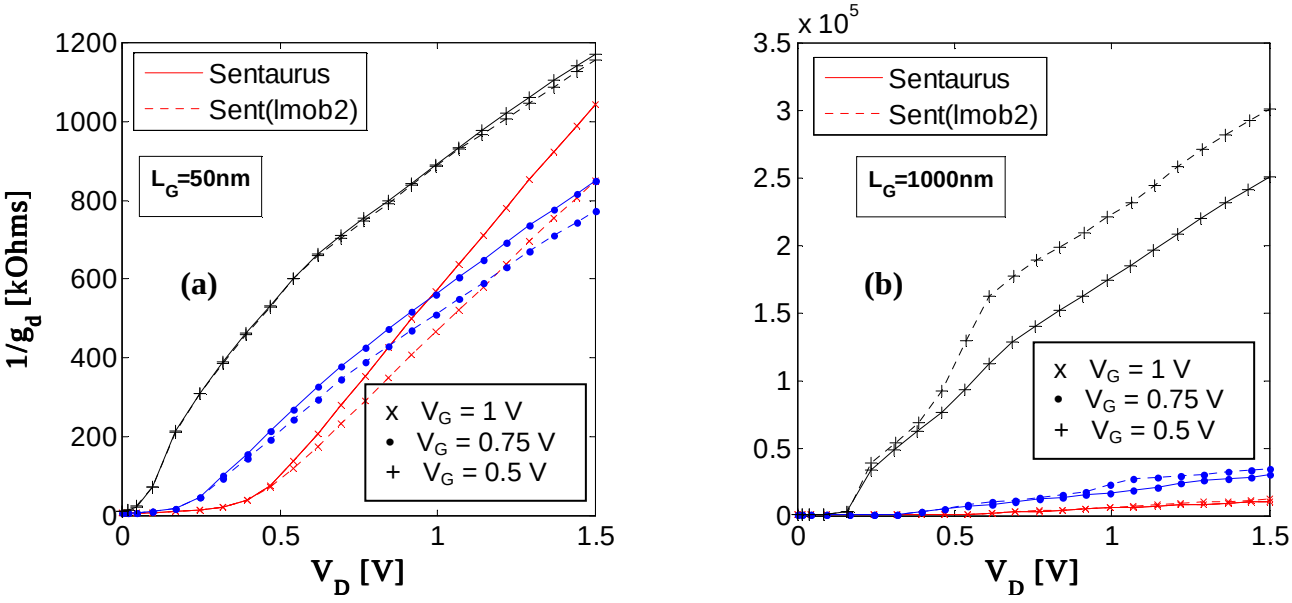


Figure 5.79: $1/g_d$-V_D characteristics for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

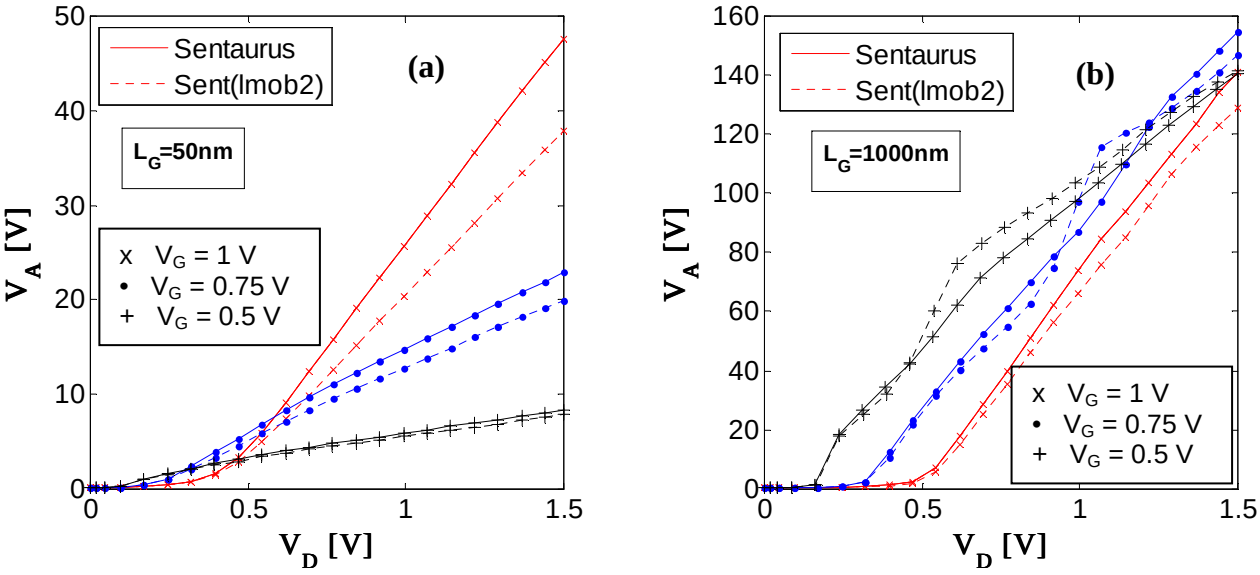


Figure 5.80: V_A-V_D characteristics for FinFET devices with T_{fin} = 20 nm: (a) short-channel (L_G = 50 nm) and (b) long-channel (L_G = 1 µm).

5.7 Effects of S/D Extension Implantation Methods – Simulation Results

In multi-gate FinFET technology is a common practice the use of high-angle, two-pass, implants to dope the sidewalls of the silicon fin. This section addresses the effects of S/D extension implantation methods, as a function of the ion implantantion (I/I) angle (α_I), resulting in different doping profiles for the S/D extensions.

5.7.1 SOI-FinFET Structures

The scheme of ion implantation (first-pass) into the source-drain region is depicted in Figure 5.81, showing its incidence angle and how it affects the doses, transversal (D_{trans}, z-axis) and top (D_{top}, y-axis) doses. The nMOS SOI-FinFET structures were simulated with Sentaurus simulator.

Angles of 0º, 10º, 45º, and 90º were used. The 0º I/I is by far the easier practical method but it results in high non-uniformity doping in the lateral fin wall. To achieve a better doping uniformity, higher I/I angles have to be considered. The 45º I/I results in the same ion beam incidence on top and lateral fin wall, with the top receiving a double dose after the two-pass tilted implant. There is a limitation for the tilt angle (Colinge, 2007) due to the shadow effect and cause by the fin height H_{fin} and pitch P_{fin} (see Figure 4.6 in Chapter 4) that can be express by the equation (5.6).

$$\alpha_I \leq tan^{-1}\left(\frac{P_{fin} - T_{fin}}{H_{fin}}\right) \tag{5.6}$$

Then, beyond a maximum angle, one fin blocks the implant from reaching the others. The 90º I/I is used as an ideal reference although it is not achievable in practice.

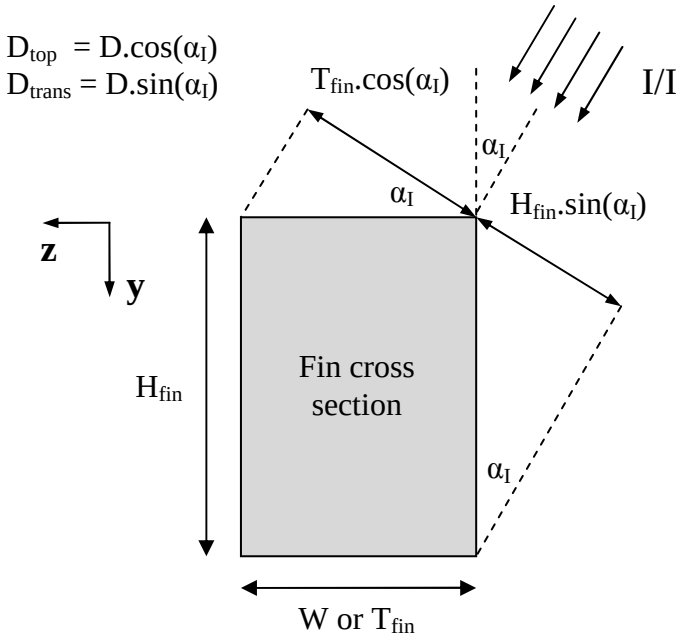


Figure 5.81: Silicon fin cross-section and how the ion implant (I/I) angle α_I affects the doses, transversal (D_{trans}, z-axis) and top (D_{top}, y-axis).

The program TRIM (the Transport of Ions in Matter) part of the SRIM (The Stopping and Range of Ions in Matter) software (SRIM, 2008) was used to calculate the projected range R_p and the "straggle" ΔR_p of the ions distribution in the top y-axis (top of the fin) and z-axis (transversal or sidewalls of the fin). It is a Monte-Carlo calculation leading to a 3D distribution of the ions in the target material, where an angle of incidence can be considered. The ΔR_p is related to the characteristic length by $\lambda = \sqrt{2}\,\Delta R_p$.

The S/D fin extensions were doped with Gaussian profiles along z-axis (transversal) and y-axis (top) and the lateral profile along x-axis was considered an Erfc function. The process parameters used to define these impurity profiles in the simulated FinFET structures are shown in Table 5.5, where λ_{lat} is the characteristic length of the lateral profile (x-axis).

TRIM simulations provided R_p and ΔR_p for each I/I angle. The energy of 10 keV for the I/I was used in TRIM simulations. The same total dose (D) on each side of the fin was considered for all I/I angles. This total dose was calculated choosing a (z-axis) peak concentration of $1x10^{20}$ cm^{-3} in the 45º I/I method as a reference.

Then the corresponding transversal (D_{trans}, z-axis) and top (D_{top}, y-axis) doses were obtained using the effective area related to the ion implantation angle α_I. This relation is depicted in Figure 5.81. Partial impurities activation after the thermal annealing is not taken into account.

Table 5.5: Process parameters used to define the impurity profiles in the simulated FinFET structures. The ion energy (Arsenic) of 10 keV was used in TRIM simulations.

α_I of I/I (deg)	**Dose - each fin side ($\#/cm^2$)**	**Axis Dose ($\#/cm^2$)**	**Axis**	**N_o ($\#/cm^3$)**	**R_p (nm)**	**ΔR_p (nm)**	**$\lambda=\sqrt{2}\,\Delta R_p$ (nm)**	**λ_{lat} (nm)**
45	$1.4x10^{14}$	$1x10^{14}$	z-axis	$1x10^{20}$	9	3.96	5.6	5.4
		$2x10^{14}$	y-axis	$2x10^{20}$	9	3.96	5.6	5.4
45	$1.4x10^{14}$	$1x10^{14}$	z-axis	$1x10^{20}$	0	3.96	5.6	5.4
		$2x10^{14}$	y-axis	$2x10^{20}$	0	3.96	5.6	5.4
10	$1.4x10^{14}$	$2.4x10^{13}$	z-axis	$3.6x10^{19}$	4	2.69	3.8	5.0
		$2.7x10^{14}$	y-axis	$2.5x10^{20}$	12.7	4.45	6.3	5.4
90	$1.4x10^{14}$	$1.4x10^{14}$	z-axis	$1.2x10^{20}$	13	4.74	6.7	5.5
0		$2.8x10^{14}$	y-axis	$2.4x10^{20}$	13	4.74	6.7	5.5

5.7.2 Simulation Results

The different I/I angles result in different doping profiles in the S/D extensions what affect the S/D parasitic resistance R_{SDE} and also affect the characteristic length of the lateral profile where λ_{lat} (x-axis). The threshold voltage V_T, on the other hand, depends strongly of the gate stack configuration and silicon fin thickness (T_{fin} = 20 nm), that are the same for the simulated FinFET devices.

Figure 5.82 and Figure 5.83 show simulated I_D-V_G characteristics for a long-channel FinFET (L_G = 1 µm) and for a short-channel FinFET (L_G = 50 nm), respectively, both for five different I/I angles of S/D extension.

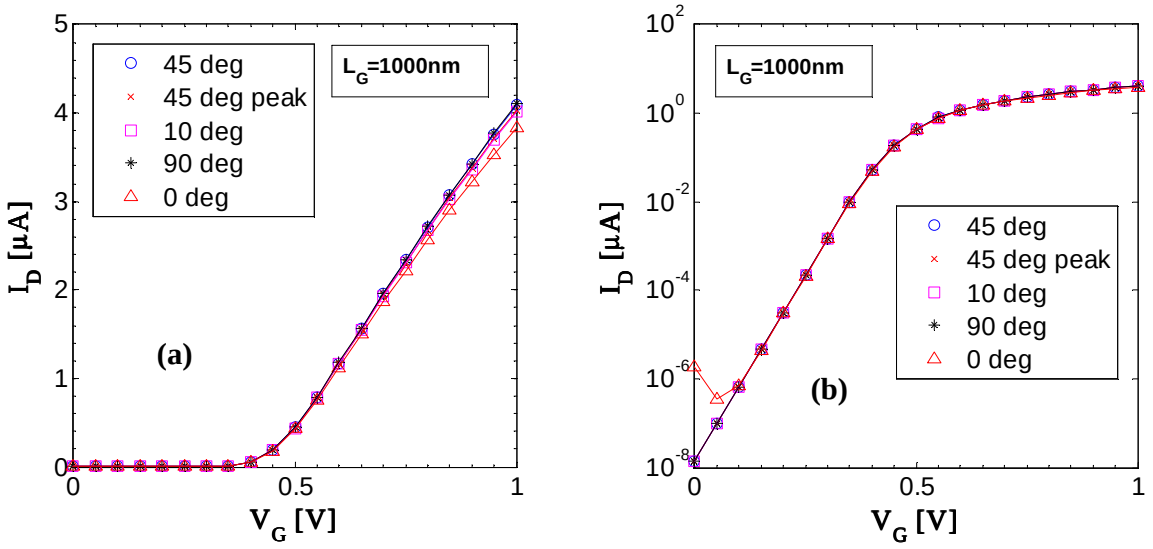


Figure 5.82: I_D-V_G characteristics (V_D = 100 mV) for a long-channel FinFET (L_G = 1 µm) and for five different I/I angles of S/D extension. (a) linear scale (b) log. scale. (T_{fin} = 20 nm)

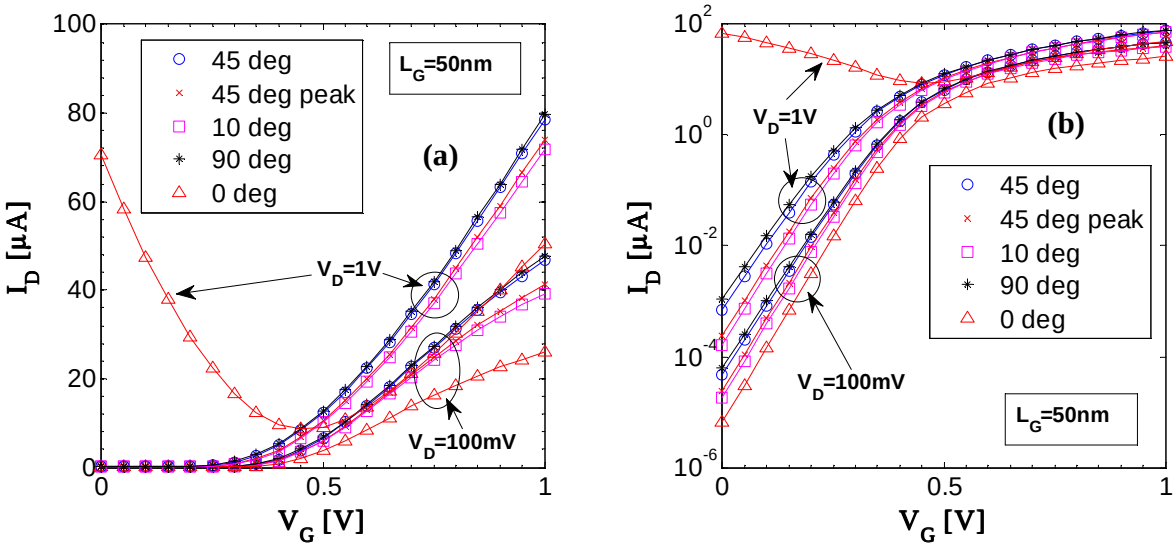


Figure 5.83: I_D-V_G characteristics for a short-channel FinFET (L_G = 50 nm) and for five different I/I angles of S/D extension. (a) linear scale (b) log. scale. (T_{fin} = 20 nm)

Figure 5.84 and Figure 5.85 show, respectively, the extracted g_m vs. V_G and g_m/I_D vs. V_G, from I_D-V_G characteristics of Figure 5.82 and Figure 5.83, both for five different I/I angles of S/D extension.

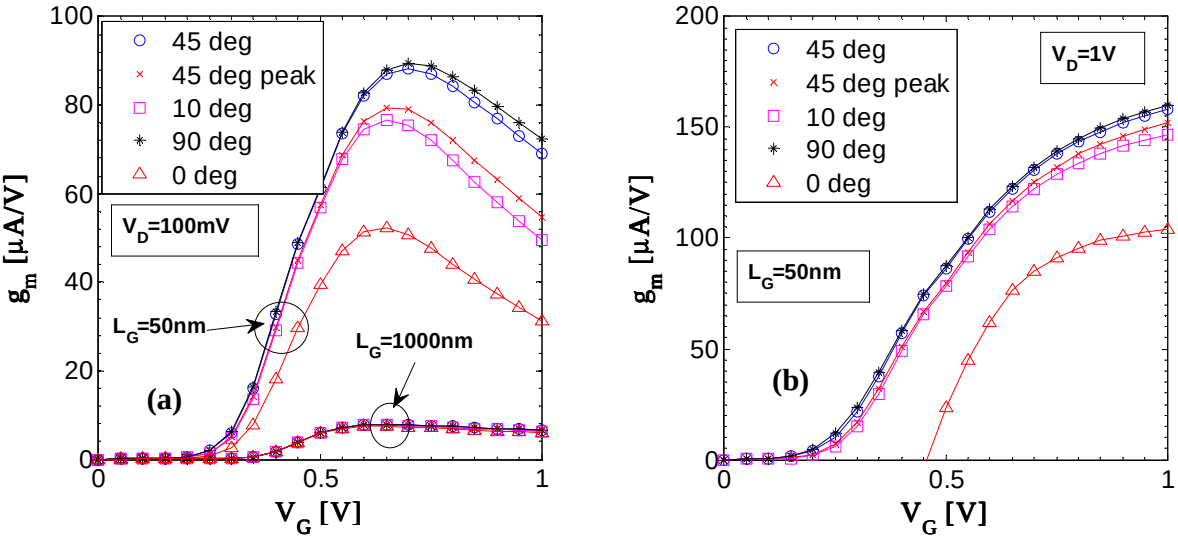


Figure 5.84: g_m versus V_G for two FinFET devices with different gate lengths (L_G=50nm and 1µm) and for five different I/I angles of S/D extension. (a) V_D = 100 mV (b) V_D = 1V. (T_{fin} = 20 nm)

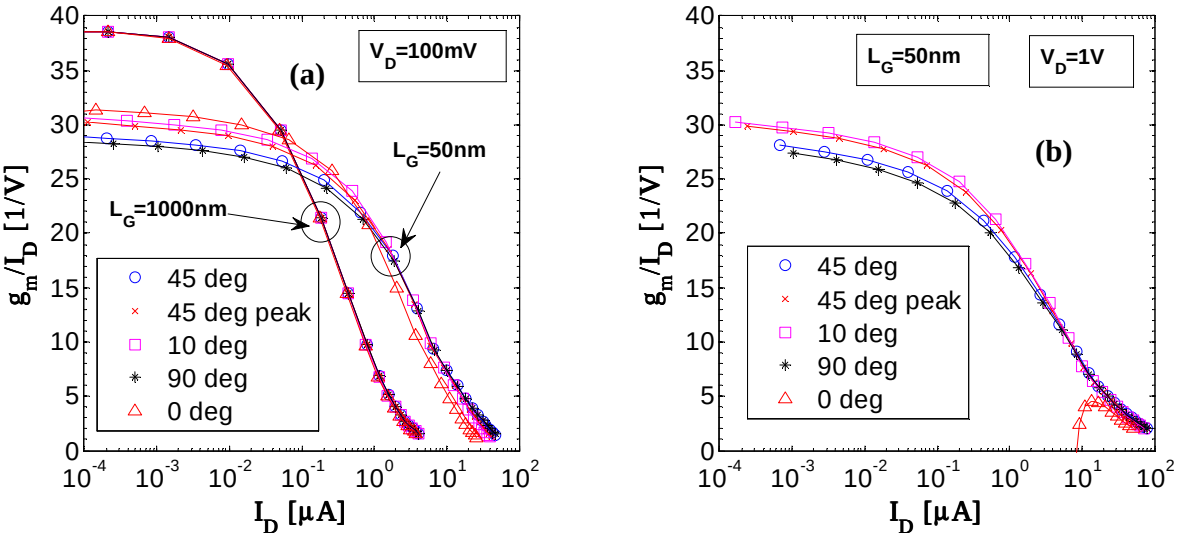


Figure 5.85: g_m/I_D versus I_D for two FinFET devices with different gate lengths (L_G=50nm and 1µm) and for five different I/I angles of S/D extension. (a) V_D = 100 mV (b) V_D = 1V. (T_{fin} = 20 nm)

Figure 5.86 shows the S/D total resistance $R_{SD} = V_D/I_D$ versus V_G for a long-channel FinFET (L_G = 1 µm) and for a short-channel FinFET (L_G = 50 nm) and for five different I/I angles of S/D extension. The extrapolation of R_{SD} for high values of V_G tends ideally to the parasitic resistance R_{SDE}. Although simple, this extrapolation method is not very accurate for extraction of R_{SDE}.

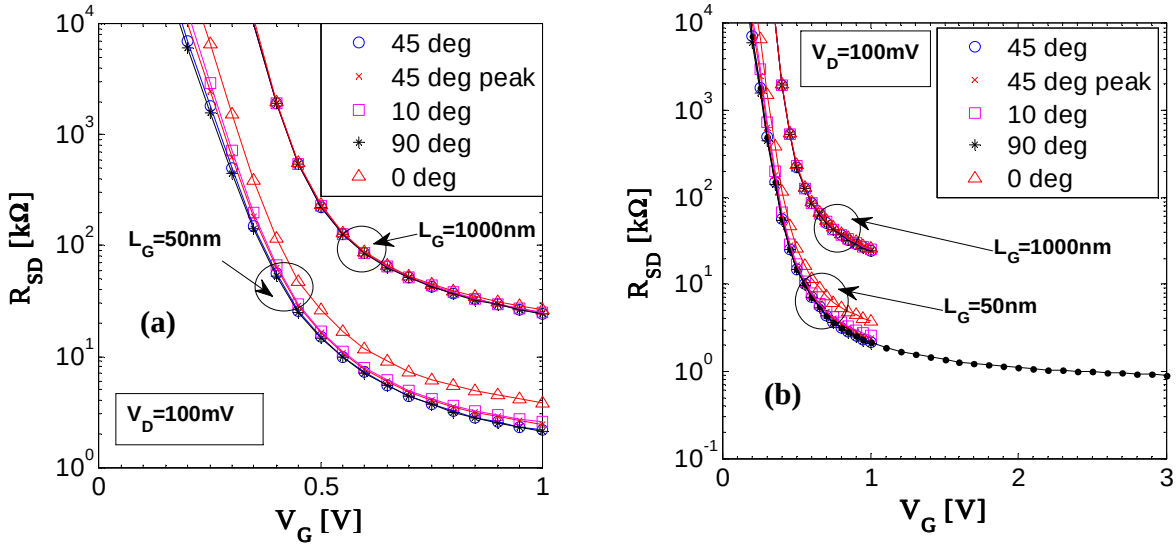


Figure 5.86: S/D total Resistance $R_{SD} = V_D/I_D$ versus V_G for two FinFET devices with different gate lengths (L_G=50nm and 1µm) and for five different I/I angles of S/D extension. (a) V_G from 0 to 1 V; (b) V_G from 0 to 3 V; V_D = 100 mV. (T_{fin} = 20 nm)

The simulated I_D-V_G characteristics in linear region of operation (V_D = 100 mV) of Figure 5.82 and Figure 5.83 were used for the extraction of the parasitic resistance R_{SDE} of the S/D extension region. Figure 5.87 shows these data from pairs of FinFET devices (a short and a long-channel SOI-FinFET) plotted as in expression (5.5), in Section 5.5.

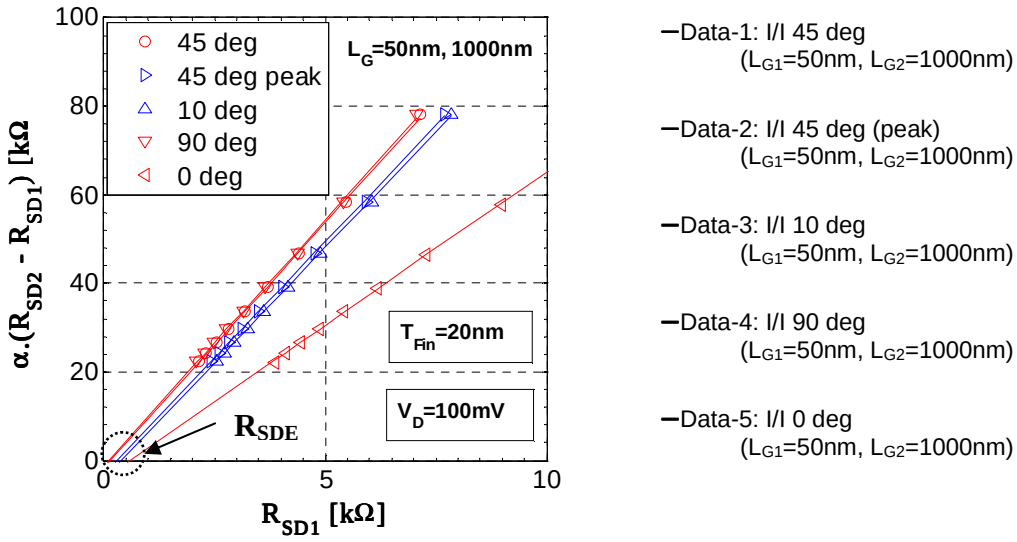


Figure 5.87: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from simulated I_D-V_G data (linear region, V_D = 100 mV, in strong inversion) of pairs of FinFET devices with different gate lengths (L_{G1} and L_{G2}, $L_{G1} < L_{G2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}.

The data were selected to be in strong inversion but with a gate voltage overdrive of only a few hundreds of milivolts to avoid that expression (5.5) lose its validity. The parameter "α" is a correction introduced to account for a difference in the threshold

voltages. However, the modulation of the effective channel length by the gate voltage is not taken into account on the analysis.

The S/D parasitic resistance R_{SDE} is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The values of the extracted S/D parasitic resistances R_{SDE} ranged from 110 to 592 Ω, as seen in Table 5.6. This is actually impacted by the implantation angle α_I and the consequent differences in the characteristic length.

Threshold voltages V_T, subthreshold slopes S, DIBL, S/D total resistances R_{SD}, and S/D parasitic resistances R_{SDE} were extracted and are summarized in the Table 5.6. The V_T voltages were extracted with the method "SD". As expected, the extracted values of V_T are not affected by the different I/I angles.

Table 5.6: Threshold voltages V_T (method "SD"), subthreshold slopes S, DIBL, S/D total resistances R_{SD}, and extracted S/D parasitic resistances R_{SDE} from simulated I_D-V_G data.

α_I of I/I (deg)	**V_T (V)** (V_D=100mV) L_G=50nm L_G=1µm		**S (mV/dec)** (V_D=100mV) L_G=50nm L_G=1µm		**DIBL (mV/V)** (V_D=100mV and 1V) L_G=50nm	**R_{SD} (kΩ)** (V_D=100mV, V_G=1V) L_G=50nm L_G=1µm		**R_{SDE} (Ω)**
45	0.400	0.450	81	60	99.4	2.14	24.4	137
45 (peak)	0.400	0.450	77	60	97.8	2.43	24.8	290
10	0.400	0.450	76	60	89.0	2.55	24.9	395
90	0.400	0.450	82	60	98.9	2.09	24.3	110
0	0.400	0.450	74	60	-----	3.85	26.1	592

The simulated I_D-V_G characteristics for a long-channel FinFET (L_G = 1 µm), shown in Figure 5.82, are very similar for the different I/I angles since differences in doping profiles in the S/D extensions are not relevant at that range of channel length. For short-channel FinFET devices (L_G = 50 nm), shown in Figure 5.83, however, there are noticeable changes.

The practical 45º I/I method and the ideal 90º I/I method show similar results (I_D-V_G, g_m, and g_m/I_D), with almost de same S and DIBL, with higher (24%) R_{SDE} in the 45º I/I case. The 45º I/I (peak) method, with the doping peak at the interface of silicon fin, shows a better S and g_m/I_D but an even higher R_{SDE}.

The 10º I/I method, with more asymmetry in the doping of silicon fin top and sidewalls, shows also a better S, g_m/I_D, and DIBL but a much higher (≈3x) R_{SDE}. The shorter characteristic length of the lateral profile λ_{lat} (x-axis) and better subthreshold regime of this I/I method end up to a higher R_{SDE}. The 0º I/I, the easier practical method but with very high non-uniformity doping in the lateral fin wall, shows poor I_D-V_G characteristics for short-channel FinFET (L_G = 50 nm) devices and presents a completely degraded behavior in the subthreshold regime for a high drain voltage (V_D = 1 V).

5.8 Conclusions

The variations of V_T, S and DIBL with respect to L_G were presented for different silicon fin thicknesses and two silicon fin doping concentrations. The V_T roll-off is present below gate lengths of 100 nm, what further indicates that the significant drop in V_T below 50 nm gate length calls for a thinner gate oxide and a narrower fin, in the range of 10 to 15 nm. On both doping concentrations, the reduction of T_{fin} of 20 nm to 15 nm reduces the V_T roll-off and improves the subthreshold slope.

The results indicate that, for FinFET technologies below 22 nm, the undoped silicon fin is the most practical, since the actual threshold voltage will depend mostly on the gate work-function and silicon fin width only. Random-doping problems and corner-effects can also be neglected in undoped FinFETs.

The degradation of device characteristics for gate lengths below 50 nm and T_{fin} of 20 nm is clearly noted, and the device with L_G of 20 nm and T_{fin} of 20 nm shows very weak characteristics that need considerable improvement. The device simulations showed that the degradation of device characteristics for gate lengths below 50 nm is alleviated in subthreshold regime by the combined effect of T_{fin} reduction from 20 to 10 nm and t_{ox} reduction below 2 nm. Further reduction of gate oxide below 2 nm causes significant tunneling through the gate oxide. Hence, for this device to work below L_G of 20 nm it is mandatory to use effectively high-k dielectric gate material to minimize the gate tunneling current and to provide also good control of the fin conductance by the metal gate. Simulation results for V_T roll-off, S, and DIBL behavior, indicate that the ratio L_G/T_{fin} (or normalized gate length) has to be larger than approximately 1.5 to 2.

The top-gate of the tri-gate structure contributes only with approximated 5% for the final current due to the aspect ratio H_{fin}/T_{fin} of 3 of the FinFET structures. The reduction of 33% (from 150 nm to 100 nm) in T_{Box} has produced negligible effect in the drain. current.

The optimization of the implantation angle and dose of the S/D regions is a key factor in the I-V characteristics of the FinFET devices, controlling many important parameters such as parasitic S/D resistances, subthreshold slope, and DIBL. Also, to minimize the parasitic S/D resistances, the industry and advanced labs developed process steps to enlarge the fin (through epitaxial regrowth of Si-Ge alloys, for instance) in the S/D regions that connect the active device with the silicon pad that connects the parallel fins of the same electrically effective device. In this work it is only considered the silicon resistance, and no consideration was given to the beneficial effects of a Si-Ge regrown S/D regions.

6 SOI-FINFET MEASUREMENTS

This chapter presents, compares, and discusses experimental characteristics of fabricated FinFETs with fin widths in the range of 5 to 20 nm. These devices were manufactured at IMEC - Interuniversity Microelectronics Center in Belgium, and were measured on wafer by microprobes. This chapter is organized as follows: first, the description of the FinFET process runs; second, the measurements procedures are explained; and third, the data analysis and the comparison with simulation results.

6.1 FinFET Process Runs

The process runs will be described briefly. Two runs with differences in the process steps were used for the experimental characterization. These runs were classified as:

a) Reference Process

b) Highly Doped Process

The basic process or "Reference Process" starts from SOI wafers with 145 nm of buried oxide thickness (T_{Box}) and a 88 nm silicon film on top. The silicon film is decreased to 65 nm (H_{fin}) after the fin etch. The gate stack is formed by atomic layer deposition (ALD) deposition of 2.5 nm SiON resulting in 2.2 nm EOT. A 5 nm thick TiN ALD film is deposited followed by a 100 nm polysilicon layer and a 60 nm silicon oxide layer. After the gate stack is formed the gate is patterning using the silicon oxide as hard mask and a dedicated etch. Tilt lightly-doped S/D implants (LDD) are performed (45º I/I) and the nitride spacers of around 35 nm are formed. Highly-doped drain implats (HDD) and a nickel silicidation for the device electrodes complete de process. In the "Highly Doped Process" there is an additional step of LDD tilt implantation that increases the doping concentration in the S/D extensions.

The mask channel length (L_{Gm}) of the measured transistors, with good controlable I_D current, ranges from 45 to 10000 nm (45, 70, 90, 130, 250 nm, 1 µm, and 10 µm); and the silicon fin thickness (T_{fin}) ranges from 5 to 20 nm (5, 10, 15, and 20 nm).

Figure 6.1 shows the basic geometry features of the measurement test structures. The maximum S/D extension length (L_{SDmax}), which is the spacing between the gate mask and the silicon pad that connects all fins, is 90 nm long, and the fin pitch (P_{fin}), which is the spacing between fins plus fin thickness, is 200 nm long. The number of parallel fins (N_T) are 5. Using the equation (5.6) of section 5.7 and a T_{fin} of 20 nm results in a maximum tilt angle for the S/D implants around 70º. This high tilt angle is not practical and it is a result of an also high P_{fin} of the test structures. A more compact array of fins is possible by decreasing P_{fin}. With a practical tilt implantation angle of 45º a minimum P_{fin} of 85 nm would be possible (H_{fin} = 65 nm).

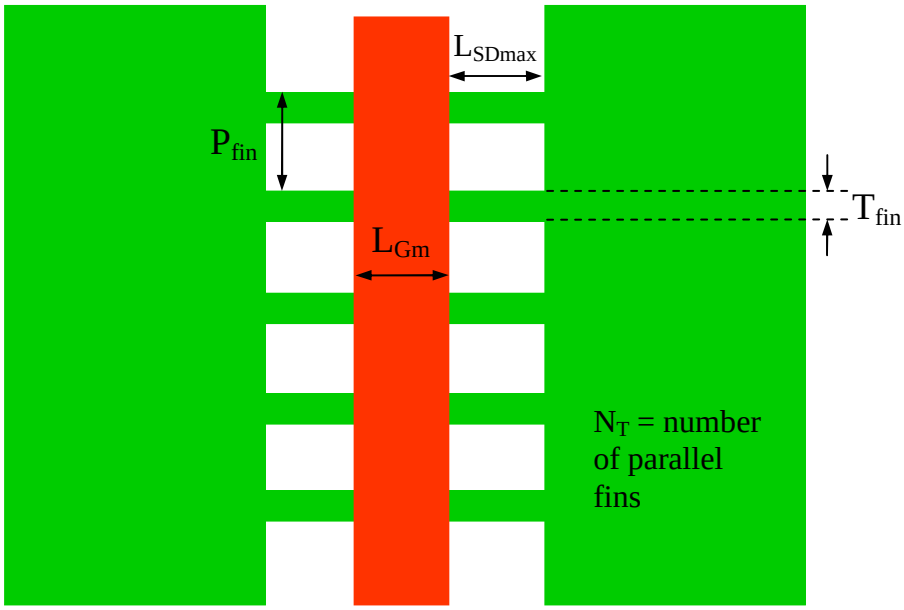


Figure 6.1: FinFET measurement test structure layout with five parallel fins ($N_T = 5$) and critical dimensions indicated: mask channel length L_{Gm}, silicon fin thickness T_{fin}, maximum S/D extension length (L_{SDmax}), and the fin pitch (P_{fin}).

6.2 Measurement Procedures

The I-V measurements presented in this Chapter and Annexes were carried out with the equipment HP4156 – a semiconductor parameter analyzer - and a probe station Suss Wafer Prober PB300, kindly provided by IMEC in Belgium. The measurement equipment is shown in APPENDIX D - Measurement Equipment.

In Figure 6.2 the measurement setup is depicted for the DUT (Device Under Test) with SMUs (Source Measure Units) configuration. Figure 6.2a shows the setup for the FinFET devices with SMU3 and SMU4 active (gate and drain respectively), and SMU1 and SMU2 grounded (source and back-substrate respectively); Figure 6.2b shows the setup for the lead and contact resistance test, in which only SMU1 and SMU4 are used (SMU1 grounded).

Lead and contact resistance can be a problem when interfering with the voltage received by the DUT, especially when its value is in the same order of magnitude of the resistance of the DUT. Remote-sensing (“Kelvin sense”) was used with force/sense connection reaching the last end of the micro-manipulator that holds the microprobe.

Lead and contact resistance measurements were carried out with V_{SMU} ranging from -200 mV to 200 mV in steps of 10 mV, resulting in values around 2 Ω. I_D-V_G measurements were carried out on n-type FinFETs devices with V_G ranging from -0.5 V to 1 V in steps of 10 mV, in the linear region of operation for two values of drain voltage (V_D = 50 mV and V_D = 100 mV), and in the saturated region of operation for V_D = 1V. I_D-V_D measurements were carried out with V_D ranging from zero volt to 1 V, in steps of 10 mV, and V_G ranging from 0 V to 1 V in steps of 125 mV.

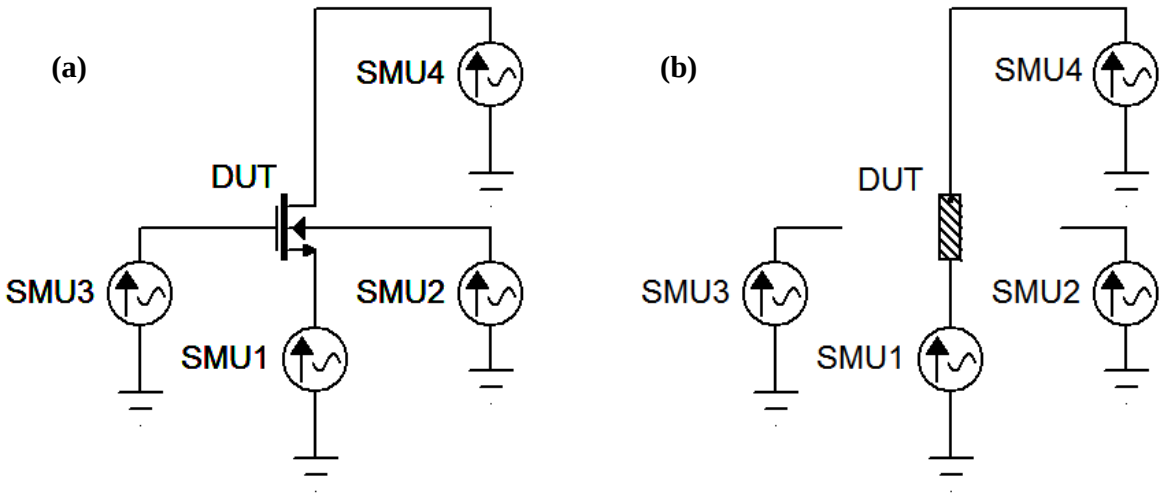


Figure 6.2: Measurement setup for the DUT (Device Under Test) with SMUs (Source Measure Units) configuration. (a) for n-type FinFET; (b) for lead and contact resistance.

6.3 Measurement Results

A set of measurement plots of Threshold Voltage V_T, Subthreshold Slope S, Drain Induced Barrier Lowering (DIBL), transconductance g_m , transconductance over drain current g_m/I_D, Early voltage V_A, and Voltage Gain A_V were produced from the original measurements, and are shown in APPENDIX B - Measurement Plots.

6.3.1 Comparison Between Measured and Simulated Devices

It is important to stress that the simulations of the double-gate n-type SOI-FinFET devices were made before the experimental measurements. What devices could be measured and the exact structural features and process characteristics were not fully known. It was then adopted in the simulations a basic SOI-FinFET structure with the process characteristics of a n-type FinFET.

Chapter 5 describes this basic double-gate n-type SOI-FinFET structure and the variations adopted in the simulations. These variations translate into three structures called “Structure-I”, “Structure-II”, and “Structure-III”.

The buried oxide thickness T_{Box} and the silicon fin height H_{fin} were set in the simulations at 150 nm and 60 nm, respectively. In the measured experimental FinFET devices these values are 145 nm and 65 nm and represent only 3.3 % less in T_{Box} and 8.3 % more in H_{fin}. A simulation comparison of FinFET structures in sub-section 5.6.5 showed that a reduction of 33 % in T_{Box} produced negligible effect in the drain current (I_D). On the other hand, even a small increase (less than 5 %) in the H_{fin} has a direct impact on I_D, although the deviation of the shape of the fin from the rectangular ideal profile could compensate the effect.

In the simulations, the physical gate length L_G ranges from 20 nm (short-channel FinFET) to 1 µm (long-channel FinFET), and the silicon fin thickness T_{fin} or W_{fin} ranges from 10 to 200 nm, which means an aspect ratio H_{fin}/T_{fin} from 0.3 to 6. Considering the simulated structures, T_{fin} ranges from 20 to 200 nm for "Structure-I"; T_{fin} is set at 15 nm and 20 nm for "Structure-II", and T_{fin} is set at 10 nm and 15 nm for "Structure-III".

For the experimental FinFET devices the mask gate length L_{Gm} of the measured transistors ranges from 45 nm to 10 µm and the silicon fin thickness T_{fin} ranges from 5 to 20 nm. There are measurements for FinFET devices with T_{fin} of 5 nm, well beyond the limit where quantum effects can be disregarded. With an aspect ratio H_{fin}/T_{fin} around 12 a great deviation of the shape of the fin from the rectangular ideal profile could be expected. In the simulations these geometries where quantum effects dominate were avoided. On the other hand, FinFET devices with physical gate length L_G of 20 nm were simulated.

The source or drain (S/D) extension length (L_{SD}) is set at 250 nm for "Structure-I" and is set at 25 nm for "Structure-II" and for "Structure-III". This extension of the fin in the simulated FinFET structures corresponds in the experimental FinFET devices to the portion of the fin that receives only the LDD implant, mentioned in the previous section, and is masked by a nitride spacer from the HDD implant. In Figure 6.1 is depicted the S/D extension length L_{SDmax} of the experimental FinFETs (L_{SDmax} of 90 nm). With the nitride spacers thickness formed around 35 nm, the S/D extension length (L_{SD}) is around 35 nm. Then the simulated FinFETs for "Structure-II" and "Structure-III" have smaller extension lengths (L_{SD} of 25 nm), with a reduction around 28 %.

The portion of the fin that receives the HDD implant is not in the simulated structures and a contact electrode (neutral) is used to connect the LDD portion of the fin. In structures "Structure-I" and "Structure-II" the contact electrodes are on the vertical cross-section at the end of the S/D extensions (Figure 5.15); in structure "Structure-III" the contact electrodes are on both sidewalls and top of the last portion of the S/D extensions (Figure 5.30).

For the experimental FinFETs the gate stack is formed by ALD of 2.5 nm SiON resulting in 2.2 nm EOT, both on top and sidewalls of silicon fin, and setting up a tri-gate FinFET structure. The simulated FinFETs have lateral-gate oxide thickness (t_{ox}) of 2 nm and the top-gate oxide thickness (t_{ox_top}) of 20 nm. A simulation comparison of FinFET structures in sub-section 5.6.3 showed that the top-gate of the simulated tri-gate structure contributes only with approximated 5% for the final current due to the high aspect ratio H_{fin}/T_{fin} of 3.

The gate electrode work-function is set to mid-gap. With T_{fin} in the order of tens of nanometers the total depletion charge Q_D contribution to V_T becomes small compared to the contribution of the gate electrode to silicon work-function difference ϕ_{ms} and tends to be negligible. Then V_T becomes strongly dependent of the gate electrode work-function.

A FinFET structure with a higher gate oxide dielectric constant ($e_{ox} = 7.2$ instead $e_{ox} = 3.9$) was simulated, similar to high-K materials, keeping $t_{ox} = 2$ nm and avoiding a thinner gate oxide and higher parasitic tunneling oxide currents, with an effective oxide thickness (EOT) of 1.1 nm.

6.3.2 I_D-V_G Characteristics

The following figures show a comparison between 3-D simulated and measured I_D-V_{GT} characteristics of FinFET devices. A minimal set of structural parameters for the experimental devices were provided by the IMEC Labs, and the differences between the simulated "Structure-III" and the actual device parameters are not herein detailed any further, due to intellectual property issues that pertain to IMEC.

Figure 6.3 and Figure 6.4 show I_D-V_{GT} characteristics for long-channel experimental FinFET devices (L_{Gm} = 1 µm) of the "Reference Process" and for long-channel simulated FinFET devices (L_G = 1 µm). Figure 6.3 for devices with T_{fin} of 20 nm and Figure 6.4 for devices with T_{fin} of 10 nm. The x-axis is gate voltage overdrive, since the simulated and measured devices had different metal work-functions, which caused differences in V_T at zero source bias.

Considering the same T_{fin}, there are not considerable differences between the I_D-V_{GT} characteristics of the long-channel devices of the "Reference Process" and the "Highly doped Process", while the last one is not presented in the figures.

In Figure 6.4 it is clear that there is a shift (around 50 mV) on the current in the subthreshold regime, a mismatch between the simulated I-V and the actual finFET measurements for a very narrow fin of 10 nm. The transconductance in the strong-inversion regime differs very much from the simulated device. These differences can be attributed to structural fabrication variations (fin cross-section) and also to quantum-confinement effects that are not modeled by this commercial 3-D device simulator. A numeric variation on V_T extracted by second-derivative method (method "SD") can also cause this shift on the current in the subthreshold regime.

Figure 6.5 and Figure 6.6 show I_D-V_{GT} characteristics for experimental FinFET devices (L_{Gm} = 90 nm, 70 nm, 45 nm) of the "Reference Process" and "Highly doped Process" and for simulated FinFET devices (L_G = 100 nm, 70 nm, 50 nm, 20 nm). These two figures are for devices with T_{fin} of 20 nm.

Figure 6.7 and Figure 6.8 show I_D-V_{GT} characteristics for experimental FinFET devices (L_{Gm} = 90 nm, 70 nm, 45 nm) of the "Reference Process" and "Highly doped Process" and for simulated FinFET devices (L_G = 100 nm, 70 nm, 50 nm, 20 nm). These two figures are for devices with T_{fin} of 10 nm.

In Figure 6.5, for the "reference process", the simulated FinFET with L_G of 50 nm and 45º I/I method has a subthreshold regime close to the experimental FinFET with L_{Gm} of 45 nm. In the strong inversion regime the experimental FinFETs have a higher drain current, exception made to the simulated FinFET with 45º I/I method, which has different S/D extensions doping.

In Figure 6.6, for the "highly doped process", the simulated FinFET with L_G of 50 nm and 45º I/I method is better compared to the experimental FinFET with L_{Gm} of 70 nm. This reflects the additional step of LDD tilt implantation that increases the doping concentration in the S/D extensions and reduces the effective channel length of the experimental FinFETs of the "highly doped process".

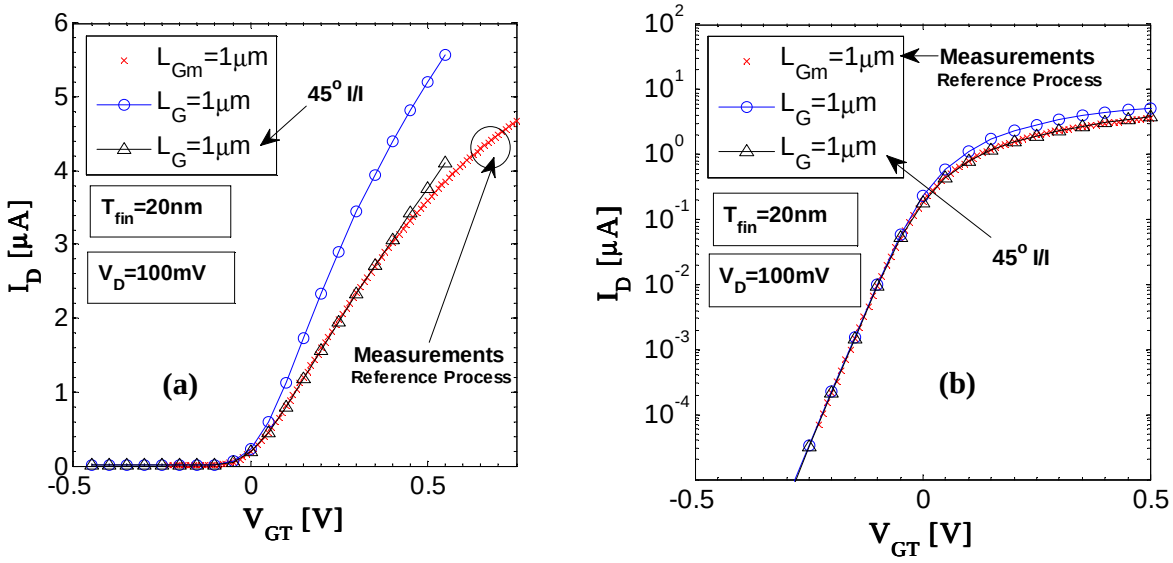


Figure 6.3: I_D-V_{GT} characteristics (V_D = 100 mV) for an experimental long-channel FinFET device (L_{Gm} = 1 μm) of the "Reference Process" and for simulated FinFET devices (L_G = 1 μm). (a) linear scale (b) log scale. (T_{fin} = 20 nm).

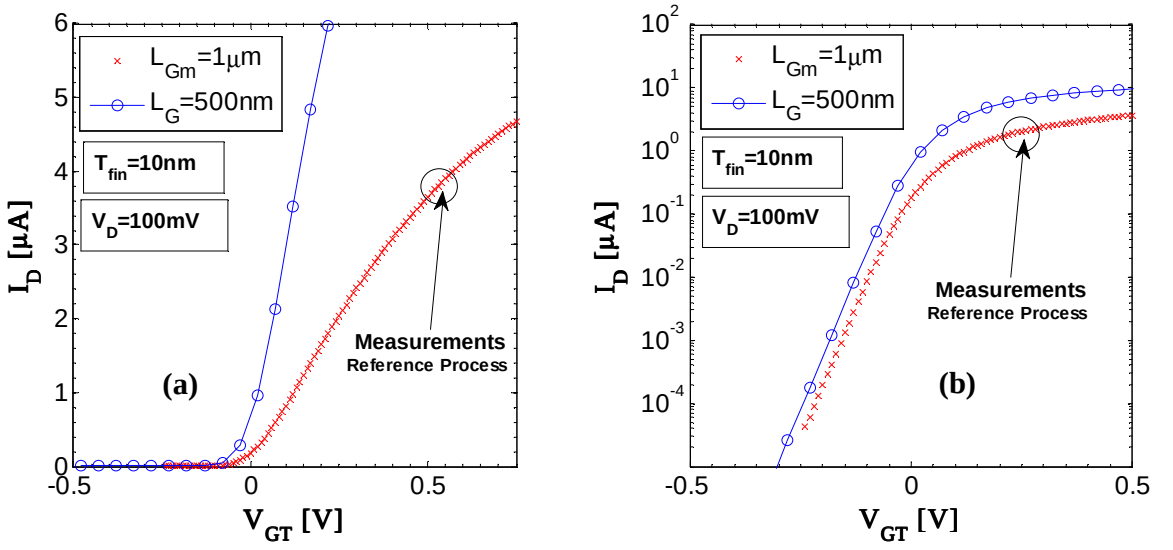


Figure 6.4: I_D-V_{GT} characteristics (V_D = 100 mV) for an experimental long-channel FinFET device (L_{Gm} = 1 μm) of the "Reference Process" and for simulated FinFET devices (L_G = 500 nm). (a) linear scale (b) log. scale. (T_{fin} = 10 nm).

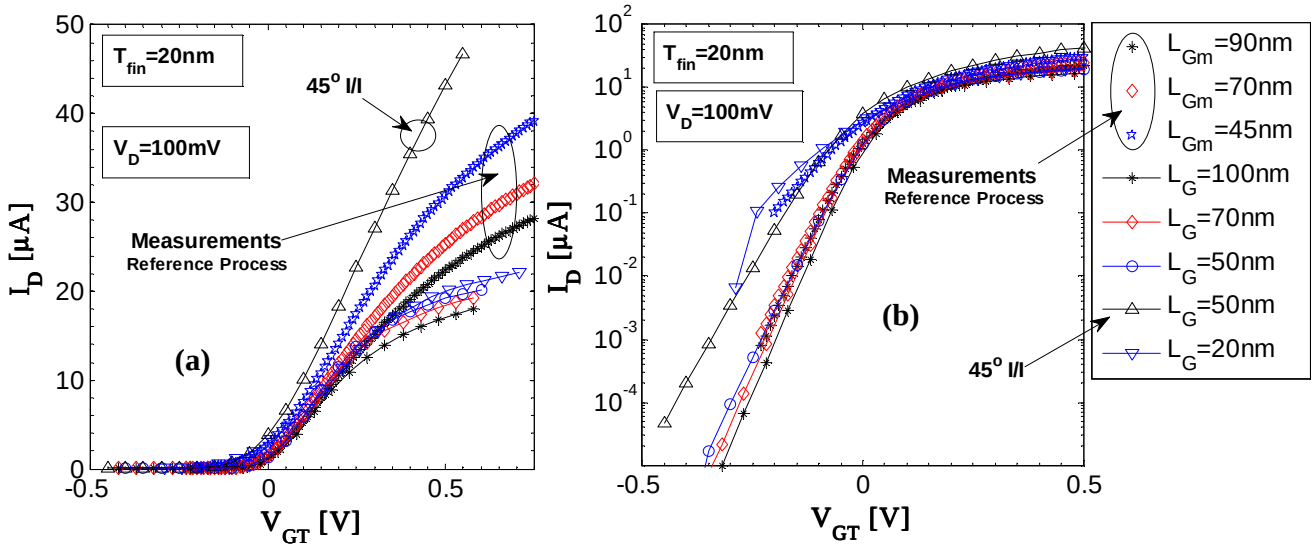


Figure 6.5: I_D-V_{GT} characteristics (V_D = 100 mV) for experimental FinFET devices (L_{Gm} = 90 nm, 70 nm, 45 nm) of the "Reference Process" and for simulated FinFET devices (L_G = 100 nm, 70 nm, 50 nm, 20 nm). (a) linear scale (b) log. scale. (T_{fin} = 20 nm).

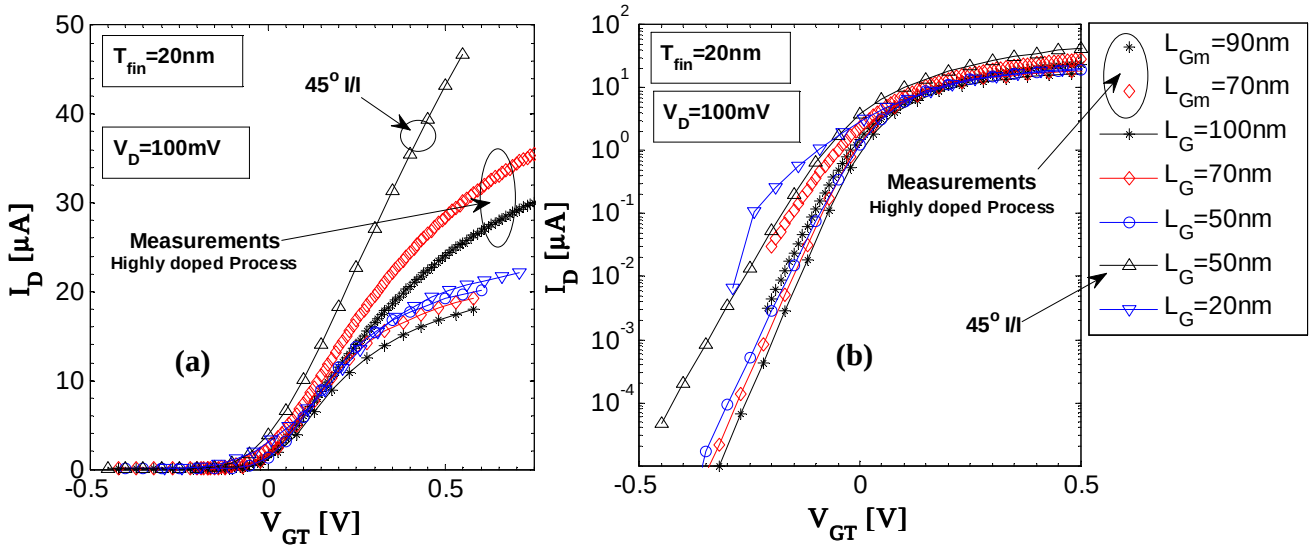


Figure 6.6: I_D-V_{GT} characteristics (V_D = 100 mV) for experimental FinFET devices (L_{Gm} = 90 nm, 70 nm) of the "Highly doped Process" and for simulated FinFET devices (L_G = 100 nm, 70 nm, 50 nm, 20 nm). (a) linear scale (b) log. scale. (T_{fin} = 20 nm).

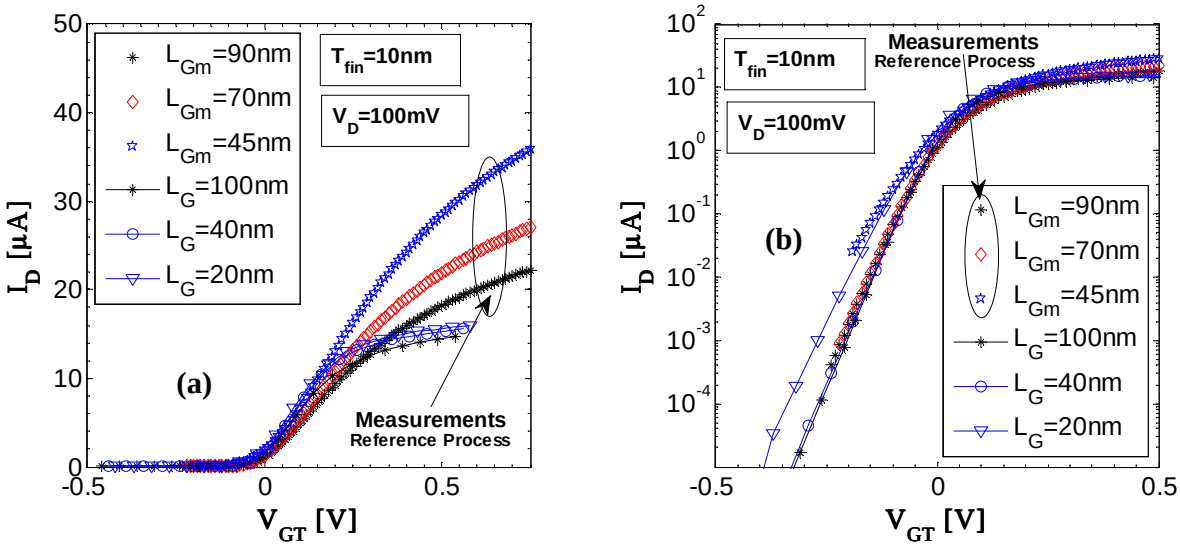


Figure 6.7: I_D-V_{GT} characteristics (V_D = 100 mV) for experimental FinFET devices (L_{Gm} = 90 nm, 70 nm, 45 nm) of the "Reference Process" and for simulated FinFET devices (L_G = 100 nm, 40 nm, 20 nm). (a) linear scale (b) log. scale. (T_{fin} = 10 nm).

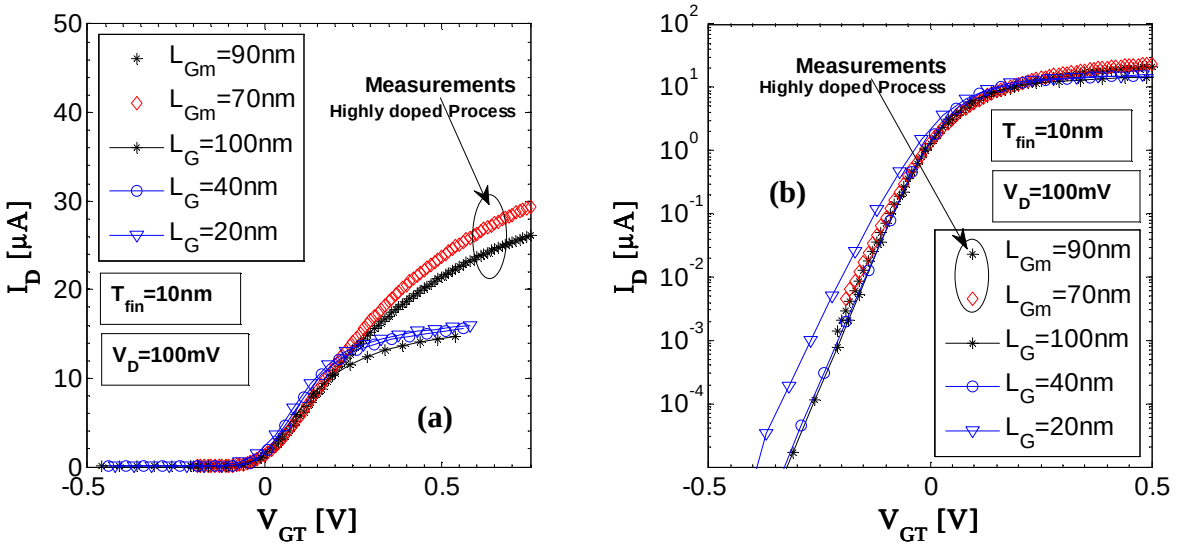


Figure 6.8: I_D-V_{GT} characteristics (V_D = 100 mV) for experimental FinFET devices (L_{Gm} = 90 nm, 70 nm) of the "Highly doped Process" and for simulated FinFET devices (L_G = 100 nm, 40 nm, 20 nm). (a) linear scale (b) log. scale. (T_{fin} = 10 nm)

6.3.3 Threshold Voltage, Subthreshold Slope and DIBL

Figure 6.9 and Figure 6.10 show the threshold voltage versus mask gate length (V_T vs. L_{Gm}) for different values of T_{fin} and compare simulated and measured FinFET devices. The simulated and measured devices had different metal work-functions, which caused differences in V_T around 200 mV.

In the simulations for T_{fin} of 20 nm and 15 nm the V_T roll-off begins deteriorate below L_{Gm} of 30 nm. One can note a better V_T roll-off for T_{fin} of 10 nm present now until L_{Gm} of 20 nm. Since quantum-effects simulation is not a main goal of this work, simulations for T_{fin} of 5 nm were not performed. However, measurements and the parameters extraction for T_{fin} of 5 nm were performed and included in the following figures and tables. Quantum-effects and roughness and shape effects from the fin etching process could have greatly affected the results.

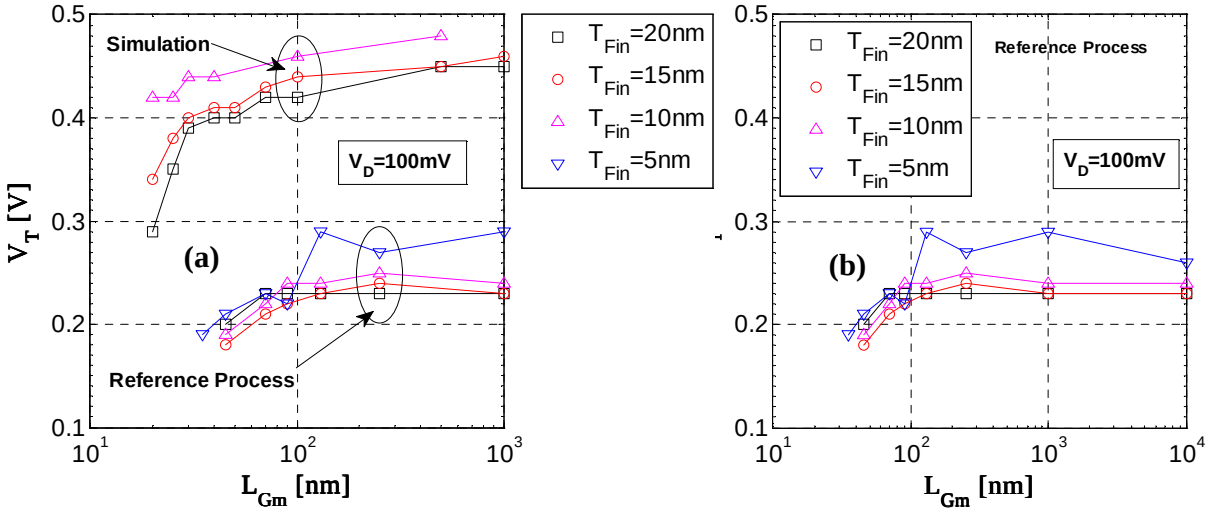


Figure 6.9: Threshold voltage (method "SD") versus mask gate length (V_T vs. L_{Gm}) for different values of T_{fin}. (a) Simulation and measurements (b) Measurements. The samples were measured in the wafer of the reference process (V_D = 100 mV).

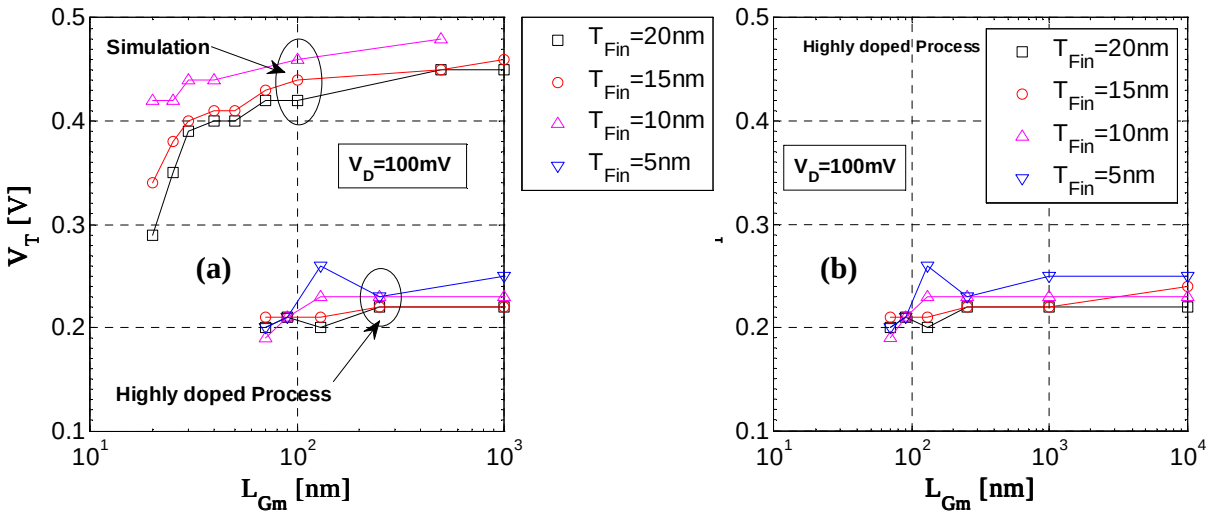


Figure 6.10: Threshold voltage (method "SD") versus mask gate length (V_T vs. L_{Gm}) for different values of T_{fin}. (a) Simulation and measurements (b) Measurements. The samples were measured in the wafer of the highly doped process (V_D = 100 mV).

Figure 6.11 and Figure 6.12 show subthreshold slope versus mask gate length (S vs. L_{Gm}) for different values of T_{fin} and compare simulated and measured FinFET devices.

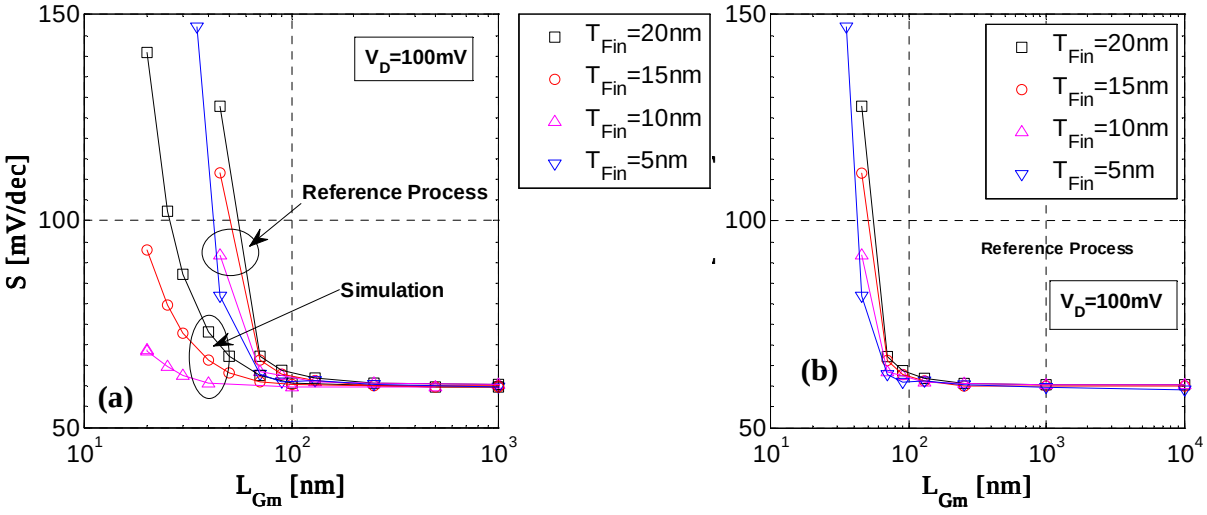


Figure 6.11: Subthreshold slope versus mask gate length (S vs. L_{Gm}) for different values of T_{fin}. (a) Simulation and measurements (b) Measurements. The samples were measured in the wafer of the reference process (V_D = 100 mV).

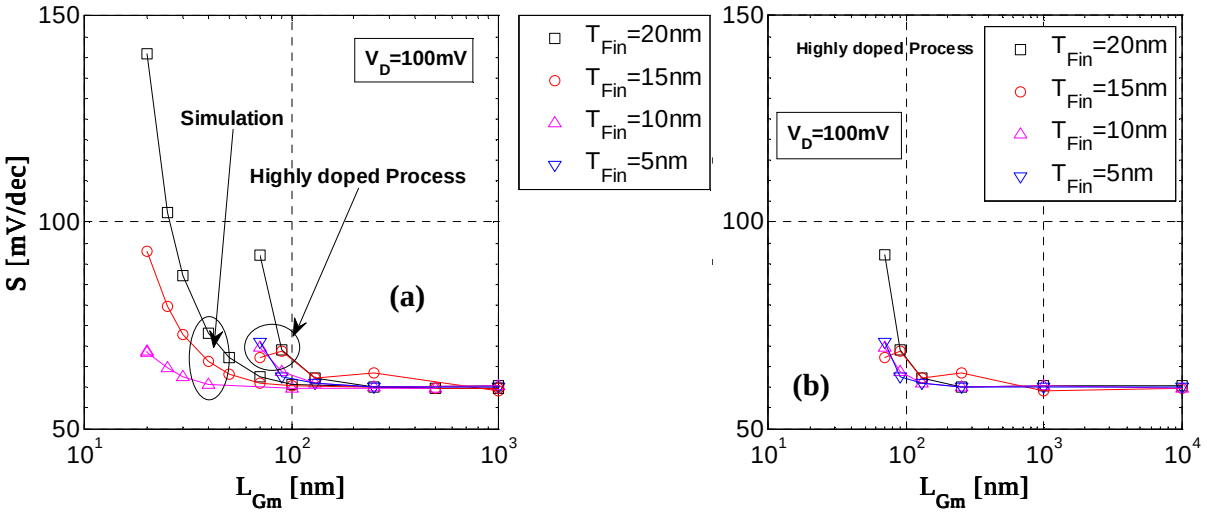


Figure 6.12: Subthreshold slope versus mask gate length (S vs. L_{Gm}) for different values of T_{fin}. (a) Simulation and measurements (b) Measurements. The samples were measured in the wafer of the highly doped process (V_D = 100 mV).

Figure 6.13 and Figure 6.14 show DIBL versus mask gate length (DIBL vs. L_{Gm}) for different values of T_{fin} and compare simulated and measured FinFET devices.

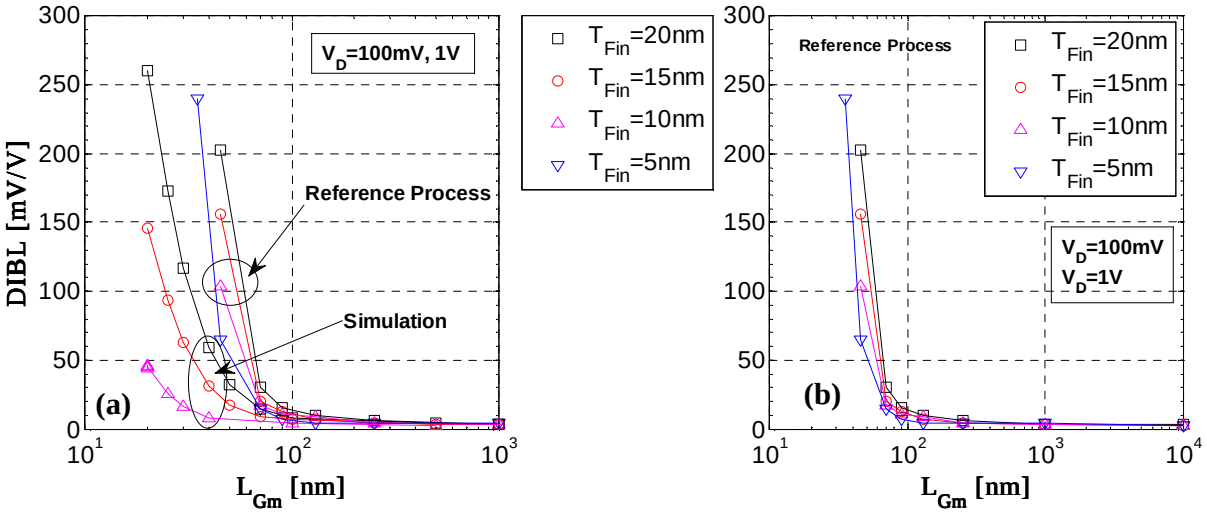


Figure 6.13: DIBL versus mask gate length (DIBL vs. L_{Gm}) for different values of T_{fin}. (a) Simulation and measurements (b) Measurements. The samples were measured in the wafer of the reference process (V_D = 100 mV and 1V).

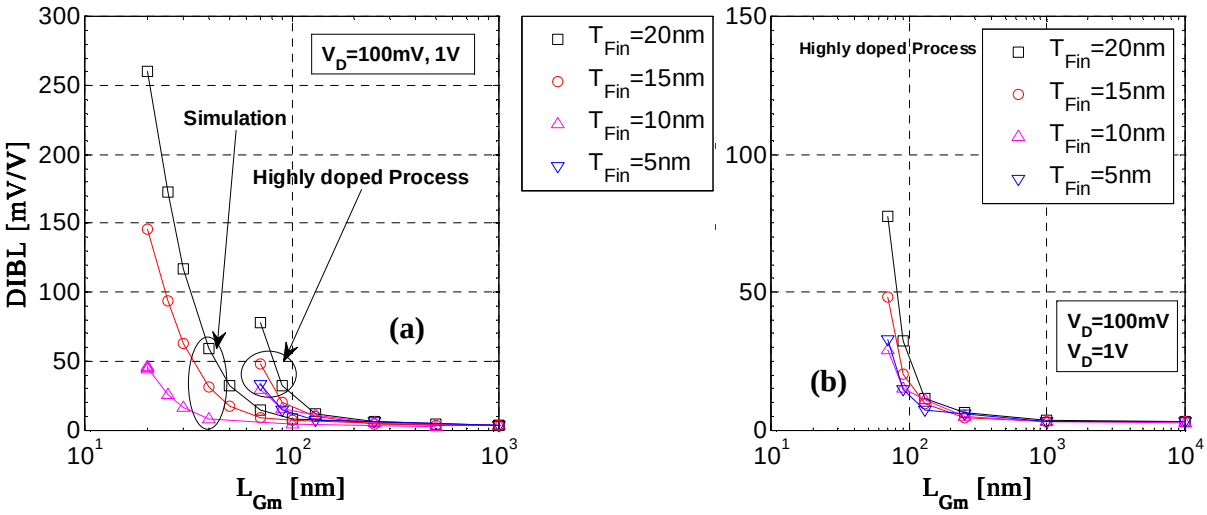


Figure 6.14: DIBL versus mask gate length (DIBL vs. L_{Gm}) for different values of T_{fin}. (a) Simulation and measurements (b) Measurements. The samples were measured in the wafer of the highly doped process (V_D = 100 mV and 1V).

6.3.4 Parameter Extraction

Effective channel length $L_{Geff} = L_{Gm} - \Delta L$, effective channel length shortening ΔL, and S/D parasitic resistance R_{SDE}, are important parameters that play a significant role in MOSFETs characterization. These parameters are physically connected to each other and normally they are extracted together. In Section 5.5 the gate length L_G was used in the definition of L_{Geff} instead of the mask gate length L_{Gm}.

Many methods of extraction of ΔL and R_{SDE} have been proposed (Terada, 1979; Suciu, 1980; de la Moneda, 1982; Whitfield, 1985). The LDD regions in MOSFET

devices are modulated by the gate voltage. These regions underlap the spacers and part of the gate and are connected to the channel which is controlled by the gate. Some methods of extraction of ΔL and R_{SDE} have addressed those dependencies (Takeuchi, 1996; Torres-Torres, 2002) trying to separate channel and S/D extensions.

In this work two methods, the Whitfield method and the Suciu method were used to extract the effective channel length shortening ΔL, and the S/D parasitic resistance R_{SDE}, in conjunction with velocity saturation parameter theta θ, and low-field mobility μ_o.

The Whitfield method was explained briefly in Section 5.5. It uses pairs of transistors of the same channel width but different channel lengths and I-V characteristics in linear region and strong inversion of transistor operation. The effective channel length shortening ΔL and the S/D parasitic resistance R_{SDE} were extracted for each pair from plots of S/D total resistances $R_{SD} = V_D/I_D$. The parameter "α" was introduced in the method as a correction to account for a difference in the threshold voltages between devices and it was not in (Whitfield, 1985).

In the Suciu method the goal is to obtain the S/D parasitic resistance R_{SDE} although it is also obtained the low-field mobility μ_o and the mobility degradation parameter theta θ. The method needs at least two transistors of different sizes but the results are better when several transistors are used. However, the modulation of the S/D extensions by the gate voltage is not taken into account. The values of low-field mobility μ_o extracted by the Suciu method were extremely high and non-physical.

In Table 6.1 and Table 6.2 the average values of the extracted parameters (ΔL, R_{SDE}, and θ) are summarized for the experimental FinFET devices of the process runs. The graphics from which those extracted parameters were originated are shown in APPENDIX C - Parameter Extraction Plots.

The negative values obtained for the effective channel length shortening ΔL reflect the fact that the boundaries of S/D extensions and channel are not very well defined and are greatly dependent of the gate voltage.

Table 6.1: Average values of the effective channel length shortening ΔL, S/D parasitic resistance R_{SDE}, mobility degradation parameter theta θ (Reference Process).

	Whitfield method				Suciu method			
T_{fin} (nm)	**ΔL (nm)** V_D=50mV,	100mV	**R_{SDE} (Ω)** V_D=50mV,	100mV	**R_{SDE} (Ω)** V_D=50mV,	100mV	**θ (1/V)** V_D=50mV,	100mV
20	-42	-68	176	88	148	111	0.55	0.54
15	-69	-83	184	149	191	171	0.63	0.53
10	-89	-91	209	234	229	217	0.65	0.54
5	23	16	412	345	313	256	0.66	0.66

Table 6.2: Average values of the effective channel length shortening ΔL, S/D parasitic resistance R_{SDE}, mobility degradation parameter theta θ (Highly Doped Process).

	Whitfield method				Suciu method			
T_{fin} (nm)	**ΔL (nm)** V_D=50mV,	100mV	**R_{SDE} (Ω)** V_D=50mV,	100mV	**R_{SDE} (Ω)** V_D=50mV,	100mV	**θ (1/V)** V_D=50mV,	100mV
20	-31	-43	195	165	205	141	0.51	0.48
15	-69	-39	121	251	225	74	0.57	0.66
10	-51	-87	301	176	311	272	0.57	0.55
5	-22	-50	386	328	216	197	1.11	1.04

7 CONCLUSIONS AND FUTURE WORK

This chapter presents the conclusions of this work and discusses the most important contributions of this thesis. The future works for pursuing new directions in the FinFETs research are also mentioned.

7.1 Conclusions

Silicon-on-Insulator (SOI) technology is nowadays a serious competitor for traditional BULK technology. SOI-MOSFETs with single-gate, double-gate and multi-gate have superior performance over traditional BULK MOSFETs.

An overview of SOI technology and multi-gate MOSFETs were presented along with the description and implementation of a charge-sheet model for the fully-depleted SOI-MOSFET and a high frequency modeling of this device. Distributed channel and distributed gate analysis along with a good physical model proved to be an asset in high frequency modeling of SOI-MOSFETs. This analysis has given the necessary encouragement to continue researching SOI devices.

The SOI-FinFET transistor have good potential for circuit applications and have been researched over the years to solve many technology issues concerning the optimization of its geometry and process parameters.

This work addressed the parameters to make the SOI-FinFET a candidate for a viable CMOS node below 22 nm. In order to achieve this goal a good understanding of the characteristics of the SOI-FinFET and the influence of process and geometry parameters on its behavior is fundamental. Due to the three-dimensional nature of the SOI-FinFET device, 3D-numerical simulation is a necessity.

The basic characteristics of the Double-Gate (DG) SOI-FinFET and the results and analysis of a 3D-numerical simulation were presented. The dependence of threshold voltage V_T and subthreshold slope S on silicon fin thickness T_{fin} and on silicon fin doping N_{fin} were demonstrated. The influence of a partial-depleted (PD) or fully-depleted (FD) silicon fin on device characteristics was shown.

The effects of random dopants fluctuations are very important and may render the mid-range silicon fin doping of 10^{17} to 10^{18} cm^{-3} unsuitable for circuits on which T_{fin} is below 20 nm and L_G is aggressively scaled below 20 nm. The undoped silicon fin, i.e., with typical doping on the order of $1x10^{15}$ cm^{-3}, is the most practical since V_T will depend mostly on the gate work-function and on the silicon fin width. Moreover, random-doping problems and corner-effects can be neglected in undoped FinFETs.

The impact on V_T and S of varying T_{fin}, N_{fin} and L_G, was investigated both by 3D device simulations and experimental measurements. The degradation of device characteristics for gate lengths below 50 nm (T_{fin} = 20 nm) is clearly noted and the device with L_G = 20 nm (T_{fin} = 20 nm) shows very weak characteristics that need considerable improvement. The device simulations showed that the degradation of device characteristics for gate lengths below 50 nm is alleviated in subthreshold regime by the combined effect of T_{fin} reduction from 20 to 10 nm and the use of high-k gate insulator.

A comparison between two device simulators, Davinci and Sentaurus, was presented in this thesis. For FinFET structures with the same doping profiles, a good agreement was obtained in the subthreshold region, where the impact of different models is not felt as much, for both short and long-channel FinFET devices. However, in moderate and strong inversion regions, Davinci over estimates the drain current. Little difference was noted between Sentaurus simulations, especially for the long-channel FinFET, even when a quantization model is used. A better set of coefficients is needed in the case of the hydrodynamic model as became clear in the simulations.

By simulations was found that the top-gate of the tri-gate structure contributes only with approximated 5% for the final current due to the aspect ratio H_{fin}/T_{fin} of 3 of the FinFET structures. An over estimation of drain current in the FinFET structures simulated with Davinci is more evident when compared with simulations done with Sentaurus and with different doping profiles. For the long-channel case, even the FinFET structures with the highest doping concentration for the S/D extensions give approximately 6% less final current. The reduction of 33% (from 150 to 100 nm) in T_{Box} has produced negligible effect in the drain current I_D simulated by Sentaurus while the increase in mobility degradation has caused a 14% reduction in I_D (short-channel device) and 23% (long-channel device).

This thesis presented the estimation of the series S/D resistance (R_{SDE}) from measurements and simulations. The S/D extensions of the fin need very accurate modeling since this portion of the device is very important to the final I-V characteristics. The control and reduction of R_{SDE} represents one of the main challenges for nanoscale FinFETs.

Geometry and process parameters optimization are a key factor to increase the performance of the SOI-FinFET for circuit design and fabrication, in particular low-voltage analog applications. The S/D extension implantation methods are of great importance in multi-gate FinFET technology. This work has shown the impact of different implantation angles with respect to the fins, and the impacts on the parasitics that have to be minimized.

Three main effects define the optimization required for FinFETs in general: (1) The control and reduction of the series S/D resistance (R_{SDE}), that require a silicided S/D extension, doping engineering and possible epitaxial regrowth over the S/D part of the fin, (2) the reduction of t_{ox} below 1 nm (or EOT below 1 nm) to make the FinFET a candidate for the 22 nm CMOS node and (3) T_{fin} in the range of 8 to 15 nm. FinFET characteristics at these regimes are dominated by quantum-size effects like tunneling through gate oxide, electron wavelength quantizing effects, and random dopant/defects fluctuations within the fin active region, and roughness and shape effects from the fin etching process. These are the effects that need further investigation to improve the electrical characteristics of these devices.

7.2 Future Work

Future woks suggested to probe further in the optimization of sub-20 nm FinFET include:

- use of 3D numerical simulators Sentaurus (Synopsys) and ISE-TCAD and the results they provide in this work, to compare with modern quantum statistical transport simulators that have physically-based transport models;
- optimize the undoped FinFET for physical gate lengths in the range of 10 to 20 nm and extremely thin fins geometry (in the range of 8 to 15 nm);
- consider the modulation of effective gate length and series S/D parasitic resistance by the gate voltage in the parameter extraction method;
- consider appropriately the quantum confinement effects on the device I-V characteristics;
- use a predictive electrical model for the FinFETs and to extract the device model parameters for circuit simulation with DG SOI FinFET;
- modeling the behavior of TAT associations (parallel/series) with Double-Gate SOI-FinFETs;
- use of both the predictive model and the TAT associations in the simulation of analog circuits, like a single-stage amplifier circuit.
- consider the effects of random dopants/defects fluctuations and variability aspects in FinFETs.

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APPENDIX A - V_T EXTRACTION METHODS

A.1 Extrapolation in the linear region of I_D-V_G curve

This method (Ortiz-Conde, 2002) consists in the linear extrapolation of I_D-V_G curve at the point of maximum transconductance (maximum $g_m=dI_D/dV_G$) and of finding V_G voltage axis intercept point. The resulting threshold voltage V_T is the intercept point voltage minus $V_D/2$. This method is simple and very popular, based on the first order I-V MOSFET transistor characteristic, valid only for low drain to source voltages (e.g. 100 mV or less). In Figure A.1 are shown curves of V_T versus gate length L_G (by device simulations with Davinci) with V_T extracted by this method, called method "LE" for short.

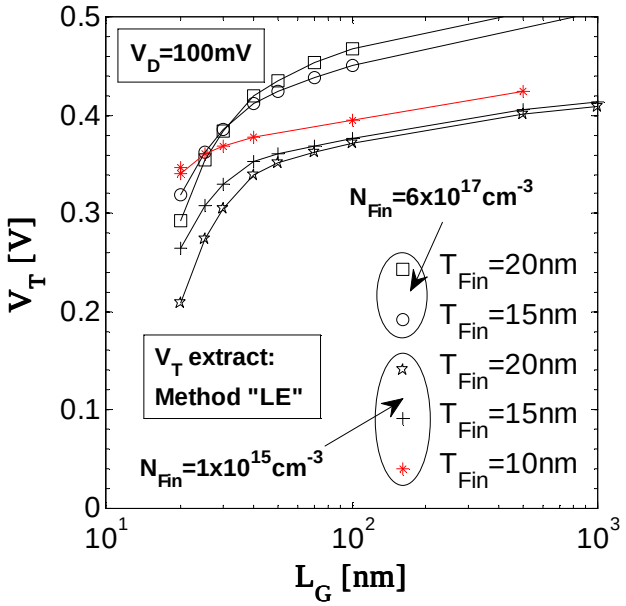

Figure A.1: Threshold voltage V_T versus gate length L_G for different values of T_{fin} and N_{fin} (V_D = 100 mV). V_T extracted by means of extrapolation in the linear region of I_D-V_G curve (method "LE" for short), obtained by device simulations with Davinci.

A.2 Second-derivative of I_D-V_G curve

This method (Ortiz-Conde, 2002)(Wong, 1987) consists of finding V_G voltage of I_D-V_G curve at the point of maximum second-derivative (maximum $dg_m/dV_G=d^2I_D/dV_G^2$), which is the resulting threshold voltage V_T. This method was developed to avoid the influence of series resistences. In Figure A.2 are shown curves of V_T versus gate length L_G (by device simulations with Davinci) with V_T extracted by this method, called method "SD" for short. One can compare these curves with those of Figure A.1 and note that the values of V_T are now probably affected by the numerical derivatives, resulting in some fluctuations along with the general tendency of decrease in V_T with the reduction of gate length.

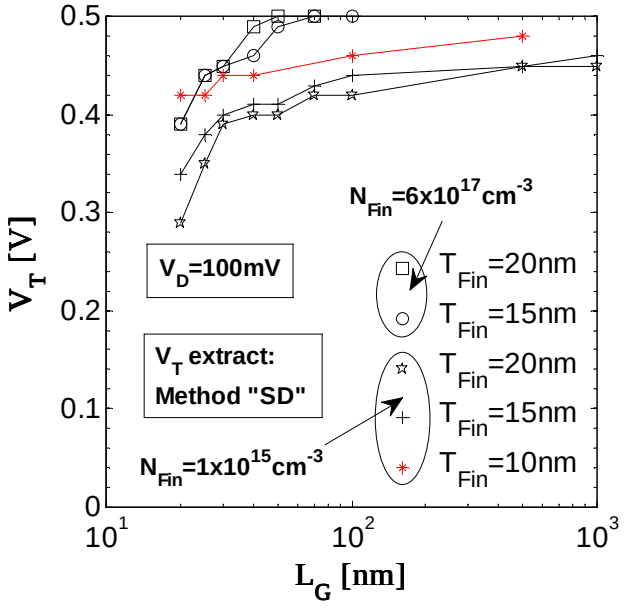

Figure A.2: Threshold voltage V_T versus gate length L_G for different values of T_{fin} and N_{fin} (V_D = 100 mV). V_T extracted by means of second-derivative of I_D-V_G curve (method "SD" for short), obtained by device simulations with Davinci.

A.3 Extrapolation in the linear region of g_m-V_G curve

This method (Ortiz-Conde, 2002)(Tsuno, 1998, 1999) consists in the linear extrapolation of g_m-V_G curve at the point of maximum derivative (maximum $dg_m/dV_G=d^2I_D/dV_G^2$) and of finding V_G voltage axis intercept point, which is the resulting threshold voltage V_T. This method was developed to be physically-based with the definition of V_T, thus excluding the influence of device parameters such as series resistances. In Figure A.3 are shown curves of V_T versus gate length L_G (by device simulations with Davinci) with V_T extracted by this method, called method "GMLE" for short. One can note that the V_T fluctuations of the previous method "SD" have disappeared and that these curves are similar in shape to those obtained by means of method "LE".

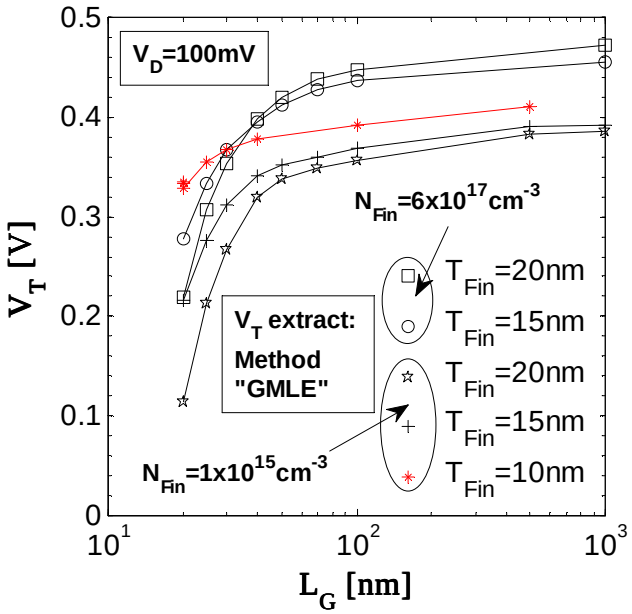

Figure A.3: Threshold voltage V_T versus gate length L_G for different values of T_{fin} and N_{fin} (V_D = 100 mV). V_T extracted by means of extrapolation in the linear region of g_m-V_G curve (method "GMLE" for short), obtained by device simulations with Davinci.

A.4 Comparison of V_T Extraction Methods

Figure A.4 shows a comparison of the three extraction methods explained in the preceding sections. The simulated data are for a FinFET structure with T_{fin} = 10 nm and N_{fin} = 1x10^{15}cm^{-3} (V_D = 100 mV). One can compare method “SD” to method “LE” and “GMLE” and note that the values of V_T are affected by numerical derivatives, but in conception is less affected by series resistances. Methods “LE” and “GMLE” present similar results, with systematically lower values for V_T than those obtained by method “SD”. Method “GMLE” also was developed to be less affected by device parameters such as series resistances.

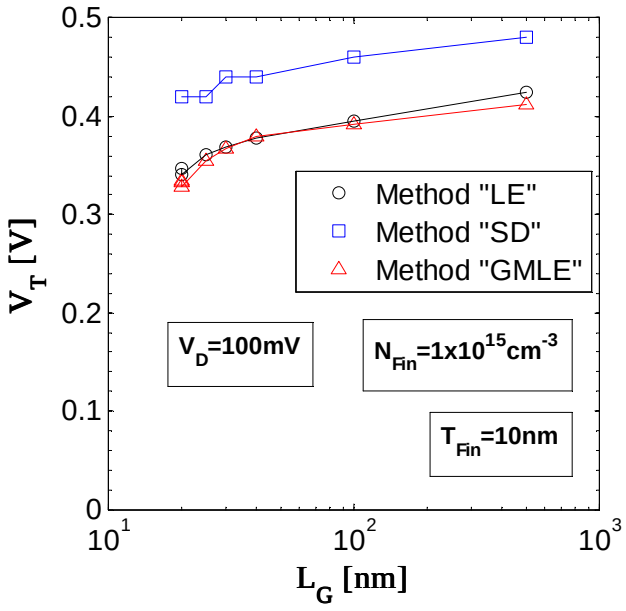

Figure A.4: Threshold voltage V_T versus gate length L_G for the three extraction methods (methods “LE”, “SD”, and “GMLE”) explained in the preceding sections (T_{fin} = 10 nm, N_{fin} = 1x10^{15} cm^{-3} and V_D = 100 mV), obtained by device simulations with Davinci.

APPENDIX B - MEASUREMENT PLOTS

B.1 Reference Process - Plots

B.1.1 V_T, S and DIBL

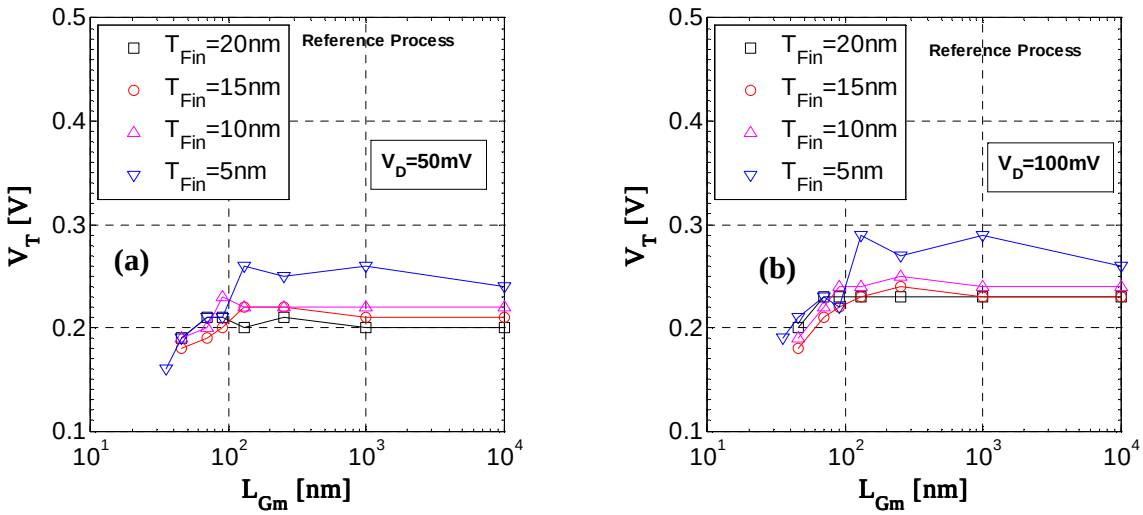

Figure B.1: Threshold voltage versus mask gate length (V_T vs. L_{Gm}) for different values of T_{fin}. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the reference process. V_T extracted by method "SD" (see Appendix A).

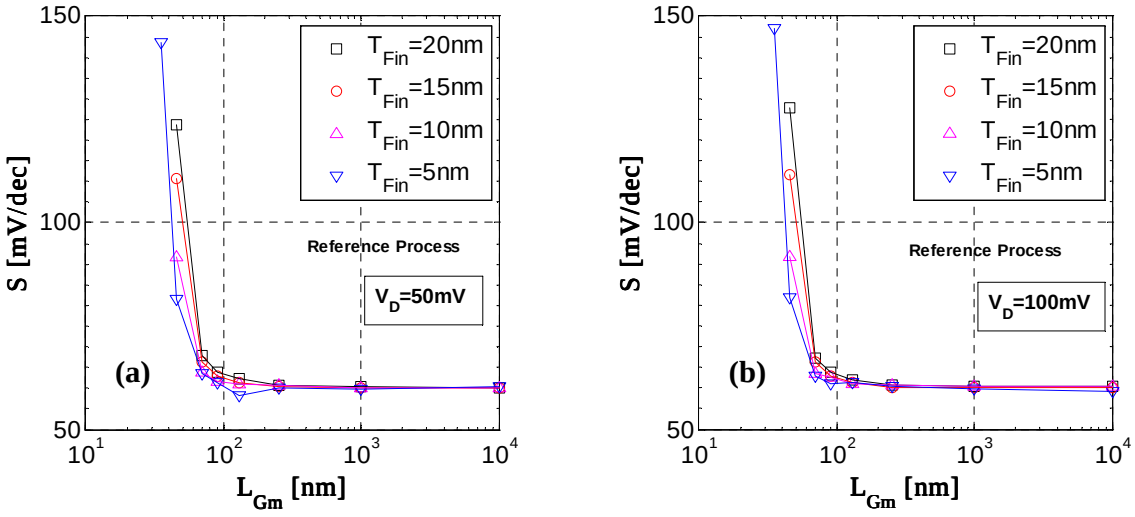

Figure B.2: Subthreshold slope versus mask gate length (S vs. L_{Gm}) for different values of T_{fin}. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the reference process.

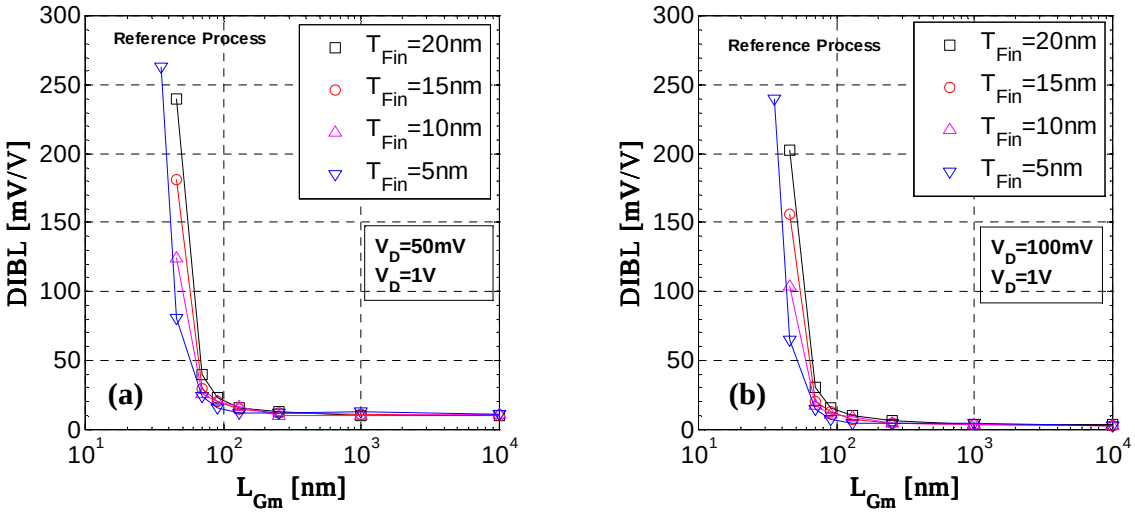

Figure B.3: DIBL versus mask gate length (DIBL vs. L_{Gm}) for different values of T_{fin}. (a) V_D = 50 mV and 1V and (b) V_D = 100 mV and 1V. The samples were measured in the wafer of the reference process.

B.1.2 g_m, g_m/I_D, V_A and A_v (T_{fin} = 20 nm)

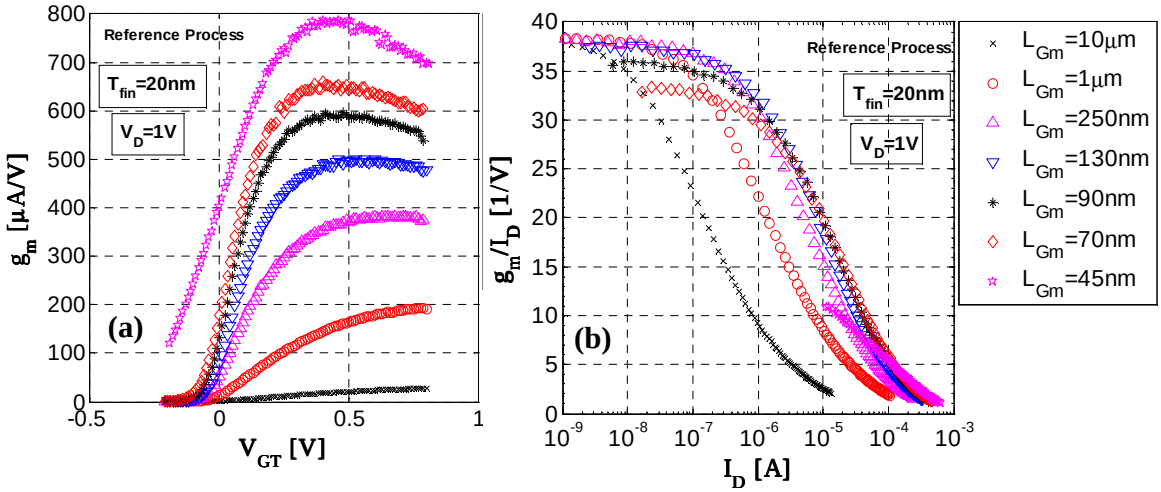

Figure B.4: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 20 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

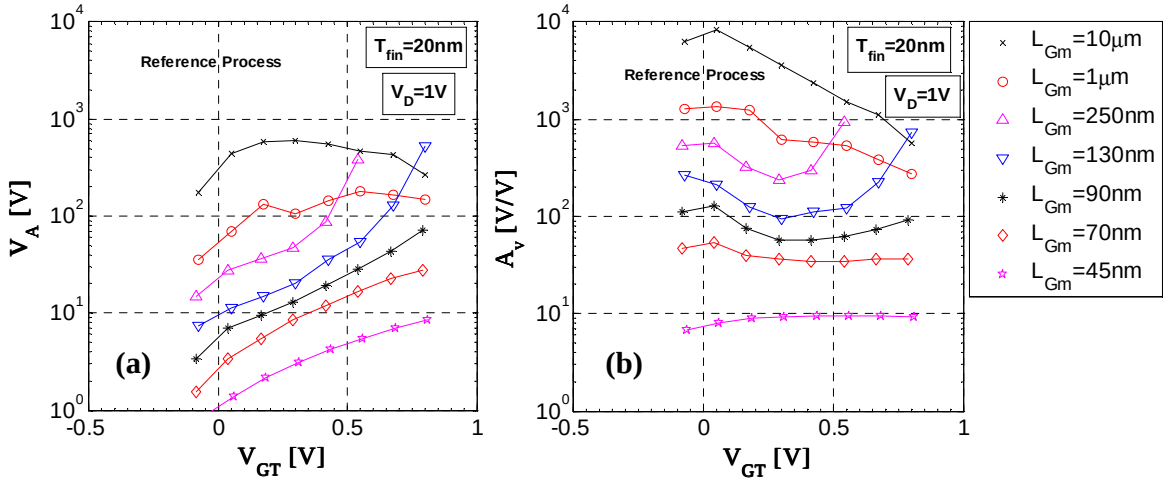

Figure B.5: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 20 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

B.1.3 g_m, g_m/I_D, V_A and A_v (T_{fin} = 15 nm)

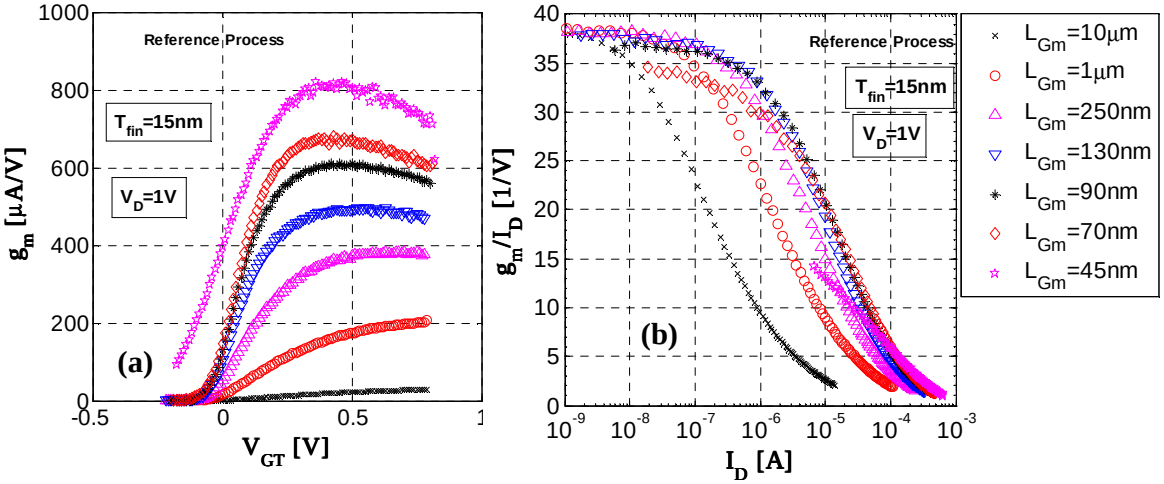

Figure B.6: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 15 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

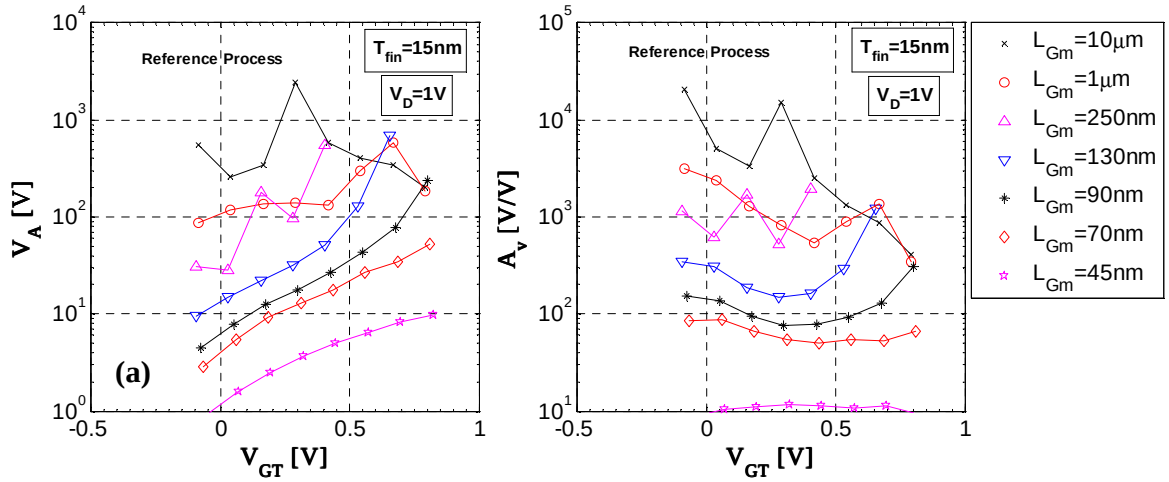

Figure B.7: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 15 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

B.1.4 g_m, g_m/I_D, V_A and A_v (T_{fin} = 10 nm)

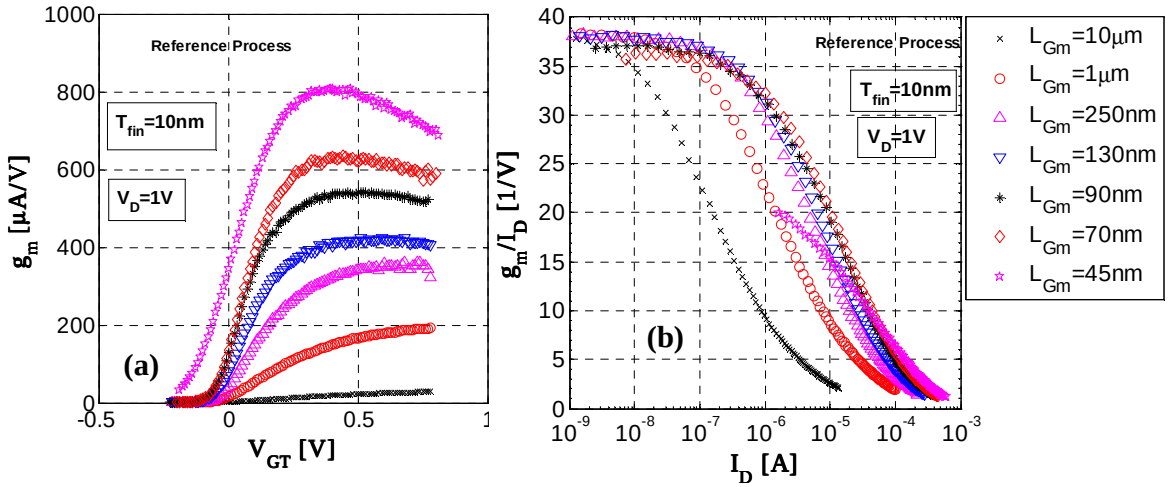

Figure B.8: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 10 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

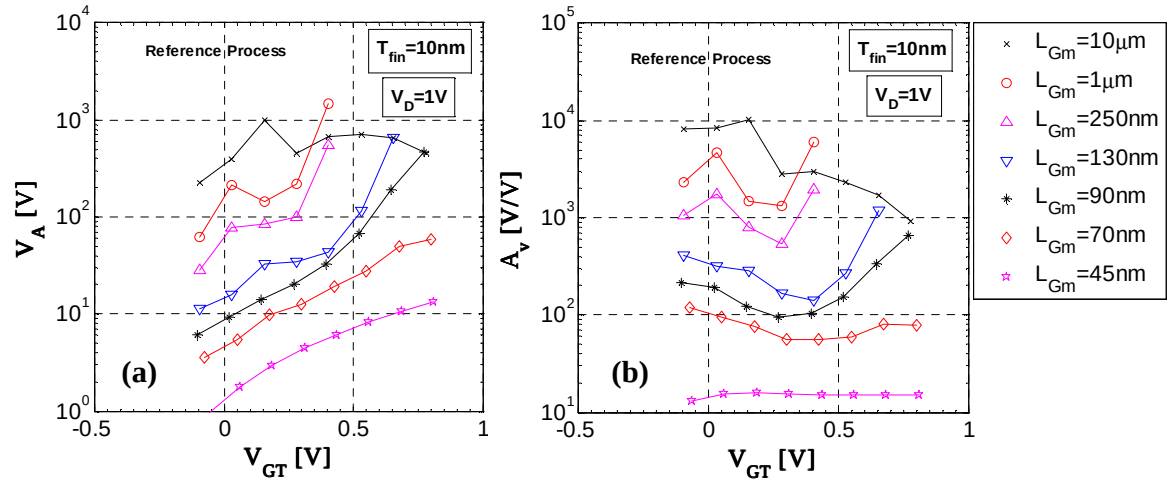

Figure B.9: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 10 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

B.1.5 g_m, g_m/I_D, V_A and A_v (T_{fin} = 5 nm)

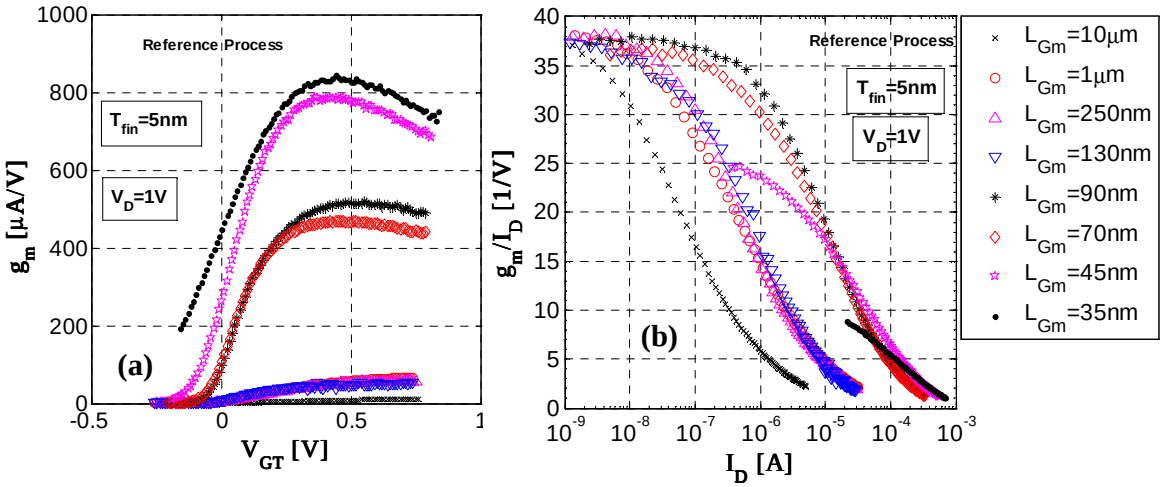

Figure B.10: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 5 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

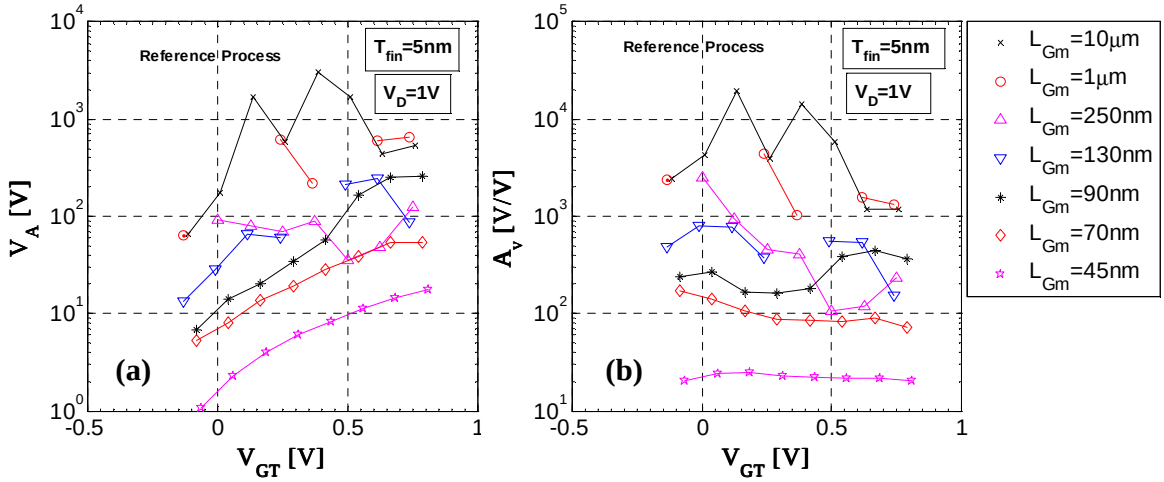

Figure B.11: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 5 nm and for different values of L_{Gm}. The samples were measured in the wafer of the reference process.

B.2 Highly Doped Process - Plots

B.2.1 V_T, S and DIBL

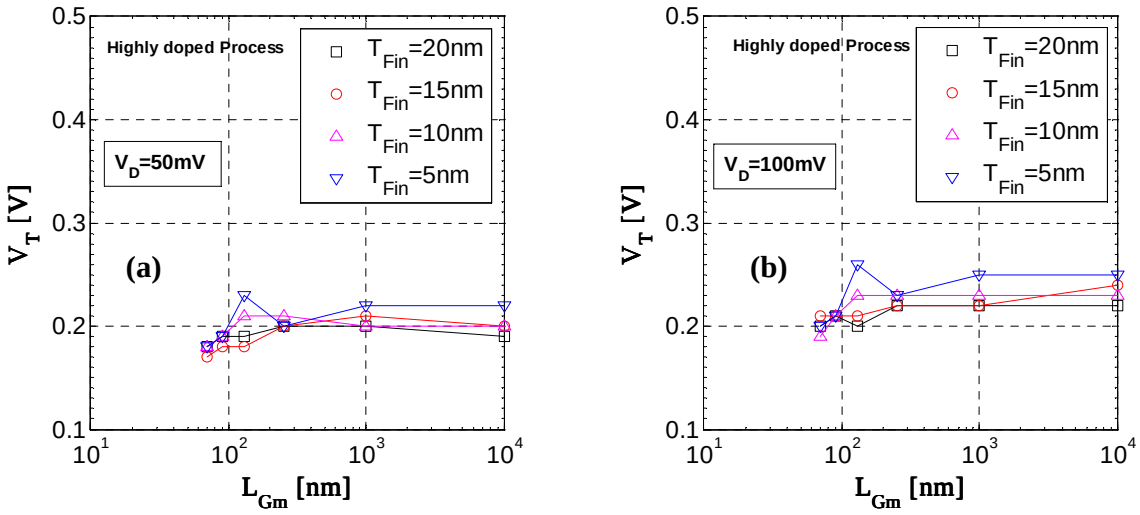

Figure B.12: Threshold voltage versus mask gate length (V_T vs. L_{Gm}) for different values of T_{fin}. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the highly doped process. V_T extracted by method "SD" (see Appendix A).

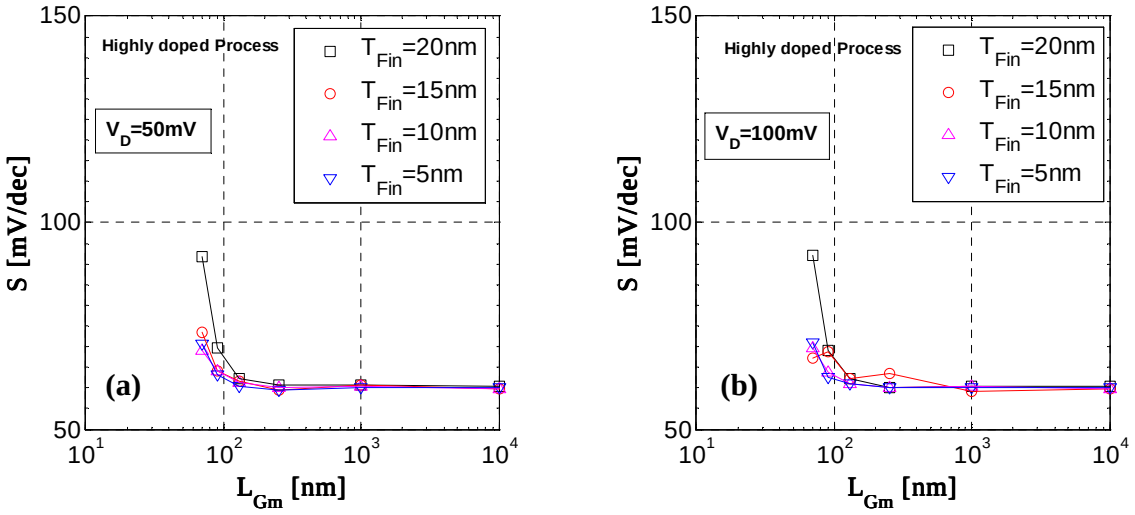

Figure B.13: Subthreshold slope versus mask gate length (S vs. L_{Gm}) for different values of T_{fin}. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the highly doped process.

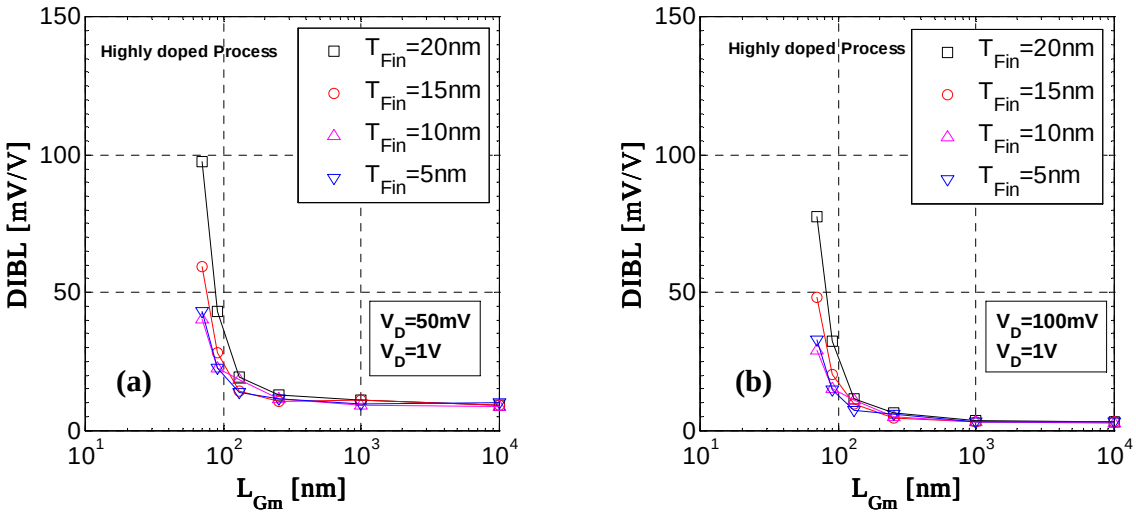

Figure B.14: DIBL versus mask gate length (DIBL vs. L_{Gm}) for different values of T_{fin}. (a) V_D = 50 mV and 1V and (b) V_D = 100 mV and 1V. The samples were measured in the wafer of the highly doped process.

B.2.2 g_m, g_m/I_D, V_A and A_v (T_{fin} = 20 nm)

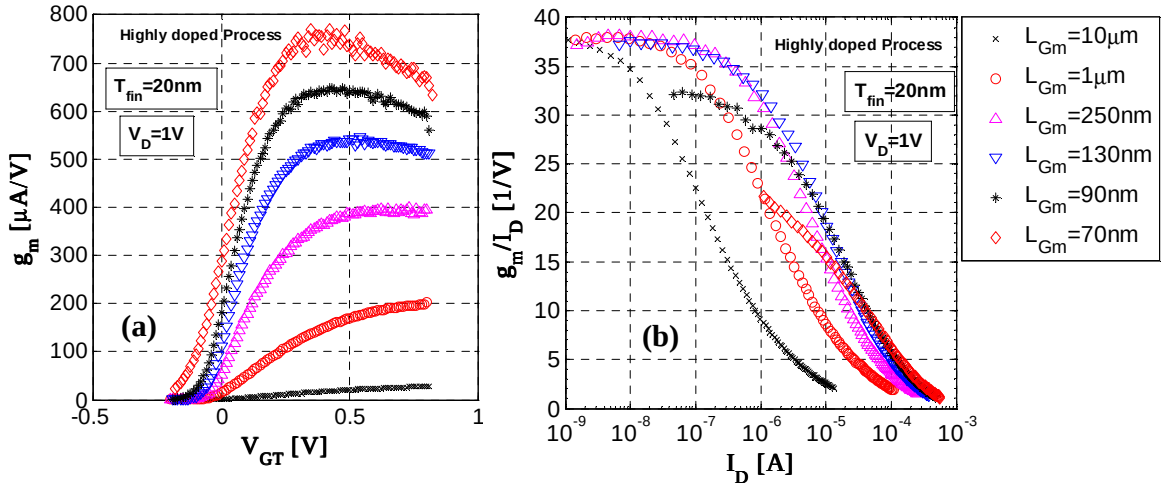

Figure B.15: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 20 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

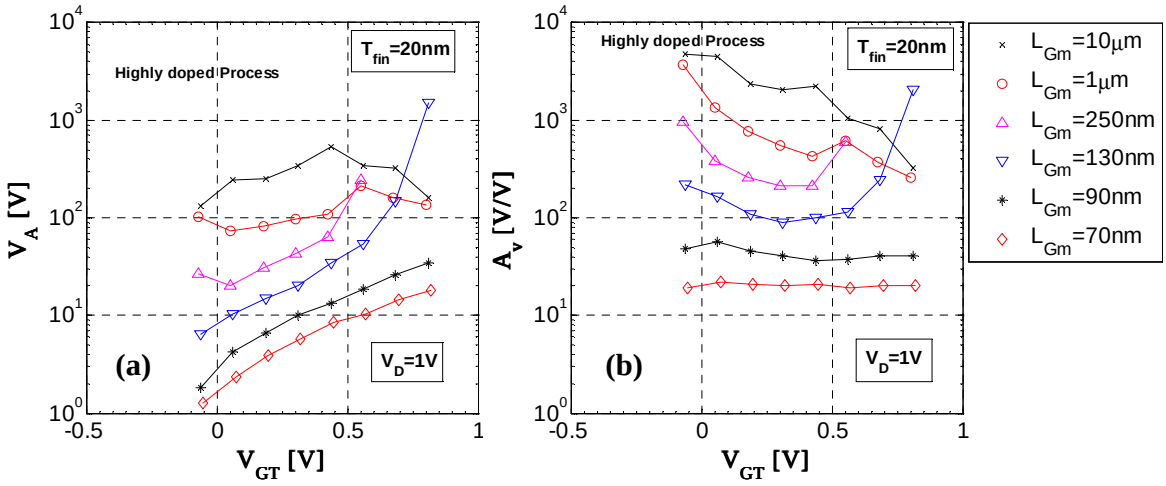

Figure B.16: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 20 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

B.2.3 g_m, g_m/I_D, V_A and A_v (T_{fin} = 15 nm)

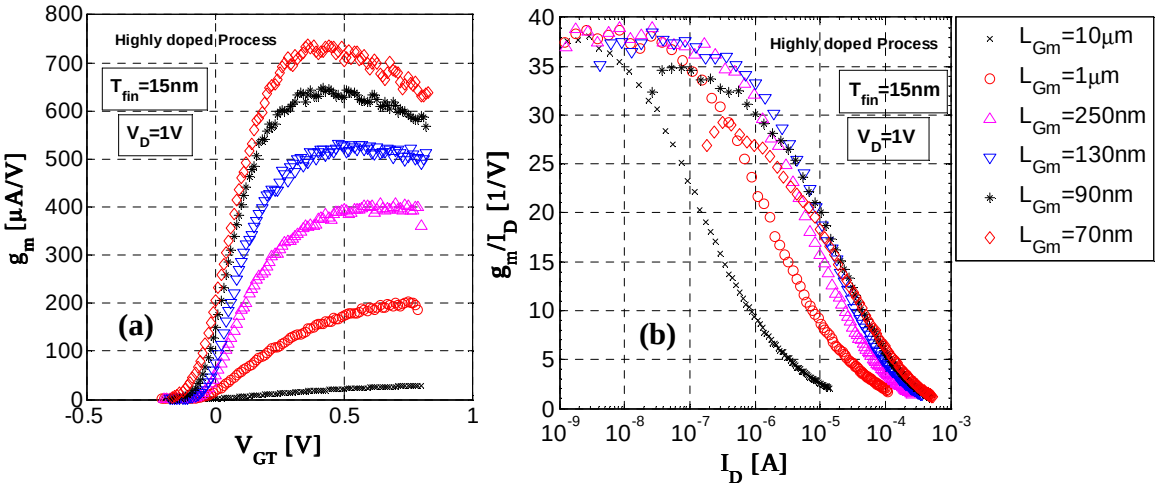

Figure B.17: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 15 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

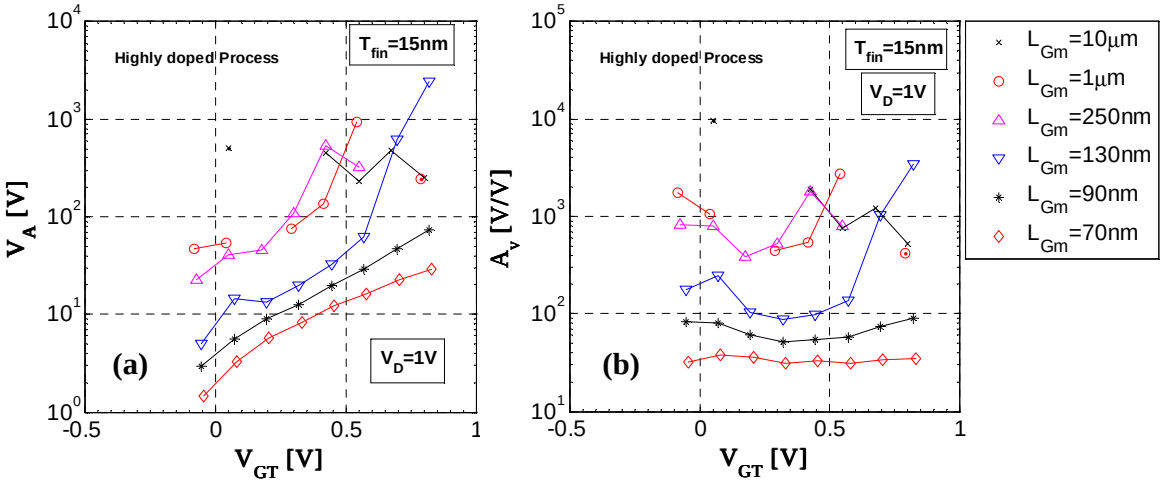

Figure B.18: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 15 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

B.2.4 g_m, g_m/I_D, V_A and A_v (T_{fin} = 10 nm)

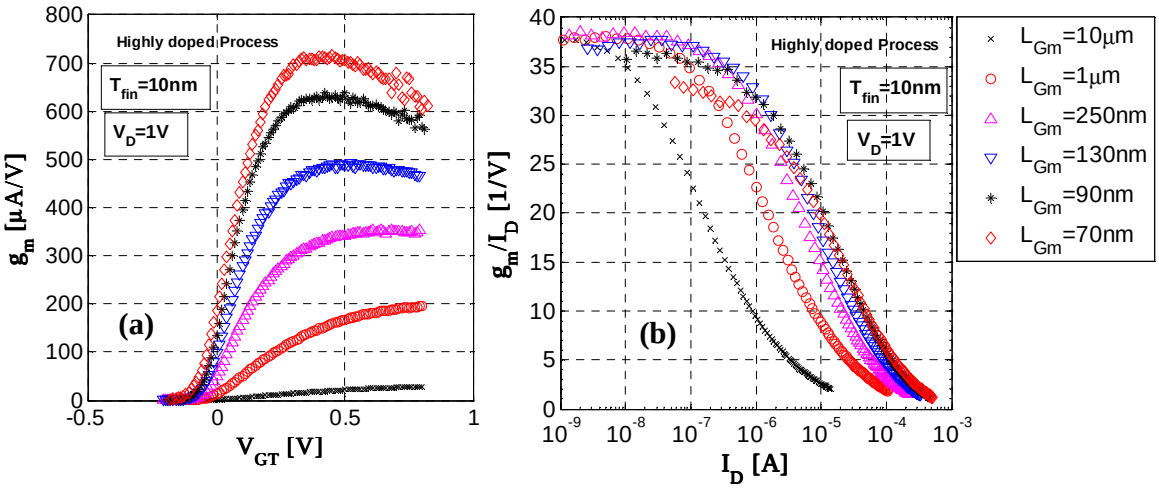

Figure B.19: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 10 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

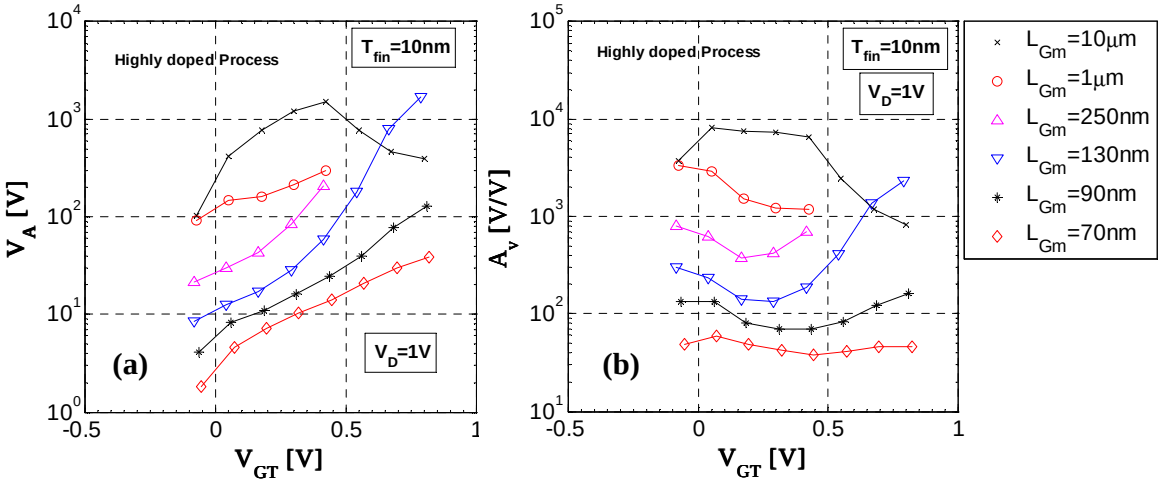

Figure B.20: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 10 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

B.2.5 g_m, g_m/I_D, V_A and A_v (T_{fin} = 5 nm)

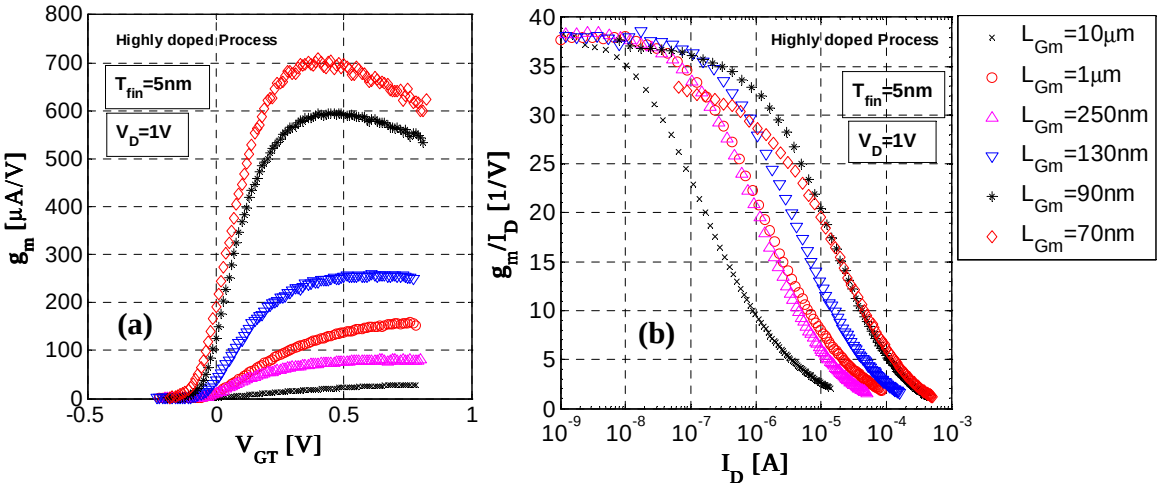

Figure B.21: (a) Transconductance versus gate voltage overdrive (g_m vs. V_{GT}) and (b) transconductance over drain current versus drain current (g_m/I_D vs. I_D) both plots in the saturation region, T_{fin} = 5 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

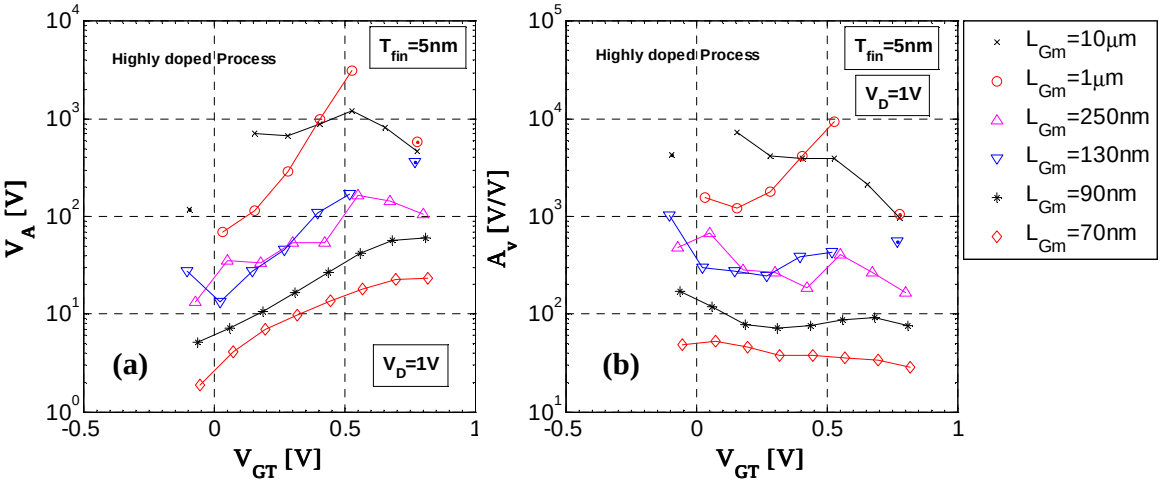

Figure B.22: (a) Early voltage versus gate voltage overdrive (V_A vs. V_{GT}) and (b) Voltage Gain versus gate voltage overdrive (A_v vs. V_{GT}) both plots in the saturation region, T_{fin} = 5 nm and for different values of L_{Gm}. The samples were measured in the wafer of the highly doped process.

APPENDIX C - PARAMETER EXTRACTION PLOTS

C.1 Reference Process - Plots

C.1.1 R_{SDE} and L_{Geff} (T_{fin} = 20 nm)

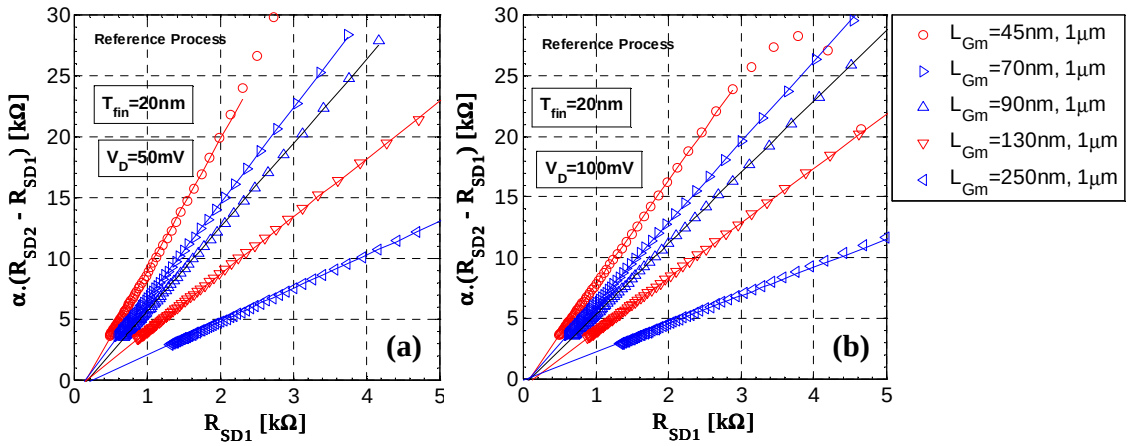

Figure C.1: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the reference process, T_{fin} = 20 nm.

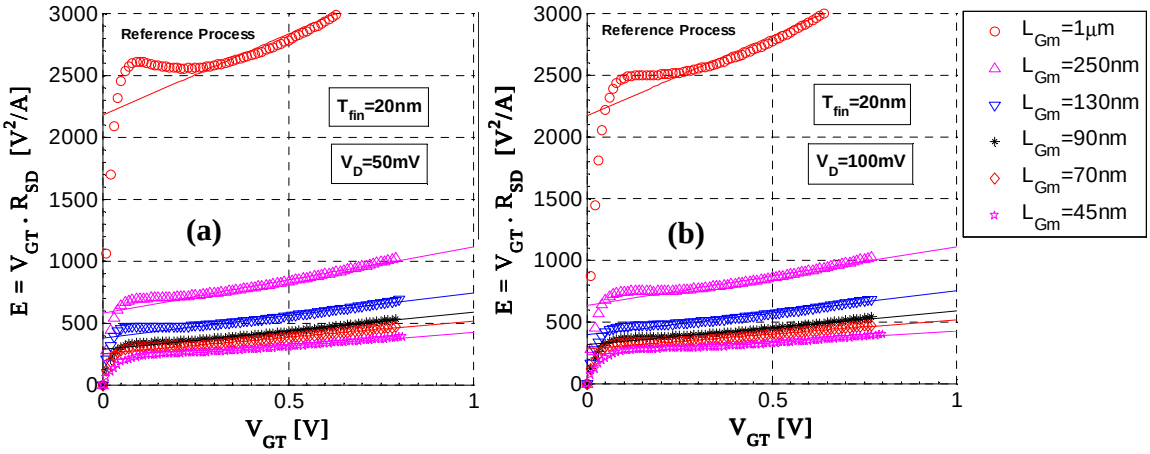

Figure C.2: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 20$ nm.

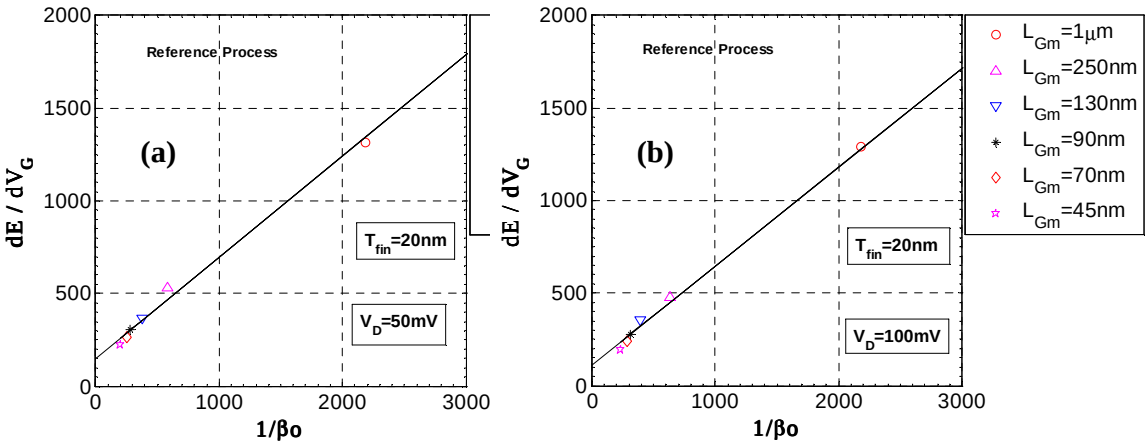

Figure C.3: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 20$ nm.

C.1.2 R_{SDE} and L_{Geff} (T_{fin} = 15 nm)

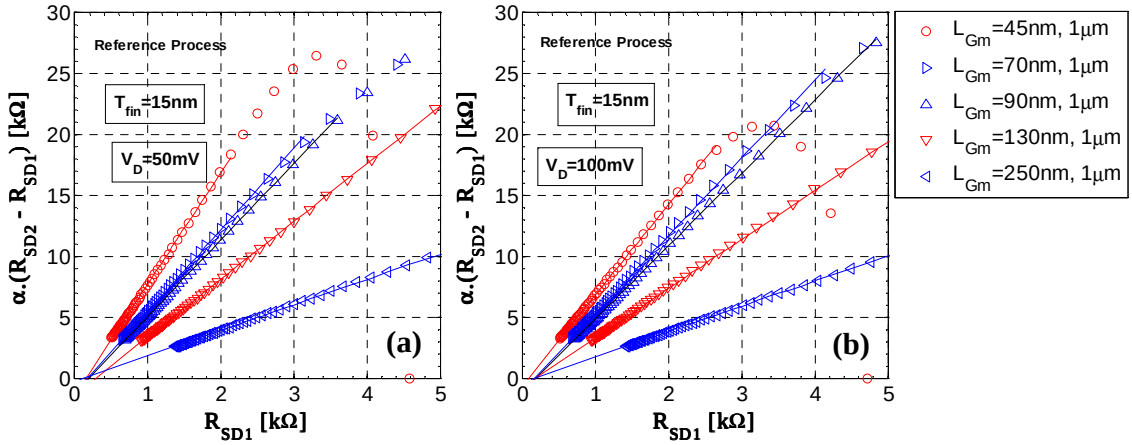

Figure C.4: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the reference process, T_{fin} = 15 nm.

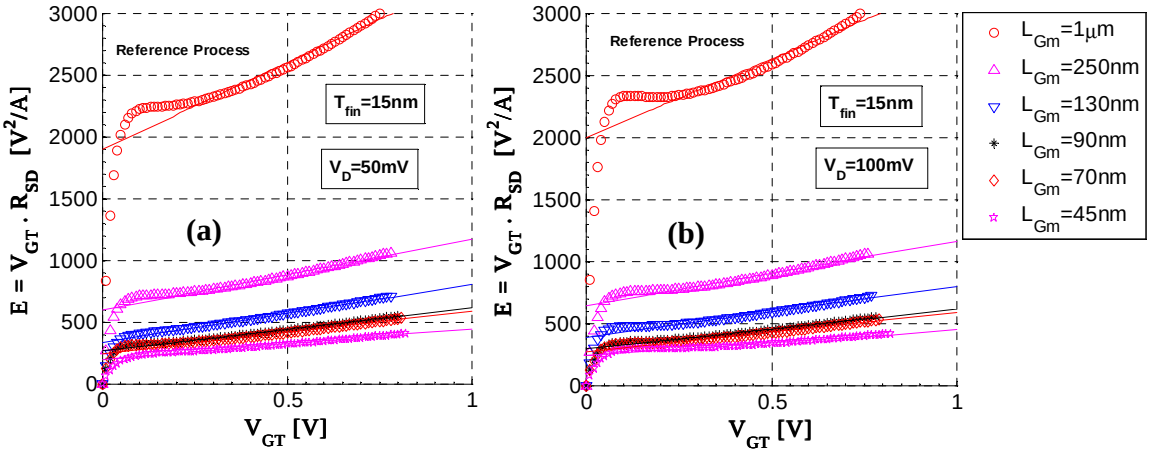

Figure C.5: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 15$ nm.

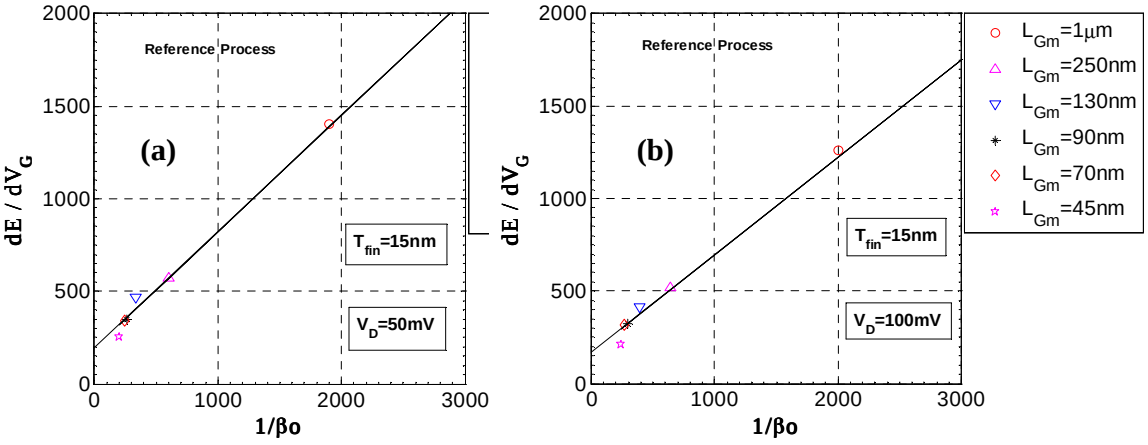

Figure C.6: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 15$ nm.

C.1.3 R_{SDE} and L_{Geff} (T_{fin} = 10 nm)

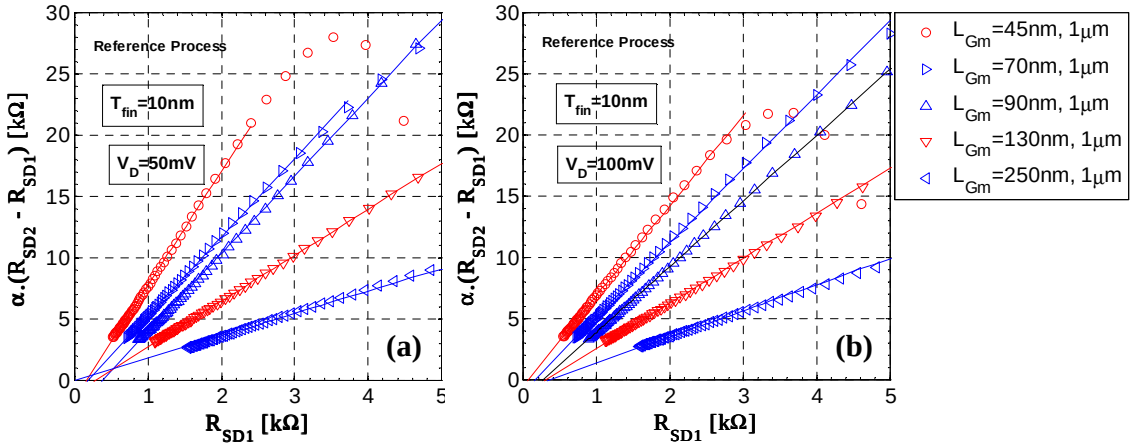

Figure C.7: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the reference process, T_{fin} = 10 nm.

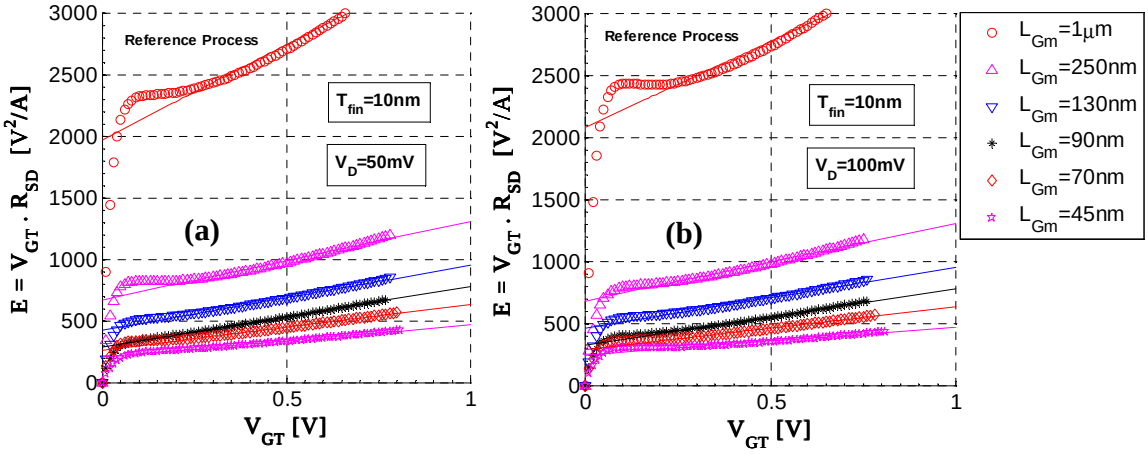

Figure C.8: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 10$ nm.

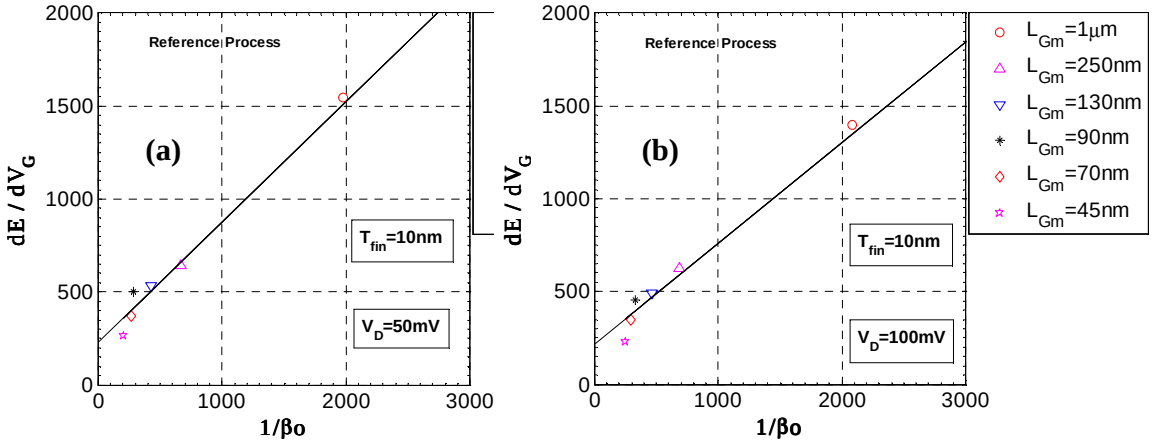

Figure C.9: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 10$ nm.

C.1.4 R_{SDE} and L_{Geff} (T_{fin} = 5 nm)

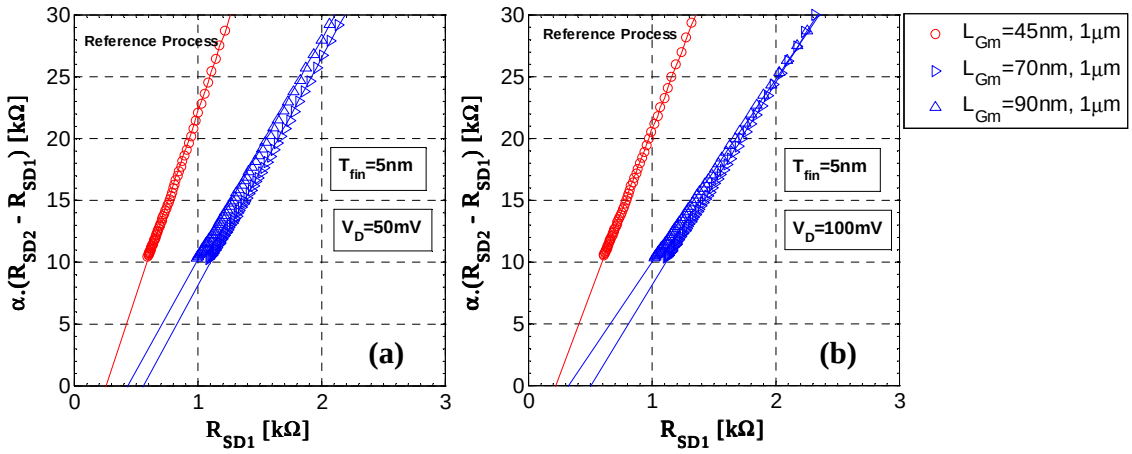

Figure C.10: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the reference process, T_{fin} = 5 nm.

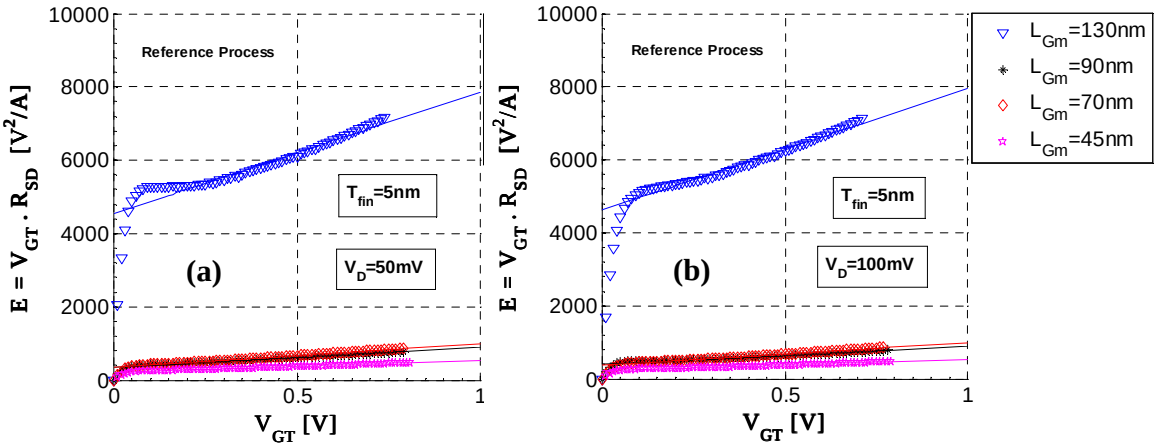

Figure C.11: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 5$ nm.

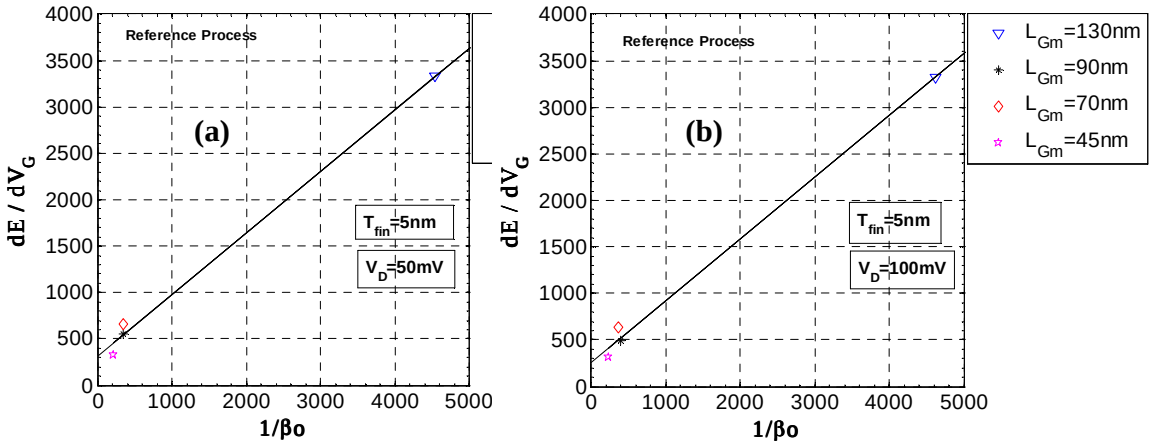

Figure C.12: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the reference process, $T_{fin} = 5$ nm.

C.2 Highly Doped Process - Plots

C.2.1 R_{SDE} and L_{Geff} (T_{fin} = 20 nm)

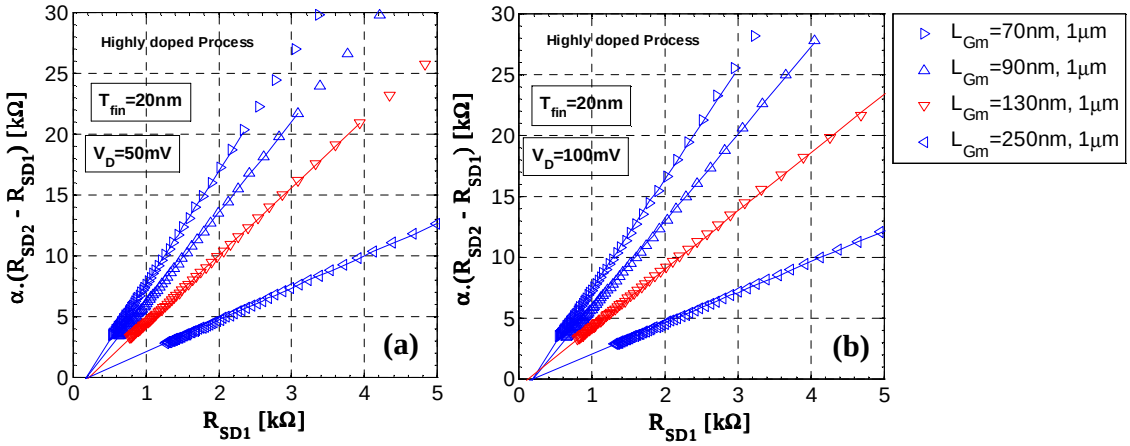

Figure C.13: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the highly doped process, T_{fin} = 20 nm.

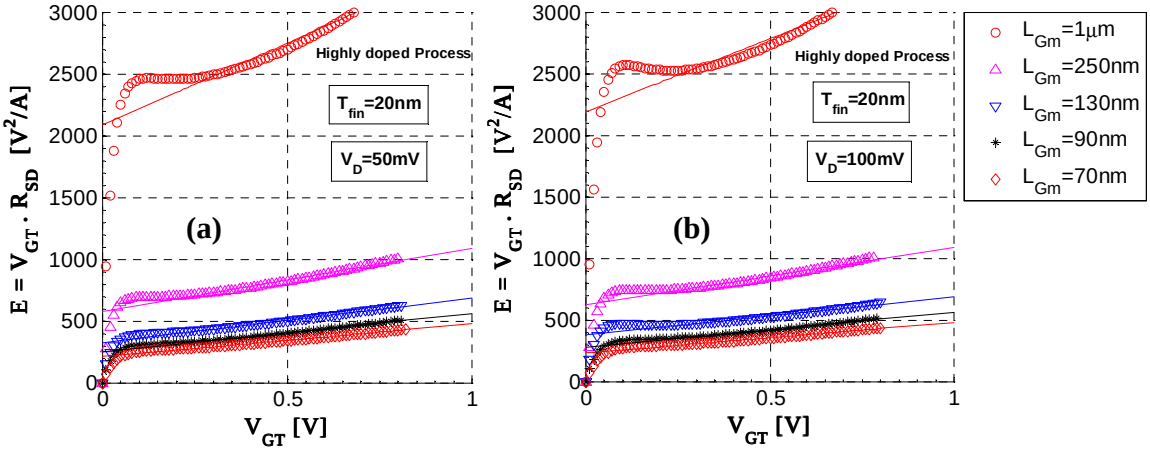

Figure C.14: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 20$ nm.

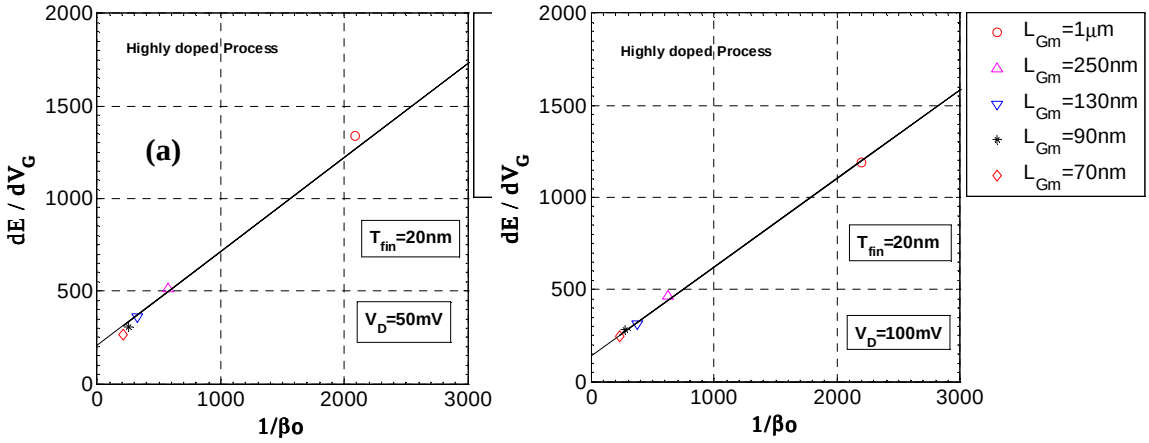

Figure C.15: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 20$ nm.

C.2.2 R_{SDE} and L_{Geff} (T_{fin} = 15 nm)

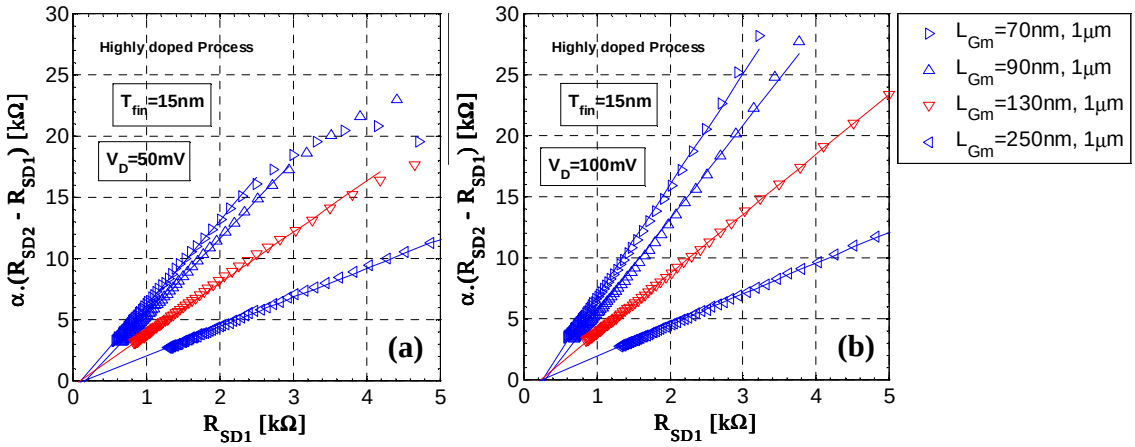

Figure C.16: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the highly doped process, T_{fin} = 15 nm.

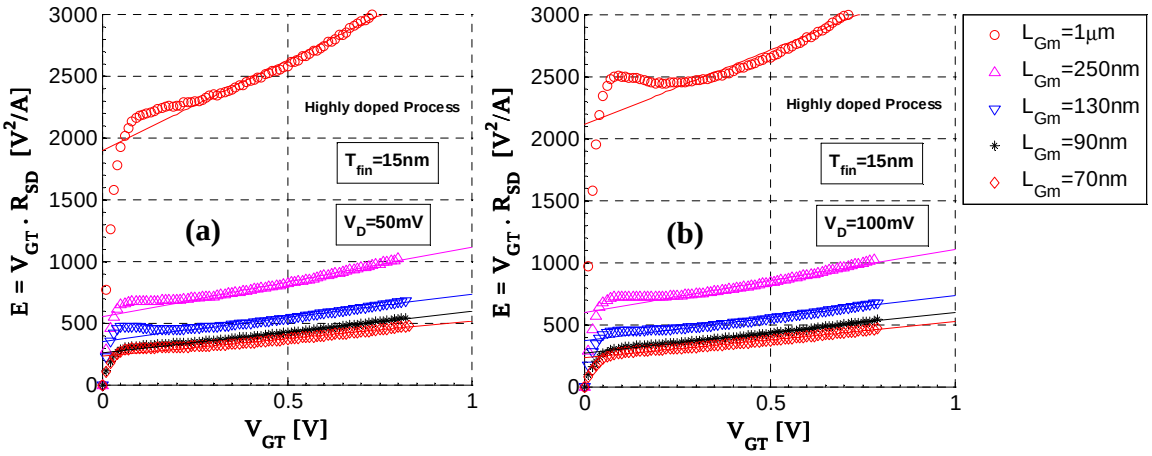

Figure C.17: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 15$ nm.

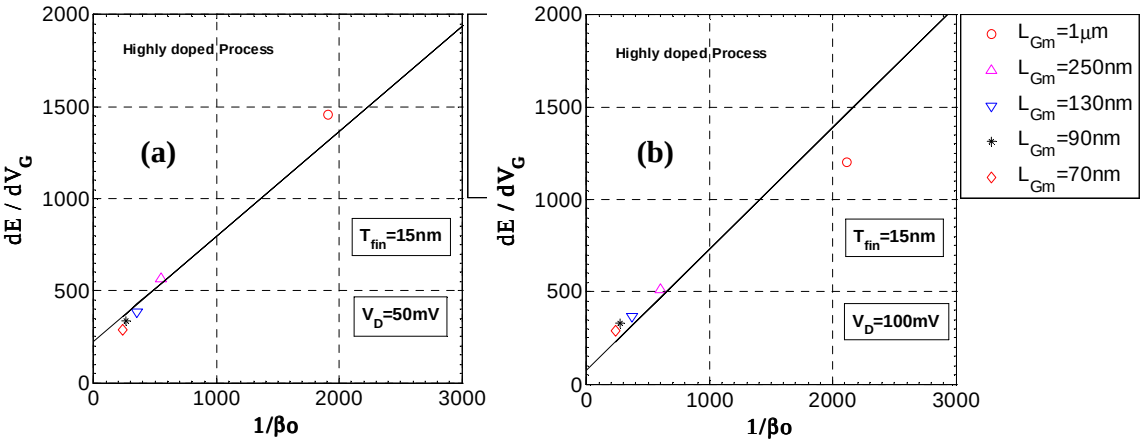

Figure C.18: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 15$ nm.

C.2.3 R_{SDE} and L_{Geff} (T_{fin} = 10 nm)

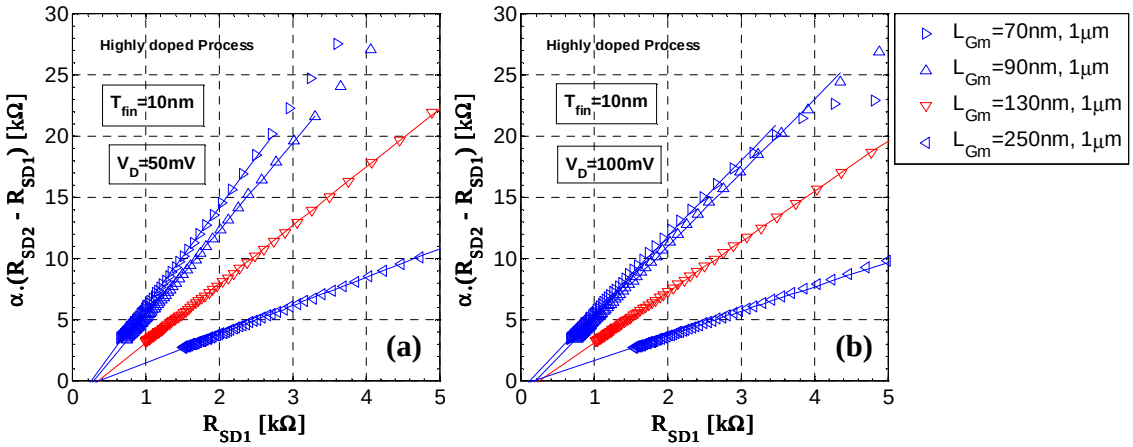

Figure C.19: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the highly doped process, T_{fin} = 10 nm.

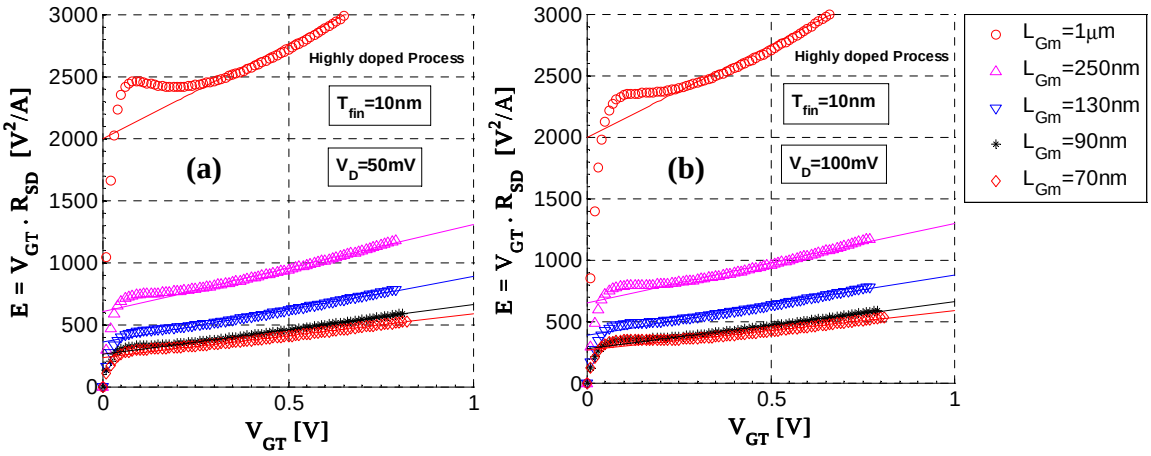

Figure C.20: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 10$ nm.

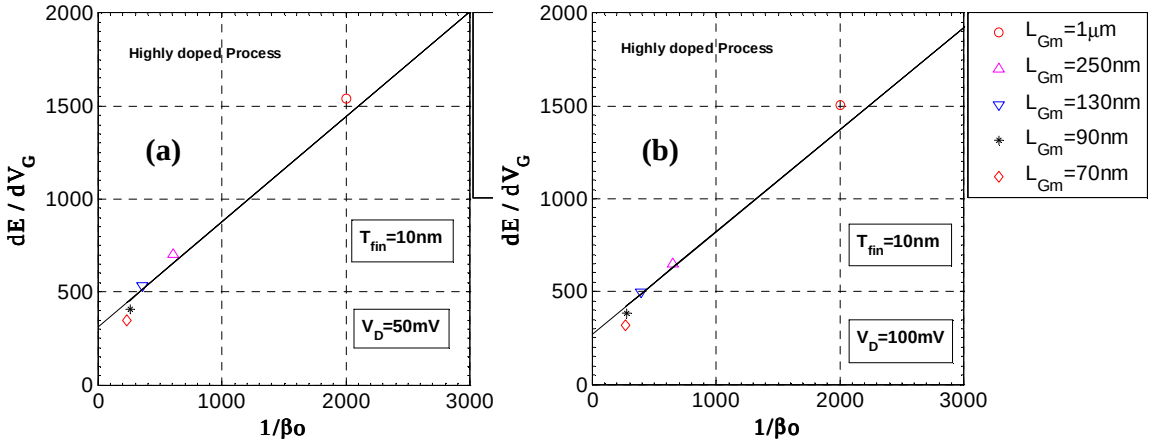

Figure C.21: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 10$ nm.

C.2.4 R_{SDE} and L_{Geff} (T_{fin} = 5 nm)

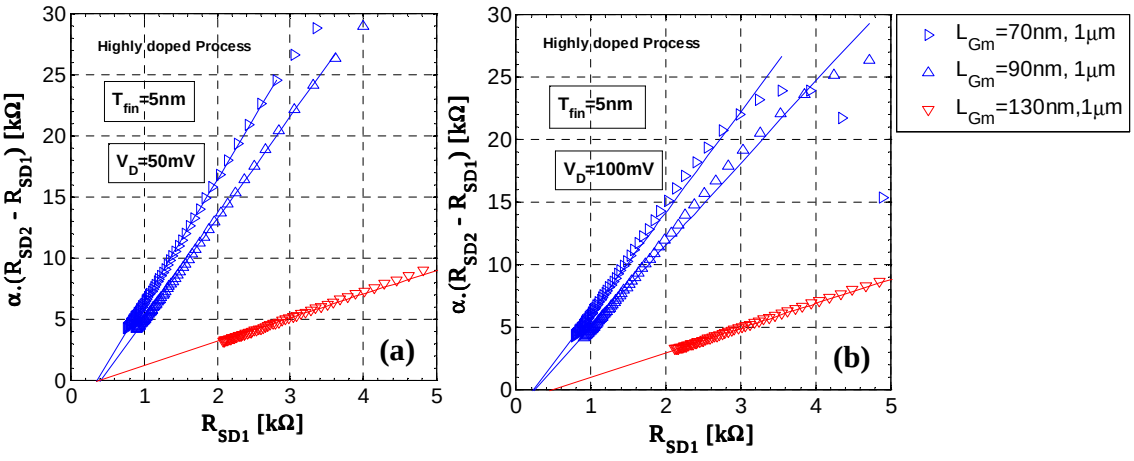

Figure C.22: S/D total resistances ($R_{SD1} = V_D/I_{D1}$ and $R_{SD2} = V_D/I_{D2}$) from I_D-V_G measurements (linear region in strong inversion) of pairs of FinFET devices with different mask gate lengths (L_{Gm1} and L_{Gm2}, $L_{Gm1} < L_{Gm2}$), plotted as the difference of the resistances (R_{SD2}-R_{SD1}) versus R_{SD1}. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the R_{SD1} axis. The parameter "α" is a correction to account for a difference in the threshold voltages. (a) V_D = 50 mV and (b) V_D = 100 mV. The samples were measured in the wafer of the highly doped process, T_{fin} = 5 nm.

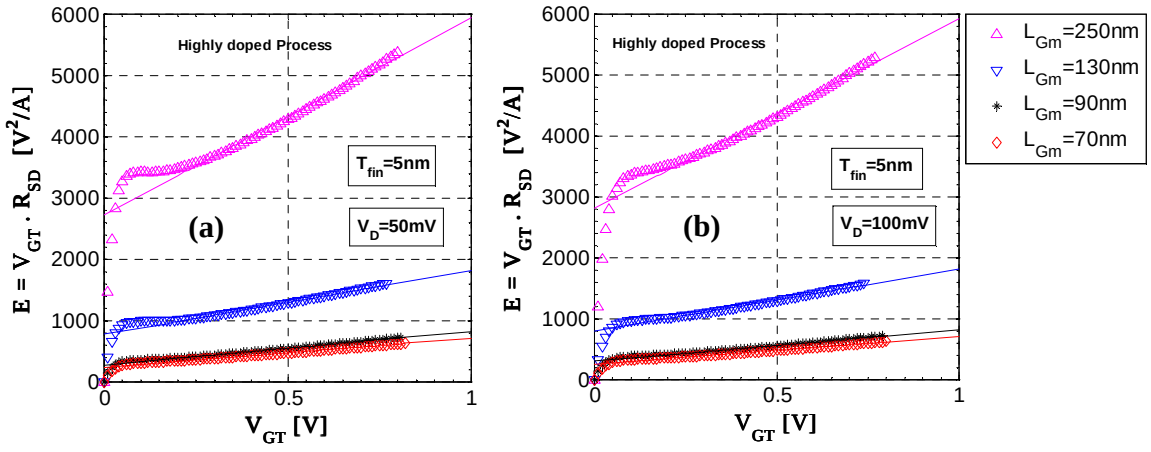

Figure C.23: Parameter "E" versus V_{GT} for several mask gate lengths. "E" is defined as the product of the gate voltage overdrive (V_{GT}) and the S/D total resistance ($R_{SD} = V_D/I_D$). The inverse of the transconductance factor ($1/\beta_o$) is found at the point of intersection between the linear fitting of data and the "E" axis. (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 5$ nm.

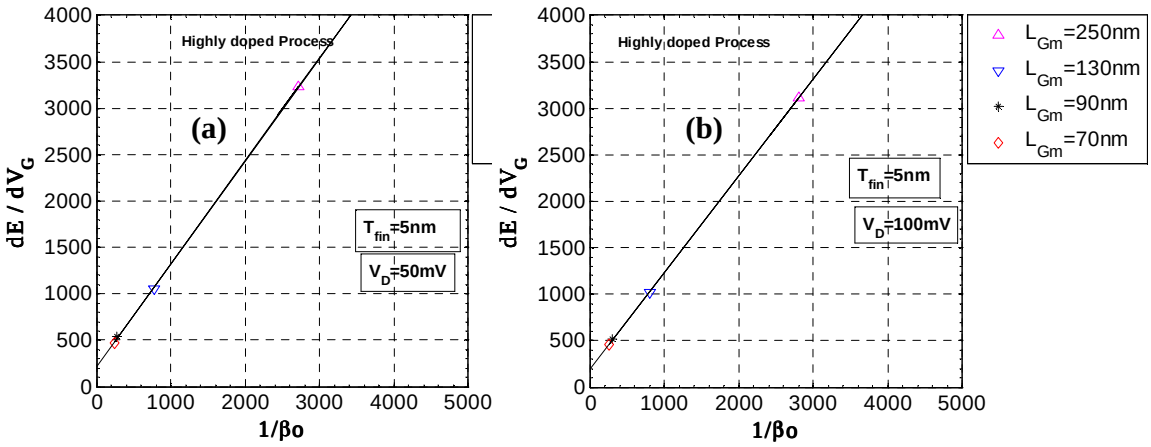

Figure C.24: Derivative of parameter "E" by V_G (from the previous "E" vs. V_{GT} plot) versus $1/\beta_o$. The S/D parasitic resistance (R_{SDE}) is found at the point of intersection between the linear fitting of data and the dE/dV_G axis. The mobility degradation parameter theta (θ) is found taking the angular coefficient of the linear fitting of data (d^2E/dV_G^2). (a) $V_D = 50$ mV and (b) $V_D = 100$ mV. The samples were measured in the wafer of the highly doped process, $T_{fin} = 5$ nm.

APPENDIX D - MEASUREMENT EQUIPMENT

D.1 Measurement System

Figure D.1: Measurement System consisting basically of an HP4156, an HP4284, a probe station Suss Wafer Prober PB300, and software applications (IMEC – Belgium).

D.2 Probe Station

Figure D.2: Probe Station Suss Wafer Prober PB300 consisting basically of micro-manipulators, shielding, wafer chamber and chuck, and joystick controller.

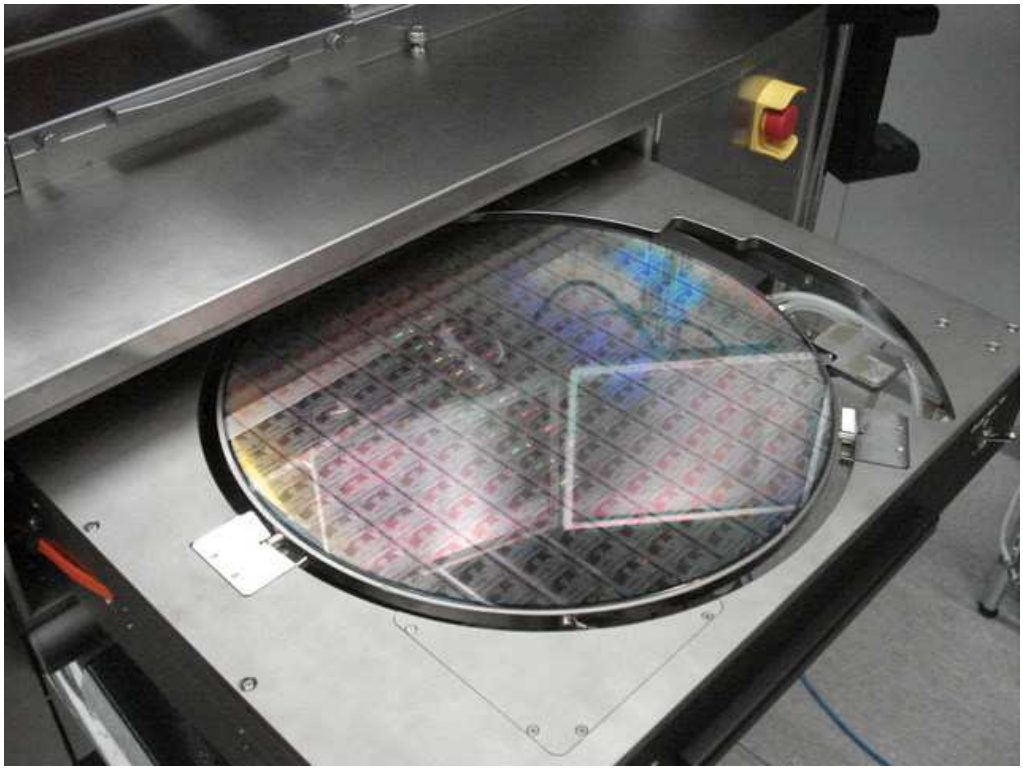

Figure D.3: Wafer chamber and chuck detail (IMEC – Belgium).

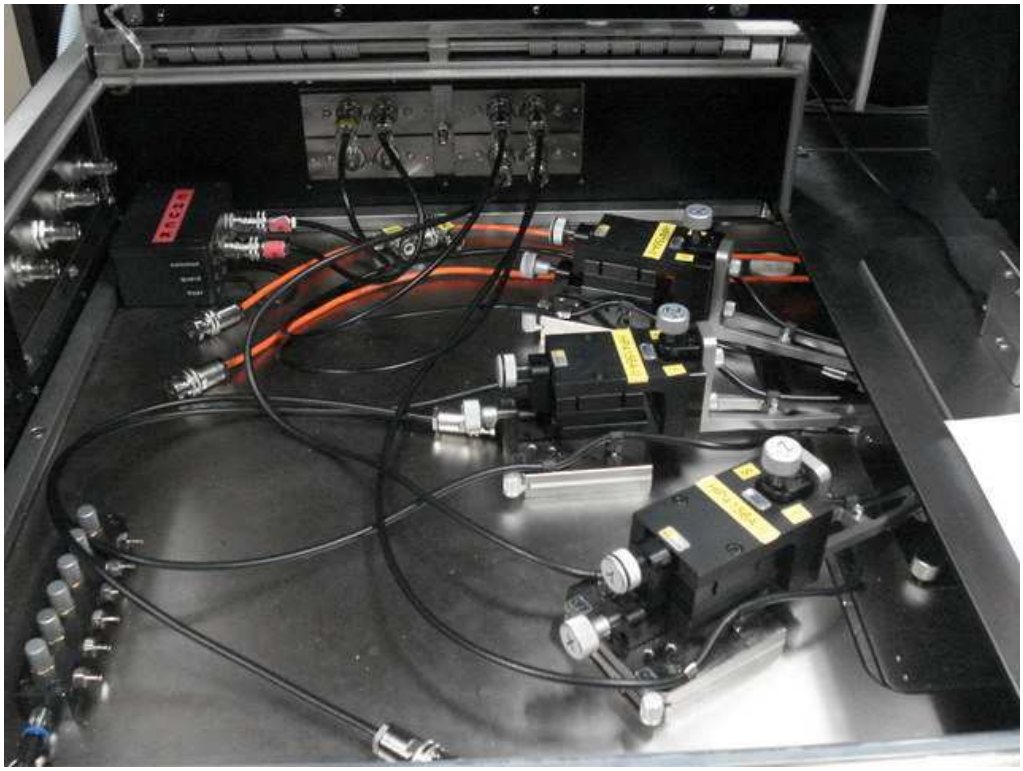

Figure D.4: Left micro-manipulators detail (IMEC – Belgium).

Figure D.5: Right micro-manipulators detail (IMEC – Belgium).

Figure D.6: Joystick Controller detail (IMEC – Belgium).

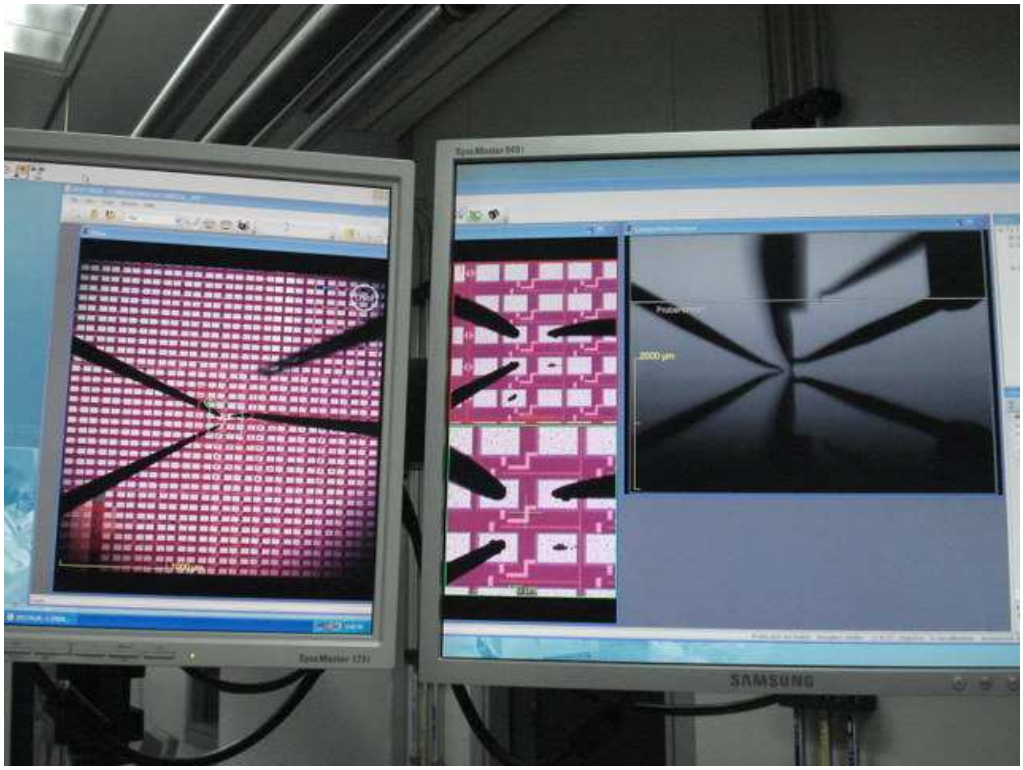

Figure D.7: Software Applications, top and side contact view (IMEC – Belgium).

D.3 HP4156 Parameter Analyzer

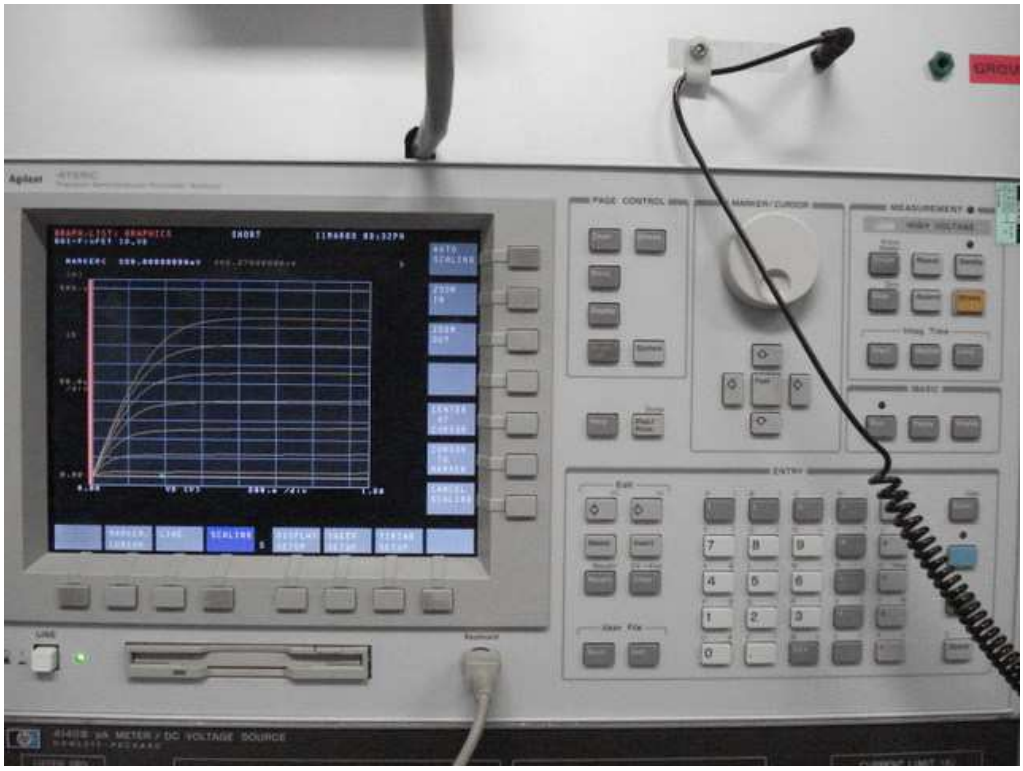

Figure D.8: HP4156 Semiconductor Parameter Analyzer main panel.

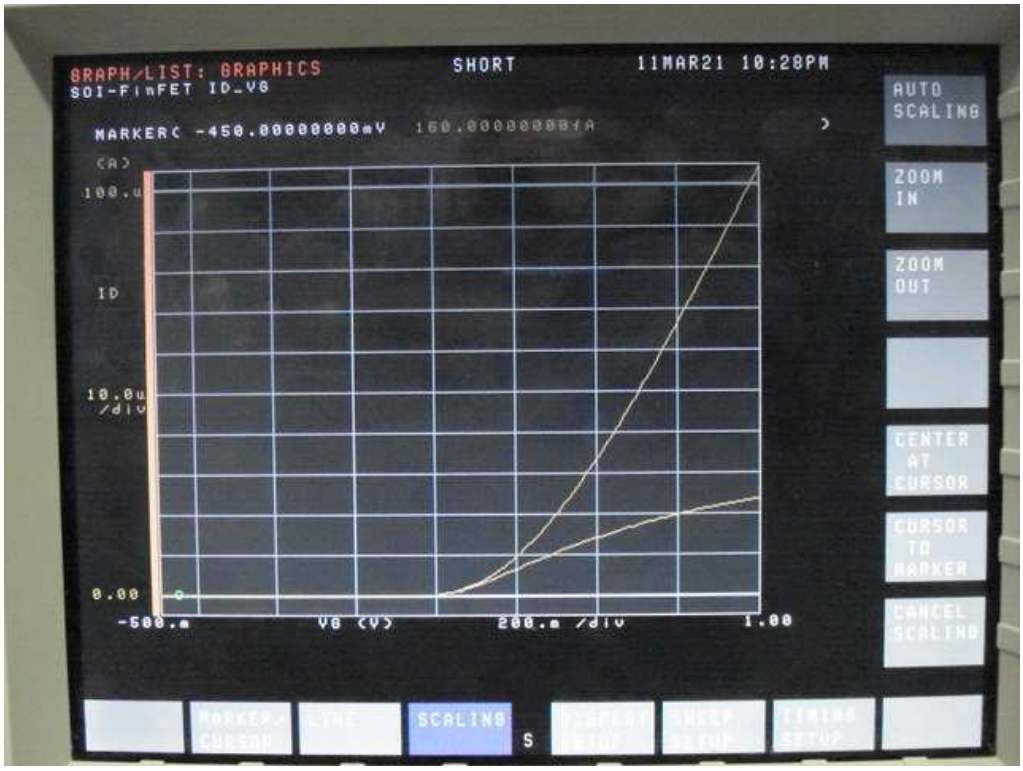

Figure D.9: FinFET I_D-V_G measurements in linear (V_D = 50 mV/100 mV) and saturated (V_D = 1V) regions of operation, linear scale (IMEC – Belgium).

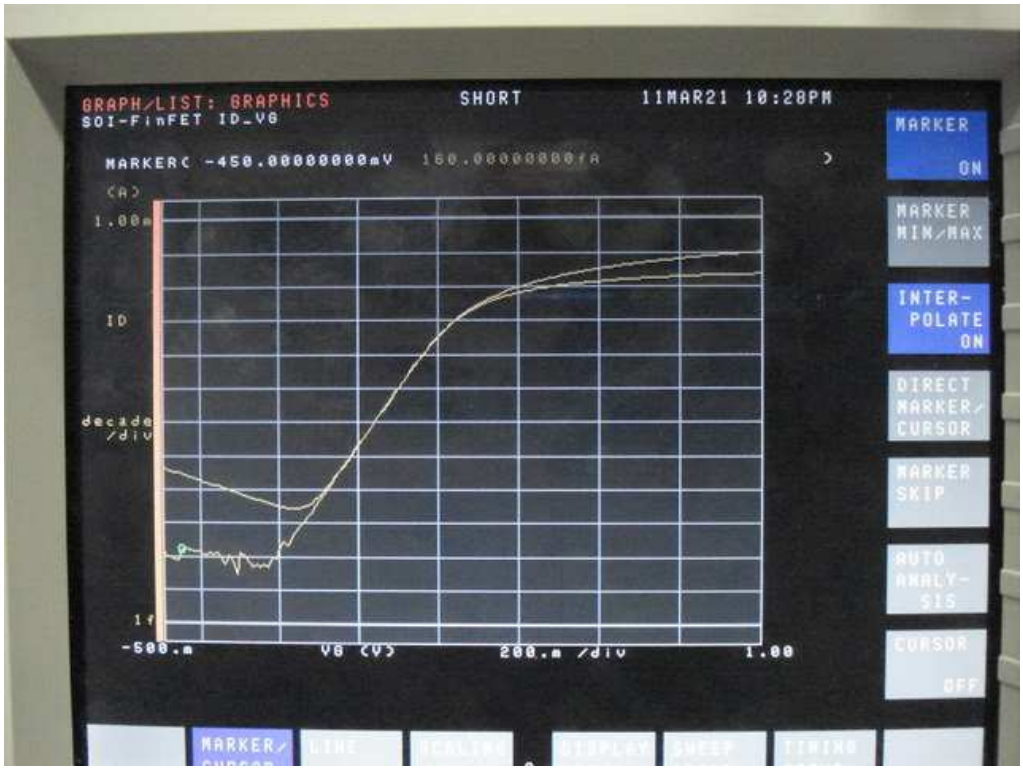

Figure D.10: FinFET I_D-V_G measurements in linear (V_D = 50 mV/100 mV) and saturated (V_D = 1V) regions of operation, log scale (IMEC – Belgium).

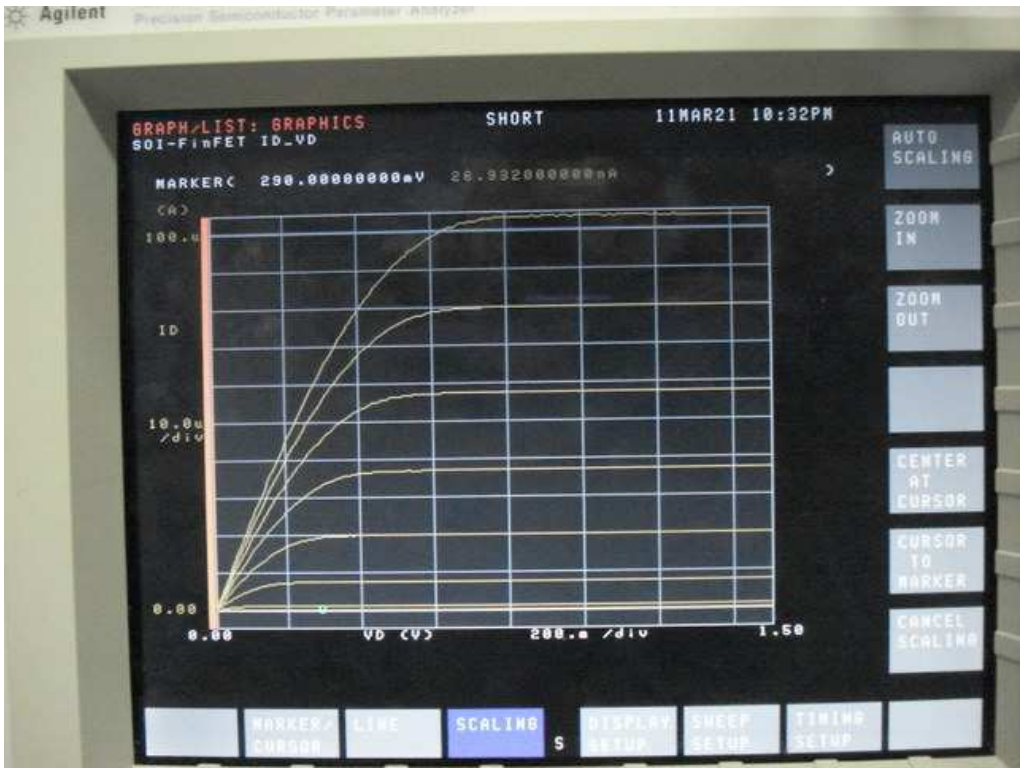

Figure D.11: FinFET I_D-V_D measurements: V_G = 125, 250, 375, 500, 625, 750, 825 mV, and 1V (IMEC – Belgium).

APPENDIX E - NANO-TRANSISTORES DE PORTA DUPLA EM SILÍCIO SOBRE ISOLANTE - SIMULAÇÃO DE FINFETS SUB-20 NM

Resumo da Tese de Doutorado como requisito parcial para a obtenção do grau de Doutor em Microeletrônica.

RESUMO

Esta Tese apresenta os resultados da simulação do transporte eletrônico em três dimensões (3D) no nano dispositivo eletrônico conhecido como “SOI-FinFET”. Este dispositivo é um transistor MOS em tecnologia Silício sobre Isolante – “Silicon-on-Insulator”, SOI – com porta dupla e cujo canal e zonas de fonte e dreno são realizadas em uma estrutura nanométrica vertical de silício chamada de “finger” ou “fin”. Como introdução ao dispositivo em questão, é feita uma revisão básica sobre a tecnologia e transistores SOI e sobre MOSFETs de múltiplas portas. A implementação de um modelo tipo “charge-sheet” para o transistor SOI-MOSFET totalmente depletado e uma modelagem deste dispositivo em altas frequências também é apresentada. A geometria do “fin” é escalada para valores menores do que 100 nm, com uma espessura entre 10 e 20 nm. Um dos objetivos deste trabalho é a definição de parâmetros para o SOI-FinFET que o viabilizem para a tecnologia de 22 nm, com um comprimento efetivo de canal menor do que 20 nm. O transistor FinFET e uma estrutura básica simplificada para simulação numérica em 3D são descritos, sendo utilizados dados de tecnologias atuais de fabricação. São apresentados resultados de simulação numérica 3D (curvas I_D-V_G, I_D-V_D, etc.) evidenciando as principais características de funcionamento do FinFET.

É analisada a influência da espessura e dopagem do “fin” e do comprimento físico do canal em parâmetros importantes como a tensão de limiar e a inclinação de sublimiar. São consideradas e analisadas duas possibilidades de dopagens da área ativa do “fin”: (1) o caso em que esta pode ser considerada não dopada, sendo baixíssima a probabilidade da presença de dopantes ativos, e (2) o caso de um alto número de dopantes ativos (> 10 é provável). Uma comparação entre dois simuladores numéricos 3D de dispositivos é realizada no intuito de explicitar diferenças entre modelos de simulação e características de descrição de estruturas 3D. São apresentadas e analisadas medidas em dispositivos FinFET experimentais. Dois métodos de extração de resistência série parasita são utilizados em FinFETs simulados e caracterizados experimentalmente. Para finalizar, são resumidas as principais conclusões deste trabalho e são propostos os trabalhos futuros e novas diretivas na pesquisa dos transistores FinFETs.

E.1 Introdução

A tecnologia de Silício-sobre-Isolante (SOI) (Colinge, 1991), com transistores SOI-MOSFET com porta única (SG) tem se tornado nos últimos anos muito competitiva em relação à tradicional tecnologia BULK (Flandre, 1996, 1999; Iñíguez, 1996; Ferreira, 1997). Transistores SOI-MOSFET com porta dupla (DG) apresentam desempenho superior aos de porta única (Doyle, 2003; Colinge, 2007; Kranti, 2007). Os transistores SOI-FinFET (Lindert, 2001), também chamados de transistores SOI-MOSFET verticais, tem demostrado nos últimos anos grande potencial para aplicações que envolvam circuitos eletrônicos, em especial circuitos analógicos de baixa-tensão (Pei, 2002; Giacomini, 2007; Pavanello, 2007a-b; Kranti, 2004, 2007). A otimização de parâmetros geométricos e de processo deste dispositivo é um ponto chave para aumentar o seu desempenho. A simulação tridimensional (3D) de dispositivos é uma poderosa ferramenta de estudo e análise e tem sido largamente utilizada (Pei, 2002; Dixit, 2005; Trivedi, 2005; Fossum, 2007; Zhao, 2008).

Um dos objetivos principais deste trabalho é determinar um conjunto de parâmetros geométricos e de processo para o SOI-FinFET que o tornem um candidato viável para a tecnologia de 22 nm. Sendo assim, um bom entendimento das características deste dispositivo e a influência destes parâmetros no seu comportamento elétrico é fundamental. É objetivo também evidenciar a influência da espessura do "fin" T_{fin} e da dopagem do "fin" N_{fin} em parâmetros importantes como a tensão de limiar V_T e a inclinação de sublimiar S.

A natureza tridimensional (3D) do SOI-FinFET torna a utilização da simulação de dispositivos em 3D uma necessidade. Assim, foi definida uma estrutura 3D deste dispositivo baseada em padrões de tecnologia atuais de processo e geométricos e os resultados de simulação são apresentados e analisados. Medidas experimentais também são apresentadas e analisadas.

E.1.1 Tecnologia SOI CMOS

A tecnologia de Silício-sobre-Isolante (SOI) (Colinge, 1991) é mencionada na primeira descrição de um IGFET (Trasistor de Efeito de Campo com Porta Isolada) pelo ano de 1926, mas infelizmente a tecnologia de então não foi capaz de produzir um dispositivo operacional sobre um substrato sólido. Na primeira metade dos anos 60 os transistores MOSFET ("metal-oxide-semiconductor field-effect-transistor") fabricados em substratos de silício tipo "Bulk" se tornaram disponíveis. Desde o início dos anos 80 a tecnologia CMOS (MOS Complementar) tem sido líder na indústria de microeletrônica mundial. A tecnologia SOI tem sido desenvolvida por mais de vinte anos e circuitos comerciais já estão disponíveis. Os circuitos integrados fabricados em Bulk CMOS ainda representam a maioria da produção industrial mundial, mas os circuitos integrados em SOI CMOS vem ganhando terreno em aplicações comerciais. As lâminas SOI (ver Figure 2.1) podem ser produzidas por várias técnicas, sendo as principais: SIMOX e "smart-cut".

A tecnologia SOI tem várias vantagens em relação à tradicional Bulk, sendo as principais: maior densidade de integração (ver Figure 2.2 e Figure 2.3); menores capacitâncias de fonte/dreno e melhores características em altas-frequências; melhor inclinação de sublimiar; e maior imunidade à radiação.

E.1.2 Transistores SOI-MOSFET

A estrutura básica de um transistor SOI nMOSFET é mostrada na Figure 2.4. Como na tecnologia Bulk, possui quatro terminais: Porta (G), fonte (S), dreno (D) e substrato ou "back" porta (Gb). O SOI-MOSFET se diferencia do Bulk-MOSFET pela presença do óxido enterrado ("buried oxide") que limita a profundidade dos implantes de fonte/dreno. A profundidade das regiões de fonte/dreno é determinada pela espessura do filme de silício t_{si}, que já sofreu redução de 10x na última década e hoje está na faixa dos 10 nm ou menos. O oxido enterrado também sofreu tal redução e está na faixa dos 25 nm. Desta forma, o terminal de substrato funciona realmente como uma segunda porta. Estes dispositivos são chamados de UTBB ou "Ultra-Thin-Body-and-Box".

E.2 Nano-Transistores de Porta Dupla em Silício Sobre Isolante - Simulação de FinFETs sub-20 nm

E.2.1 Modelamento do Transistor SOI-MOSFET em Alta-Frequência

Foi desenvolvido um modelo numérico tipo "lençol de cargas" (Brews, 1978; Tsividis, 1994) para o transistor SOI nMOSFET totalmente depletado, canal traseiro ("back") em depleção desde a fonte até o dreno. O modelo é baseado na aproximação de canal gradual (ver Figure 3.4 e Figure 3.5). Como o modelo básico só é válido para canais longos, foram introduzidos efeitos de canal curto tais como: saturação de velocidade, modulação do comprimento efetivo do canal, e condução aumentada induzida pelo dreno (DICE) ou como hoje é mais conhecido, redução de barreira induzida pelo dreno (DIBL). O modelo possui uma sólida base física e necessita de apenas alguns parâmetros de ajuste, tais como: campo elétrico crítico transversal E_c, velocidade de saturação v_{sat}, mobilidade a baixo campo μ_o, e tensões de bandas planas para os terminais das portas. Uma definição formal da tensão de limiar V_T não é necessária.

Foi desenvolvido um método de modelar o transistor SOI nMOSFET totalmente depletado em alta-frequência (acima de GHz). O método é baseado na subdivisão do canal (Tsividis, 1994), considerando o transistor como sendo composto por sub-transistores (Figure 3.18). O modelo numérico de "lençol de cargas" é então utilizado para calcular os potenciais ao longo do canal e todos os parâmetros DC e AC dos sub-transistores, que são combinados para formar um modelo geral de parâmetros "y", equações (3.60) e (3.61), com todas as condutâncias (4) e transcondutâncias (16), válido em alta-frequência. A subdivisão da porta também é considerada, uma vez que resistências e capacitâncias parasitas ao longo da porta se tornam importantes em alta-frequência (Figure 3.20). Desta forma, é possível estender a validade dos modelos quase-estáticos para frequências onde eles não seriam mais aplicáveis. A análise de canal distribuído e porta distribuída em conjunto com um modelo sólido e de base física se mostrou de grande valia na modelagem em alta-frequência do transistor SOI-MOSFET. Os resultados obtidos com os modelos desenvolvidos foram comparados com resultados experimentais e se mostraram bastante satisfatórios (Figure 3.26). Esta metodologia básica pode ser aplicada para MOSFETs multi-porta, mas o modelo de "lençol de cargas" deve ser modificado ou substituído por outro para incluir detalhes importantes da física dos dispositivos multi-porta.

E.2.2 Transistores MOSFET Multi-Porta

Os transistores MOSFET multi-porta (Figure 4.3) são considerados como peças chave para o contínuo desenvolvimento das tecnologias CMOS para atingir os objetivos impostos pela indústria dos semicondutores (Figure 4.1). Os dispositivos FinFET (Figure 4.5) vem ganhando impulso nos últimos anos como uma maneira de aliviar as complexidades da manufatura de dispositivos CMOS de "estado-da-arte" para tecnologias 22 nm até 10 nm.

Transistores FinFET são MOSFETs multi-porta com estruturas verticais chamadas de "finger" ou "fin" e podem ser produzidos em tecnologia SOI ou BULK (Figure 4.3). O fluxo de processo para estes transistores (porta dupla ou tripla) é muito próximo daquele utilizado para SOI-MOSFETs e as lâminas SOI podem ser utilizadas. Os transistores SOI-FinFET se beneficiam das qualidades intrínsecas da tecnologia SOI, mas é importante notar que Bulk-FinFETs são uma realidade e opção concreta (Figure 4.10).

Tanto os transistores SOI-FinFET como os Bulk-FinFET apresentam uma melhor possibilidade de redução de dimensões (preservando as características principais) do que os transistores planares MOSFETs e têm vantagens e desvantagens um em relação ao outro (Chiarella, 2009; Poljak, 2009). SOI-FinFETs teriam vantagens em circuitos analógicos em termos de ganho de tensão e descasamento, segundo (Chiarella, 2009). Por outro lado, os Bulk-FinFETs tem vantagens em termos do custo das lâminas, transferência de calor do canal e compatibilidade com dispositivos planares Bulk CMOS.

Recentemente uma outra opção se tornou viável como maneira de melhorar o compromisso complexidade-desempenho e compatibilidade-custo. A utilização de dispositivos SOI totalmente depletados com Ultra-Thin-Body-and-Box (ou UTBB - Figure 4.11) tem tornado a tecnologia SOI planar competitiva com os SOI-FinFETs e os Bulk-FinFETs (Lammers, 2011; Skotnicki, 2011).

E.2.3 Simulação do Transistor SOI-FinFET Porta Dupla

Foi definida uma estrutura 3D do transistor nmos SOI-FinFET porta dupla (Chau, 2002) baseada em padrões atuais de processo e geométricos. Esta estrutura foi chamada de "Structure-I" (Figure 5.2 e Figure 5.3). Foram utilizados perfis gaussianos para dopar as extensões de fonte/dreno e um "fin" dopado (Figure 5.5 e Figure 5.6). Nesta etapa foi utilizado o simulador Davinci.

A "Structure-I" foi utilizada como referência na primeira parte das simulações onde o comprimento do canal foi mantido ($L_G = 1\ \mu m$). Foi verificada a influência da variação da espessura do "fin" (T_{fin} entre 20 e 200 nm) e da dopagem do "fin" N_{fin} nas características I-V do SOI-FinFET bem como na tensão de limiar V_T e na inclinação de sublimiar S (Figuras 5.8 a 5.14).

Foi definida uma segunda estrutura 3D chamada de "Structure-II" (Figure 5.15 e Figure 5.16) que incorporou refinamentos visando a simulação de comprimentos de canal ultra curtos (L_G entre 20 e 1000 nm) e T_{fin} de 15 e 20 nm. Foi verificada a influência da variação de L_G, T_{fin} e N_{fin} nas características I-V do SOI-FinFET, em V_T, S e no DIBL (Figuras 5.17 a 5.29).

Uma terceira estrutura foi definida, “Structure-III” (Figure 5.30 e Figure 5.31), que incorporou refinamentos nas extensões de fonte/dreno (novo contato) e no óxido de porta (tipo “high-K”). Foi utilizado um “fin” não dopado e T_{fin} de 10 e 15 nm (L_G entre 20 e 1000 nm). Nesta parte das simulações também foi verificada a influência da variação de L_G e T_{fin} nas características I-V do SOI-FinFET, em V_T, S e no DIBL (Figuras 5.32 a 5.56).

Uma nova etapa de simulações utilizou o simulador Sentaurus. Foram comparados resultados obtidos com o simulador Davinci e diferentes tipos de modelos aplicados. Algumas variações de geometria e dopagem foram introduzidas, mas a estrutura utilizada foi basicamente a “Structure-II” (Figure 5.57). Foram utilizados L_G de 50 e 1000 nm e T_{fin} de 20 nm.

Primeiro foram comparadas simulações para vários modelos, uma estrutura de porta tripla e um modelo quântico. Depois foram comparadas simulações para três dopagens diferentes nas extensões de fonte/dreno. Finalmente, foram comparadas simulações para uma redução em T_{Box} e para uma variação em um parâmetro de controle da mobilidade (Figuras 5.61 a 5.80).

Foi implementado um método de extração das resistências parasitas de fonte/dreno e aplicado nos resultados de simulação (Figure 5.71, Figure 5.87).

Uma etapa final de simulação comparou diversas formas de dopagem nas extensões de fonte/dreno variando o ângulo do implante (Figure 5.81e Figuras 5.82 a 5.87).

E.2.4 Medidas em Transistores SOI-FinFET

Foram realizadas medidas experimentais em transistores SOI-FinFETs fabricados nos laboratórios do IMEC (Interuniversity Microelectronics Center), na Bélgica, para dois tipos de processo: “Processo de Referência” e “Processo de Alta Dopagem”. A diferença entre os dois processos está somente em uma dopagem adicional de LDD que é realizada no “Processo de Alta dopagem”.

Os transistores medidos tem cinco (5) “fin” em paralelo, L_G entre 45 nm e 10 µm e T_{fin} de 5, 10 15 e 20 nm (Figure 6.1).

Foram utilizadas as facilidades de medida dos Laboratórios do IMEC (Figuras D.1 a D.11), que gentilmente concordou com a sua utilização, sendo um HP4156 (analisador de parâmetros de semicondutores) e uma estação de prova (Suss Wafer Prober PB300) com microponteiras de teste.

Todas as medidas foram realizadas no modo force/sense com prévio teste de resistência de contato (menor que 2 Ω). Para cada transistor SOI-FinFET medido foram levantadas as curvas: I_D-V_G para V_G entre 0 e 1 V, na zona linear (V_D = 50 e 100 mV), e na zona de saturação com (V_D = 1 V); I_D-V_D para V_D entre 0 e 1 V, V_G entre 0 e 1 V.

Foi verificada a influência da variação de L_G e T_{fin} nas características I-V dos SOI-FinFETs, em V_T, S e no DIBL (Figuras 6.3 a 6.14). O método implementado para a extração das resistências parasitas de fonte/dreno foi aplicado às medidas experimentais (Table 6.1 e Table 6.2).

E.3 Conclusões e Trabalhos Futuros

A tecnologia de Silício-sobre-Isolante (SOI) se mostra atualmente muito competitiva em relação à tradicional tecnologia BULK. Transistores SOI-MOSFET com porta única, porta dupla ou porta múltipla (multi-porta) apresentam desempenho superior aos tradicionais transistores BULK MOSFET.

Foi apresentada uma visão geral da tecnologia SOI e dos transistores MOSFET multi-porta juntamente com a descrição e implementação de um modelo tipo "lençol de cargas" para o transistor SOI nMOSFET totalmente depletado, e um modelamento deste dispositivo em alta-frequência (acima de GHz). A análise de canal distribuído e porta distribuída em conjunto com um modelo sólido e de base física se mostrou de grande valia na modelagem em alta-frequência do transistor SOI-MOSFET.

O transistor SOI-FinFET tem grande potencial para aplicações que envolvam circuitos eletrônicos e tem sido objeto de pesquisas ao longo dos anos para resolver diversos desafios tecnológicos em relação à otimização de parâmetros geométricos e de processo deste dispositivo.

Este trabalho visou determinar um conjunto de parâmetros geométricos e de processo para o SOI-FinFET que o tornassem um candidato viável para a tecnologia de 22 nm e abaixo. Sendo assim, um bom entendimento das características deste dispositivo e a influência destes parâmetros no seu comportamento elétrico é fundamental. A natureza tridimensional (3D) do SOI-FinFET torna a utilização da simulação de dispositivos em 3D uma necessidade.

Foram apresentadas as características básicas de um SOI-FinFET de porta dupla e os resultados e análise de simulação de dispositivos em 3D. Foi demonstrada a influência da espessura T_{fin} e da dopagem do "fin" N_{fin} na tensão de limiar V_T e na inclinação de sublimiar S. Também foi demonstrada a influência de um "fin" parcialmente depletado (PD) e totalmente depletado (FD) nas características do SOI-FinFET.

Os efeitos de flutuações randômicas de dopantes são muito importantes e podem tornar dopagens na ordem de 10^{17} a 10^{18} cm^{-3} não apropriadas para uso em FinFETs com T_{fin} abaixo de 20 nm e L_G escalado agressivamente abaixo de 20 nm. O "fin" não dopado, ou com dopagem típica na ordem de $1x10^{15}$ cm^{-3}, é o mais prático para ser utilizado no transistores FinFET uma vez que V_T depende primeiramente da função trabalho da porta e da espessura do "fin". Além disso, problemas randômicos de dopagem e "efeitos de canto" podem ser desprezados em um "fin" não dopado.

O impacto da variação de T_{fin}, de N_{fin} e de L_G em V_T e S foi investigada por simulação de dispositivos em 3D e por medidas experimentais. A degradação das características dos transistores FinFET para comprimentos de porta abaixo de 50 nm (T_{fin} = 20 nm) é claramente notada e o dispositivo com L_G = 20 nm (T_{fin} = 20 nm) demonstrou características pobres e necessidade de considerável aprimoramento. As simulações indicaram que a degradação das características para L_G abaixo de 50 nm é amenizada na região de sublimiar com a redução de T_{fin} de 20 para 10 nm e o uso de um material isolante de porta tipo "high-k".

Nesta tese foi apresentada uma comparação entre os simuladores Davinci e Sentaurus. Foi obtida uma boa concordância na região de sublimiar para as estruturas FinFET com os mesmos perfis de dopagem, uma vez que nesta região a diferença entre modelos utilizados não é muito sentida. Entretanto nas regiões de inversão moderada e forte, as simulações Davinci superestimaram I_D. Pequenas diferenças foram notadas

entre simulações Sentaurus, especialmente no caso de estruturas FinFET de canal longo e quando um modelo de quantização foi utilizado. Um melhor conjunto de parâmetros de ajuste é necessário no caso do modelo hidrodinâmico.

Um ponto importante verificado foi que a porta de topo de uma estrutura FinFET de tripla porta contribui com apenas 5% para I_D, considerando-se uma relação H_{fin}/T_{fin} de 3. Fica evidente a superestimação de I_D nas estruturas FinFET no caso das simulações feitas com Davinci quando se compara com as simuladas feitas com Sentaurus e com diferentes perfis de dopagem. Para canais longos, mesmo nas estruturas com a maior dopagem nas extensões de fonte/dreno, foi obtida uma corrente I_D aproximadamente 6% menor.

A redução de 33% (de 150 a 100 nm) in T_{Box} produziu um efeito mínimo em I_D nas simulações feitas com Sentaurus, enquanto que um incremento na degradação de mobilidade causou 14% de redução em $I_{D.}$

Esta tese apresentou uma estimativa para as resistências parasitas de fonte/dreno a partir de resultados de simulação e medidas elétricas em transistores FinFET. As extensões de fonte/dreno do “fin” devem ser cuidadosamente modeladas uma vez que são fundamentais nas características I-V dos dispositivos. O controle e redução das resistências parasitas de fonte/dreno são um grande desfio na tecnologia dos FinFETs manométricos.

A otimização de parâmetros geométricos e de processo são um ponto chave para melhorar o desempenho dos transistores SOI-FinFET para o projeto e fabricação de circuitos, em particular para aplicações de baixa-tensão. Os métodos de implantação das extensões de fonte/dreno são de grande importância na tecnologia dos transistores FinFET multi-porta. Neste trabalho foi mostrado a influência da utilização de diferentes ângulos de implantação nas extensões de fonte/dreno e o impacto nos parâmetros parasitas.

Três aspectos principais geralmente definem a otimização necessária dos transistores FinFETs: (1) O controle e redução das resistências série parasitas de fonte/dreno, que requerem silicetação das extensões de fonte/dreno, engenharia de dopagem e possível crescimento epitaxial das regiões de fonte/dreno; (2) a redução de t_{ox} abaixo de 1 nm (ou EOT abaixo de 1 nm) de forma a tornar o FinFET um candidato viável para a tecnologia de 22 nm, e (3) T_{fin} na faixa de 8 a 15 nm. As características dos FinFETs nestes regimes são dominadas por efeitos quânticos tais como tunelamento pelo óxido de porta, efeitos de quantização no comprimento de onda do elétron, efeitos de flutuações randômicas de dopantes/defeitos; efeitos de rugosidade e geometria no processo de definição do “fin”. Estes são os efeitos que devem ser melhor investigados para aprimorar as características elétricas destes dispositivos.

Trabalhos futuros sugeridos para explorar a otimização dos transistores FinFETs sub-20 nm:

- uso dos simuladores Sentaurus (Synopsys) e ISE-TCAD e dos resultados deste trabalho para comparar com simuladores modernos de transporte estatístico quântico baseados em modelos físicos;
- otimizar o transistor FinFET (não dopado) para comprimentos físicos de porta na faixa dos 10 a 20 nm e espessuras de “fin” na faixa dos 8 a 15 nm;

- considerar no método de extração de parâmetros a modulação pela tensão de porta do comprimento efetivo de porta e das resistências série parasitas;
- considerar apropriadamente o efeito de confinamento quântico nas características I-V do transistor FinFET;
- uso de um modelo elétrico preditivo para FinFETs e extração dos parâmetros elétricos para simulação de circuitos com FinFETs;
- modelar o comportamento de associações TAT paralelas/série com FinFETs;
- uso de um modelo elétrico preditivo e de associações TAT paralelas/série com FinFETs para simular circuitos analógicos (p.ex. um estágio amplificador);
- considerar efeitos de flutuações randômicas de dopantes/defeitos e aspectos de variabilidade em FinFETs.