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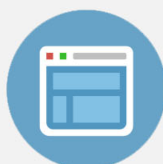

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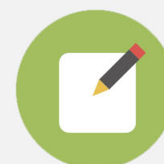

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SiO_2/SiC structures annealed in $D_2{}^{18}O$: Compositional and electrical effects

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Effects of water vapor annealing on SiO_2/4H-SiC structures formed following different routes were investigated using water isotopically enriched in ^{18}O and ^{2}H (D). Isotopic exchange between oxygen from the water vapor and oxygen from SiO_2 films deposited on 4H-SiC was observed in the whole depth of the films, differently from the behavior of SiO_2 films thermally grown on 4H-SiC. The highest amount of D was obtained in the sample with the highest negative fixed charge concentration, suggesting that the D incorporation occurs in defects in the structure that exist prior to the annealing. As a consequence of the water annealing, a significant reduction in the negative effective charge in metal-oxide-semiconductor capacitors and the removal of the SiO_2/SiC interfacial region was observed, attributed to the reduction of the amount of SiO_xC_y compounds in the interfacial region. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4869124]

The properties of silicon carbide (SiC) make it a suitable semiconductor to replace Si in devices that require high power, high frequency, and/or high temperature applications. A dielectric film of silicon dioxide (SiO_2) can be thermally grown on it, in a similar way as on Si.[1,2] However, the SiO_2/SiC interface formed by thermal oxidation of SiC presents a higher interface state density (D_{it}) than the SiO_2/Si one.[3] Negative fixed charge is also observed to be an intrinsic defect related to the SiC thermal oxidation,[4–6] which is present mainly in the SiO_2/SiC interfacial region.[7,8] Such defects lead to poor channel mobilities in SiC-based metal-oxide-semiconductor field effect transistors (MOSFETs).[9,10] The origin of these defects can be related to the formation, during thermal oxidation, of a non-abrupt SiO_2/SiC interfacial region, observed by Nuclear Reaction Profiling (NRP), Transmission Electron Microscopy (TEM), and X-ray Reflectivity (XRR),[6,11,12] where silicon oxycarbide (SiC_xO_y) compounds are found.[13,14] In order to improve the quality of the SiO_2/SiC interface, different post-oxidation treatments have been employed,[3,15,16] as well as alternative routes to form SiO_2 films on SiC, aiming at minimizing the electrical degradation from thermal oxidation.[17–19] Concerning thermal oxidation conditions, it was observed that oxidations and/or reoxidations involving water vapor can lead to a higher dielectric strength,[20] lower values of D_{it},[20–23] and higher channel mobility[24] as compared to dry oxidations. For the Si-case, wet oxidation leads to a lower oxide breakdown voltage as compared to the dry one.[25] Besides, device instabilities were attributed to the presence of water-related species in SiO_2/Si structures.[26] These effects highlight the importance of understanding the interaction of water vapor with SiO_2/SiC and SiO_2/Si. In fact, we have reported[27,28] that the substrate plays an important role in water vapor interaction with SiO_2 films thermally grown on SiC and on Si: in the SiO_2/SiC case, hydrogen was observed to be incorporated in the surface, bulk, and interfacial region of the SiO_2 film, while in the SiO_2/Si case hydrogen was mainly incorporated in the near-surface region of the SiO_2 film. Besides, larger isotopic exchange between oxygen from the water vapor and oxygen from the thermally grown SiO_2 film was observed for oxides grown on SiC compared with those grown on Si. To deeply explore the nature of these interactions and to understand its consequences, the effects of water vapor annealing in SiO_2/SiC structures was investigated in this work. SiO_2 films were formed either by thermal oxidation, sputtering deposition, or by a short oxidation time prior to the oxide deposition. Since it was observed that these different routes lead to different electrical properties,[19] a relation between the electrical properties and water vapor interaction can be unrevealed. Oxygen profile and areal density of hydrogen, incorporated from water vapor during annealing, were obtained by nuclear reaction techniques. Electrical characteristics were obtained from capacitance voltage (C-V) curves, while film thickness and density were determined by XRR measurements.

Silicon-faced n-type 4H-SiC (0001) wafers on-axis doped with nitrogen ($3.1 \times 10^{15}\,cm^{-3}$) were cleaned with standard Piranha and RCA (Radio Corporation of America) routines,[29] etched in a 5% HF solution, and rinsed in deionized water. For thermal oxidation, samples were then immediately loaded in a static pressure, resistively heated quartz tube furnace, which was pumped down to 2×10^{-7} millibars before being pressurized with oxygen. SiO_2 films were thermally grown at 1100 °C under 100 millibars of dry natural O_2 on SiC for different oxidation times. SiO_2 films (21–24 nm thick) were deposited by RF sputtering using a SiO_2 target. This system was pumped down to 10^{-8} millibars and then Ar was introduced in the chamber at a constant flux, keeping the pressure at 2.7×10^{-3} millibars during sputtering with power at 90 W from a target with a 2 in. diameter. Under these conditions, the deposition rate is $\sim$0.1 Å/s. Concerning annealings, samples were annealed under 2×10^{-7} millibars at 700 °C for 30 min prior to submission to the water vapor annealing (without exposure to the atmospheric air) that was performed at temperatures ranging from 200 to 800 °C, for 1 h, under 10 millibars of water vapor, simultaneously, enriched in the ^{18}O and ^{2}H (D), hereafter, called $D_2{}^{18}O$ annealing. The use of the isotopes

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^{18}O and D (natural abundances of 0.2 and 0.015%, respectively) allows one to distinguish them from O and H incorporated during air exposure and/or from O of SiO_2 films deposited and/or thermally grown. D quantification was accomplished by nuclear reaction analysis (NRA), using the $D(^3He,p)^4He$ nuclear reaction[30] at 700 keV (sensitivity and accuracy can reach 4×10^{12} at/cm^2 and 10%, respectively). ^{18}O profiles were determined using the narrow resonance ($\Gamma \sim 100$ eV) in the cross section curve of the $^{18}O(p,\alpha)^{15}N$ nuclear reaction at 151 keV.[31] Al was thermally evaporated to obtain MOS structures using a mechanical mask aiming at forming circular capacitors with a diameter of 200 μm. An InGa eutectic was used as back contact. The C-V curves were taken from inversion to accumulation at 100 kHz with a 0.25 V/s rate using a HP4284A Precision *LCR* Meter. XRR analyses were performed in a PANalytical X'Pert PRO equipment using Cu Kα_1 radiation ($\lambda = 1.5406$ Å) and scanning in 0.003° steps. Data simulation were performed using the Parratt formalism for Reflectivity.[32]

Incorporations of D, from water annealings performed at different temperatures, in SiO_2/SiC structures formed by different routes are presented in Fig. 1. At the lowest annealing temperature, D was incorporated in similar amounts in all samples. However, for higher temperatures, amounts of D incorporated in samples where the SiO_2 film was deposited directly on the SiC surface were larger than in the other samples. Such result corroborates the hypothesis that the D incorporation is related to the presence of electrically active defects, since previous works[2,18,19] reported a higher concentration of D_{it} and/or effective charge (Q_{eff}) in oxides deposited directly on SiC as compared to other routes. Besides, Fig. 1 also indicates the influence in the D incorporation of two different routes using thermal oxidation employed to form SiO_2 films on SiC: a SiO_2 film thermally grown (final thickness $\sim$ 14 nm) and a thin film thermally grown ($\sim$3 nm) followed by the deposition by sputtering of a $\sim$23 nm SiO_2 film. At 600 °C and 800 °C, the SiO_2 film formed only by thermal oxidation presented slightly larger amounts of D incorporated due to annealing temperatures in water vapor, even though been thinner. These results are also in good agreement with the electrical properties observed for structures with dielectric films obtained by similar routes:[19] thermal oxidation in O_2 of SiC for a longer oxidation time induces higher negative effective charge in the SiO_2/SiC interfacial region compared with the thermal growth of a thin SiO_2 film followed by the deposition by sputtering of additional SiO_2 film.

Concerning the incorporation of oxygen due to exposure to $D_2{}^{18}O$, ^{18}O profiles were determined for samples which SiO_2 films $\sim$23 nm thick were deposited by sputtering on SiC and that incorporated D in larger amounts: exposures at 600 and 800 °C. Besides, a profile from a SiO_2 film 20 nm thick thermally grown on SiC and exposed to the $D_2{}^{18}O$ at 600 °C is presented for comparison. It can be observed in Fig. 2 that in the case of the sample with the deposited film annealed in water vapor at 600 °C, around 35% of isotopic exchange between ^{18}O from the $D_2{}^{18}O$ and ^{16}O from deposited SiO_2 film was observed along all depths of the oxide film, indicating the high mobility of O atoms. This is a different behavior from the one observed in the SiO_2 film thermally grown on SiC and submitted to the $D_2{}^{18}O$ annealing under the same condition, where the ^{18}O profile is observed not only through whole oxide film bulk in smaller amounts (around 15% of isotopic exchange), but also in an complementary error-function (erfc)-like ^{18}O profile in the near-surface region of the oxide. Such difference in this ^{18}O profile can be explained by the presence of peroxide defects in the near surface region of oxide film thermally grown,[33] that are not present in the case of the deposited SiO_2 film. On the other hand, for the annealing at 800 °C, a total isotopic exchange between ^{18}O from the $D_2{}^{18}O$ and ^{16}O from the deposited SiO_2 film occurred, in a similar way to what occurs for SiO_2 films thermally grown annealed at higher temperatures.[28] A slightly thicker $Si^{18}O_2$ film can be observed for the sample annealed at 800 °C, which could indicate an extra SiC oxidation due to the annealing at a higher temperature.

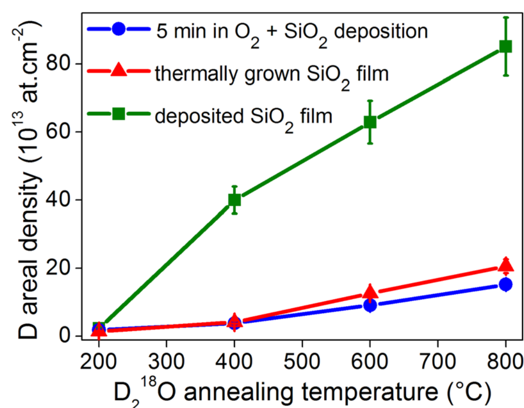

FIG. 1. Deuterium areal densities in SiO_2/SiC samples after annealing in $D_2{}^{18}O$ performed at different temperatures. SiO_2/SiC samples prior the water annealing were synthesized according to three different routes: Oxidized in 100 millibars of O_2 at 1100 °C for 10 h (thermally grown SiO_2 films yielding $\sim$14 nm thickness); only with a SiO_2 film deposited by sputtering (deposited SiO_2 film yielding $\sim$23 nm thickness); or oxidized for 5 min followed by SiO_2 film deposition by sputtering (5 min in $^{18}O_2 + SiO_2$ deposition yielding $\sim$26 nm thickness). Bars correspond to experimental accuracy of 10%.

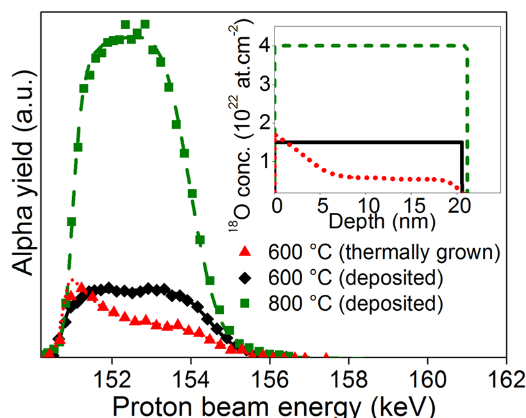

FIG. 2. Experimental (symbols) excitation curves of the $^{18}O(p,\alpha)^{15}N$ nuclear reaction around the resonance at 151 keV and the corresponding simulations (lines) for a SiO_2 film 20 nm thick thermally grown on SiC submitted to $D_2{}^{18}O$ annealing at 600 °C and for SiO_2 films $\sim$23 nm thick deposited by sputtering and submitted to $D_2{}^{18}O$ annealing at 600 or at 800 °C. Inset: ^{18}O profiles obtained in the simulations using the same line types. 4×10^{22} $^{18}O/cm^3$ corresponds to the oxygen concentration in stoichiometric SiO_2.

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However, the worse depth resolution for a ∼20 nm thick film prevents the certitude about this interpretation.

To understand how the D incorporation affects the electrical properties, C-V curves of MOS capacitors were obtained before and after $D_2{}^{18}O$ annealings and are presented in Fig. 3 for SiO_2 films formed by the three different routes. A positive shift from the ideal curve can be observed for all samples, indicating the presence of negative effective charge. The sample with the smaller shift from the ideal curve is the one with a thin SiO_2 film thermally grown prior to the oxide film deposition, fact related to a reduced electrical degradation.[19] After the water vapor annealing, a significant reduction on the shift from the ideal curve can be observed for all samples, indicating reduction of the negative effective charge. One possible explanation for the origin of negative fixed charge in SiO_2/SiC interfacial region is the presence of the O-lone pair state.[5] The reduction of the negative effective charge observed due to the water vapor annealing can be related with the D incorporation presented in Fig. 1, in the sense that this incorporated D could be bonded to oxygen, making the defect electrically inactive.

Finally, in order to obtain information about the water vapor annealing structural and compositional effects on SiO_2/SiC samples, XRR measurements were performed for

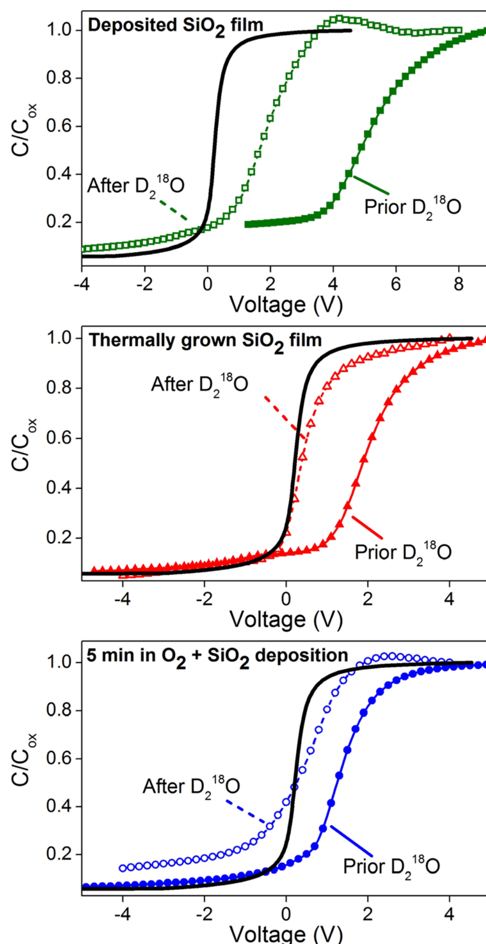

FIG. 3. C-V curves of Al/SiO_2/4H-SiC structures before (full symbols and solid lines) and after (open symbols and dashed lines) the annealing under 10 millibars of $D_2{}^{18}O$ at 800 °C for 1 h. SiO_2 films formed by sputtering deposition (squares), by thermal oxidation for 4 h (triangles), and by thermal oxidation for 5 min followed by sputtering deposition (circles) are presented. Ideal C-V curves (solid black lines) are presented for comparison.

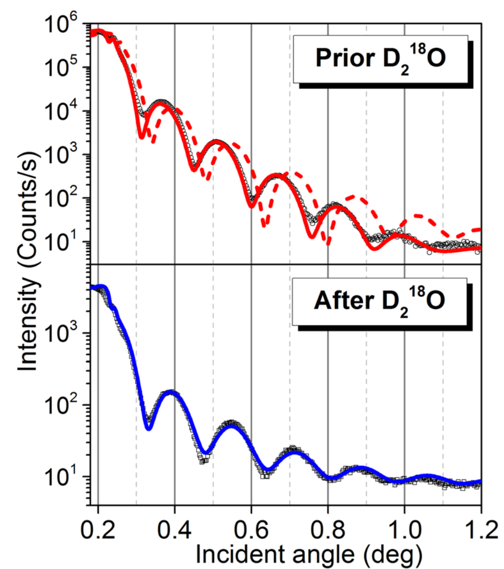

FIG. 4. XRR data (symbols) and simulation (lines) from SiO_2/4H-SiC structures formed by thermal oxidation for 5 min followed by sputtering deposition prior and after the annealing under 10 millibars of $D_2{}^{18}O$ at 800 °C for 1 h. The dashed line corresponds to a simulation of the sample prior water vapor annealing assuming that there is no interfacial layer. Parameters extracted from simulations using solid lines are presented in Table I.

samples with the best electrical properties prior to the water vapor annealing, namely, thermal oxidation for 5 min followed by sputtering deposition. XRR data and simulations are presented in Fig. 4 for these samples prior and after the $D_2{}^{18}O$ annealing. Parameters used in the solid line simulations are shown in Table I. Prior to $D_2{}^{18}O$ annealing, a satisfactory simulation can only be obtained when an interfacial layer between the SiO_2 film and the 4H-SiC substrate is included. As commented before, the presence of such interlayer was already observed and related with the electrical degradation due to thermal oxidation.[11] In our simulation, the interlayer presents a density value between those of the SiO_2 film and the SiC substrate. After the $D_2{}^{18}O$ annealing, no major modification can be observed in the SiO_2 film density and thickness. However, for the simulation, there was no need to consider an interlayer between the SiO_2 film and the 4H-SiC substrate. Such modification can be related to improvements in the electrical properties from the water vapor annealing. Similar effects using SiO_2/SiC post-oxidation annealing (POA) in NO ambient, an annealing that reduces D_{it} in the SiO_2/SiC interface region, were already observed:[11,12] a reduction in the SiO_2/SiC interfacial region thickness was observed after NO annealing, highlighting the importance of the reduction of this interfacial region thickness to the electrical properties improvement of SiC-based devices.

TABLE I. Parameters extracted from XRR solid line simulations presented in Fig. 4. The density of SiC was assumed to be 3.21 g/cm^3 in all simulations.

	Film thickness (nm)		Film density (g/cm^3)	
Sample	SiO_2 film	Interfacial layer	SiO_2 film	Interfacial layer
SiO_2/SiC	26	2	2.3	2.8
SiO_2/SiC + $D_2{}^{18}O$	25	…	2.4	…

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In conclusion, incorporation of H and O due to water vapor annealings in SiO_2 films formed by different routes on 4H-SiC and its effects in electrical and compositional properties were investigated. It was observed that the electrical quality of the structure prior to the water vapor annealing plays a major role in D incorporation: the highest amount of D was incorporated in SiO_2 films deposited on SiC (films that presented the highest negative effective charge concentration) as compared to SiC samples submitted to thermal oxidations. ^{18}O profiles were seen to depend on SiO_2 film formation route and on annealing temperature. Besides, electrical measurements evidenced that the water vapor annealing reduced the negative effective charge from MOS capacitors for all SiO_2 film formation routes, indicating a passivation of electrical defects in the SiO_2/SiC interfacial region. The modification in the interface region is confirmed by XRR results, which indicate that the water vapor annealing can remove the SiO_2/SiC interlayer, responsible for the interfacial region electrical degradation.

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